University of Missouri-Rolla
Electromagnetic Compatibility Laboratory

PWB Power Bus Structures: Theory and Design

Power Bus Noise, Decoupling, Ground Bounce, Power Islands, Bypass Capacitors, Shoot-Through Current, Interplane Capacitance, Delta-I Noise, Embedded Capacitance, Self-Resonance, Mutual Inductance...

Presented by
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University of Missouri-Rolla

IEEE EMC Society

Rocky Mountain Chapter

November 11, 1999

B. Rubin and W. D. Becker, “The Modeling of Delta-i Noise in High Performance Computer Modules,” *Conference Record of the 17th Asilomar Conference on Circuits, Systems, and Computers*, IEEE Cat. # 83CH1939-8, Oct. 31-Nov. 2, 1983.

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A. R. Djordjevic and T. K. Sarkar, “An Investigation of Delta-I Noise on Integrated Circuits,” *IEEE Trans. on Electromagnetic Compat.*, vol. 35, no. 2, May 1993.

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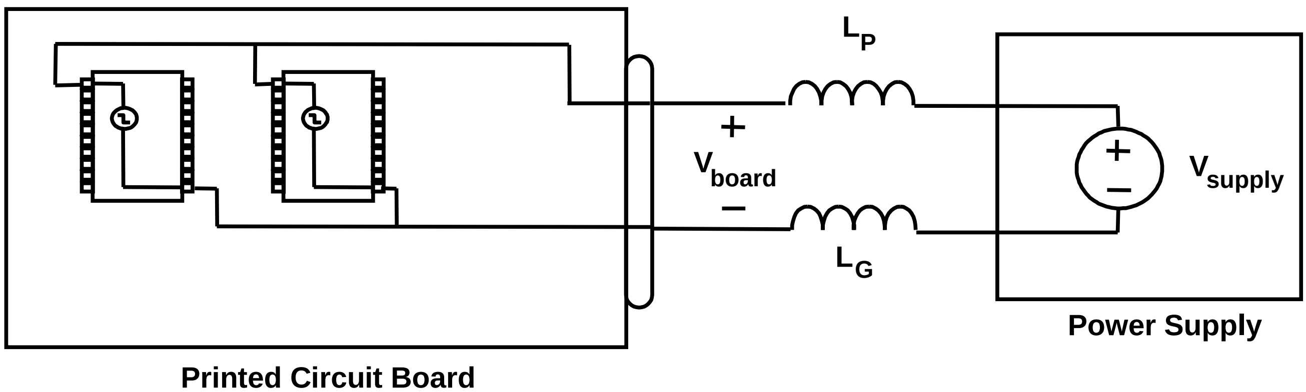
T. H. Hubing, J. L. Drewniak, T. P. Van Doren, F. Sha, and M. Wilhelm, “An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling,” *Proceedings of the 1995 IEEE International Symposium on Electromagnetic Compatibility,* Atlanta, GA, August 1995, pp. 308-312.

H. Shi, F. Sha, J. L. Drewniak, T. H. Hubing, T. P. Van Doren, and F. Yuan, "Simulation and Measurement for Decoupling on Multilayer PCB DC Power Buses," *Proceedings of the 1996 IEEE International Symposium on Electromagnetic Compatibility,* Santa Clara, CA, August 1996, pp. 430-435.

A lot of people have been looking at the power bus noise problem for a long time.

What Causes Power Bus Noise?



Power Distribution Model ~ (0 - 5 MHz)

A lot of equation writing and picture drawing accompanied this page. The bottom line is that devices draw current faster than sources with non-zero impedance can supply it.

Why is this a problem?

Why is this a problem?

Signal Integrity is compromised.

Signal integrity engineers want the power bus to supply as much current as the active devices can draw. This part of the presentation discussed the effect of power bus noise on signal waveforms.

Why is this a problem?

Can result in conducted and radiated EMI.

The power bus can be a reasonably good antenna at its resonant frequencies. At other frequencies, it is not a good antenna but it is often connected or coupled to the things that are good antennas.

In response to questions from the audience, there was also a discussion of shoot-through current in CMOS devices. Numerous figures and equations were drawn on a poster board in the room. The shoot-through current in CMOS devices can be estimated using the power dissipation capacitance, Cpd.

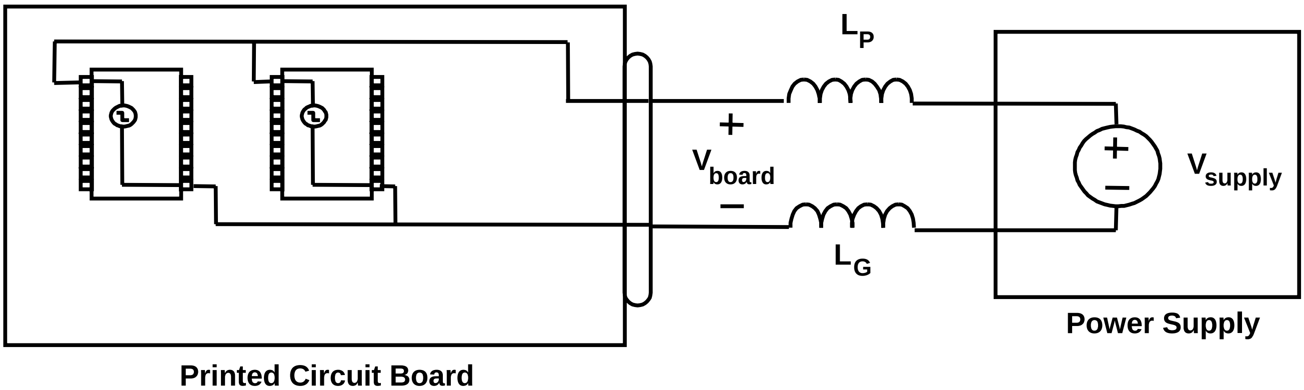
Conflicting goals?

Do we want a low-impedance power bus that can supply lots of current without a significant change in voltage?

Do we want a high-impedance power bus that isolates each device from other devices?

The best design solution often depends on your perspective.

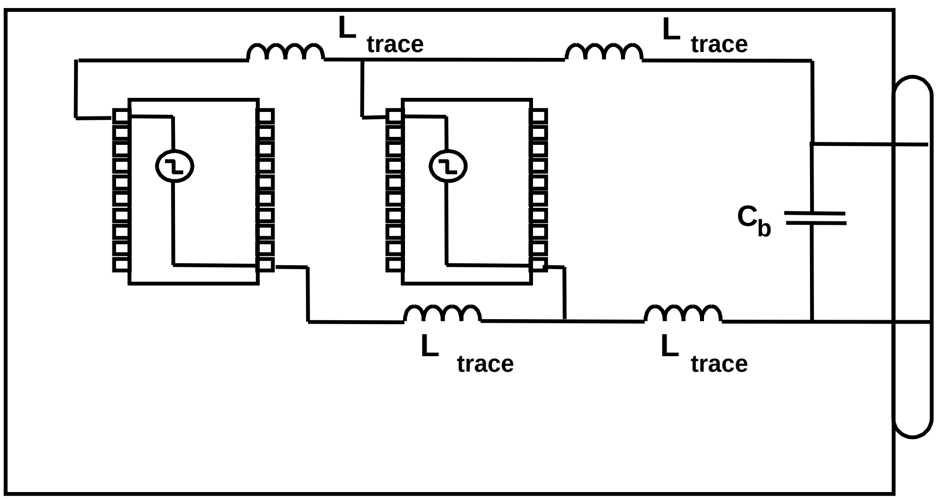
What is the solution?



Power Distribution Model ~ (0 - 5 MHz)

With a few equations and a lot of arrows, the effectiveness of a bulk decoupling capacitor for reducing power bus noise was evaluated here.

What is the solution above 5 MHz?

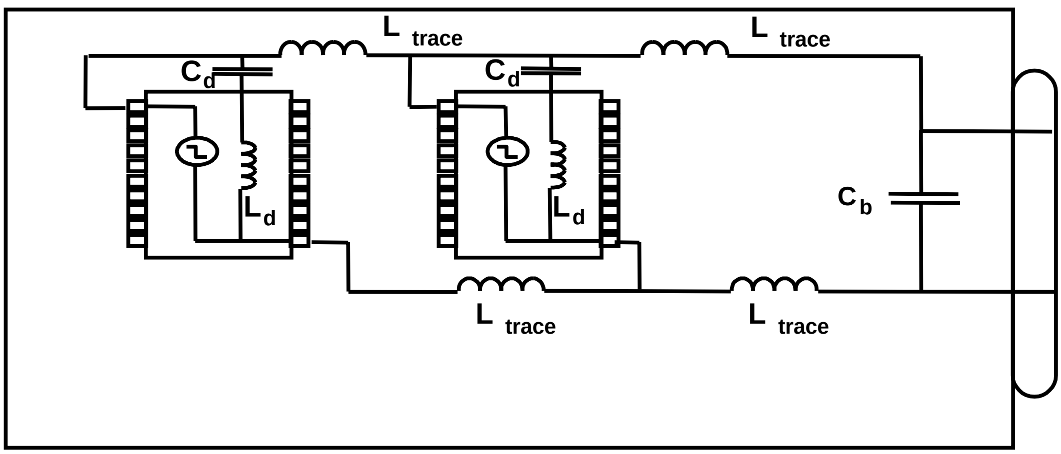


Power Distribution Model ~ (5 - 50 MHz)

Board without power and ground planes

Then local decoupling capacitors were included to increase the frequency range of effective decoupling.

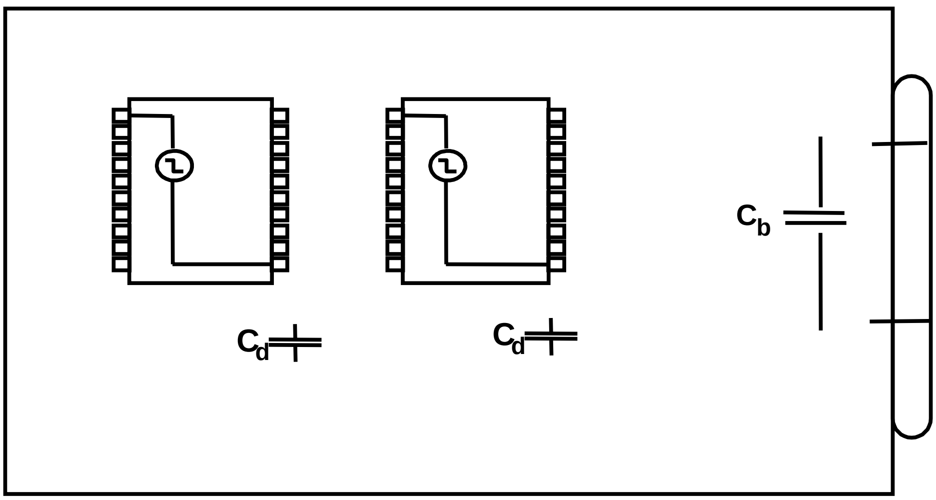
What is the solution above 50 MHz?



Power Distribution Model ~ (50 - 500 MHz)

Board without power and ground planes

What is the solution above 50 MHz?

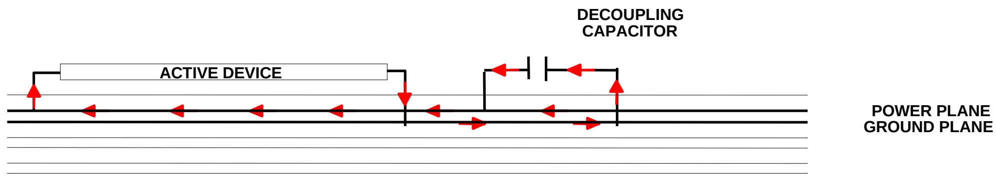


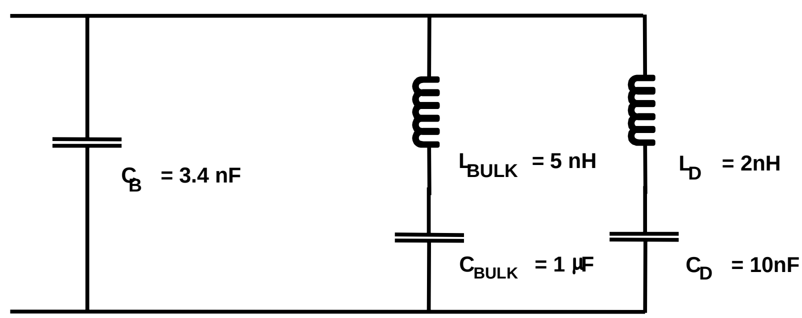
Power Distribution Model ~ (5 - 500 MHz)

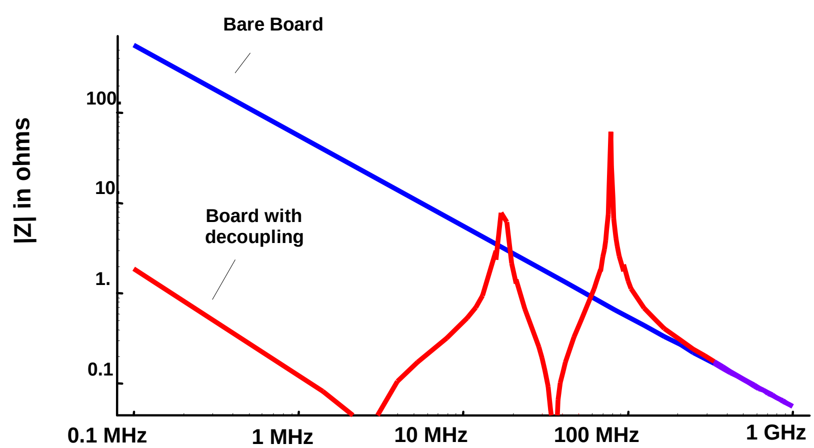
Board with power and ground planes

Power and ground planes are important when significant energy is drawn from the power bus at frequencies above 50 MHz. They provide a low inductance connection to decoupling capacitors (and yes, they also provide interplane capacitance).

How can we model boards with planes?

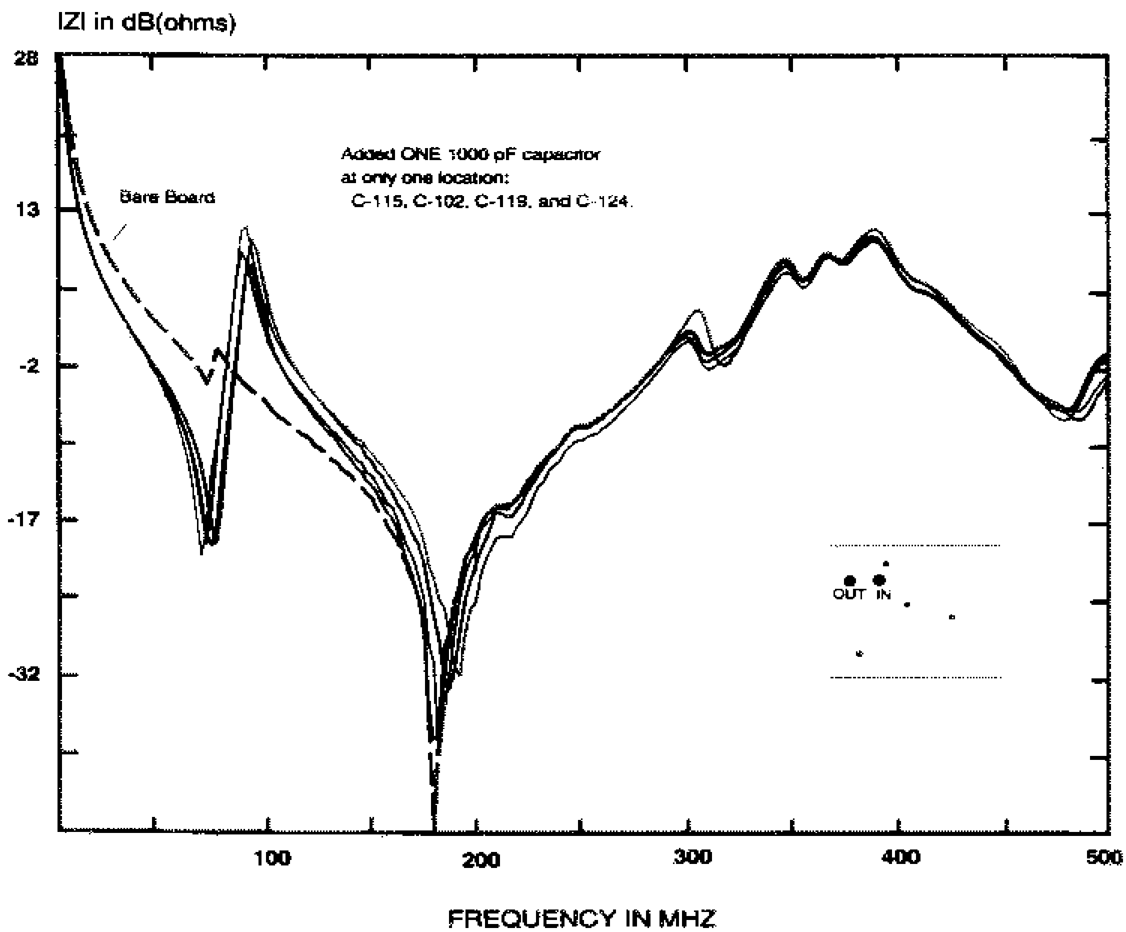






A discussion of power bus modeling of boards with power and ground planes accompanied this transparency.

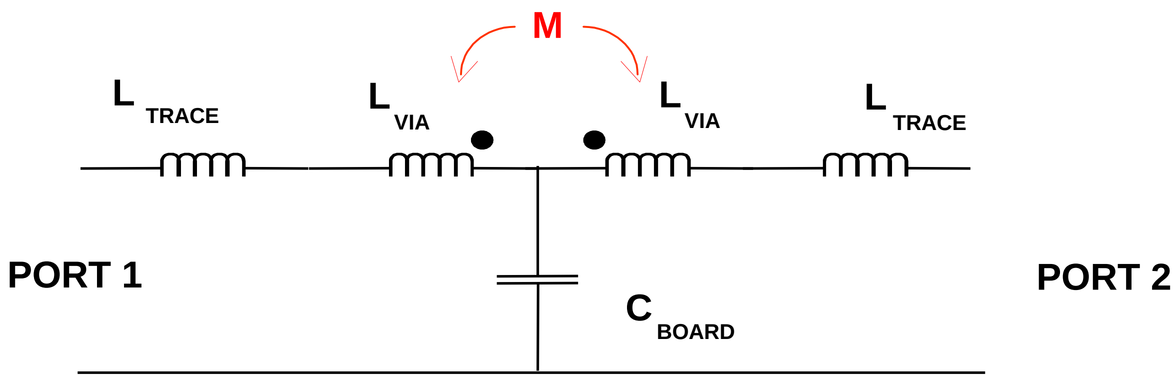
10-Layer Board Impedance Measurement

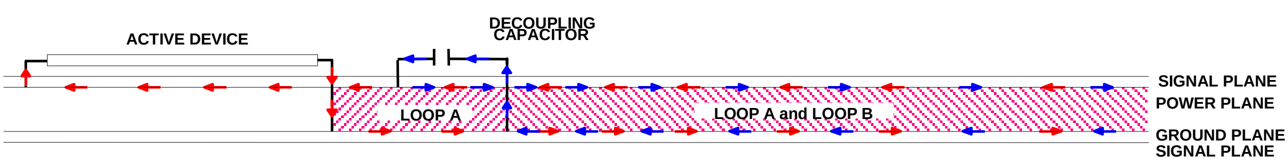


Effect of placing a single 1000 pF capacitor at different places on the board

On boards with closely spaced planes, the location of a single decoupling capacitor is not important. Current is drawn from the planes at high frequencies and from the capacitors with the lowest connection inductance at lower frequencies.

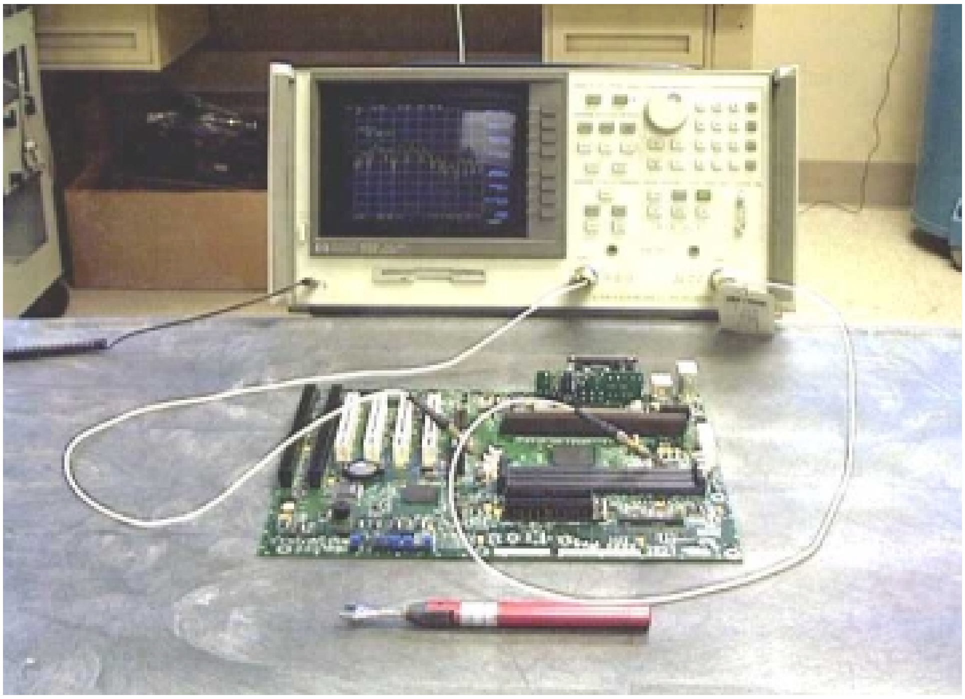
4-Layer Board Decoupling

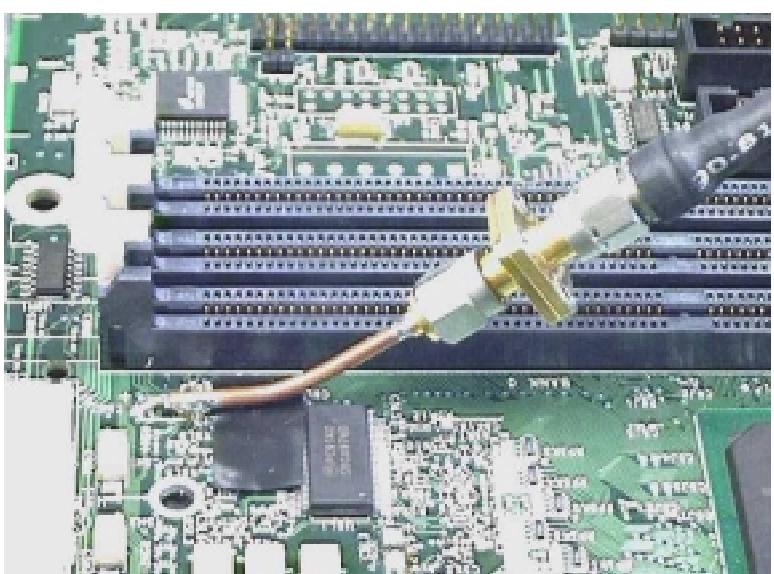




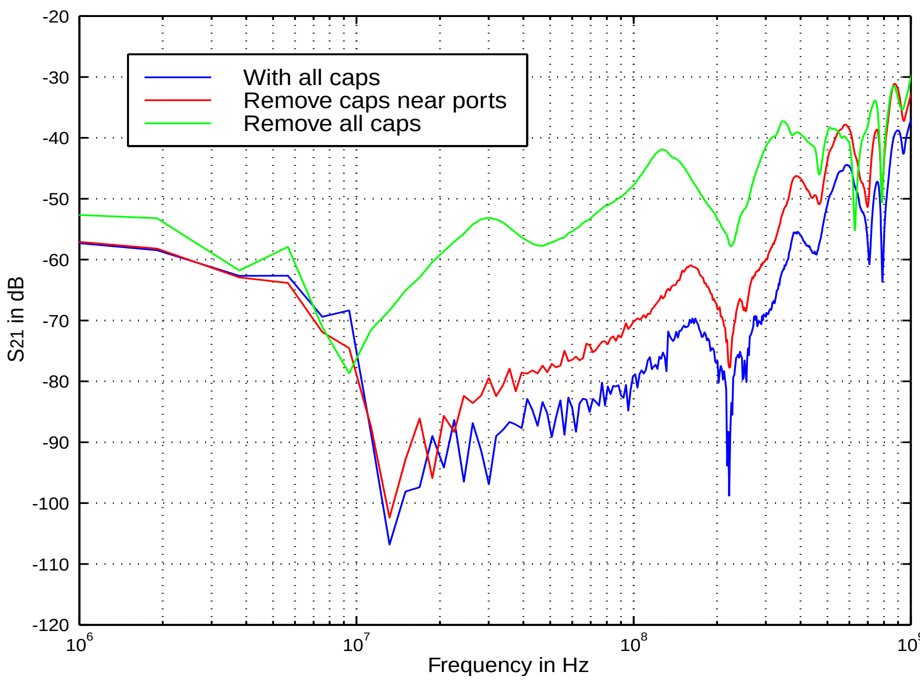
On boards with a spacing between power and ground planes of ~30 mils (0.75 mm) or more, the inductance of the planes can no longer be neglected. In particular, the mutual inductance between the vias of the active device and the vias of the decoupling capacitor are important. The mutual inductance will tend to cause the majority of the current to be drawn from the nearest decoupling capacitor and not from the planes.

4-Layer Board Measurements



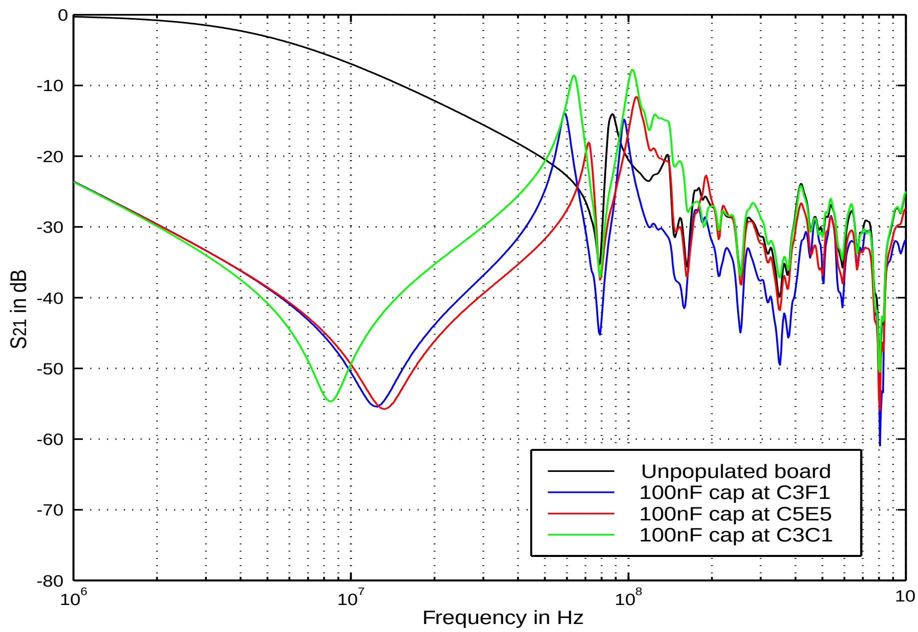


4-Layer Board Measurements

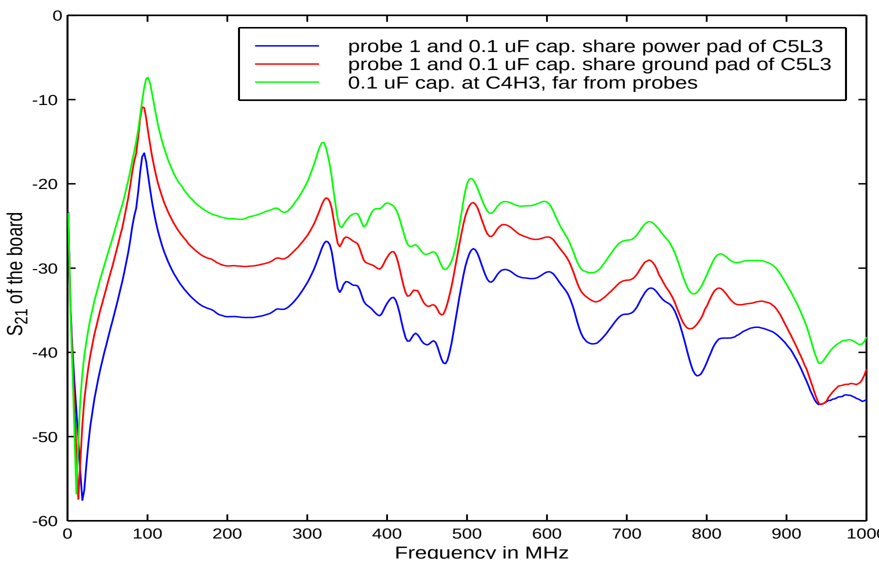


On 4-Layer boards with a 30-mil or greater spacing between the planes, current is drawn from the nearest well-connected capacitors.

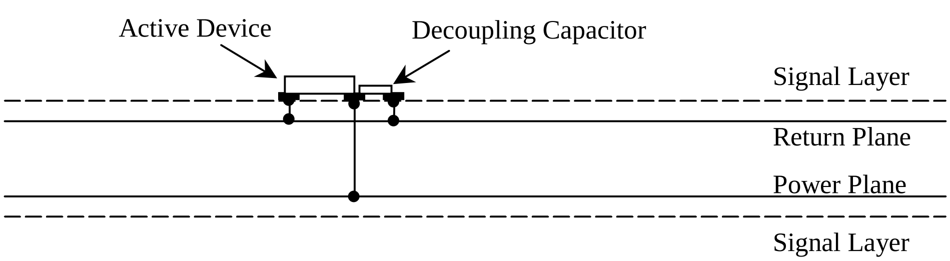
4-Layer Board Measurements

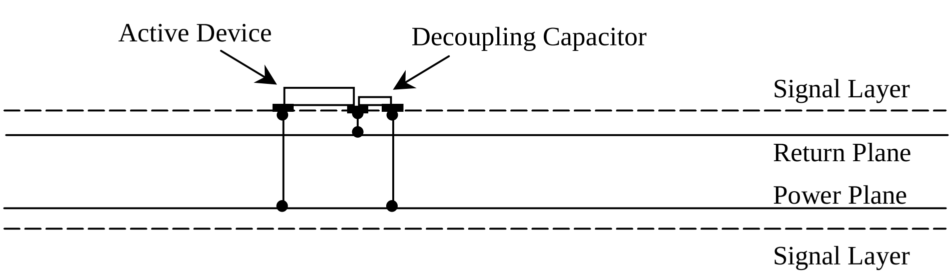


4-Layer Board Measurements



$|S_{21}|$ With Capacitor Sharing One Pad With Port 1





Sharing the via that extends between the planes maximizes mutual inductance, but it is not worth doing if you need to put traces on your decoupling capacitor pads.

References

T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. Hockanson, “Power Bus Decoupling on Multilayer Printed Circuit Boards,” *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-37, no. 2, May 1995, pp. 155-166.

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Power Bus Decoupling Summary

On boards with closely spaced* power and ground planes:

the location of the decoupling capacitors is not critical

the value of the local decoupling capacitors is not critical, but it must be greater than the interplane capacitance

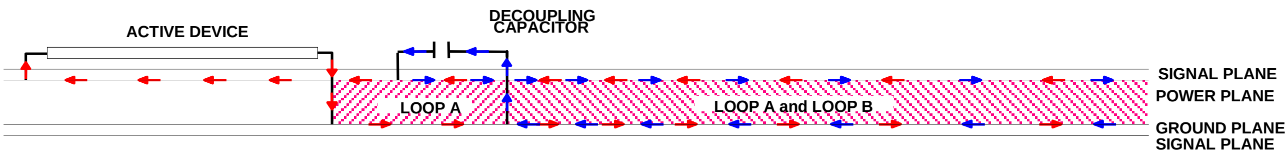
the inductance of the connection is the most important parameter of a local decoupling capacitor

none of the local decoupling capacitors are effective above a couple hundred megahertz

none of the local decoupling capacitors are supplying significant charge in the first few nanoseconds of a transition.

*The definition of "closely spaced" depends on the size of the board and the dielectric properties of the board. For most boards this is approximately 10 mils or less.

Power Bus Decoupling Summary



On boards with widely spaced* power and ground planes:

local decoupling capacitors should be located as close to the active device as possible

the value of the local decoupling capacitors should be 10,000 pF or greater

the inductance of the connection is the most important parameter of a local decoupling capacitor

local decoupling capacitors can be effective up to 1 GHz or higher if they are connected properly.

There are exceptions to every rule, so seek the advice of your company EMC laboratory when deciding on the amount of decoupling and how to implement it.

*The definition of "widely spaced" depends on the size of the board and the dielectric properties of the board. For most boards this is approximately 30 mils or more.