CMOS Technology & Business Trends

Can the semiconductor industry afford to continue advancing?

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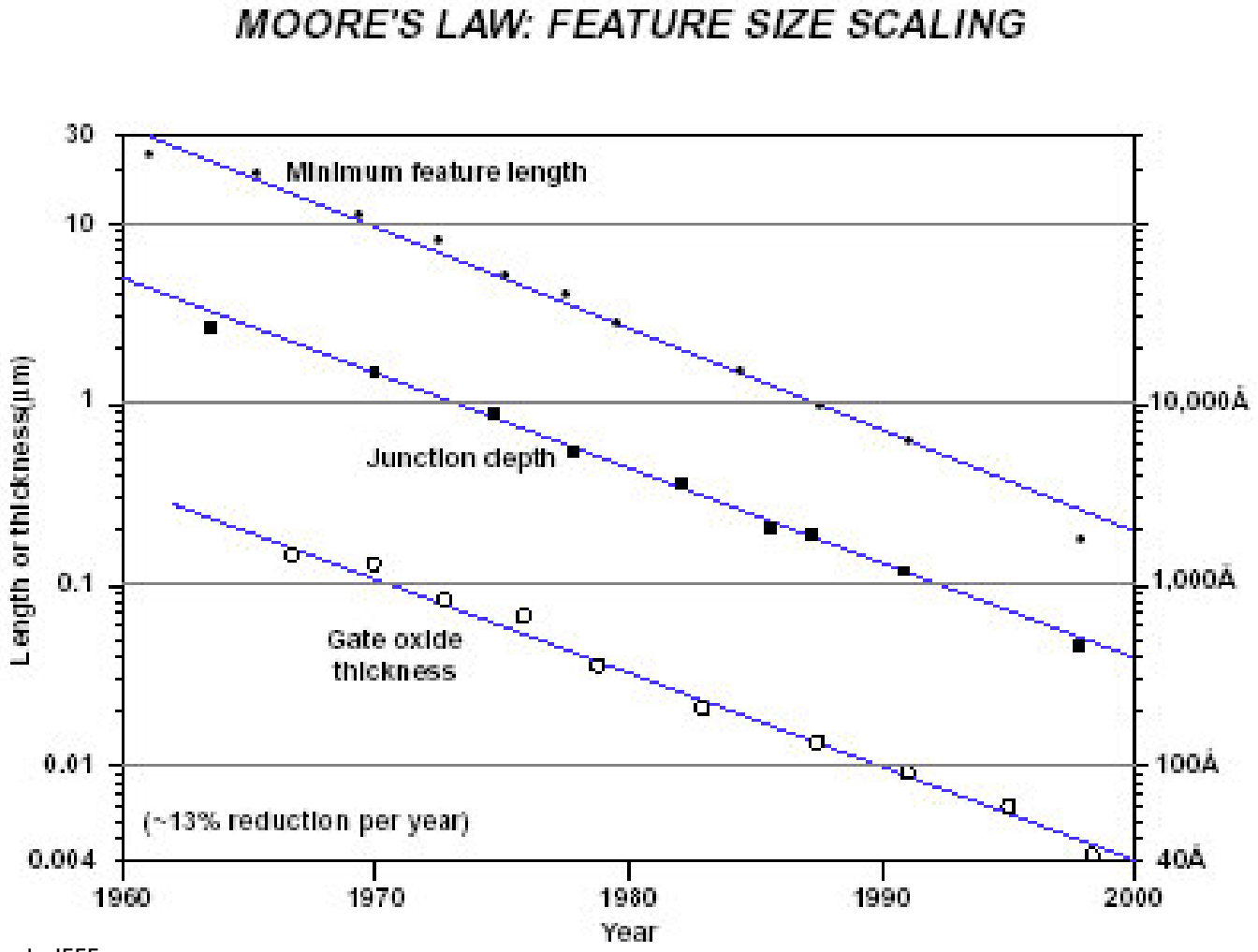
Disclaimers

- Not a thoroughly researched paper – just an accumulation of observations by longtime worker in the field made to provoke thought
- These opinions are my own, not Agilent Technologies'
- Many figures & illustrations are from the *2002 Intel Developer's Forum*
  - Copyrighted but publicly available
  - I have similar information from other sources but obtained it under condition of nondisclosure
  - My conclusion is different than Intel's

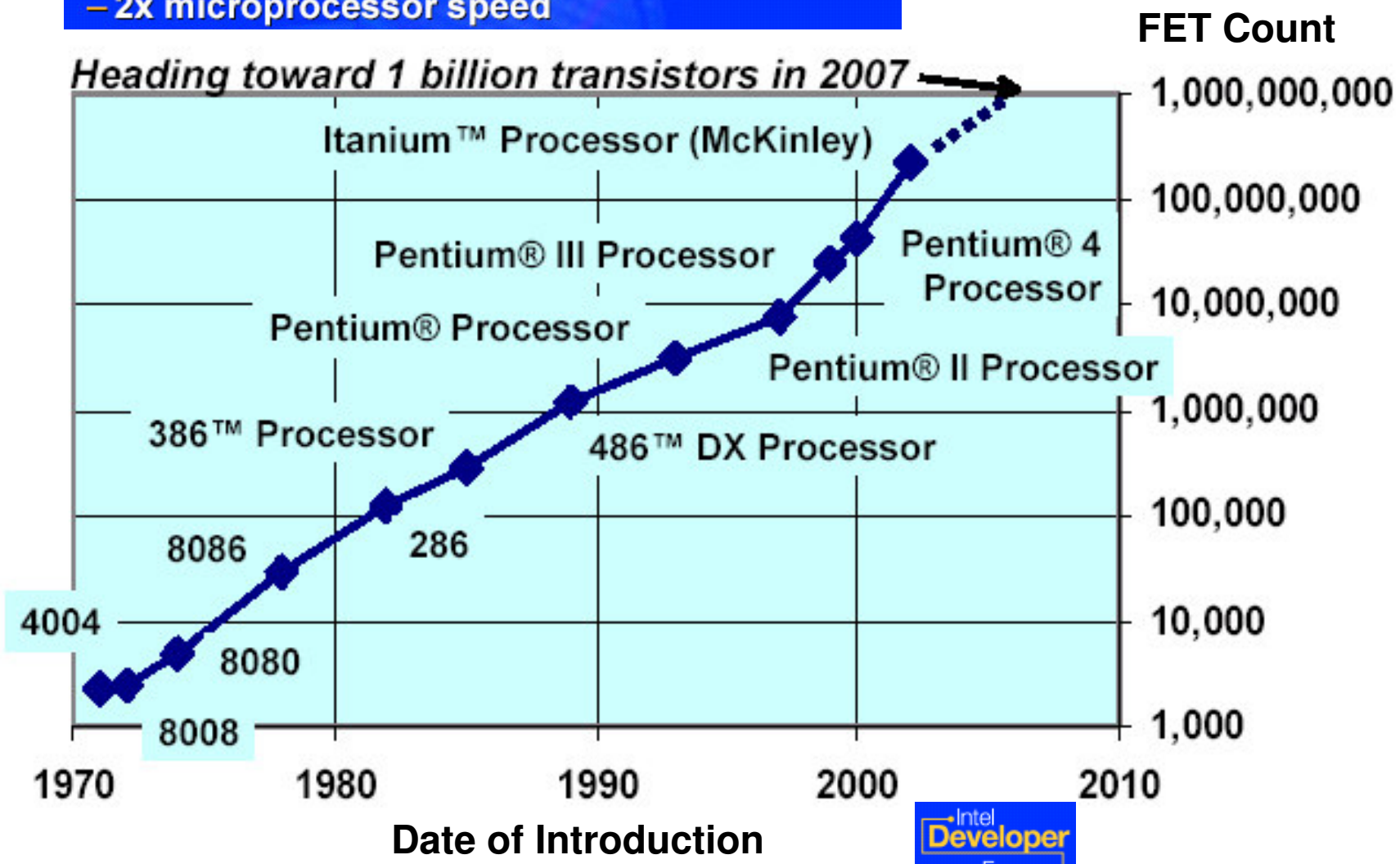
The Past – The Legend

The semiconductor industry, lead by CMOS technology, has had an astounding run of increasing functionality and performance at lower cost and power for over 40 years.

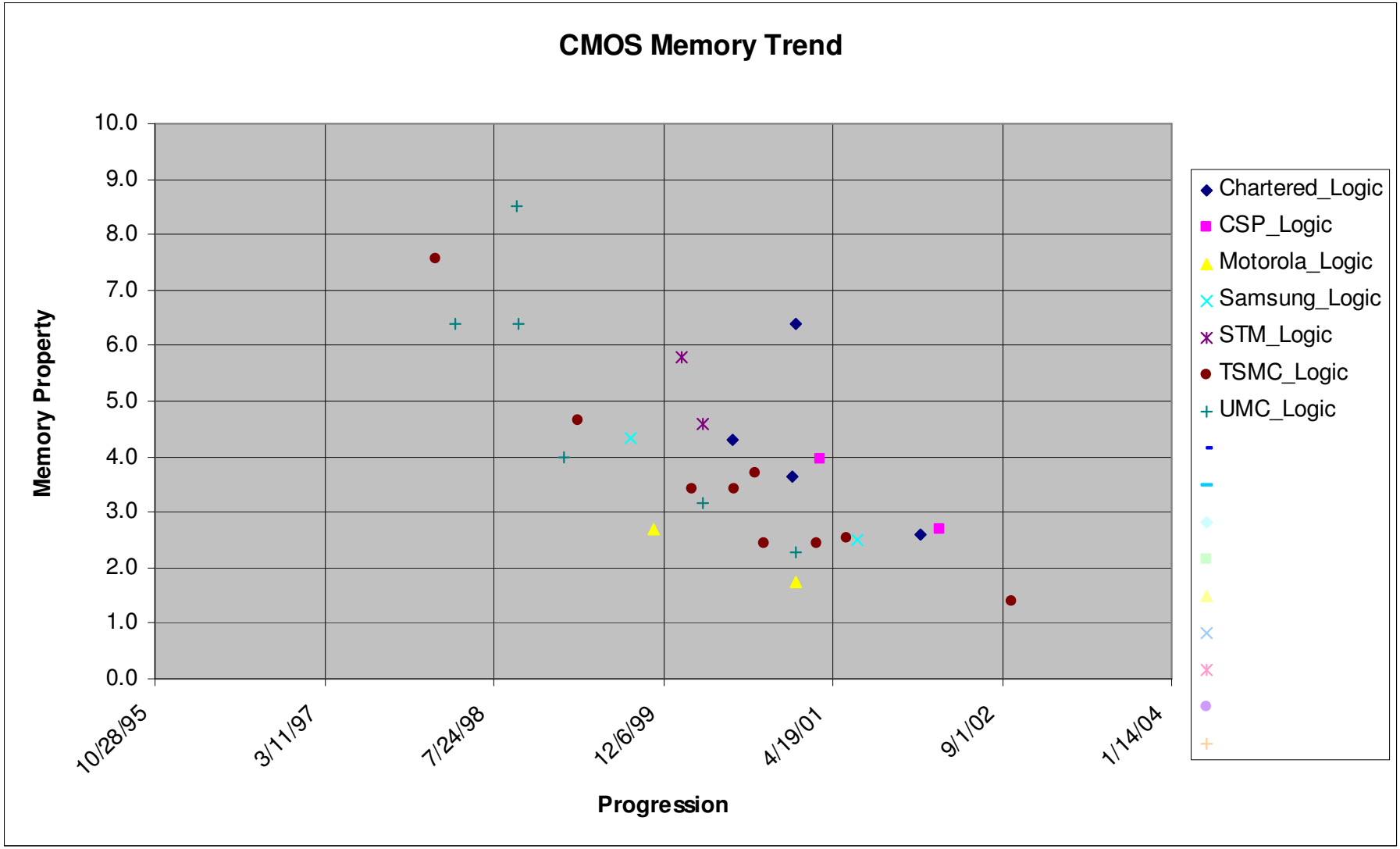


Achievement: Intel Processor Lineage

New technology generation every 2 years
- 2x die per wafer with ½ transistor cost
- 2x microprocessor speed

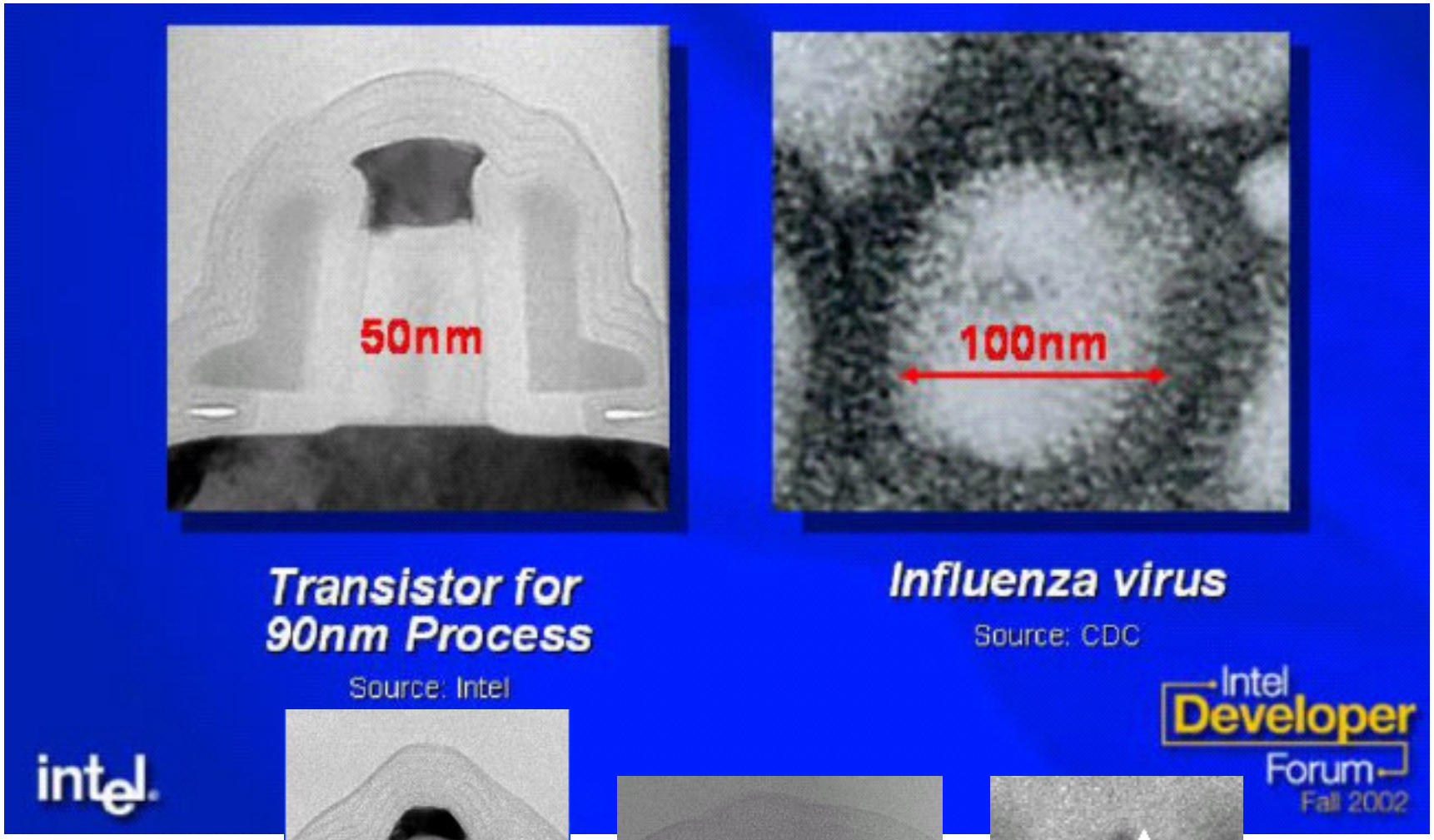


Achievement: CMOS SRAM Cell Area



SRAM Cell Area (μm^2) vs. PP Date

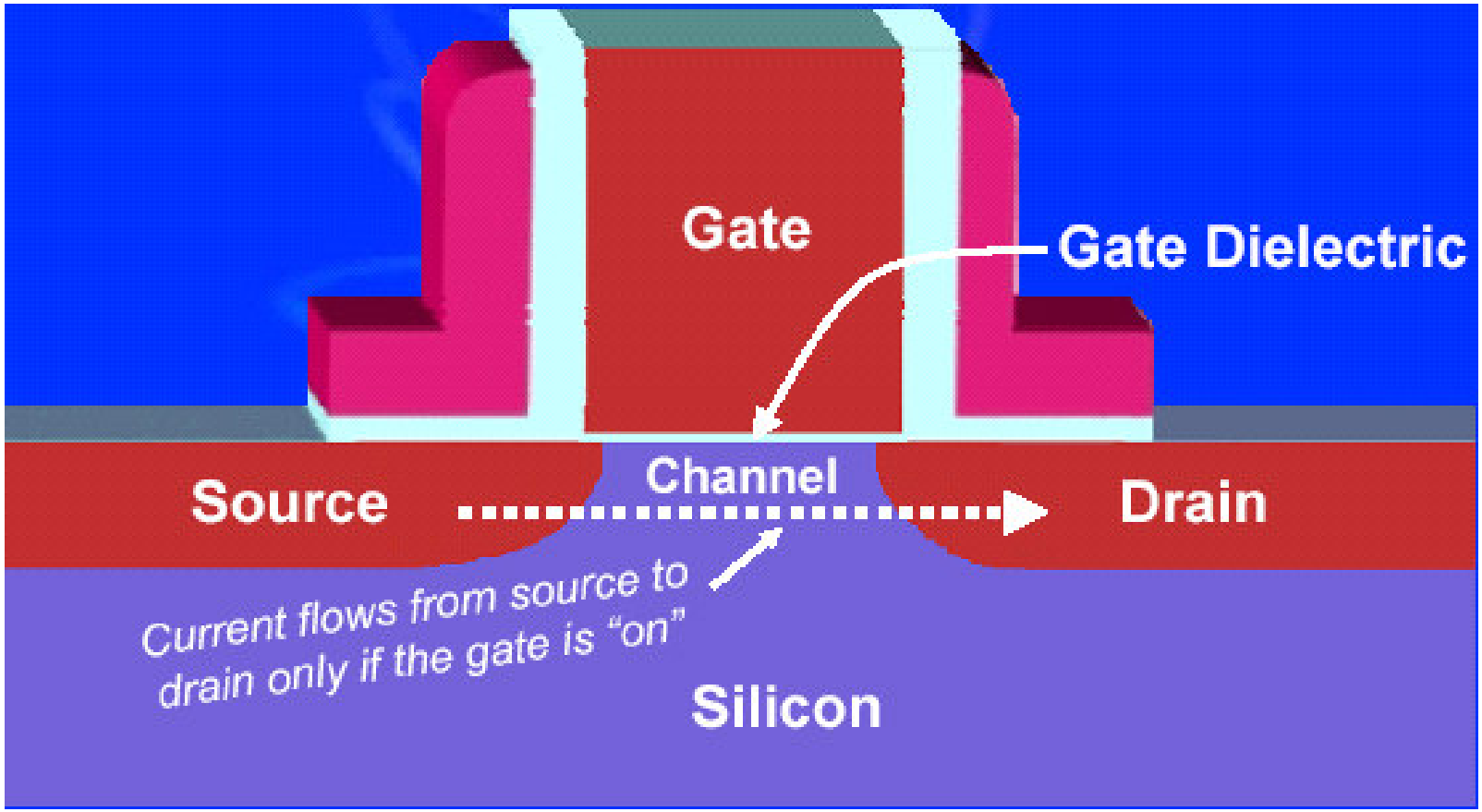
Achievement: The Shrinking MOSFET



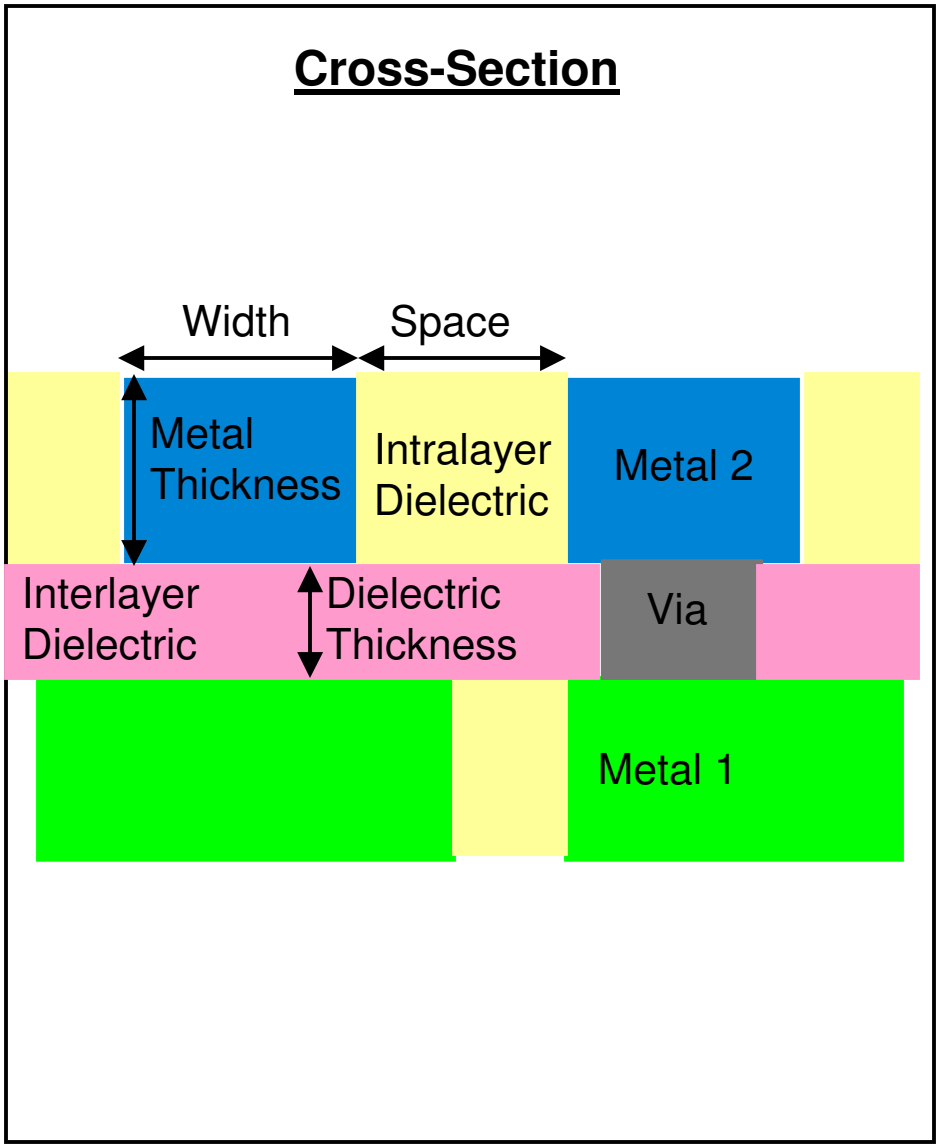
The Present – The Challenge

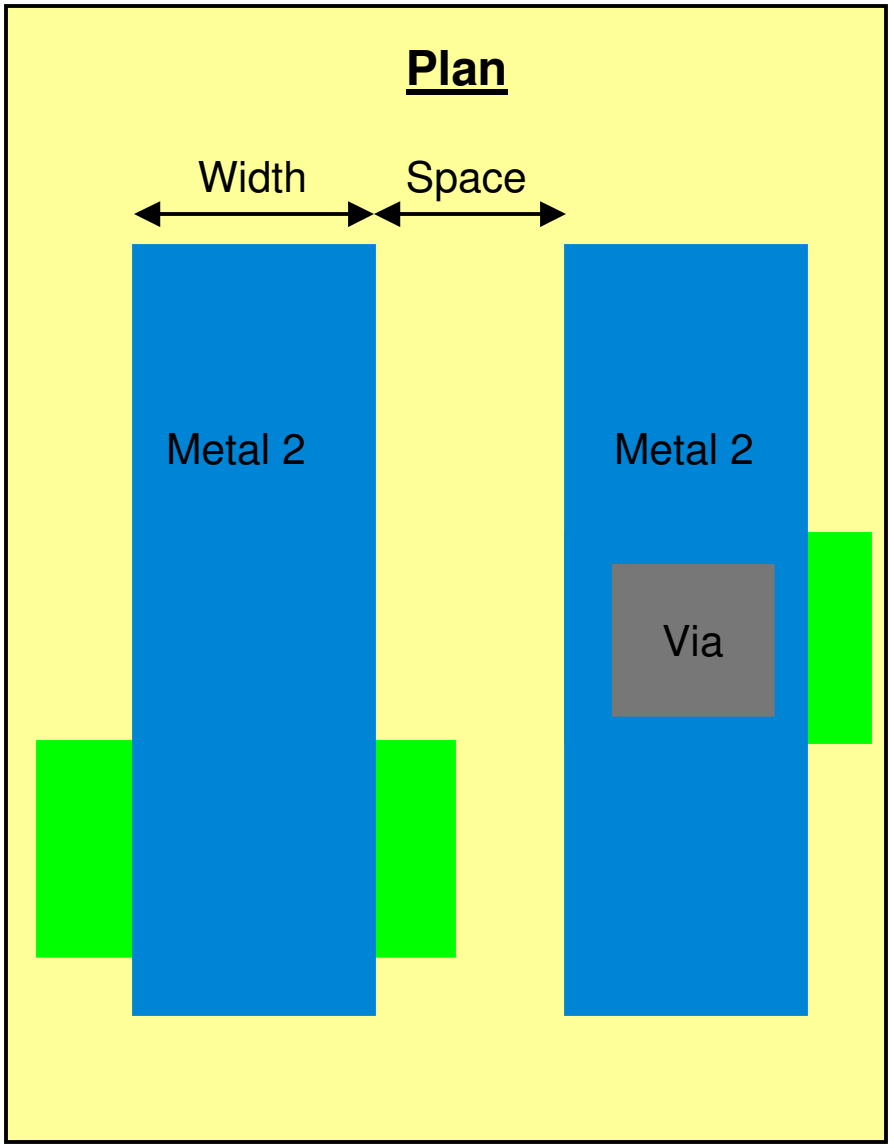
- Semiconductor industry has hit some inflection points
- Technical:
  - Changes in materials
  - New reliability mechanisms
  - Power consumption
- Business:
  - Megafabs
  - Fragmented value chain
  - Mask costs
  - Minimum lot costs
  - Design costs
- Will these be overcome as past obstacles have or will they profoundly change the character of the industry?

The MOSFET


Gate
Gate Dielectric
Source
Channel
Drain
Current flows from source to drain only if the gate is "on"
Silicon

Interconnect (Wiring)





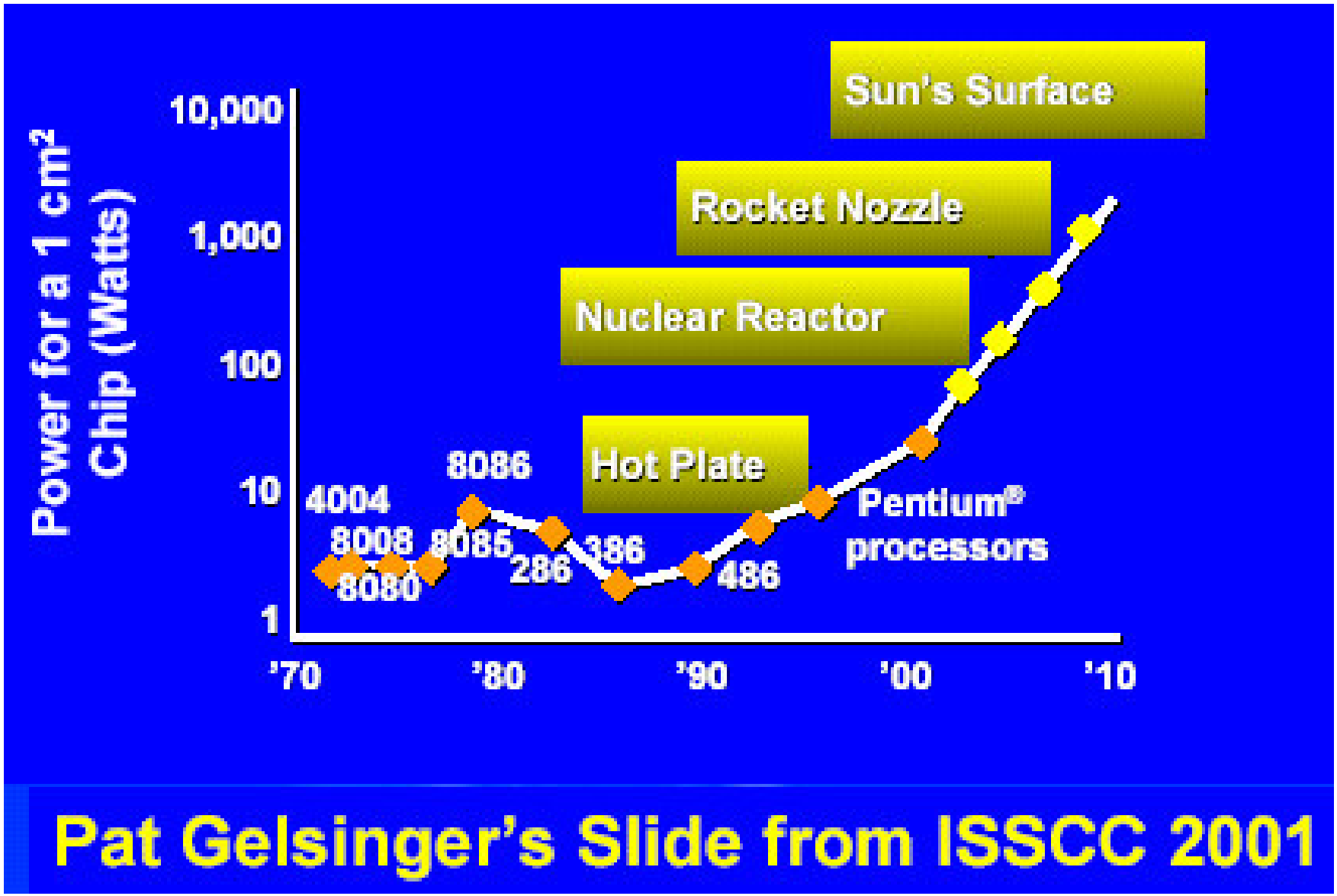
What Enabled These Achievements

- Device Structures
  - Planar MOSFET
  - Lateral scaling
- Materials
  - Semiconductor – Silicon
  - Insulator – SiO_2
    - MOSFET gate
    - Interconnect
  - Conductor - Aluminum
- Manufacturing
  - Patterning by photolithography & etch
    - Features > wavelength of light
    - Masks made by e-beam & resemble circuit
  - Material formation by thin film deposition & ion implantation
  - Smaller $\Rightarrow$ cheaper, faster, lower power
- Design
  - Automated physical design
  - Simulation of lumped devices
- Business Model – Integrated Device Manufacturer

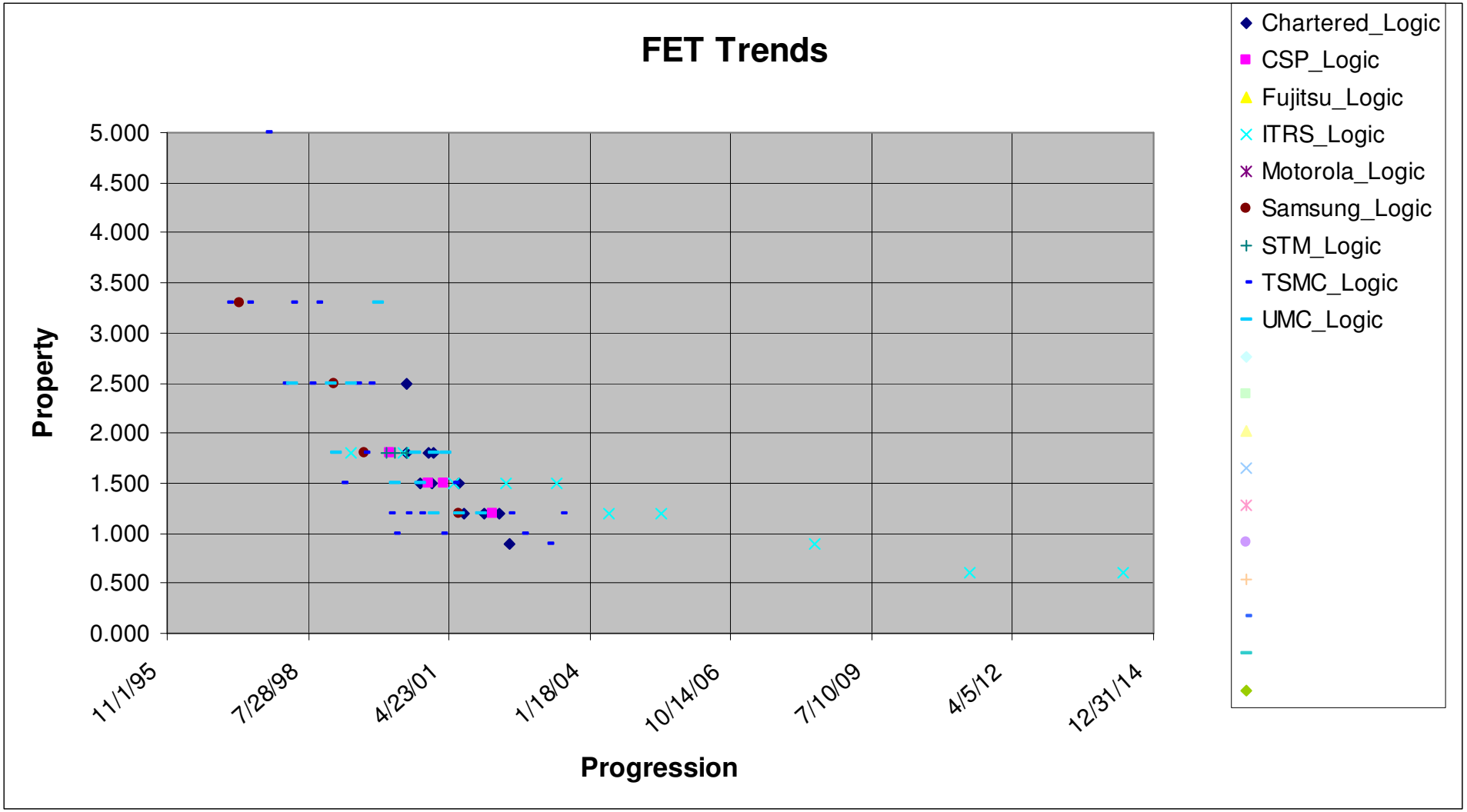
Limits to Enablers – Inflection Pts.

- Device Structures
  - Vertical dimensions don't scale as much as lateral ⇒ Interconnect R & C, Cross-talk
  - High electric fields ⇒ Breakdown, Hot carriers
- Materials
  - Semiconductor – velocity saturation, breakdown
  - Insulator – current tunnels through thin layers, TDDB
  - Conductor – resistance, high current density causes EM
- Manufacturing
  - Lithography – Features smaller than wavelength of available light
  - Economics – lower cost/function only if lots of functions
  - Can't risk differentiating technology
- Design
  - Extreme complexity – integrate more & more types of functions
  - Distributed effects hard to simulate
  - Power dissipation rules performance
  - NRE more than startup can afford
- Business Model - Disaggregated value chain
  - Technology develop costs more than one company can afford
  - Fab cost more than one company can afford
  - Can't afford to design all IP blocks, other's IP required

Power Dissipation

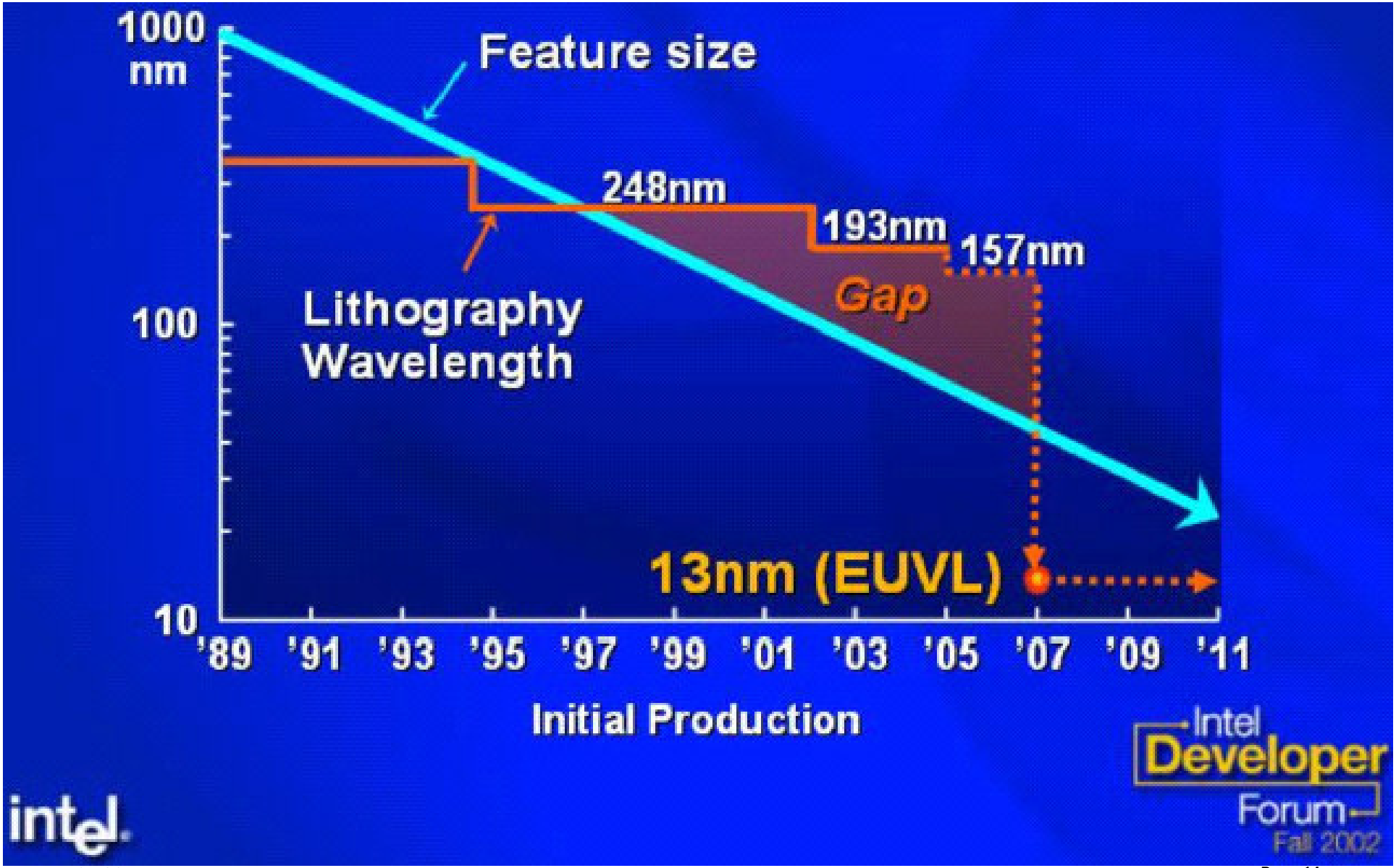


Dropping Supply Voltage



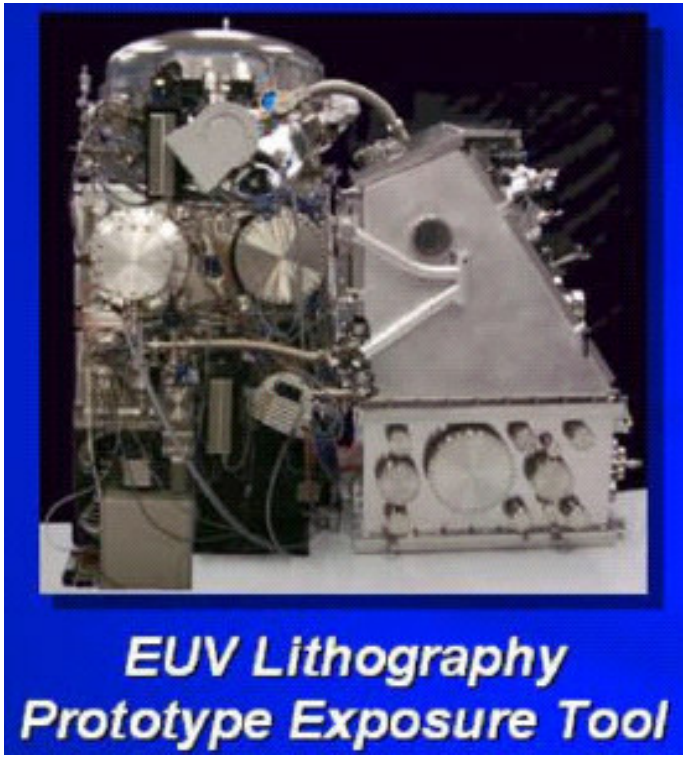
Supply Voltage (V) vs. PP Date

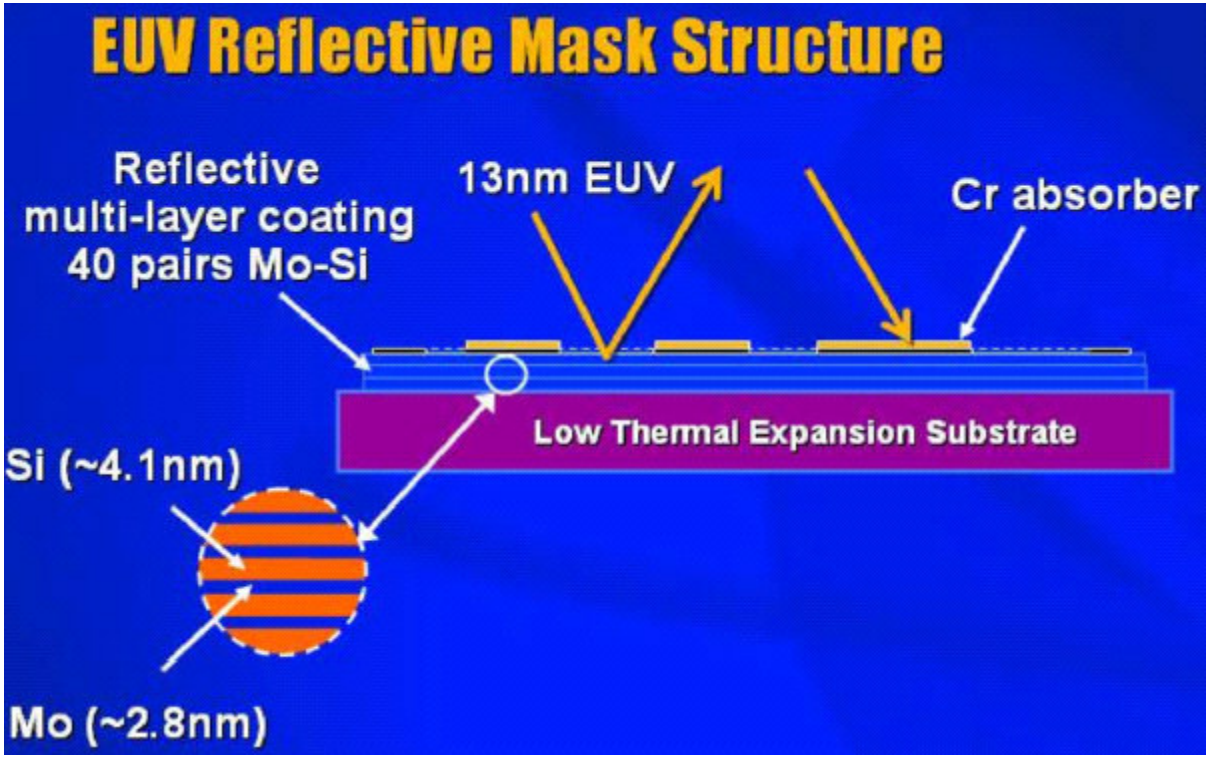
Lithography – Exceeding Optics



Lithography – Extreme UV

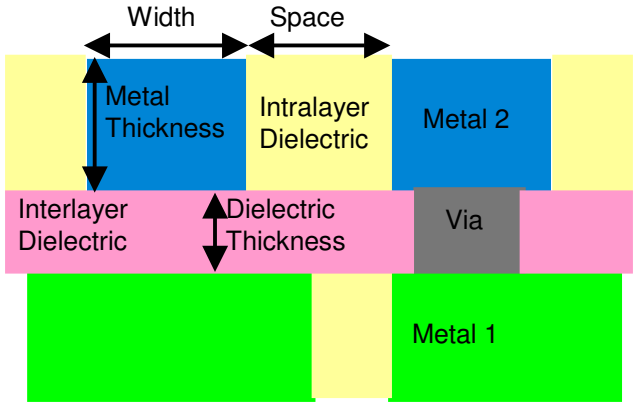
- EUV source is laser, not mercury lamp
- EUV absorbed by air ⇒ operate in vacuum
- EUV absorbed by glass ⇒
  - Use reflective optics
  - Use reflective masks
- EUV absorbed by metal ⇒ use Bragg reflectors





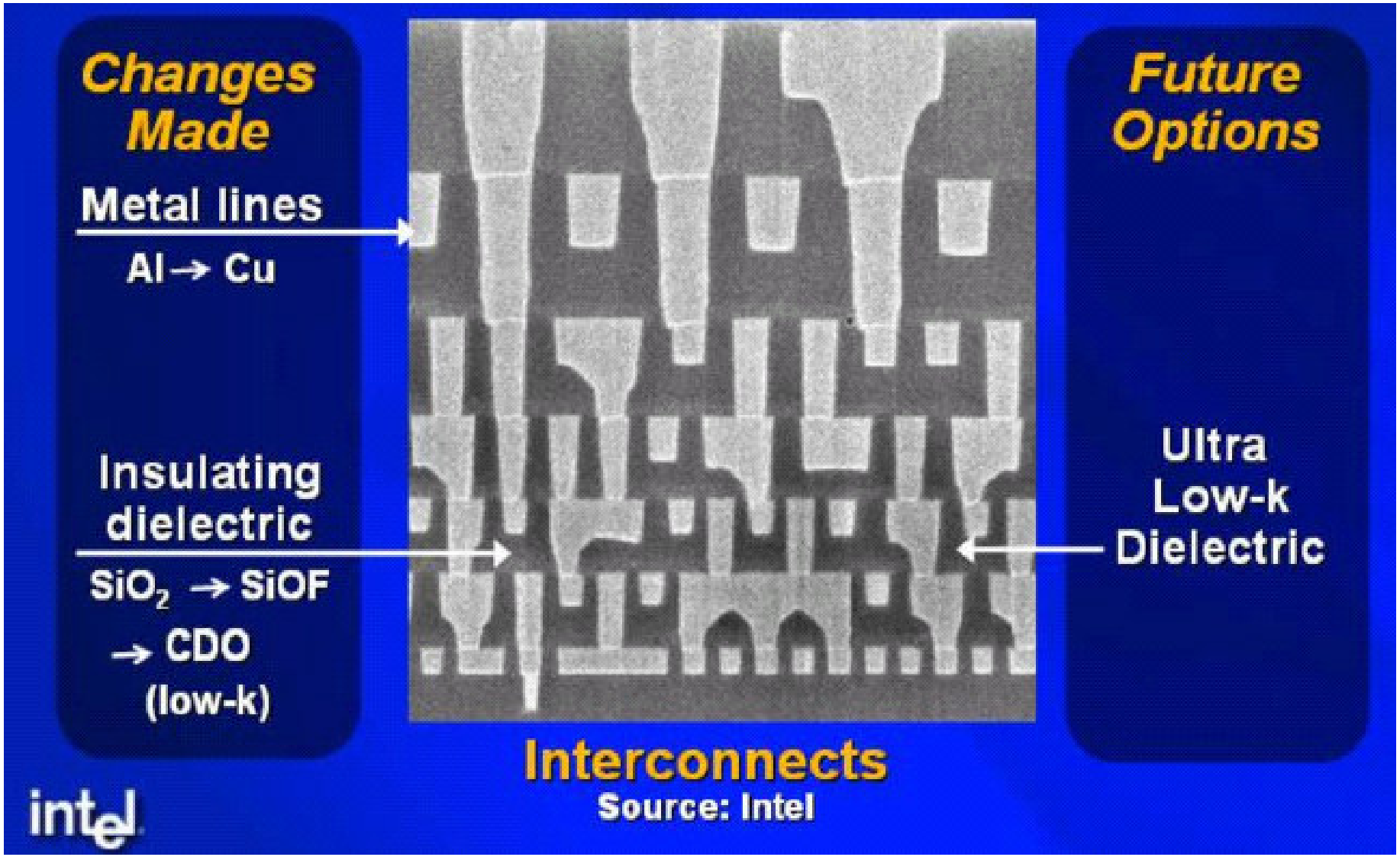
Interconnect Problems & Solutions

- Resistance & electromigration
  - Problem – Area & current scale in opposite directions while V decreases
  - Solutions & Issues
    - Higher aspect lines
      - Difficult patterning thick metal
      - Dielectric coverage
      - Higher intralevel capacitance
    - More metal layers ⇒ Complexity, yield
    - Replace Al with Cu for lower ρ, higher mass
      - Can't etch Cu ⇒ damascene process, reverse of Al
      - Cu causes leakage in Si & dielectrics ⇒ barrier jacket



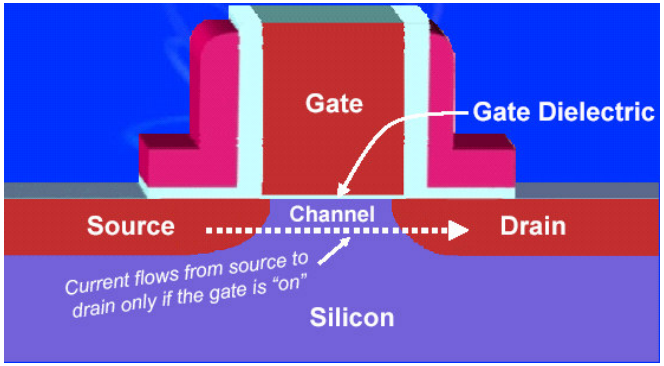
- Capacitance
  - Problem – Narrower space & thinner dielectric ⇒ higher C
  - Solution & Issues
    - Thinner metal by lower ρ
      - Risks EM
      - Higher R
    - Thicker dielectric ⇒ high aspect vias ⇒ hard to etch & fill
    - Lower dielectric constant κ (ε)
      - Poor mechanical strength
      - Poor adhesion
      - Unstable κ

Advanced Interconnect



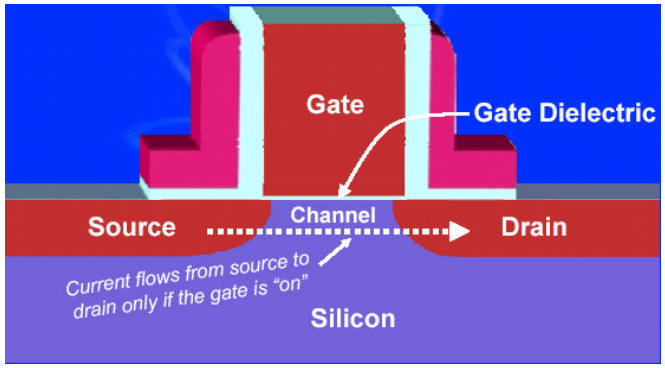
Transistor Problems & Solutions

- Off Leakage
  - Problem – High drain E field controls gate, punches thru to source
  - Solutions & Issues
    - Drop V ⇒ less drive I, IR drops
    - Channel engineering ⇒ complexity
    - SOI ⇒ defects, complexity, hysterisis
    - Dual gate ⇒ complex, not planar
- Hot Carriers
  - Problem – High E field accelerates carriers into gate degrading I-V
  - Solutions & Issues
    - Lower voltage ⇒ less drive I, IR drops
    - Drain engineering ⇒ Drain resistance, complexity
- Mobility Saturation
  - Problem – Carrier velocity not proportional to E at high field
  - Solution & Issues
    - SOI to achieve low off leak at low doping ⇒ defects, complexity, hysterisis
    - Strained silicon to increase intrinsic mobility ⇒ defects, complexity
    - Compound semiconductors ⇒ major integration problems!!!

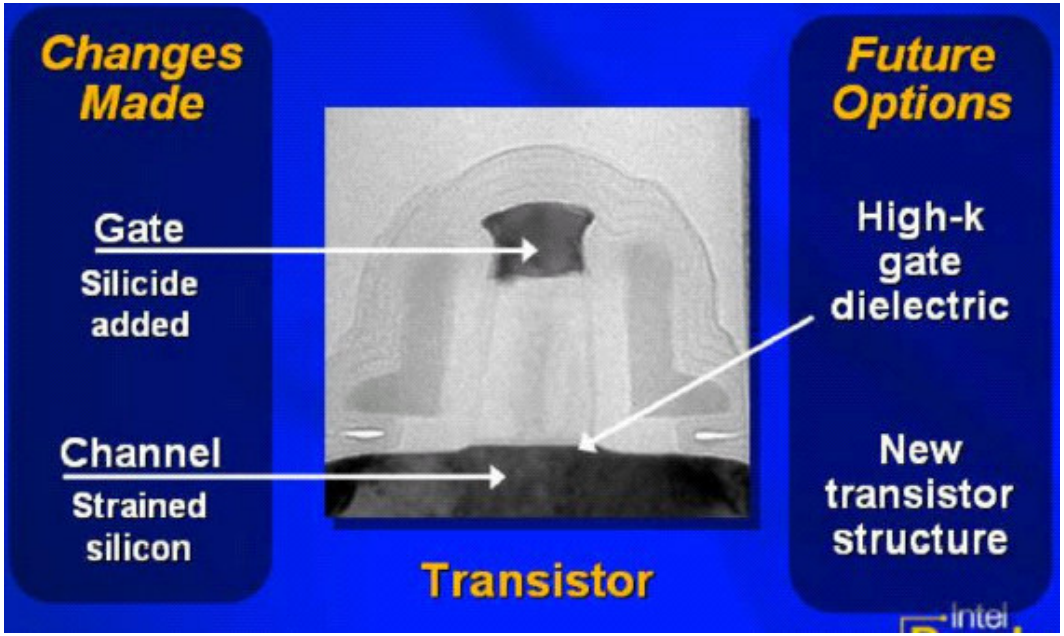


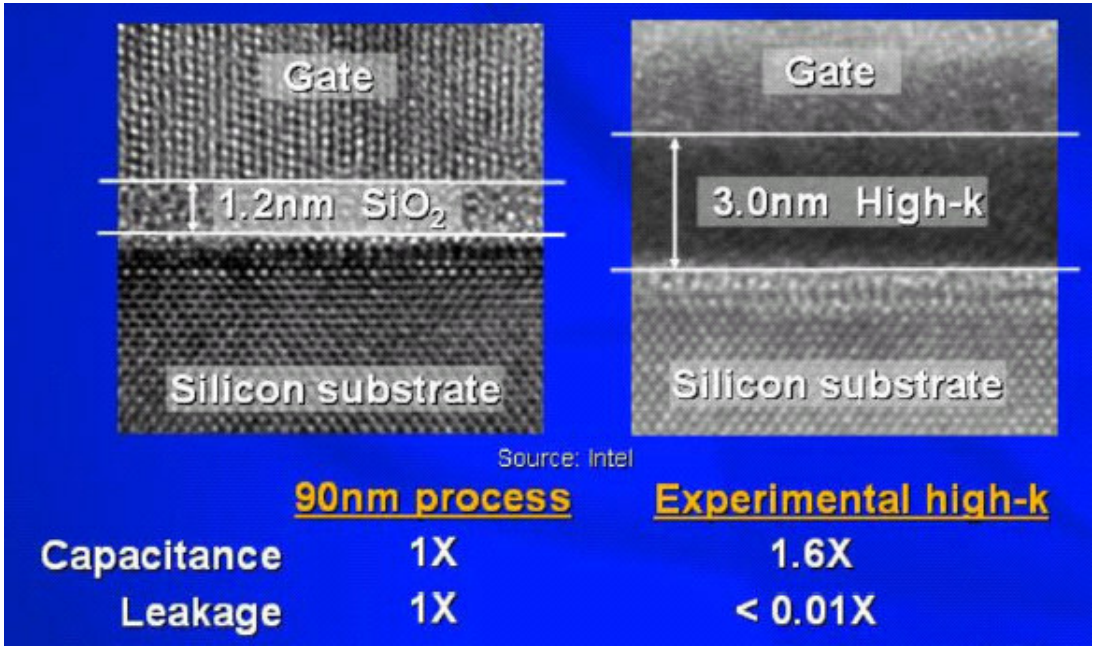
Transistor Problems & Solutions (cont.)

- Gate leakage
  - Problem – Quantum mechanical tunneling through thin insulators
  - Solution & Issues – High κ gate dielectric (HfO, ZrO) $\Rightarrow$ same E field at thicker dielectric
    - Film growth
    - Interface charge & scattering
- Parasitic Capacitance & Resistance
  - Problems
    - Higher doping for everything else increase S/D junction C
    - Shorter gates, smaller contacts increase gate and S/D R
  - Solutions & Issues
    - Decrease junction C with SOI $\Rightarrow$ defects, complexity, hysterisis
    - Decrease gate R with metal gate $\Rightarrow$ interface, integration



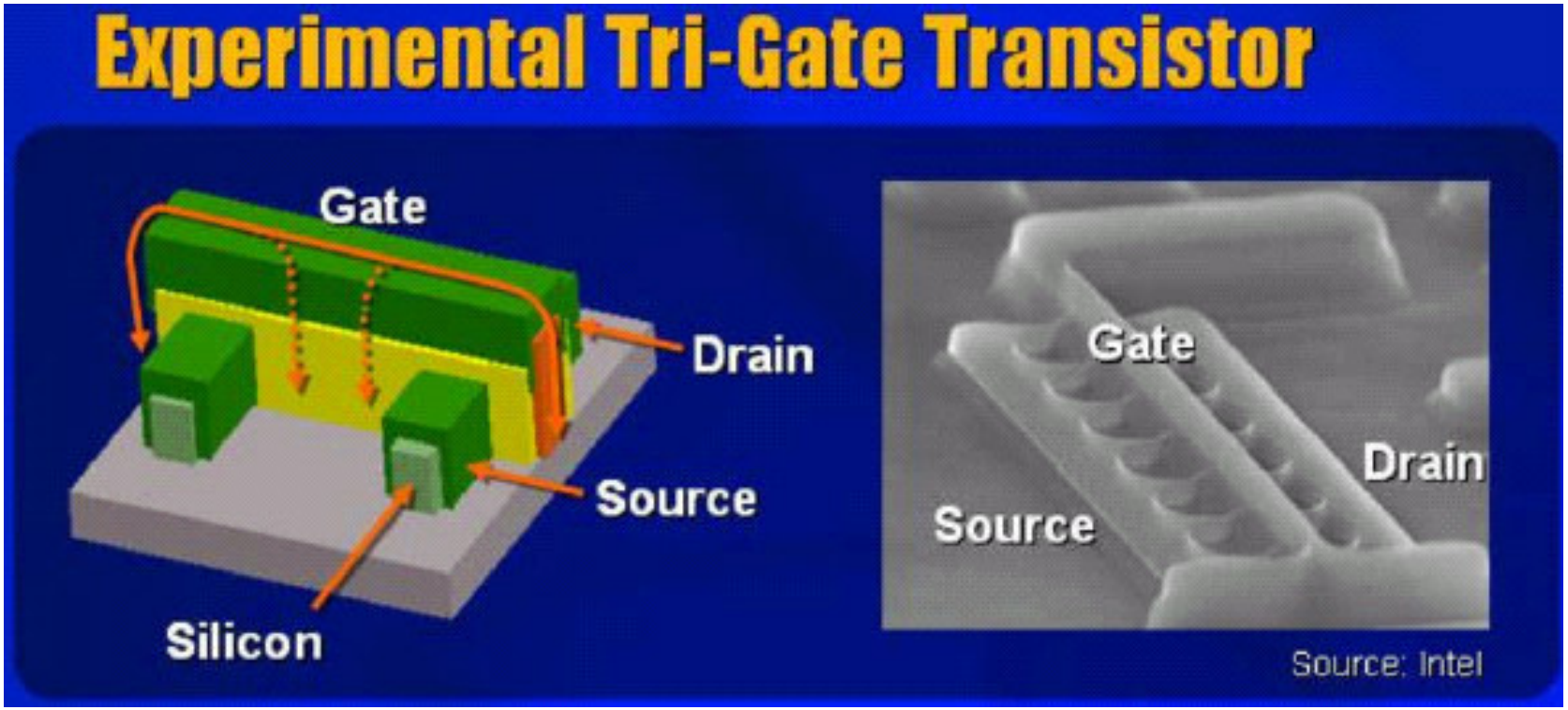
Transistors – New Materials





CMOS Technology Trends, IEEE
Nov. 6, 2002

Transistors – New Structures



Increasingly Important Defects

Defect/Fault Type	Causes
Open defects	• More metal layers & vias • Subtractive Cu replacing additive Al ⇒ discontinuous trench fill • Weak low K dielectrics
Bridging defects	• More metal layers • Subtractive Cu replacing additive Al ⇒ polish smearing
Delay faults	• Interconnect dominates delay & defect density ⇒ delay defects dominate • Common manifestation of open defect • Cross-talk causes signal-dependent delay
Cross-talk faults	• Interconnect dominates delay • Higher aspect metal spaces • Variable dielectric constant
Parametric faults	• Digital: Delay & Cross-talk faults • More analog/MS/RF circuitry ⇒ matching important • Matching difficult for very small devices • Microloading, lens uniformity, proximity effects ⇒ larger intra-die parameter variation

Intel's Conclusion

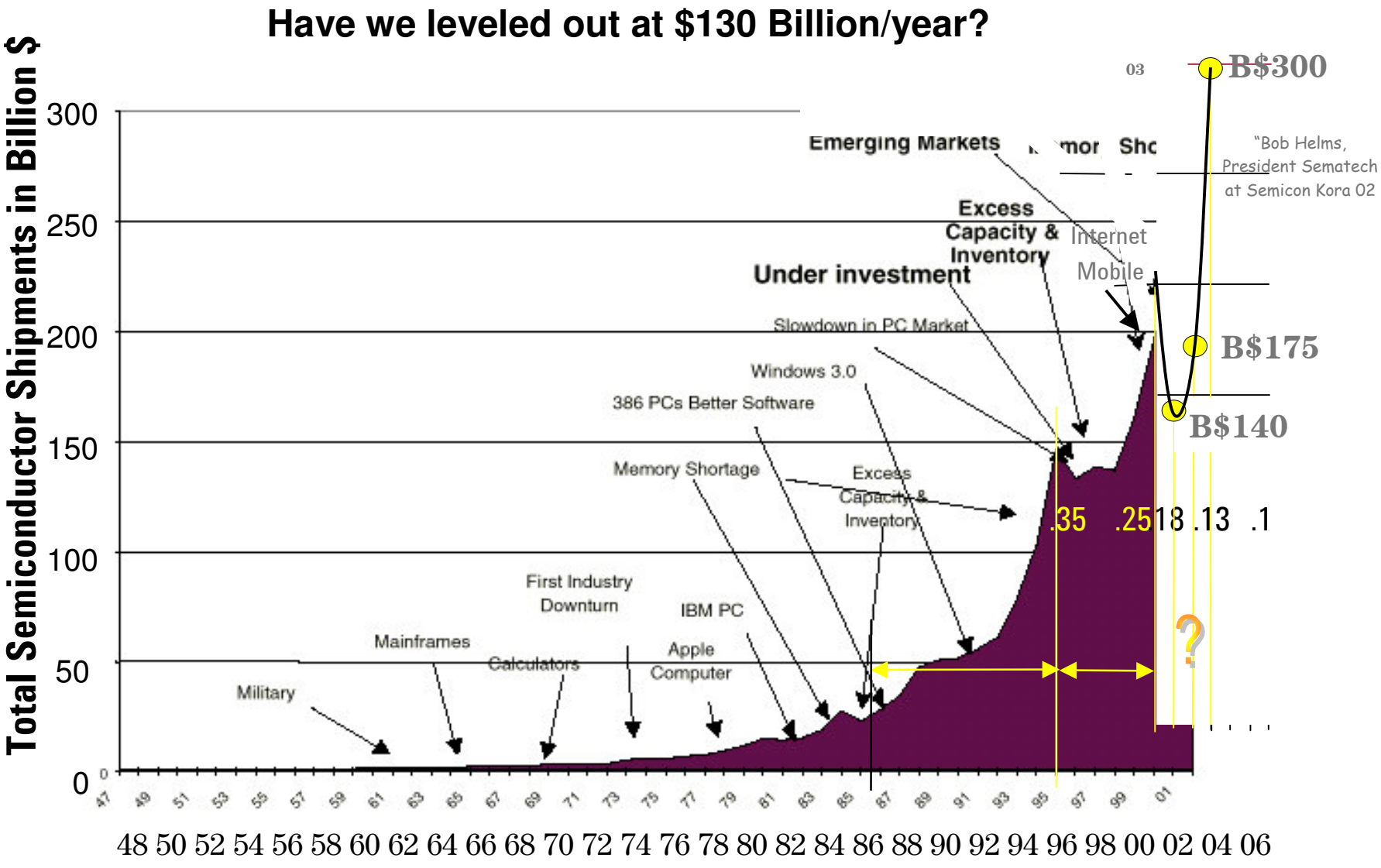
- We still have not found a fundamental barrier to Moore's Law
  - Silicon scaling will continue through the end of this decade
  - There will be a new generation every two years
- New materials and new structures are required
  - Lithography
  - Transistors
  - Interconnects
  - Packaging

But can we afford to do these … and for what kinds of products?

Business Challenges

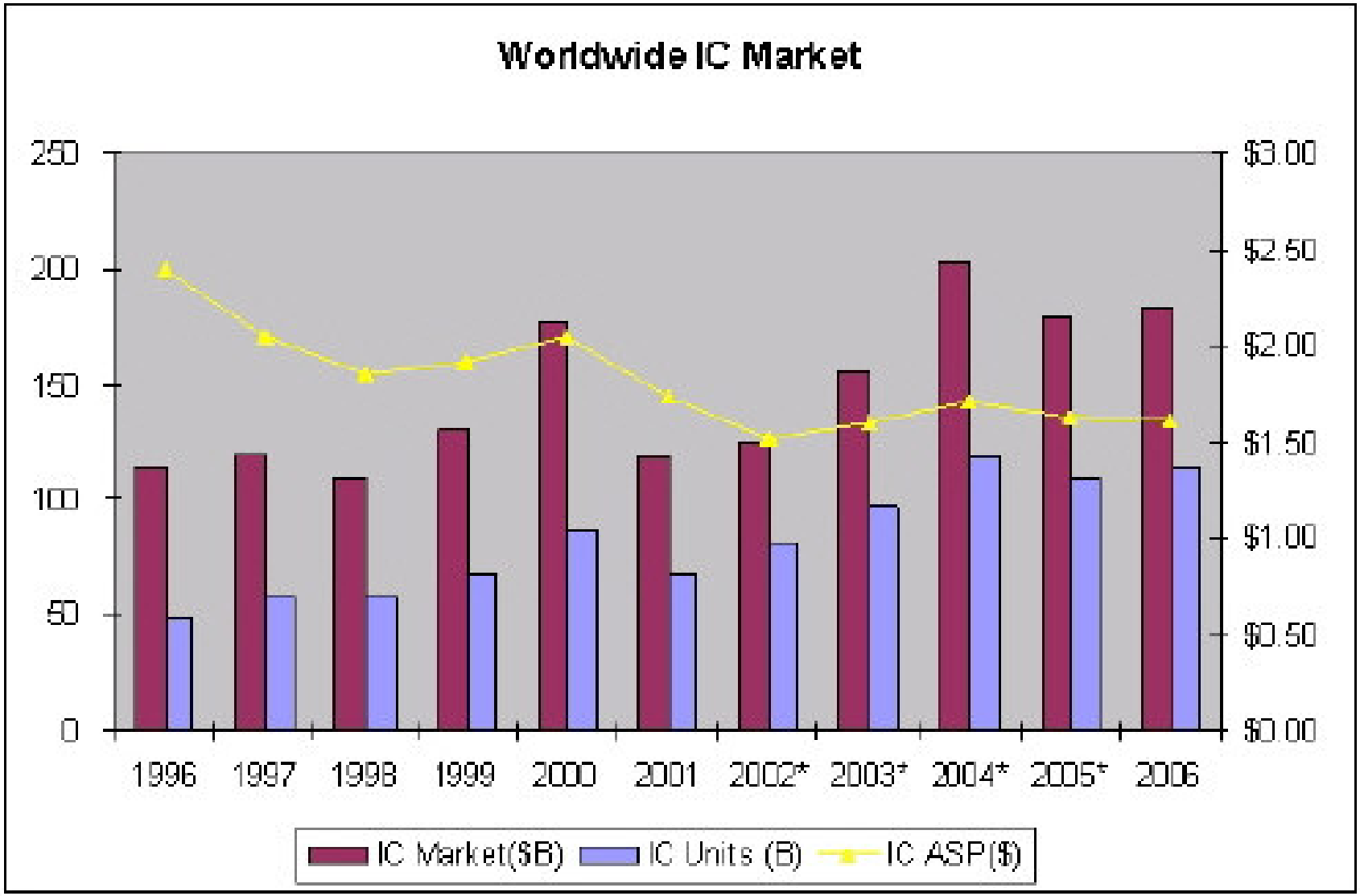
- "High tech" exempt from economy ⇒ *Is* the economy
- Market: industrial ⇒ consumer
- Skyrocketing design NRE
- Skyrocketing fab cost
- Skyrocketing process development cost
- Success determined by time to market & volume, not technology
- Individual companies can't afford to do everything themselves, not even in one area

The Semiconductor Roller Coaster



Semico Research until 2000, 2001-2006 guessed bathtub scenario

Recent WW IC Market



Changing End Uses

	Was	Is
Markets	❖Industrial ❖Military/Aerospace ❖High-end consumer	❖Consumer ❖Information utility infrastructure
Products	❖Minicomputers ❖Workstation computers ❖Personal computers ❖Industrial/laboratory instruments ❖Comms infrastructure	❖DVD/CD players ❖Cell phones ❖PDAs, MP3 players, other personal portable devices ❖Personal computers ❖Server computers ❖Comms switches & routers
Drivers	❖Digital speed ❖Density ❖Quality	❖Integration of diverse functions ❖Portability ❖Cost

Determinants of Cost

- Manufacturing
  - Recurring
    - Wafer cost
    - Yield
    - Test
    - Package
  - Nonrecurring
    - Masks
    - Characterization lot
- Design
  - Designer-months
  - Number of turns
  - EDA licenses
  - Design IP licenses

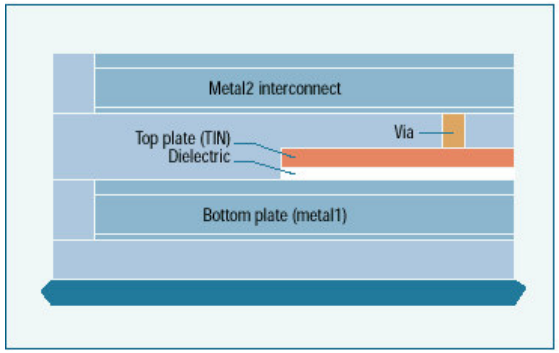
Integrating New Functions

Functions Beyond Digital

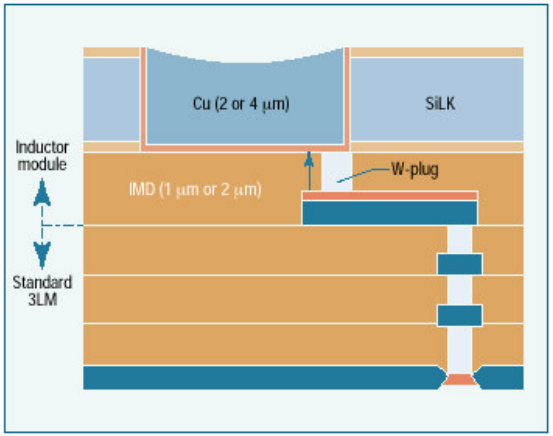
- Analog
- Radio
- High-speed serial comms
- Optical
- Sensors

Requiring New Devices

- Memory
  - High density – DRAM
  - Nonvolatile – Flash, Ferroelectric
- High quality passives for RF & analog
  - Inductor
  - Capacitor
  - Resonator
- Transistors
  - High V FET
  - Low leak, low power FET
  - High F_T BJT

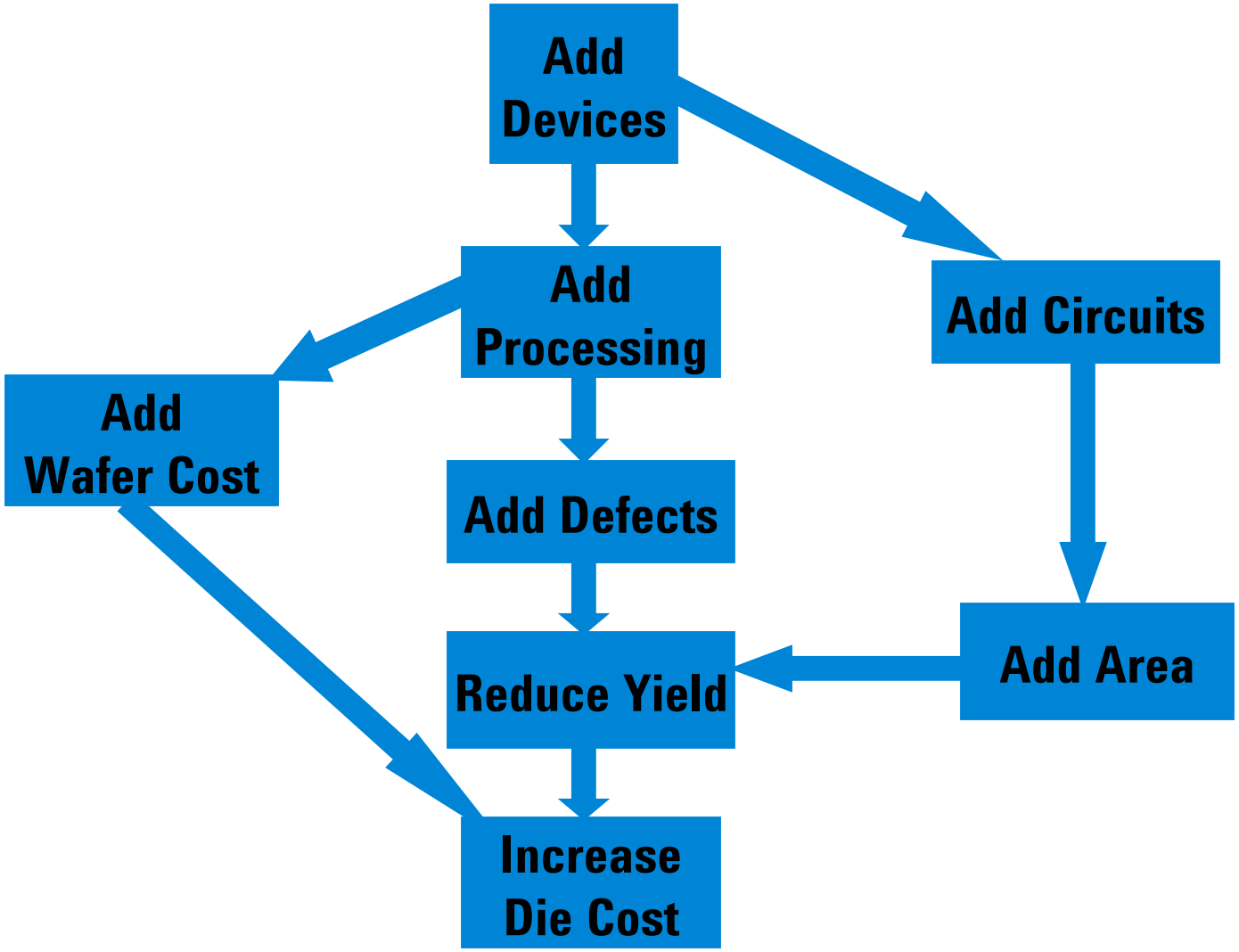


Capacitor

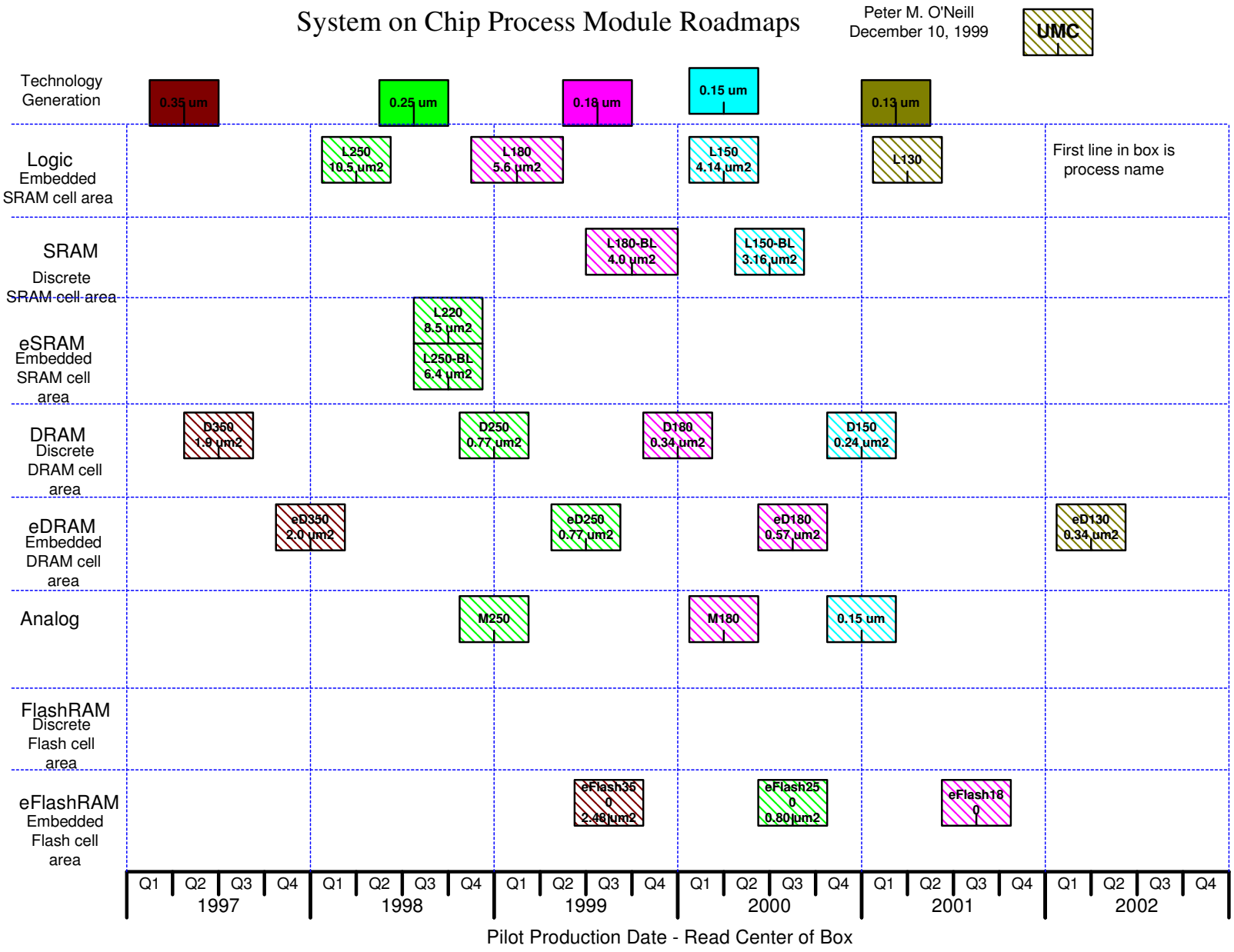


Inductor

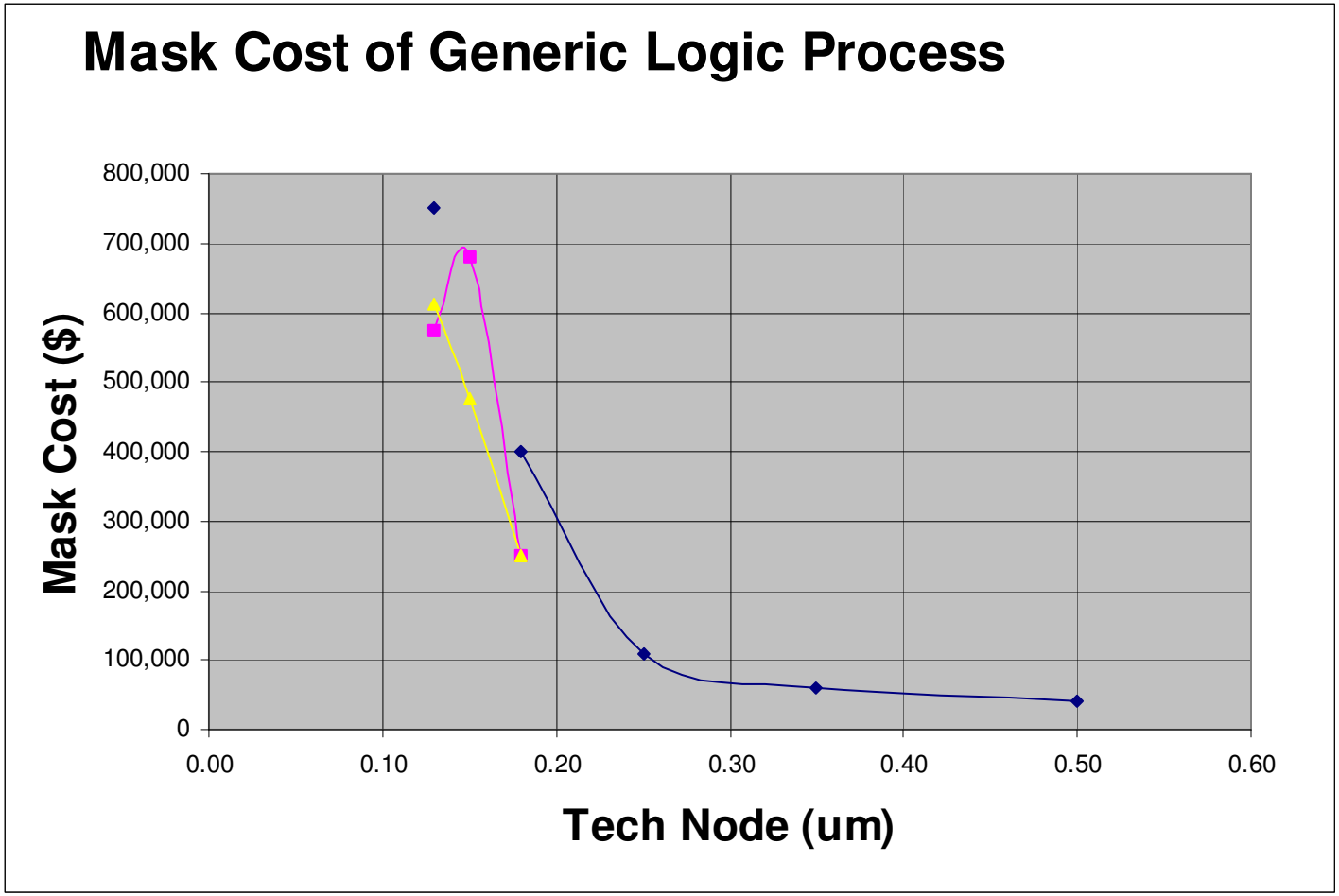
Cost of Process Complexity to Integrate More Functions



Complex Process Delays Time To Market



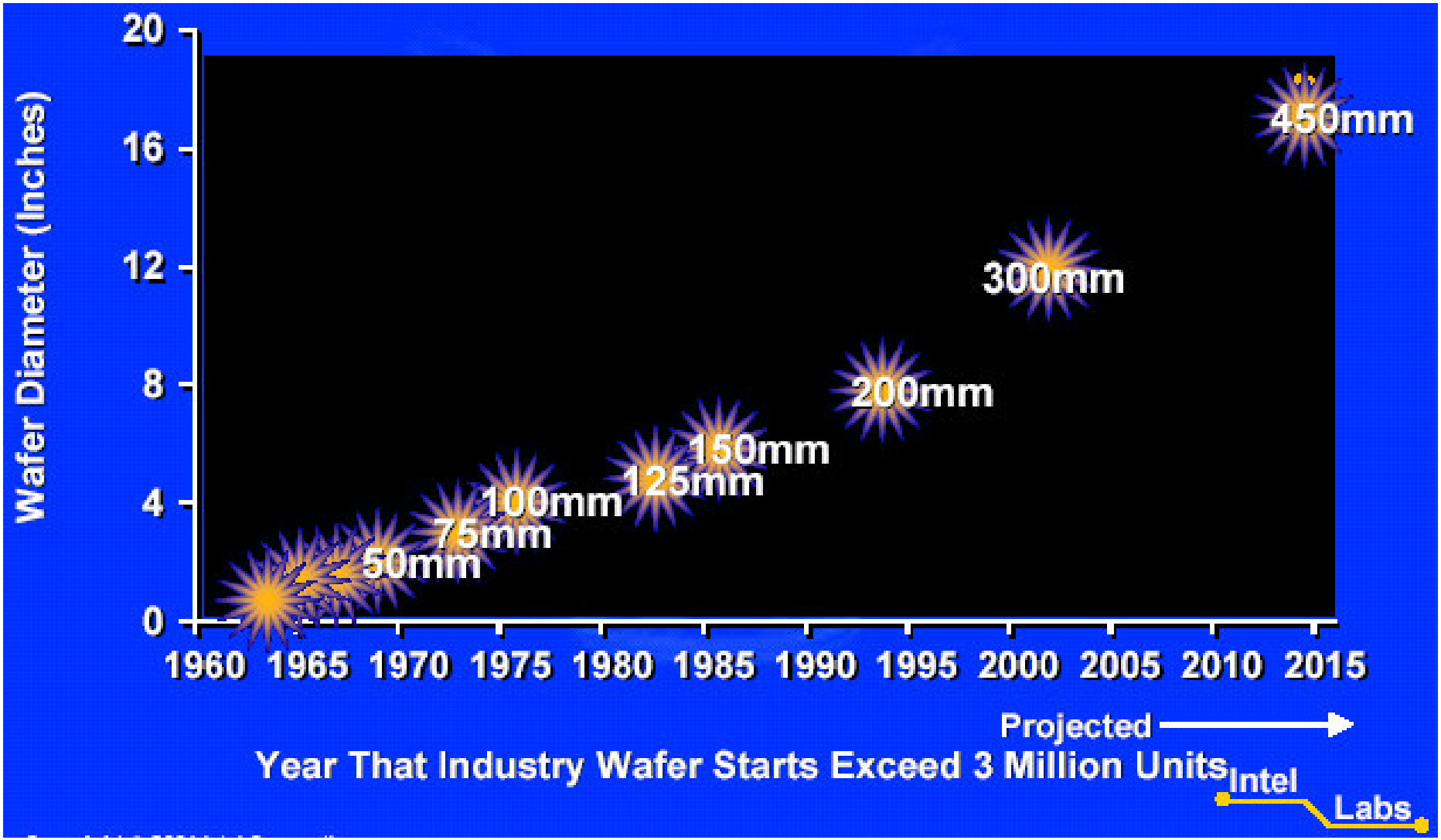
Rising Costs of the Null Chip



Prototype lot cost rising similarly ($80k in 0.15 μm):

- **More complex process**
- **Larger wafers**

Wafer Size


Wafer Diameter (Inches)
20
16
12
8
4
0
1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015
50mm
75mm
100mm
125mm
150mm
200mm
300mm
450mm
Projected
Year That Industry Wafer Starts Exceed 3 Million Units
Intel
Labs

300mm Fab

United Microelectronics Fab
12A, Tainan, Taiwan

Rising Fab Costs

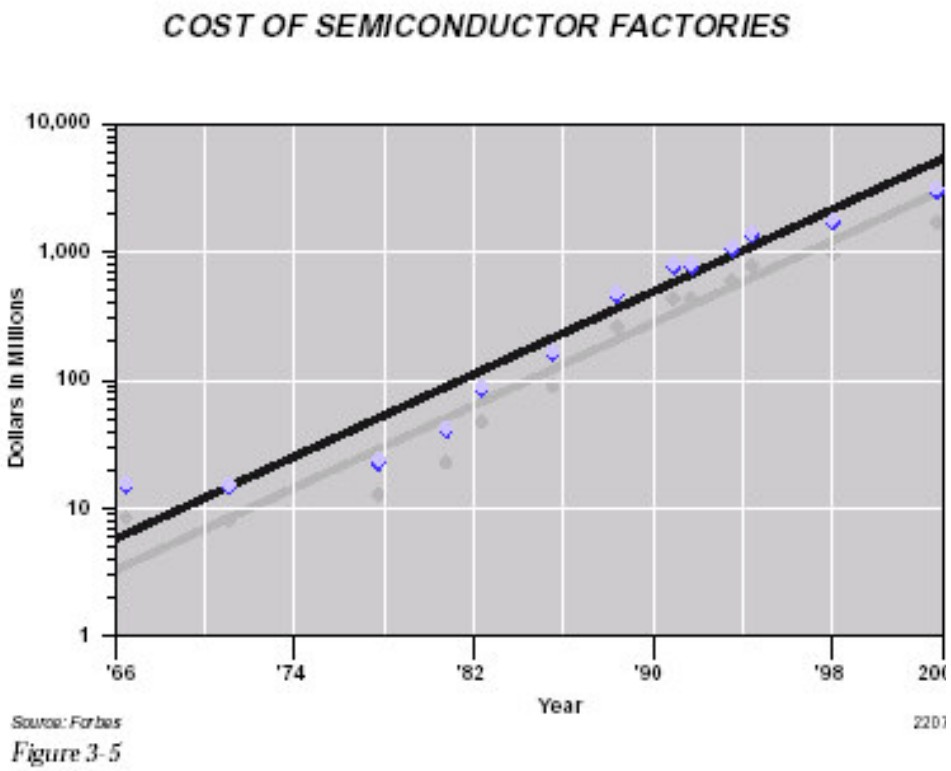
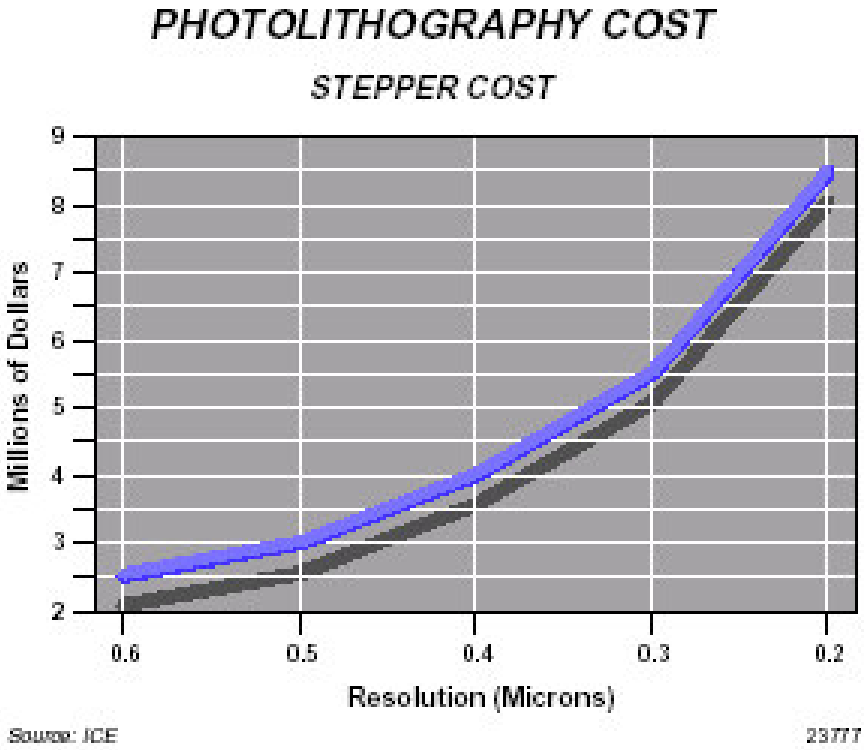
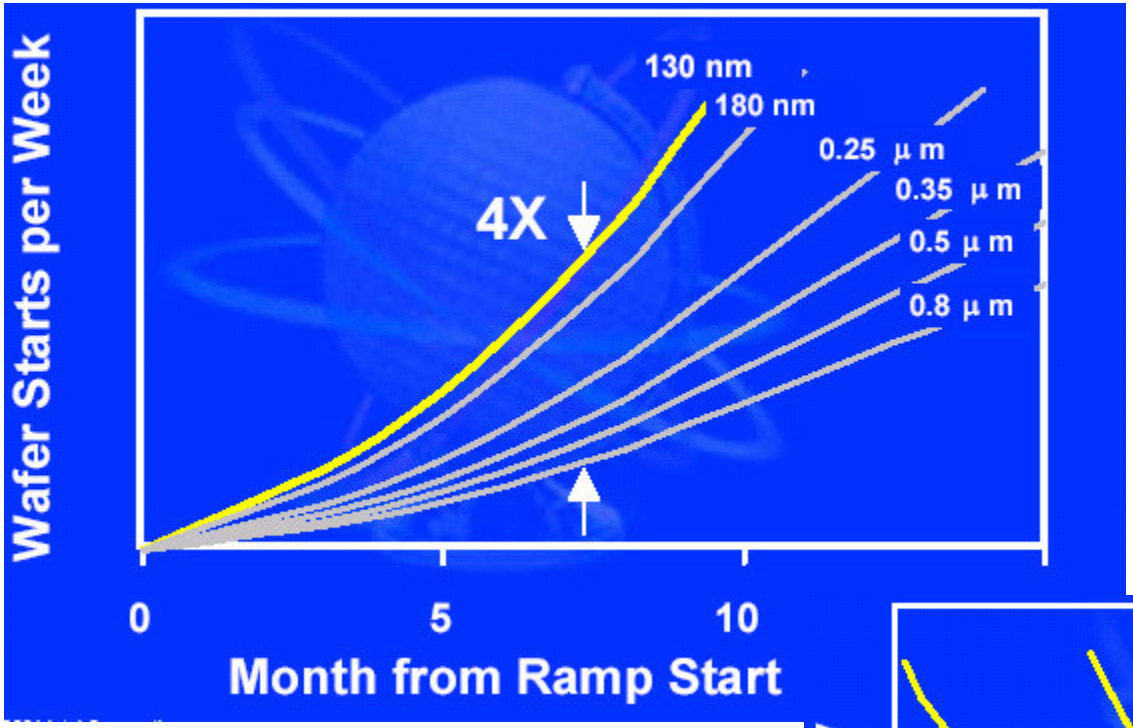
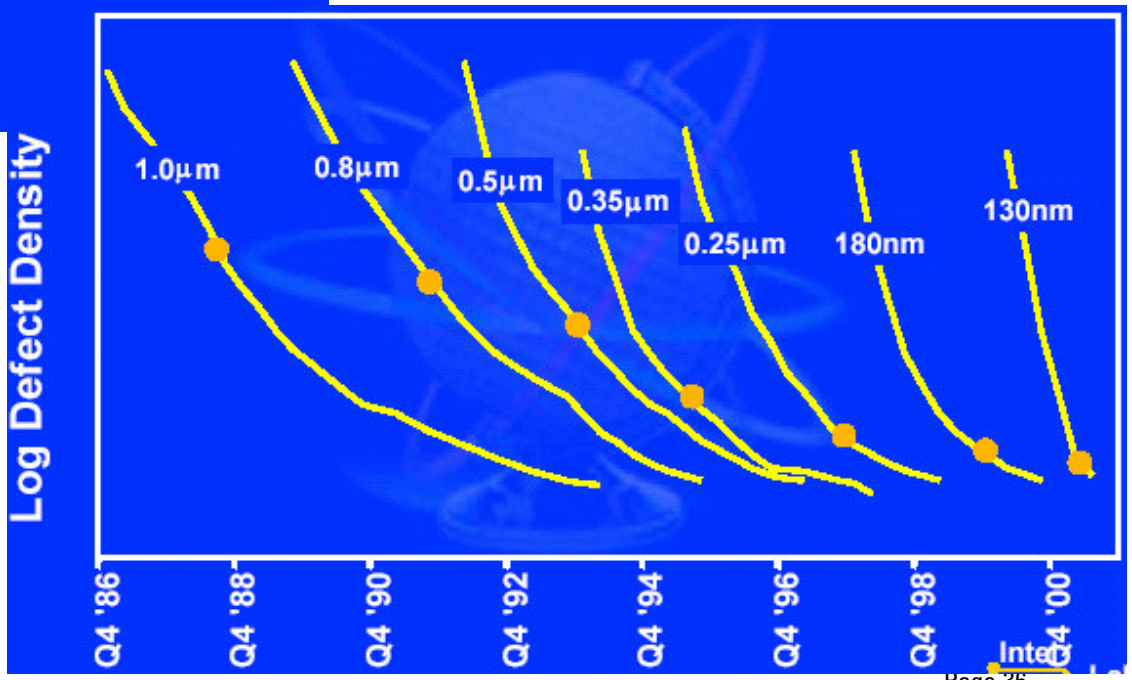


Figure 3-5



Pressure to Ramp Faster





Integrated Circuit Value Chain

Product Design

Value	Example	Source
Product Definition	Printer, Workstation	
System Design	Network interface card, printer electronics	End Product Co.
Product-Specific IP		
Software IP	PhotoRET	ASIC Design House
Design & Test Tools & Methods	Synthesis, Datapath, FAST Scan	EDA Vendor
High Level Standard IP	PCI, JPEG, SCSI	End Product Co.
Foundation Standard IP	Cell library	Design Block Vendor, Foundry

Assembly & Test

Value	Source	Example
Test	Electrical, thermal, mechanical	Test & Assembly Vendor, Test Service, IDM
Assembly		Assembly Vendor
Package Characteristics		Package Vendor
Package Technologies	FCOL, PBGA, CLGA	

Silicon Process

Value	Example	Source
Volume Fab		Foundry 1, Foundry 2
Prototype Fab		IDM
Mask Making		Mask Service
Process Characteristics	LOR, EDR, SPICE	IDM, Design House, Modeling Service
Process Technology	0.13um CMOS, BiCMOS	

Directs the delivery of the other values

Management

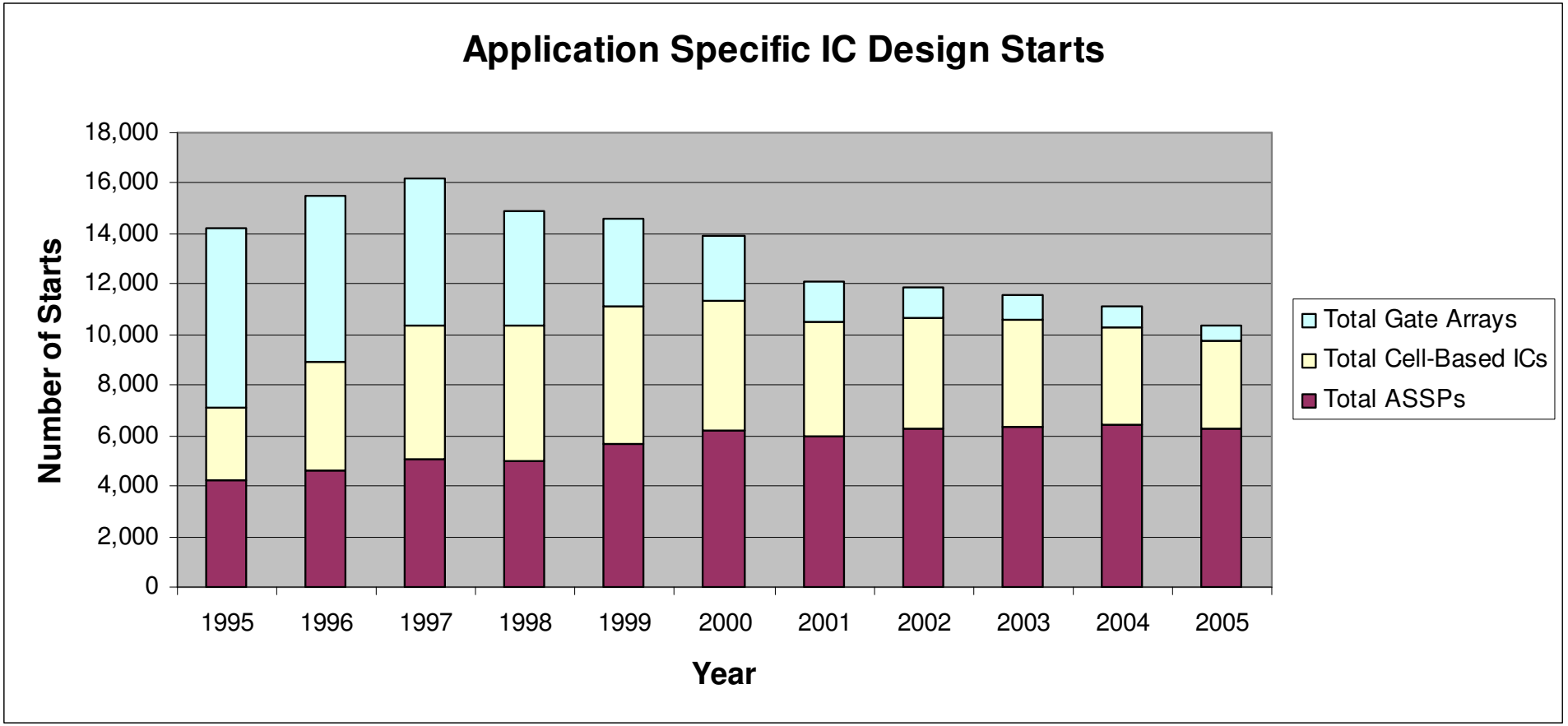
Value	Example	Sources
Supply Chain Management		Design House, Supply Chain Manager
Technology Program Management		
Product Design Management		

Consequences of Business Challenges

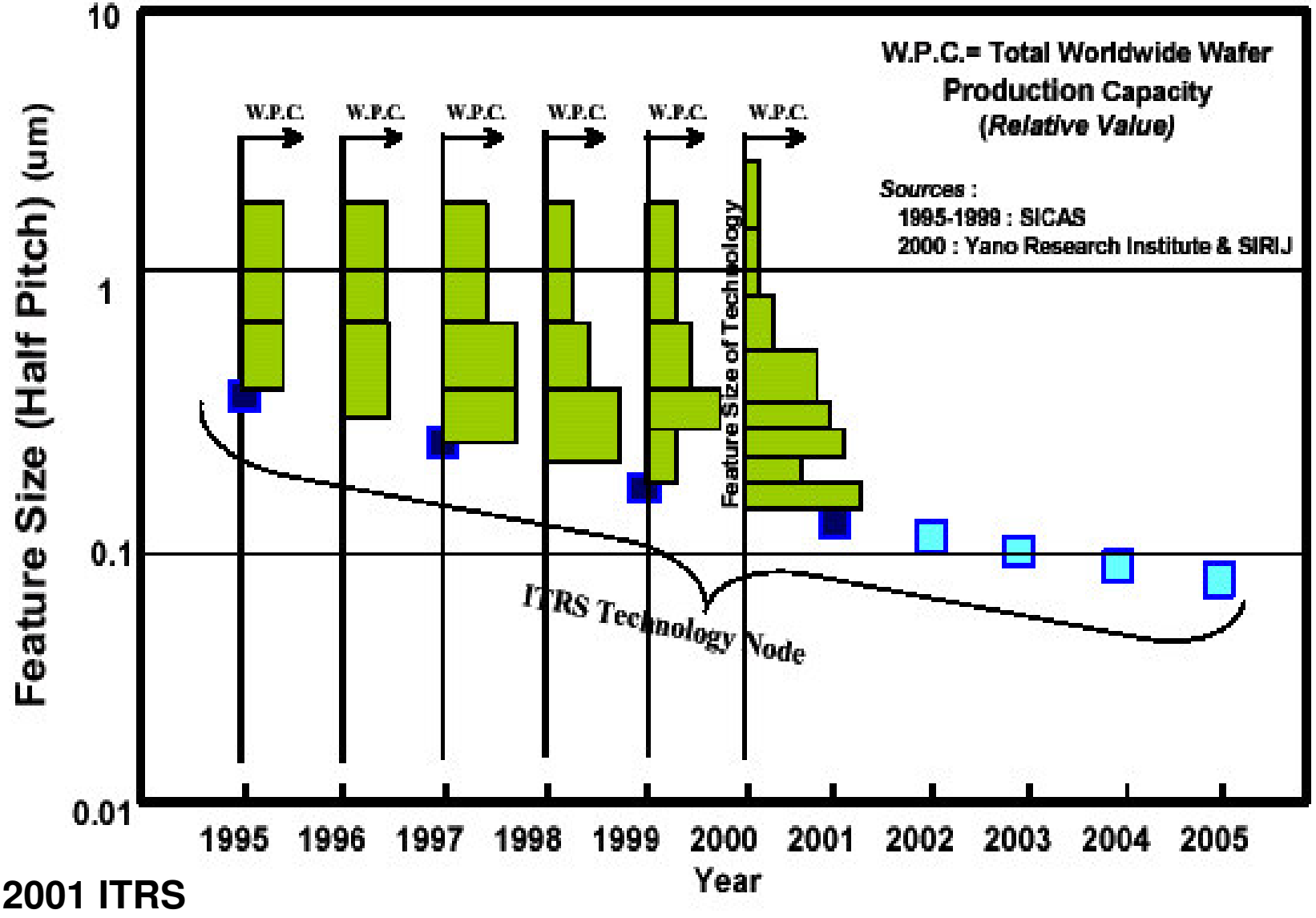
- Dominance of foundry/fabless model
- Process technology developed by & fabs operated by consortia ⇒ Less technology differentiation
- Fewer unique designs
  - ASICs replaced by programmable platforms
  - Fewer IC designers
- Stick to key value added & milk it for all it's worth:
  - If you're world-class at something, sell it to everyone
  - If you're not, buy it from someone who is
- Small design houses move from selling complete chips to selling design IP blocks to those who can afford chip NRE
- Slower process technology advancement, more use of older technologies

Custom Design Starts

Gartner Dataquest - September 2001



Not Everything is at the Limit



2001 ITRS

Nanotechnology – The Way Around the Roadblocks?

- Patterning: photolithography ⇒ Self assembly
- Materials: mixtures & structures that don't occur in normal chemistry
- Replaces requirement for perfection with fault-tolerance