

# CMOS Technology & Business Trends

*Can the semiconductor industry  
afford to continue advancing?*

**Peter M. O'Neill**

**Automated Test Innovations**

**Agilent Laboratories**



**Agilent Technologies**

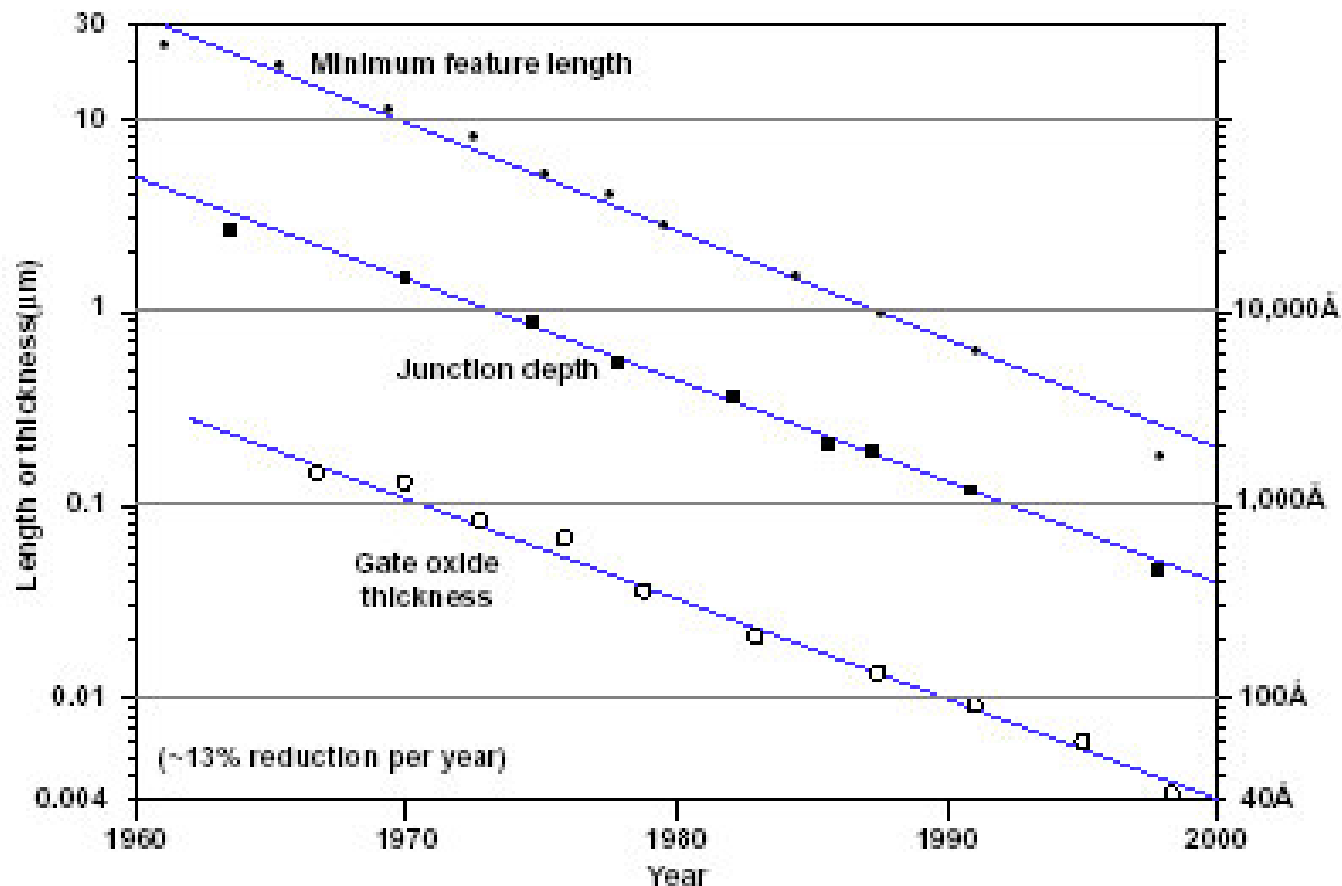
# Disclaimers

- ❖ **Not a thoroughly researched paper – just an accumulation of observations by longtime worker in the field made to provoke thought**
- ❖ **These opinions are my own, not Agilent Technologies’**
- ❖ **Many figures & illustrations are from the *2002 Intel Developer’s Forum***
  - **Copyrighted but publicly available**
  - **I have similar information from other sources but obtained it under condition of nondisclosure**
  - **My conclusion is different than Intel’s**

# The Past – The Legend

The semiconductor industry, lead by CMOS technology, has had an astounding run of increasing functionality and performance at lower cost and power for over 40 years.

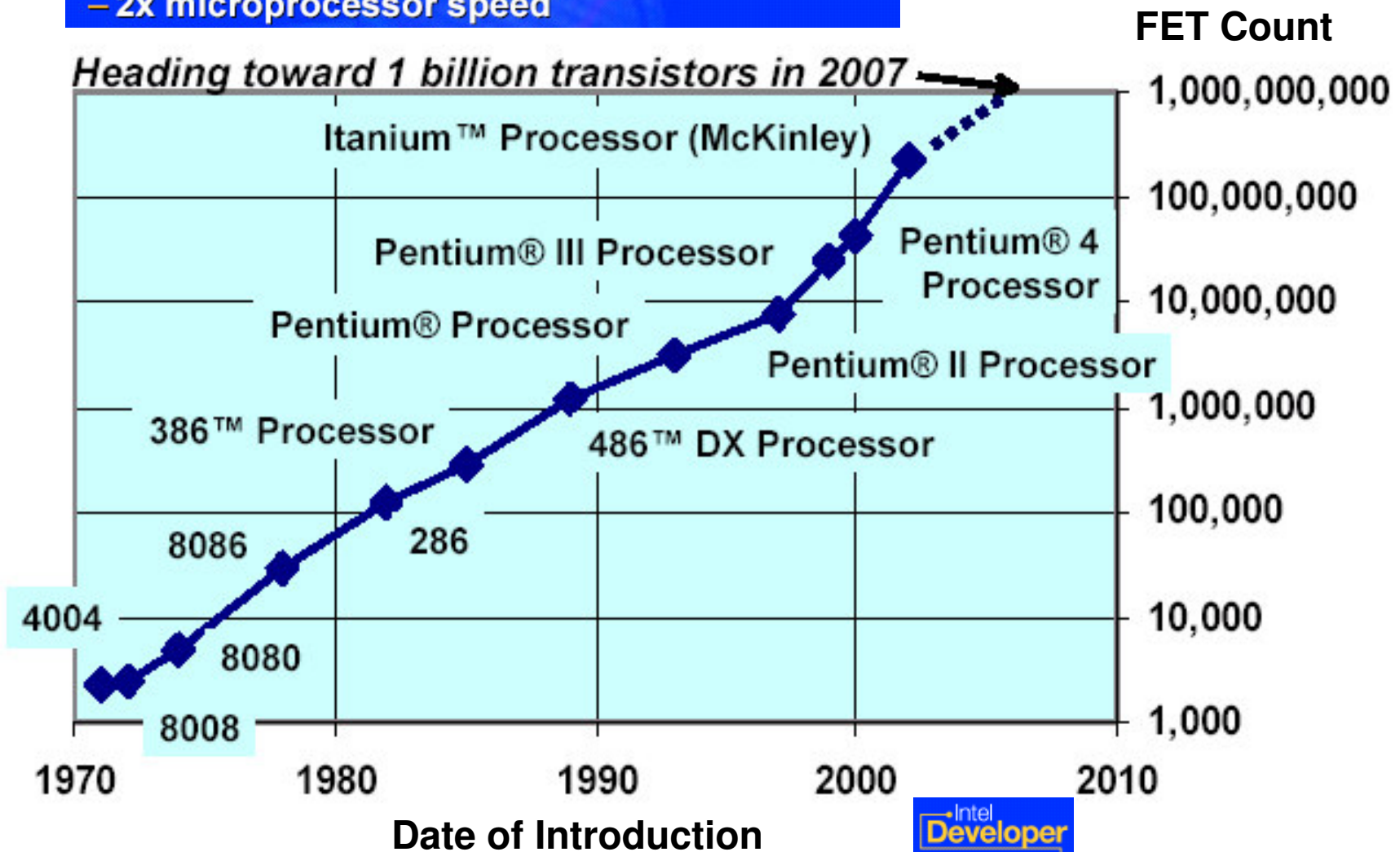
## MOORE'S LAW: FEATURE SIZE SCALING



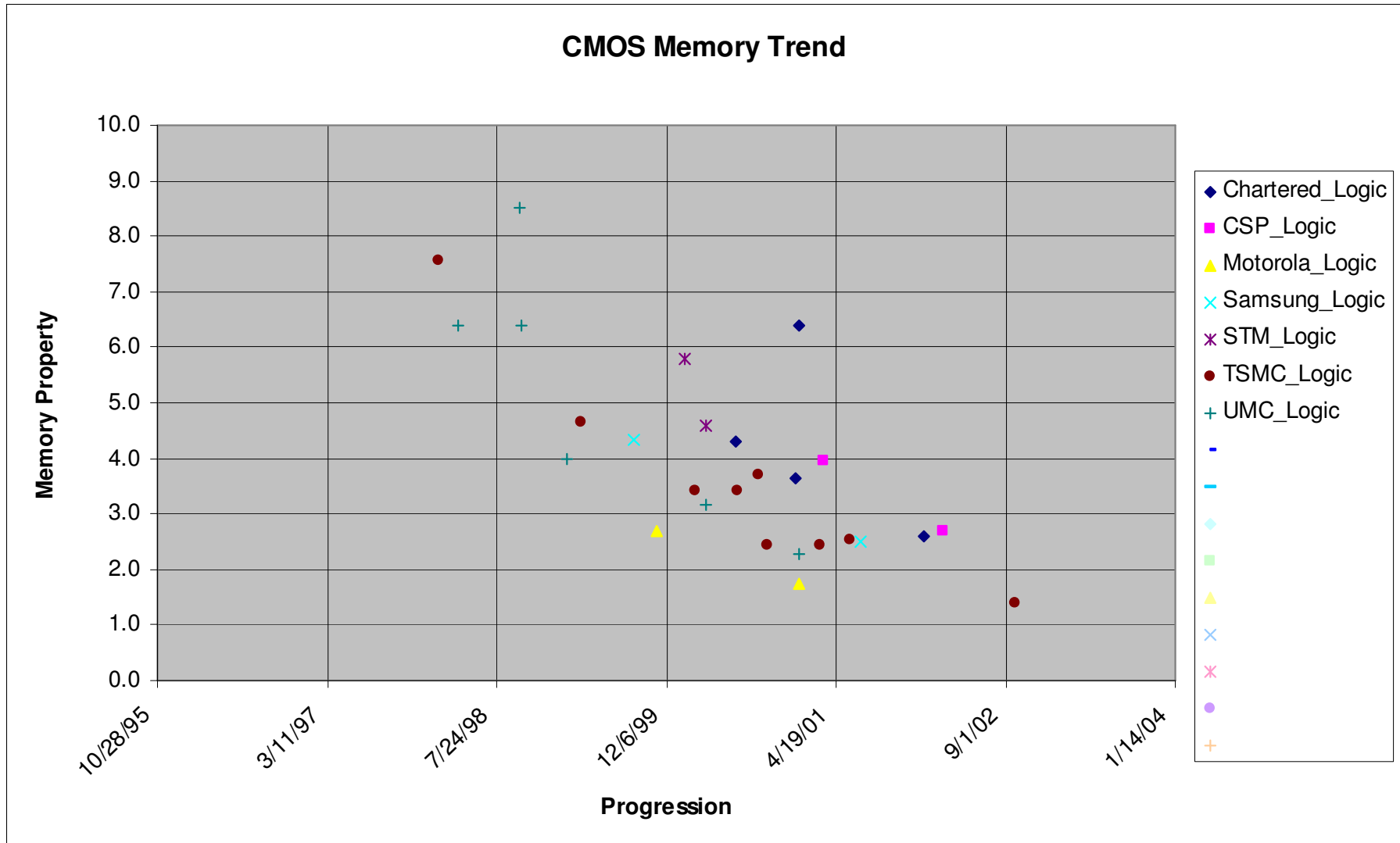
# Achievement: Intel Processor Lineage

New technology generation every 2 years

- 2x die per wafer with 1/2 transistor cost
- 2x microprocessor speed

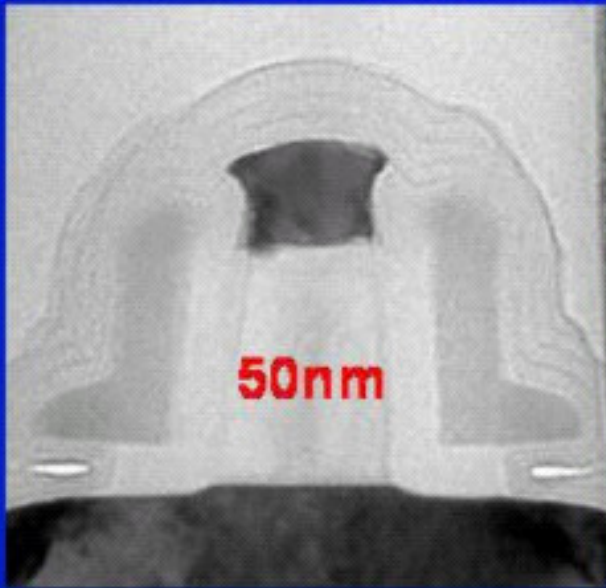


# Achievement: CMOS SRAM Cell Area



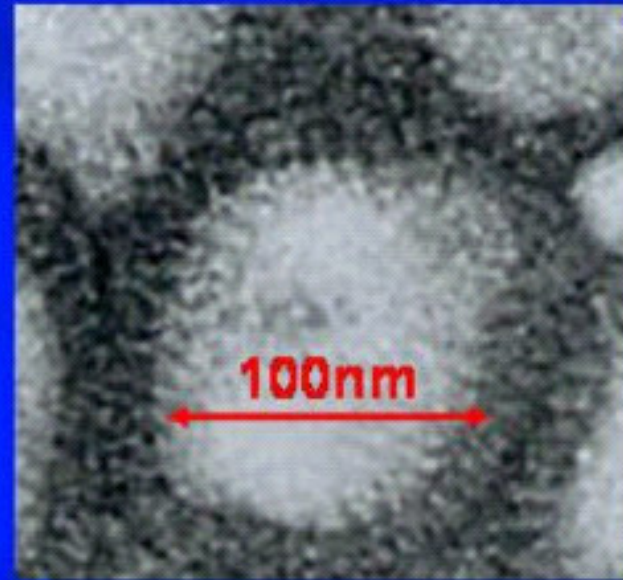
## SRAM Cell Area ( $\mu\text{m}^2$ ) vs. PP Date

# Achievement: The Shrinking MOSFET



**Transistor for  
90nm Process**

Source: Intel

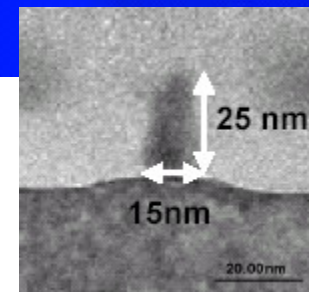
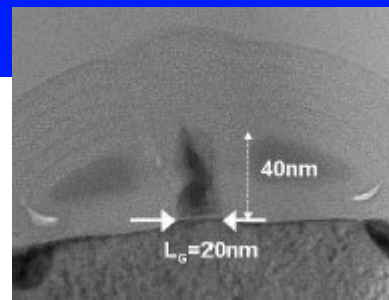
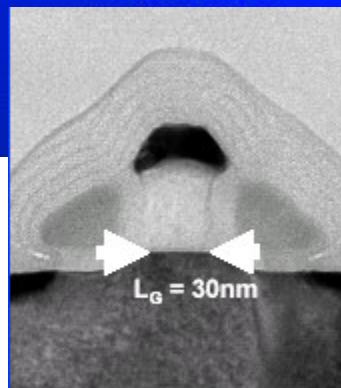


**Influenza virus**

Source: CDC

intel.

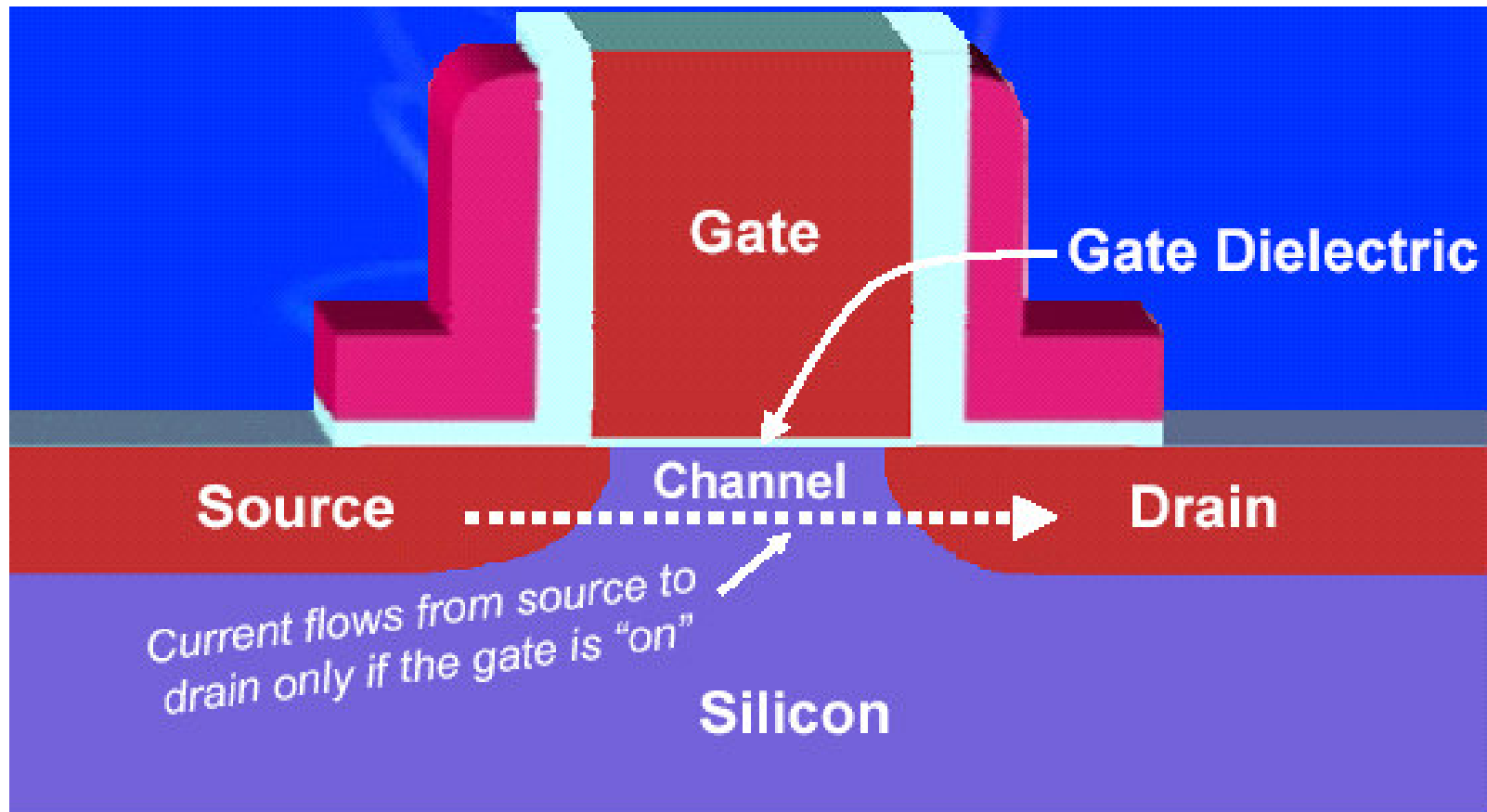
Intel  
**Developer**  
Forum  
Fall 2002



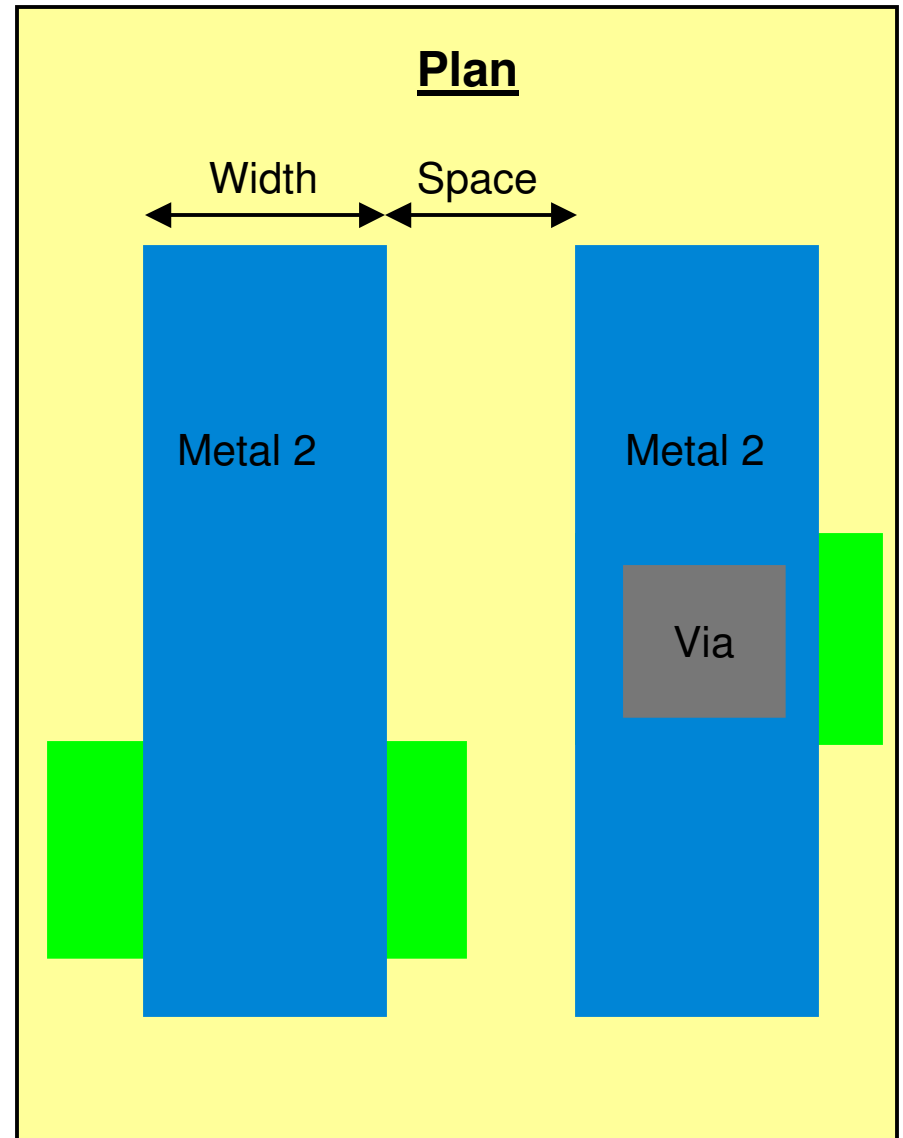
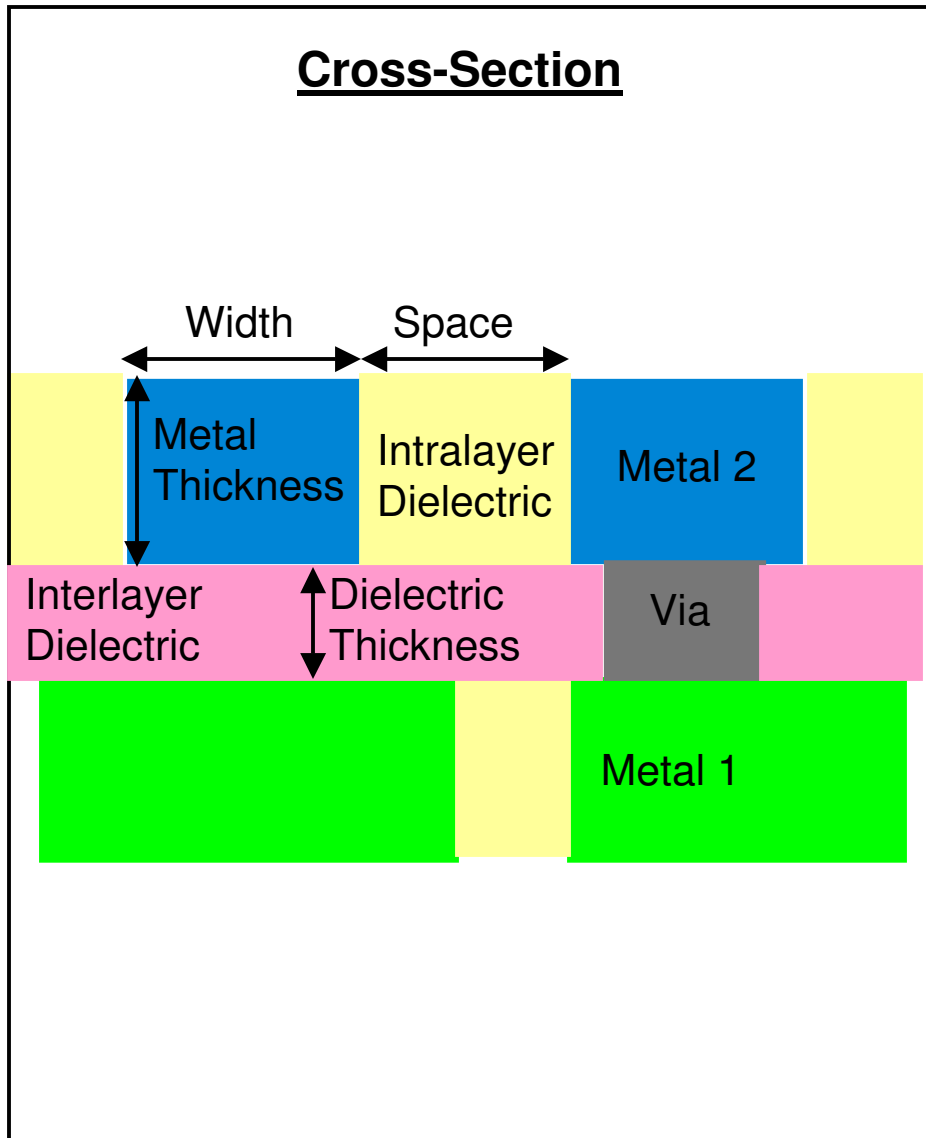
# The Present – The Challenge

- ❖ **Semiconductor industry has hit some inflection points**
- ❖ **Technical:**
  - **Changes in materials**
  - **New reliability mechanisms**
  - **Power consumption**
- ❖ **Business:**
  - **Megafabs**
  - **Fragmented value chain**
  - **Mask costs**
  - **Minimum lot costs**
  - **Design costs**
- ❖ **Will these be overcome as past obstacles have or will they profoundly change the character of the industry?**

# The MOSFET



# Interconnect (Wiring)



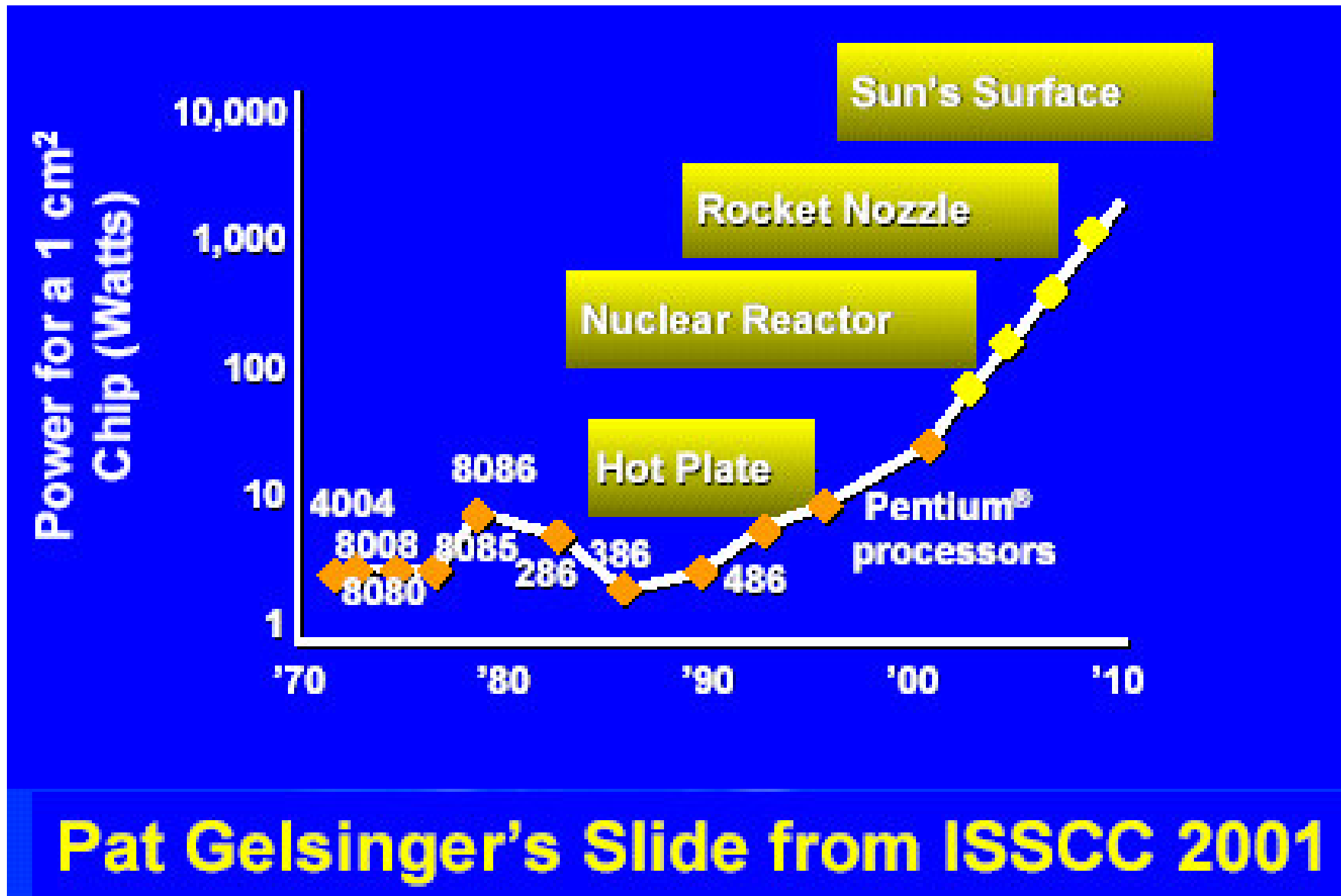
# What Enabled These Achievements

- ❖ Device Structures
  - Planar MOSFET
  - Lateral scaling
- ❖ Materials
  - Semiconductor – Silicon
  - Insulator – SiO<sub>2</sub>
    - MOSFET gate
    - Interconnect
  - Conductor - Aluminum
- ❖ Manufacturing
  - Patterning by photolithography & etch
    - Features > wavelength of light
    - Masks made by e-beam & resemble circuit
  - Material formation by thin film deposition & ion implantation
  - Smaller ⇒ cheaper, faster, lower power
- ❖ Design
  - Automated physical design
  - Simulation of lumped devices
- ❖ Business Model – Integrated Device Manufacturer

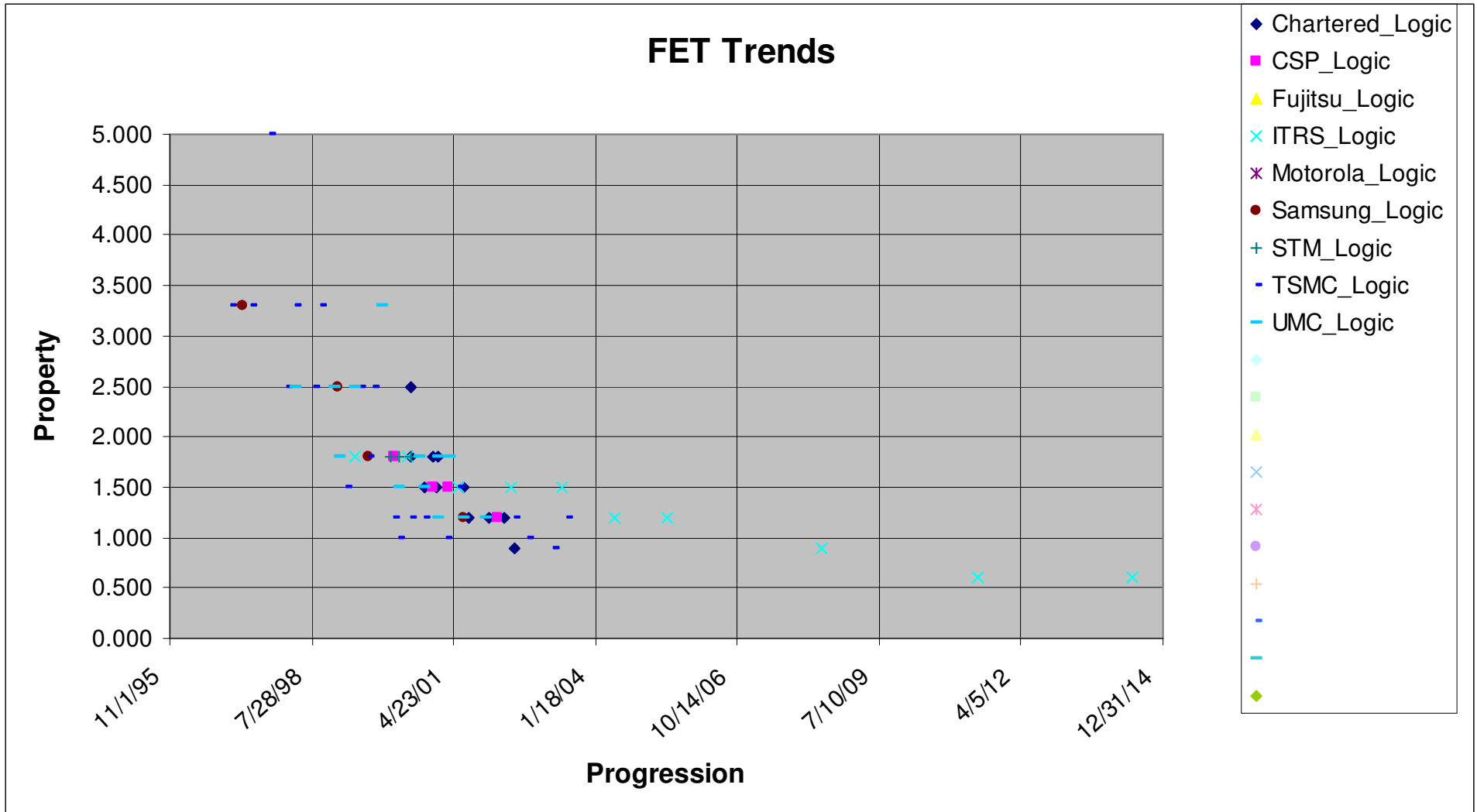
# Limits to Enablers – Inflection Pts.

- ❖ Device Structures
  - Vertical dimensions don't scale as much as lateral  $\Rightarrow$  Interconnect R & C, Cross-talk
  - High electric fields  $\Rightarrow$  Breakdown, Hot carriers
- ❖ Materials
  - Semiconductor – velocity saturation, breakdown
  - Insulator – current tunnels through thin layers, TDDB
  - Conductor – resistance, high current density causes EM
- ❖ Manufacturing
  - Lithography – Features smaller than wavelength of available light
  - Economics – lower cost/function only if lots of functions
  - Can't risk differentiating technology
- ❖ Design
  - Extreme complexity – integrate more & more types of functions
  - Distributed effects hard to simulate
  - Power dissipation rules performance
  - NRE more than startup can afford
- ❖ Business Model - Disaggregated value chain
  - Technology develop costs more than one company can afford
  - Fab cost more than one company can afford
  - Can't afford to design all IP blocks, other's IP required

# Power Dissipation

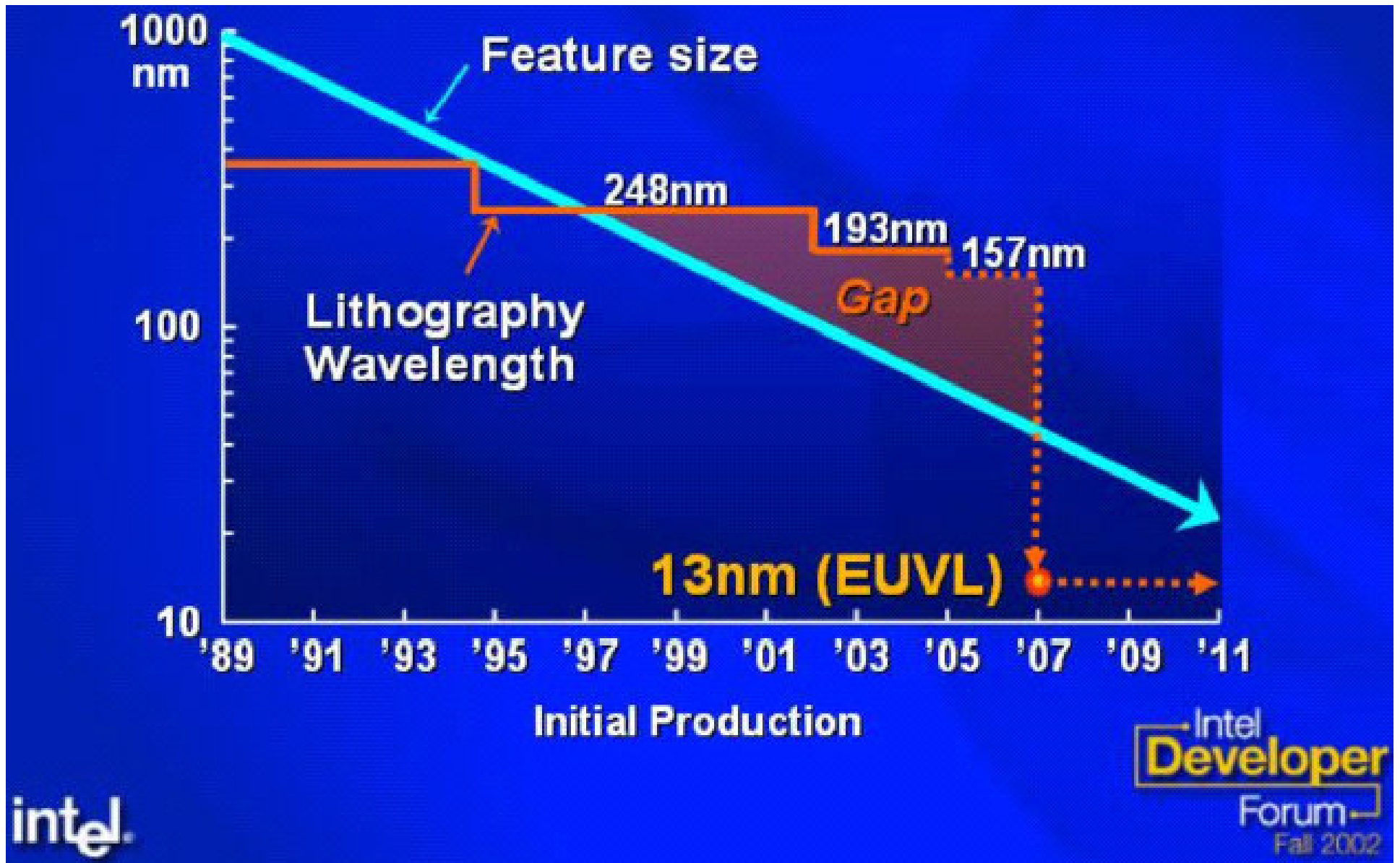


# Dropping Supply Voltage



## Supply Voltage (V) vs. PP Date

# Lithography – Exceeding Optics

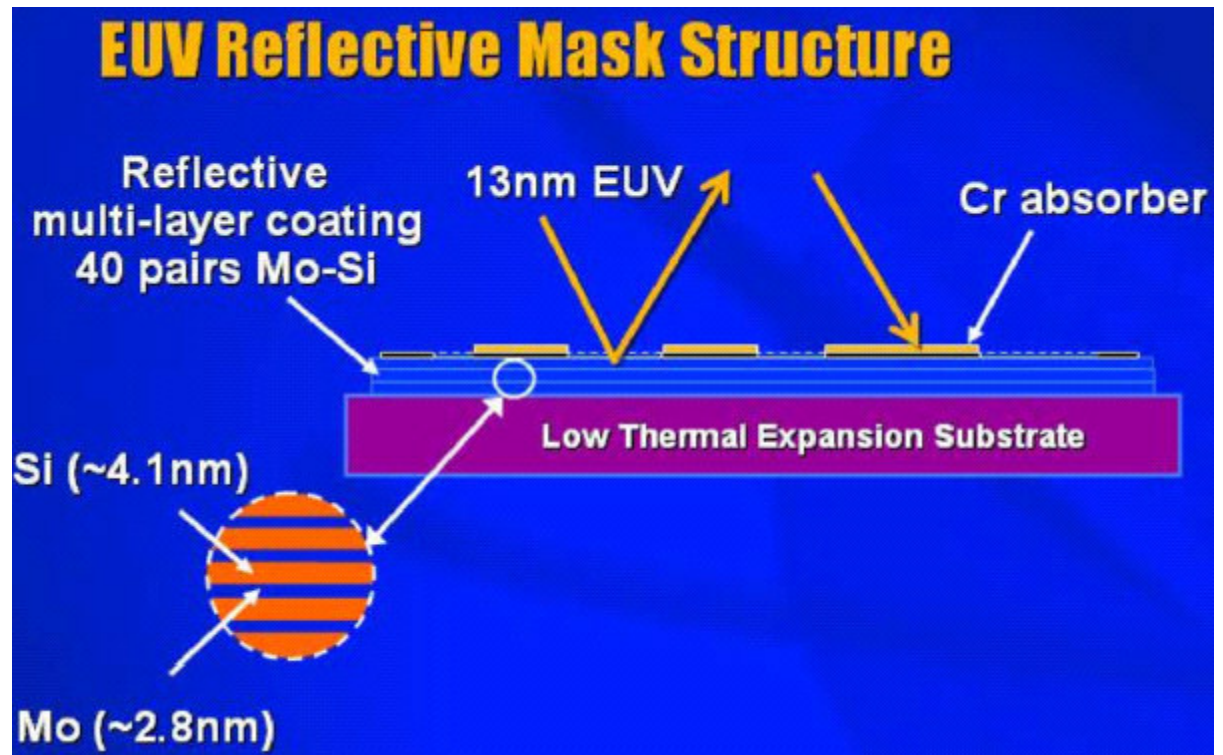
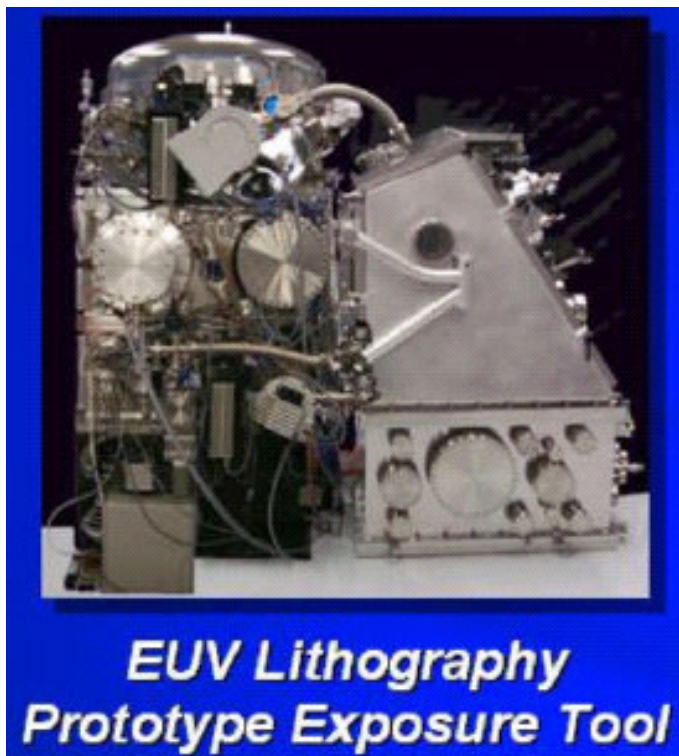


intel.

Intel  
**Developer**  
Forum  
Fall 2002

# Lithography – Extreme UV

- ❖ EUV source is laser, not mercury lamp
- ❖ EUV absorbed by air  $\Rightarrow$  operate in vacuum
- ❖ EUV absorbed by glass  $\Rightarrow$ 
  - Use reflective optics
  - Use reflective masks
- ❖ EUV absorbed by metal  $\Rightarrow$  use Bragg reflectors



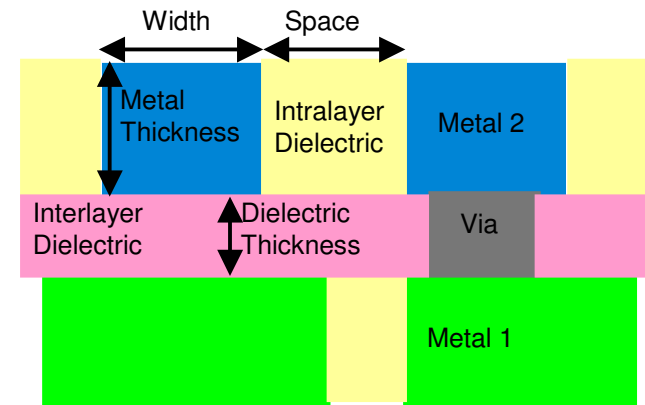
# Interconnect Problems & Solutions

## ❖ Resistance & electromigration

➤ Problem – Area & current scale in opposite directions while  $V$  decreases

### ➤ Solutions & Issues

- Higher aspect lines
  - Difficult patterning thick metal
  - Dielectric coverage
  - Higher intralevel capacitance
- More metal layers  $\Rightarrow$  Complexity, yield
- Replace Al with Cu for lower  $\rho$ , higher mass
  - Can't etch Cu  $\Rightarrow$  damascene process, reverse of Al
  - Cu causes leakage in Si & dielectrics  $\Rightarrow$  barrier jacket



## ❖ Capacitance

➤ Problem – Narrower space & thinner dielectric  $\Rightarrow$  higher  $C$

### ➤ Solution & Issues

- Thinner metal by lower  $\rho$ 
  - Risks EM
  - Higher  $R$
- Thicker dielectric  $\Rightarrow$  high aspect vias  $\Rightarrow$  hard to etch & fill
- Lower dielectric constant  $\kappa$  ( $\epsilon$ )
  - Poor mechanical strength
  - Poor adhesion
  - Unstable  $\kappa$

# Advanced Interconnect

**Changes Made**

**Metal lines**  
Al → Cu

**Insulating dielectric**  
SiO<sub>2</sub> → SiOF  
→ CDO  
(low-k)

**Future Options**

Ultra Low-k Dielectric

**Interconnects**  
Source: Intel

intel.

The image shows a cross-sectional micrograph of a multi-layer interconnect structure. It features several layers of metal lines and insulating dielectric. Arrows point from the text annotations to the corresponding layers in the micrograph. The metal lines are shown as vertical and horizontal structures, while the dielectric layers are the spaces between them. The structure is complex, with multiple layers and vias connecting the different levels.

# Transistor Problems & Solutions

## ❖ Off Leakage

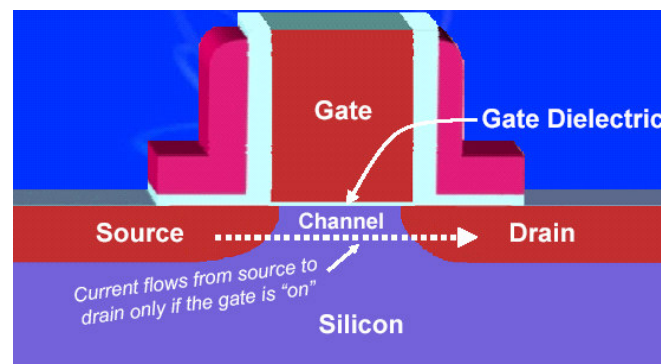
- Problem – High drain E field controls gate, punches thru to source
- Solutions & Issues
  - Drop V  $\Rightarrow$  less drive I, IR drops
  - Channel engineering  $\Rightarrow$  complexity
  - SOI  $\Rightarrow$  defects, complexity, hysteresis
  - Dual gate  $\Rightarrow$  complex, not planar

## ❖ Hot Carriers

- Problem – High E field accelerates carriers into gate degrading I-V
- Solutions & Issues
  - Lower voltage  $\Rightarrow$  less drive I, IR drops
  - Drain engineering  $\Rightarrow$  Drain resistance, complexity

## ❖ Mobility Saturation

- Problem – Carrier velocity not proportional to E at high field
- Solution & Issues
  - SOI to achieve low off leak at low doping  $\Rightarrow$  defects, complexity, hysteresis
  - Strained silicon to increase intrinsic mobility  $\Rightarrow$  defects, complexity
  - Compound semiconductors  $\Rightarrow$  major integration problems!!!



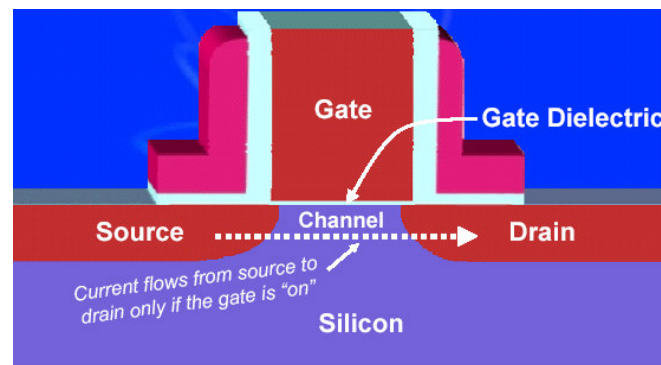
# Transistor Problems & Solutions (cont.)

## ❖ Gate leakage

- Problem – Quantum mechanical tunneling through thin insulators
- Solution & Issues – High  $\kappa$  gate dielectric (HfO, ZrO)  $\Rightarrow$  same E field at thicker dielectric
  - Film growth
  - Interface charge & scattering

## ❖ Parasitic Capacitance & Resistance

- Problems
  - Higher doping for everything else increase S/D junction C
  - Shorter gates, smaller contacts increase gate and S/D R
- Solutions & Issues
  - Decrease junction C with SOI  $\Rightarrow$  defects, complexity, hysteresis
  - Decrease gate R with metal gate  $\Rightarrow$  interface, integration

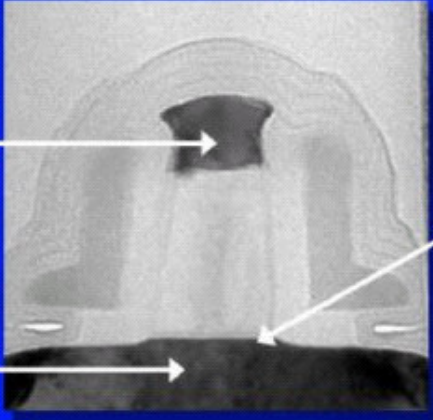


# Transistors – New Materials

**Changes Made**

**Gate**  
Silicide added

**Channel**  
Strained silicon



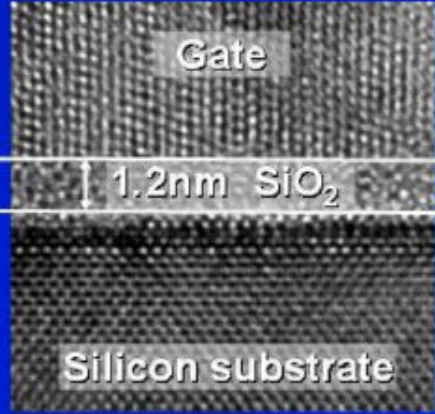
**Transistor**

**Future Options**

High-k gate dielectric

New transistor structure

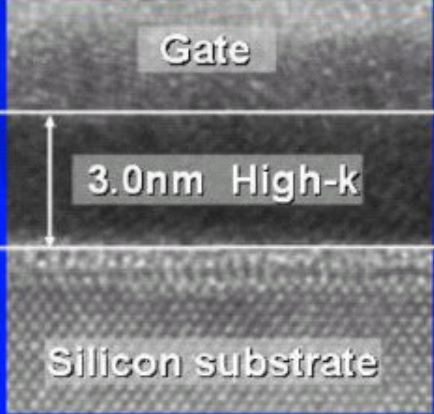
Intel



Gate

1.2nm SiO<sub>2</sub>

Silicon substrate



Gate

3.0nm High-k

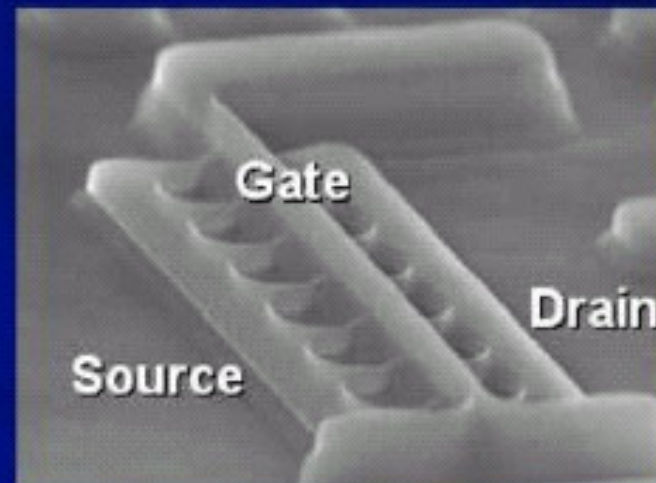
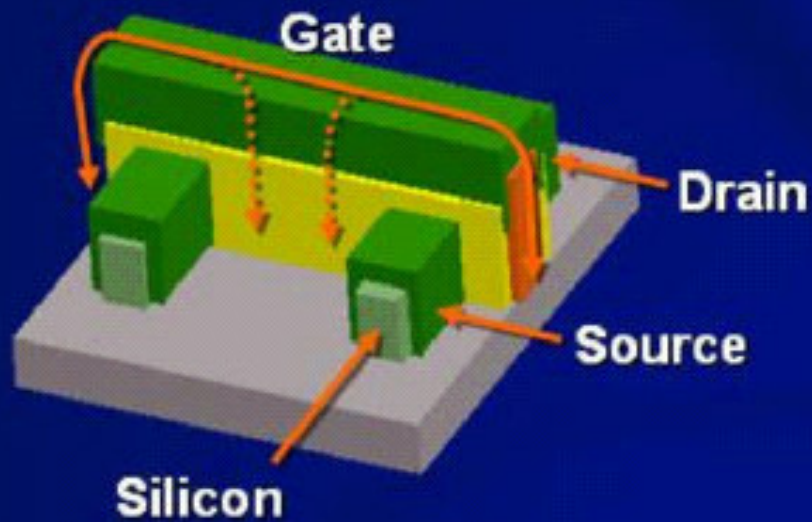
Silicon substrate

Source: Intel

	<u>90nm process</u>	<u>Experimental high-k</u>
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

# Transistors – New Structures

## Experimental Tri-Gate Transistor



Source: Intel

# Increasingly Important Defects

Defect/Fault Type	Causes
Open defects	<ul style="list-style-type: none"> <li>• More metal layers &amp; vias</li> <li>• Subtractive Cu replacing additive Al <math>\Rightarrow</math> discontinuous trench fill</li> <li>• Weak low K dielectrics</li> </ul>
Bridging defects	<ul style="list-style-type: none"> <li>• More metal layers</li> <li>• Subtractive Cu replacing additive Al <math>\Rightarrow</math> polish smearing</li> </ul>
Delay faults	<ul style="list-style-type: none"> <li>• Interconnect dominates delay &amp; defect density <math>\Rightarrow</math> delay defects dominate</li> <li>• Common manifestation of open defect</li> <li>• Cross-talk causes signal-dependent delay</li> </ul>
Cross-talk faults	<ul style="list-style-type: none"> <li>• Interconnect dominates delay</li> <li>• Higher aspect metal spaces</li> <li>• Variable dielectric constant</li> </ul>
Parametric faults	<ul style="list-style-type: none"> <li>• Digital: Delay &amp; Cross-talk faults</li> <li>• More analog/MS/RF circuitry <math>\Rightarrow</math> matching important</li> <li>• Matching difficult for very small devices</li> <li>• Microloading, lens uniformity, proximity effects <math>\Rightarrow</math> larger intra-die parameter variation</li> </ul>

# Intel's Conclusion

- **We still have not found a fundamental barrier to Moore's Law**
  - Silicon scaling will continue through the end of this decade
  - There will be a new generation every two years
- **New materials and new structures are required**
  - Lithography
  - Transistors
  - Interconnects
  - Packaging

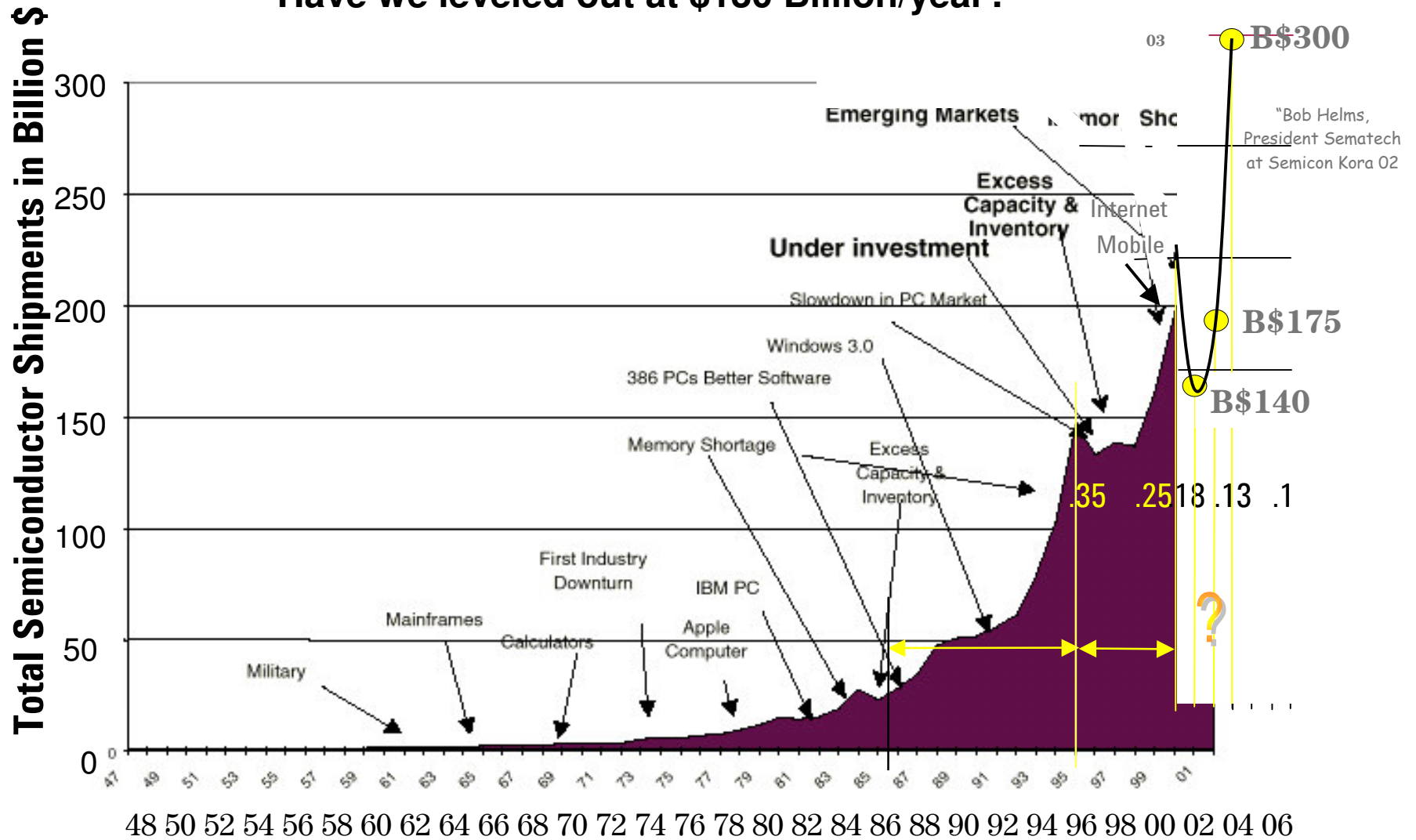
**But can we afford to do these ... and for what kinds of products?**

# Business Challenges

- ❖ “High tech” exempt from economy  $\Rightarrow$  *Is the economy*
- ❖ Market: industrial  $\Rightarrow$  consumer
- ❖ Skyrocketing design NRE
- ❖ Skyrocketing fab cost
- ❖ Skyrocketing process development cost
- ❖ Success determined by time to market & volume, not technology
- ❖ Individual companies can't afford to do everything themselves, not even in one area

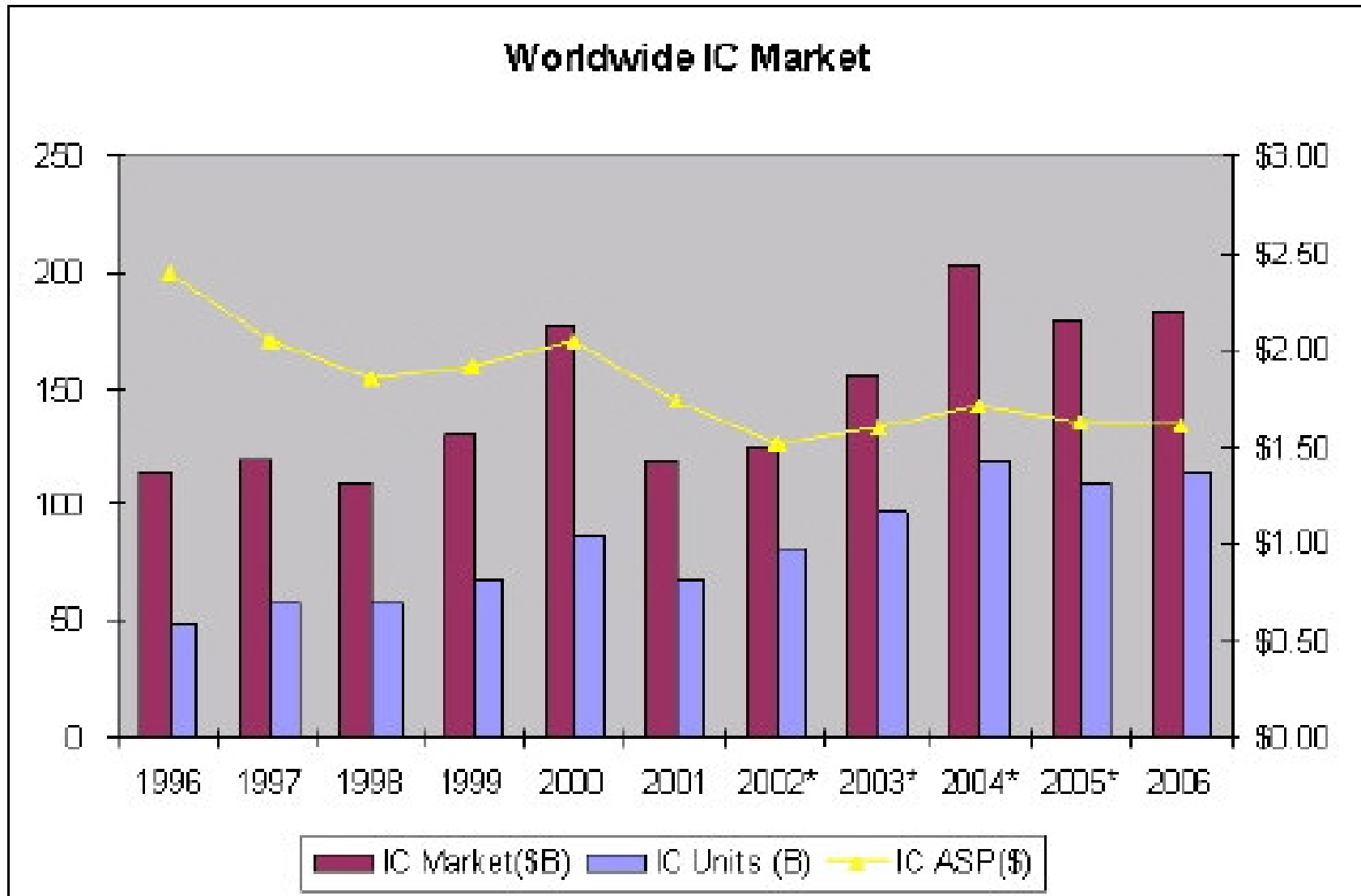
# The Semiconductor Roller Coaster

Have we leveled out at \$130 Billion/year?



Semico Research until 2000, 2001-2006 guessed bathtub scenario

# Recent WW IC Market



# Changing End Uses

	<b>Was</b>	<b>Is</b>
<b>Markets</b>	<ul style="list-style-type: none"> <li>❖ Industrial</li> <li>❖ Military/Aerospace</li> <li>❖ High-end consumer</li> </ul>	<ul style="list-style-type: none"> <li>❖ Consumer</li> <li>❖ Information utility infrastructure</li> </ul>
<b>Products</b>	<ul style="list-style-type: none"> <li>❖ Minicomputers</li> <li>❖ Workstation computers</li> <li>❖ Personal computers</li> <li>❖ Industrial/laboratory instruments</li> <li>❖ Comms infrastructure</li> </ul>	<ul style="list-style-type: none"> <li>❖ DVD/CD players</li> <li>❖ Cell phones</li> <li>❖ PDAs, MP3 players, other personal portable devices</li> <li>❖ Personal computers</li> <li>❖ Server computers</li> <li>❖ Comms switches &amp; routers</li> </ul>
<b>Drivers</b>	<ul style="list-style-type: none"> <li>❖ Digital speed</li> <li>❖ Density</li> <li>❖ Quality</li> </ul>	<ul style="list-style-type: none"> <li>❖ Integration of diverse functions</li> <li>❖ Portability</li> <li>❖ Cost</li> </ul>

# Determinants of Cost

## ❖ Manufacturing

- **Recurring**
  - **Wafer cost**
  - **Yield**
  - **Test**
  - **Package**
- **Nonrecurring**
  - **Masks**
  - **Characterization lot**

## ❖ Design

- **Designer-months**
- **Number of turns**
- **EDA licenses**
- **Design IP licenses**

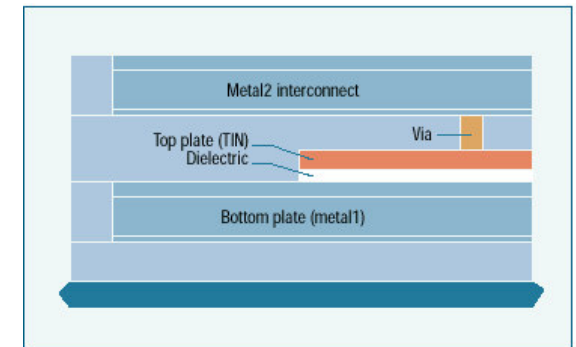
# Integrating New Functions

## Functions Beyond Digital

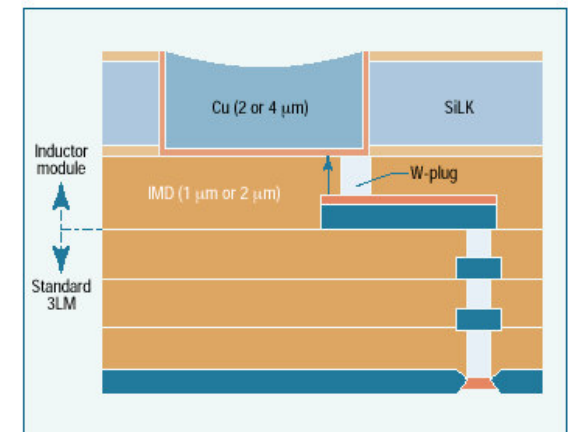
- ❖ Analog
- ❖ Radio
- ❖ High-speed serial comms
- ❖ Optical
- ❖ Sensors

## Requiring New Devices

- ❖ Memory
  - High density – DRAM
  - Nonvolatile – Flash, Ferroelectric
- ❖ High quality passives for RF & analog
  - Inductor
  - Capacitor
  - Resonator
- ❖ Transistors
  - High V FET
  - Low leak, low power FET
  - High  $F_T$  BJT

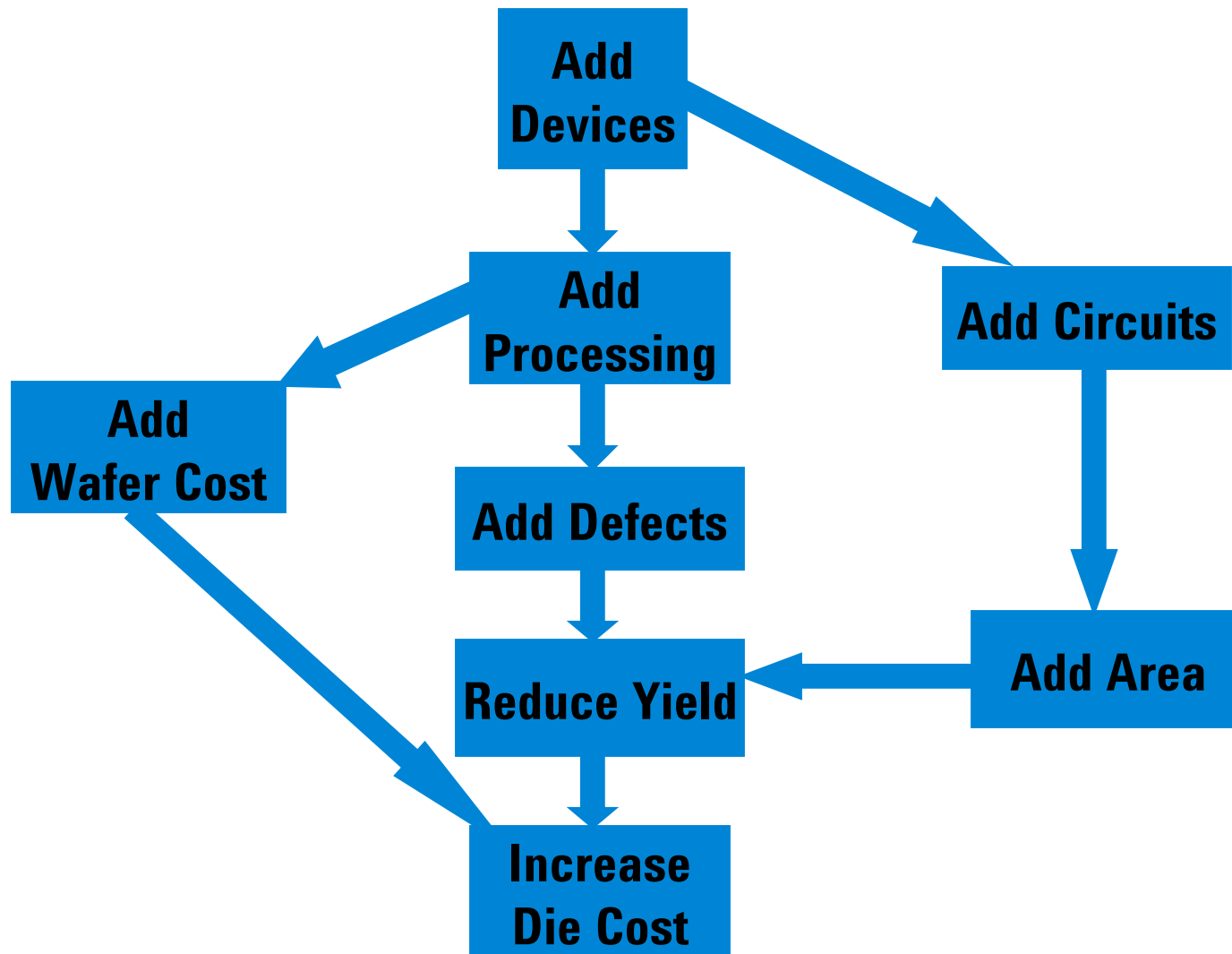


Capacitor



Inductor

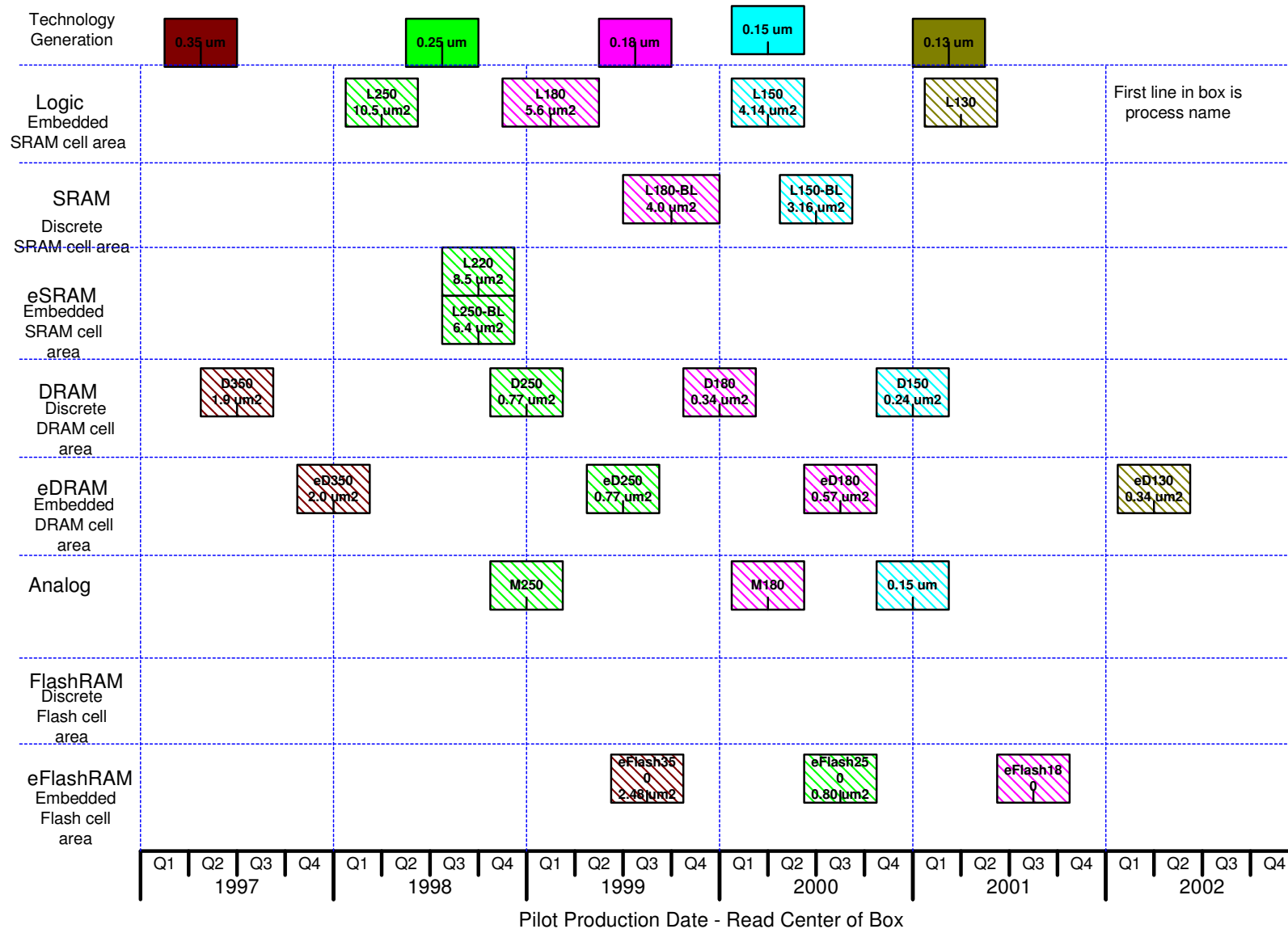
# Cost of Process Complexity to Integrate More Functions



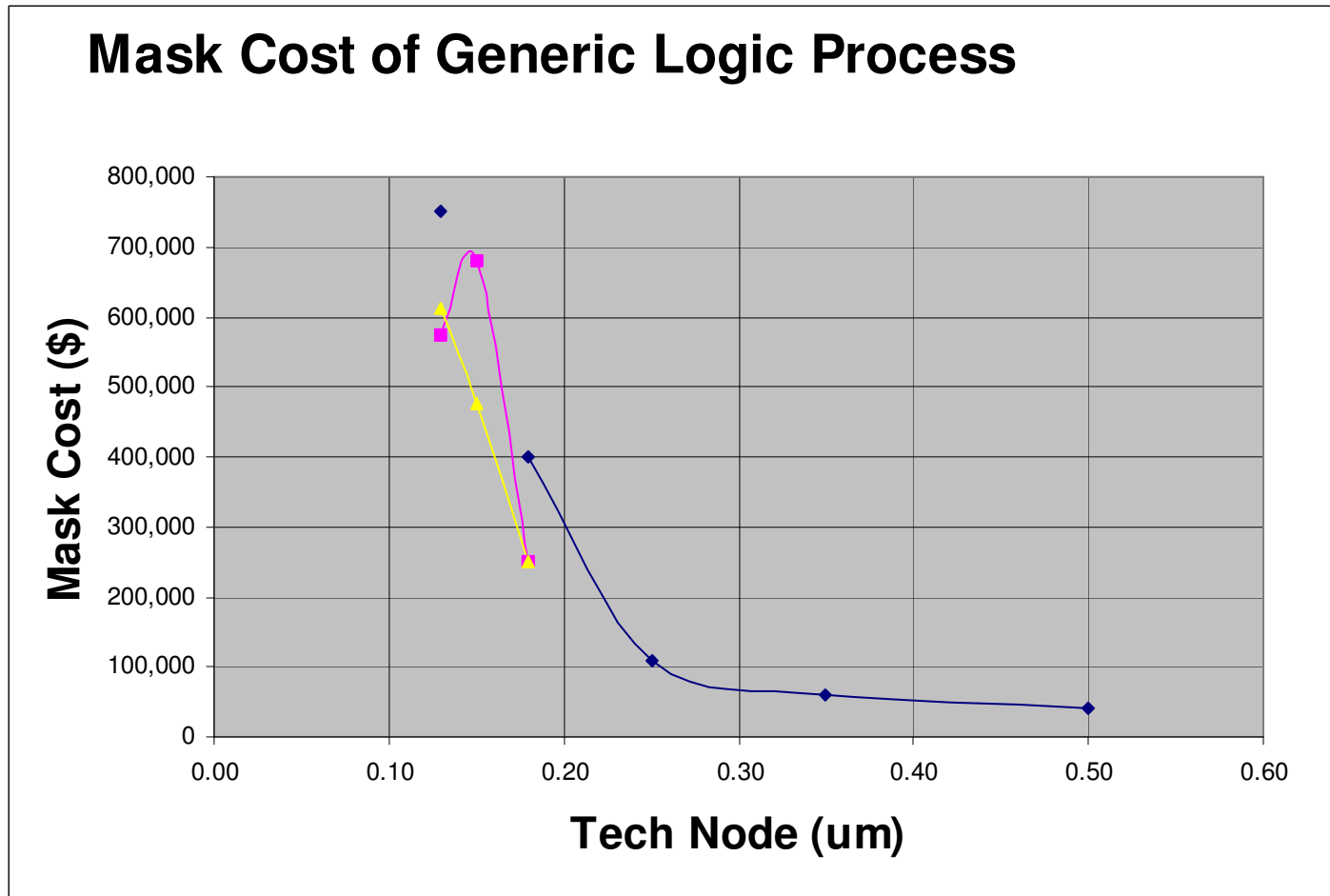
# Complex Process Delays Time To Market

## System on Chip Process Module Roadmaps

Peter M. O'Neill  
December 10, 1999



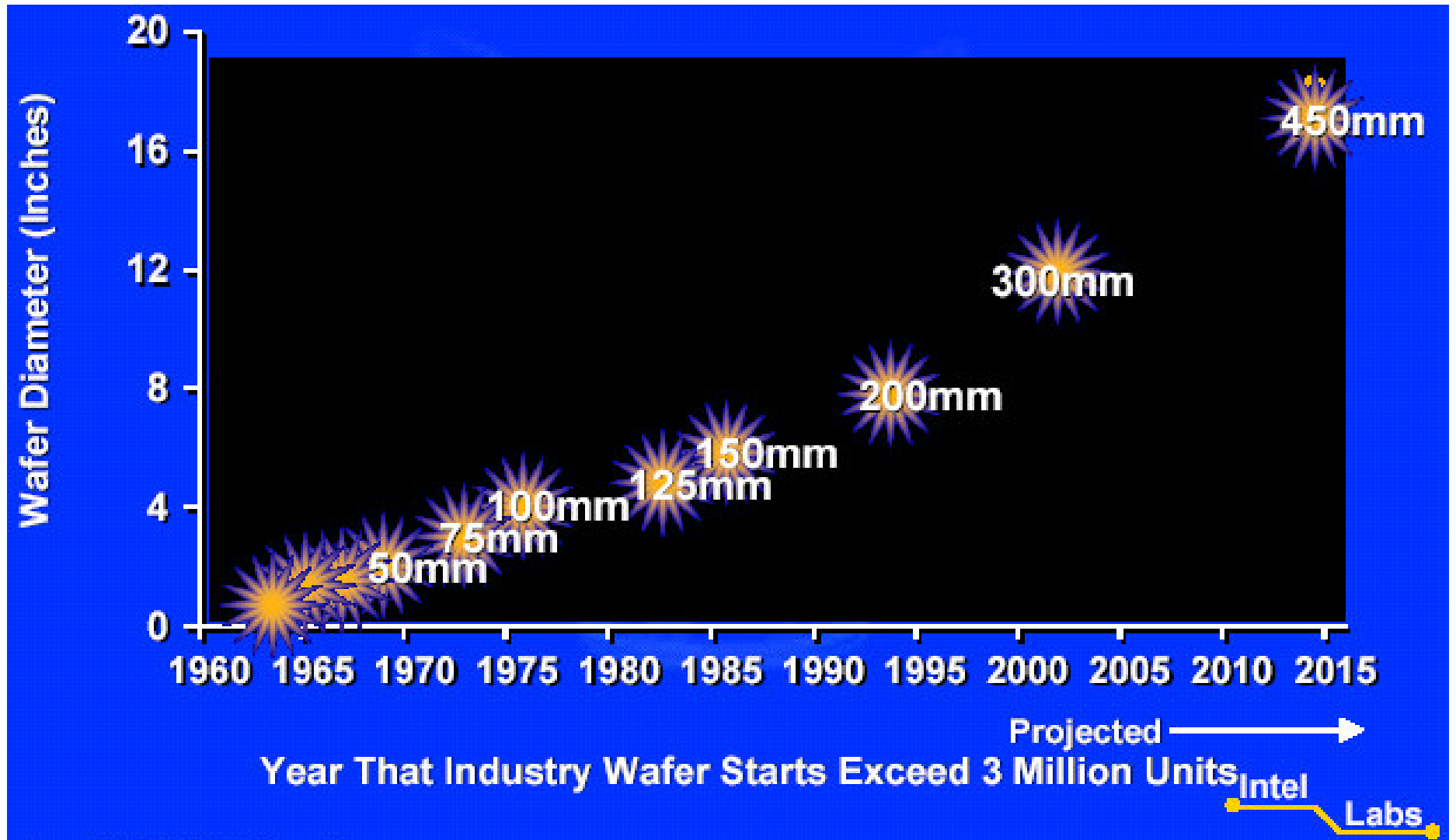
# Rising Costs of the Null Chip



**Prototype lot cost rising similarly (\$80k in 0.15  $\mu\text{m}$ ):**

- **More complex process**
- **Larger wafers**

# Wafer Size



# 300mm Fab

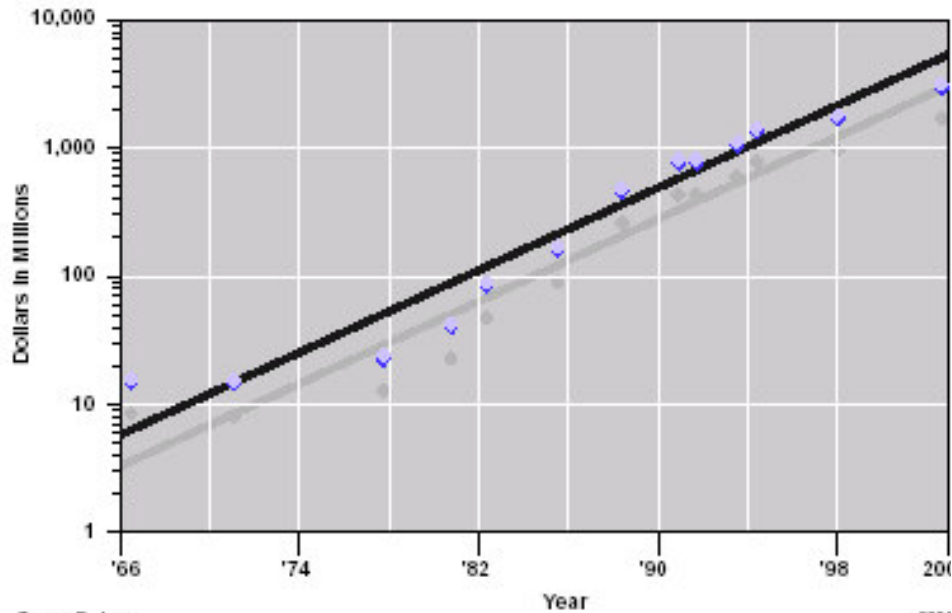
## United Microelectronics Fab 12A, Tainan, Taiwan



Nov. 6, 2002

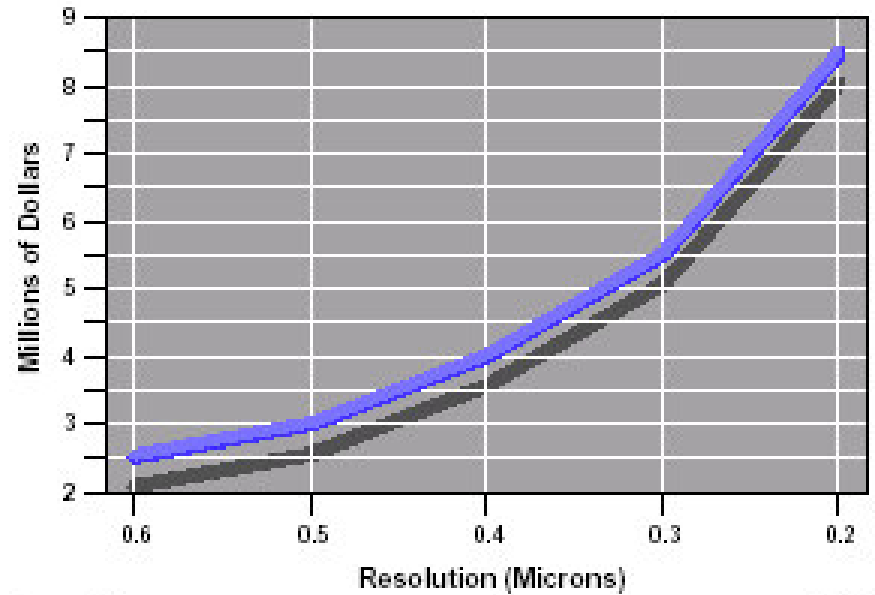
# Rising Fab Costs

*COST OF SEMICONDUCTOR FACTORIES*



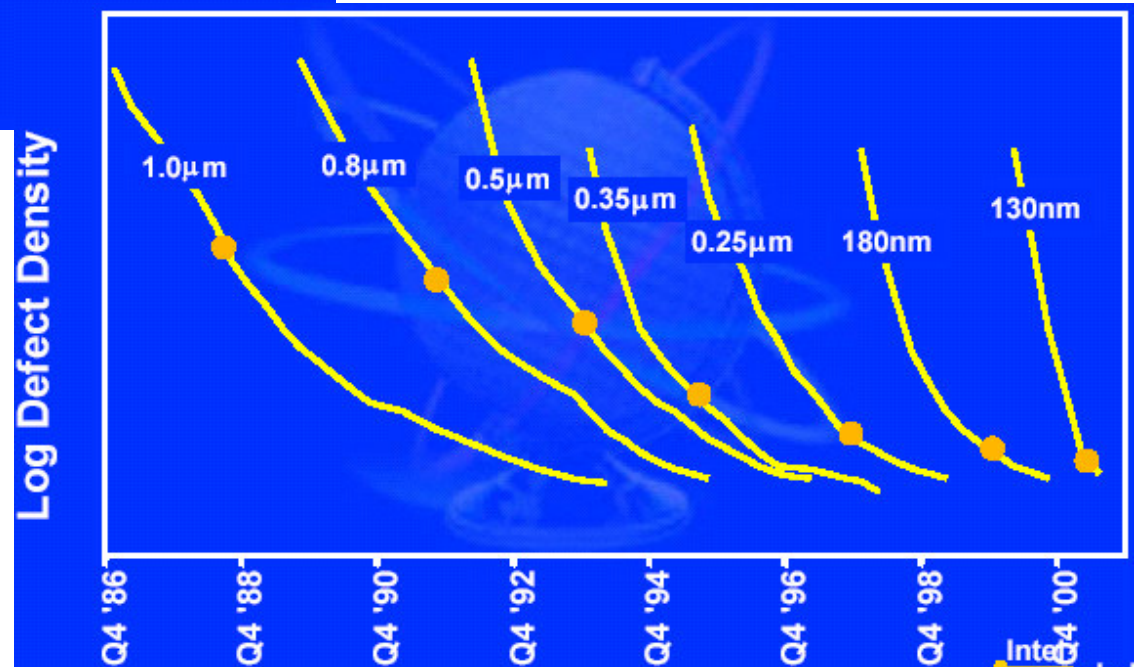
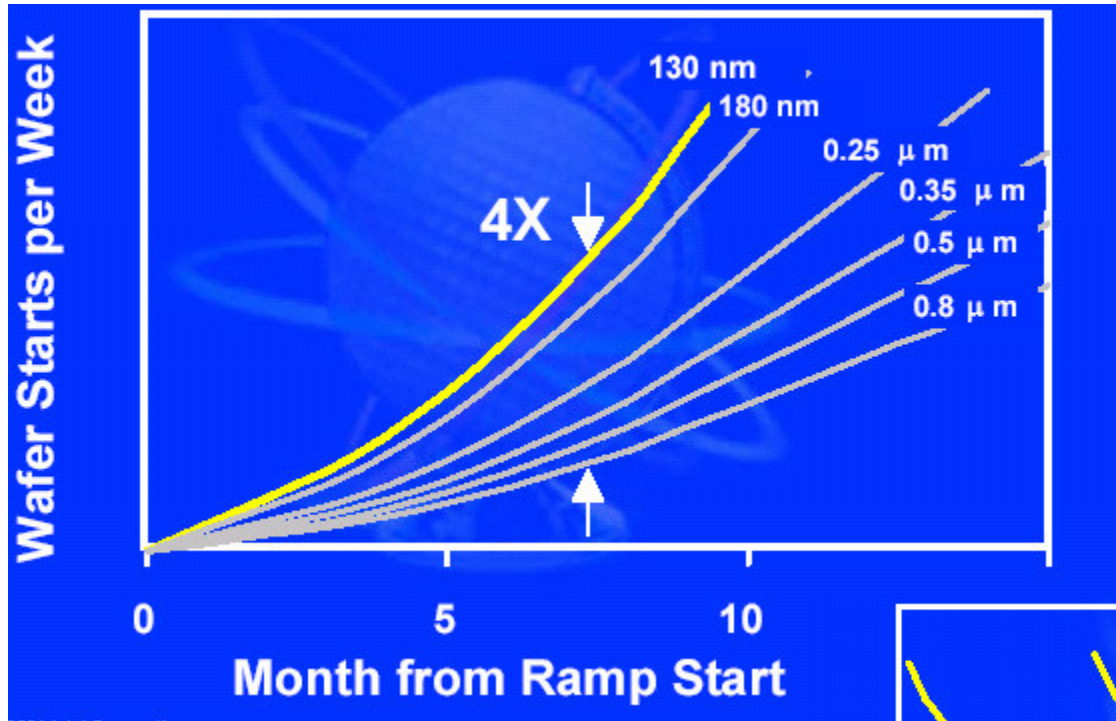
Source: Forbes  
Figure 3-5

*PHOTOLITHOGRAPHY COST  
STEPPER COST*



Source: ICE

# Pressure to Ramp Faster



# Integrated Circuit Value Chain

Greater Value or Time Sequence

Product Design		
Value	Example	Source
Product Definition	Printer, Workstation	
System Design	Network interface card, printer electronics	
Product-Specific IP		End Product Co.
Software IP	PhotoRET	ASIC Design House
Design & Test Tools & Methods	Synthesis, Datapath, FAST Scan	
High Level Standard IP	PCI, JPEG, SCSI	End Product Co.    EDA Vendor    Design Block Vendor
Foundation Standard IP	Cell library	Foundry

Assembly & Test			Silicon Process		
Value	Source	Example	Value	Example	Source
Test		Test & Assembly Vendor    Test Service	Volume Fab		Foundry 2
Assembly		Assembly Vendor	Prototype Fab		IDM    Foundry 2
Package Characteristics	Electrical, thermal, mechanical		Mask Making		Foundry 1    Mask Service
Package Technologies	FCOL, PBGA, CLGA	Package Vendor    IDM	Process Characteristics	LOR, EDR, SPICE	IDM    Design House    Modeling Service
			Process Technology	0.13um CMOS, BiCMOS	

Directs the delivery of the other values

Management		
Value	Example	Sources
Supply Chain Management		Design House    Supply Chain Manager
Technology Program Management		
Product Design Management		

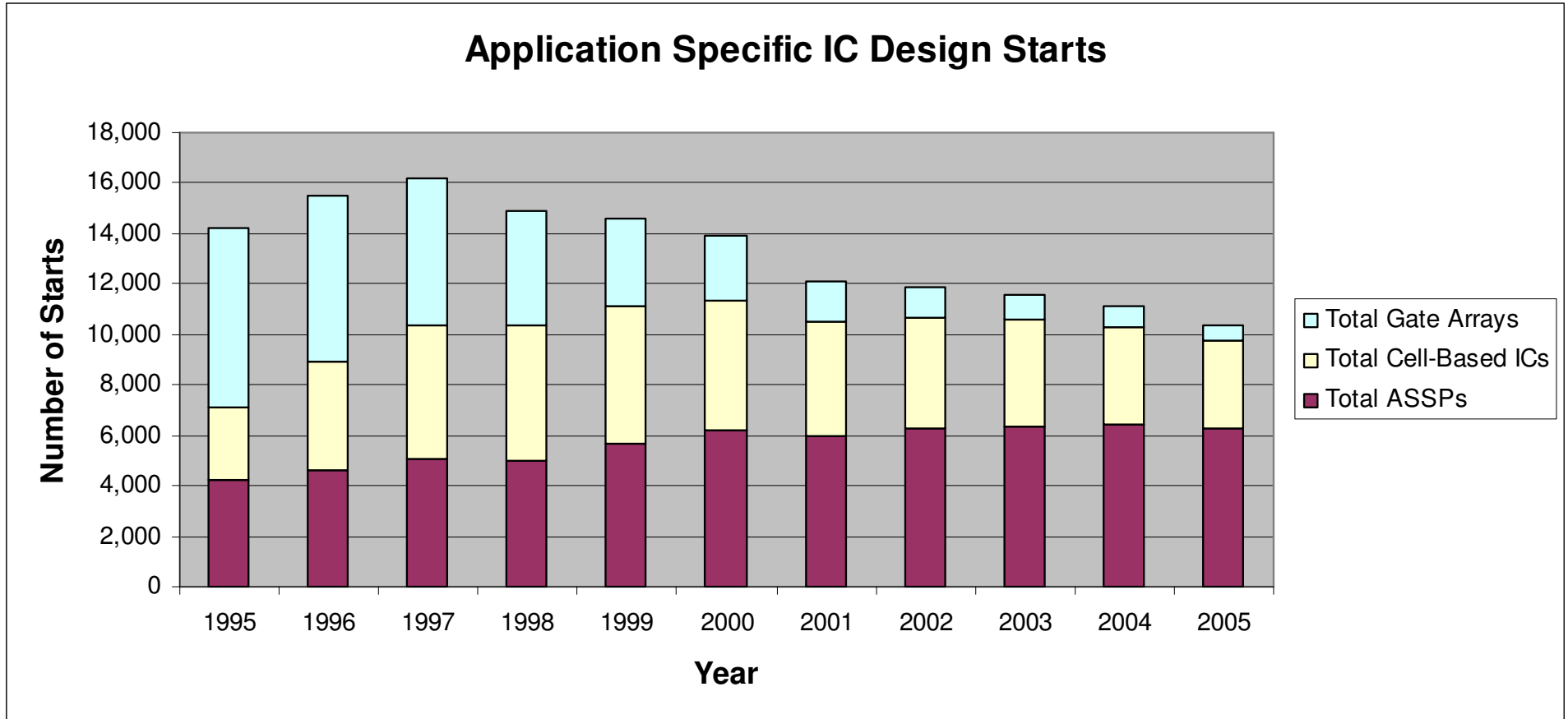
# Consequences of Business Challenges

- ❖ **Dominance of foundry/fabless model**
- ❖ **Process technology developed by & fabs operated by consortia ⇒ Less technology differentiation**
- ❖ **Fewer unique designs**
  - **ASICs replaced by programmable platforms**
  - **Fewer IC designers**
- ❖ **Stick to key value added & milk it for all it's worth:**
  - **If you're world-class at something, sell it to everyone**
  - **If you're not, buy it from someone who is**
- ❖ **Small design houses move from selling complete chips to selling design IP blocks to those who can afford chip NRE**
- ❖ **Slower process technology advancement, more use of older technologies**

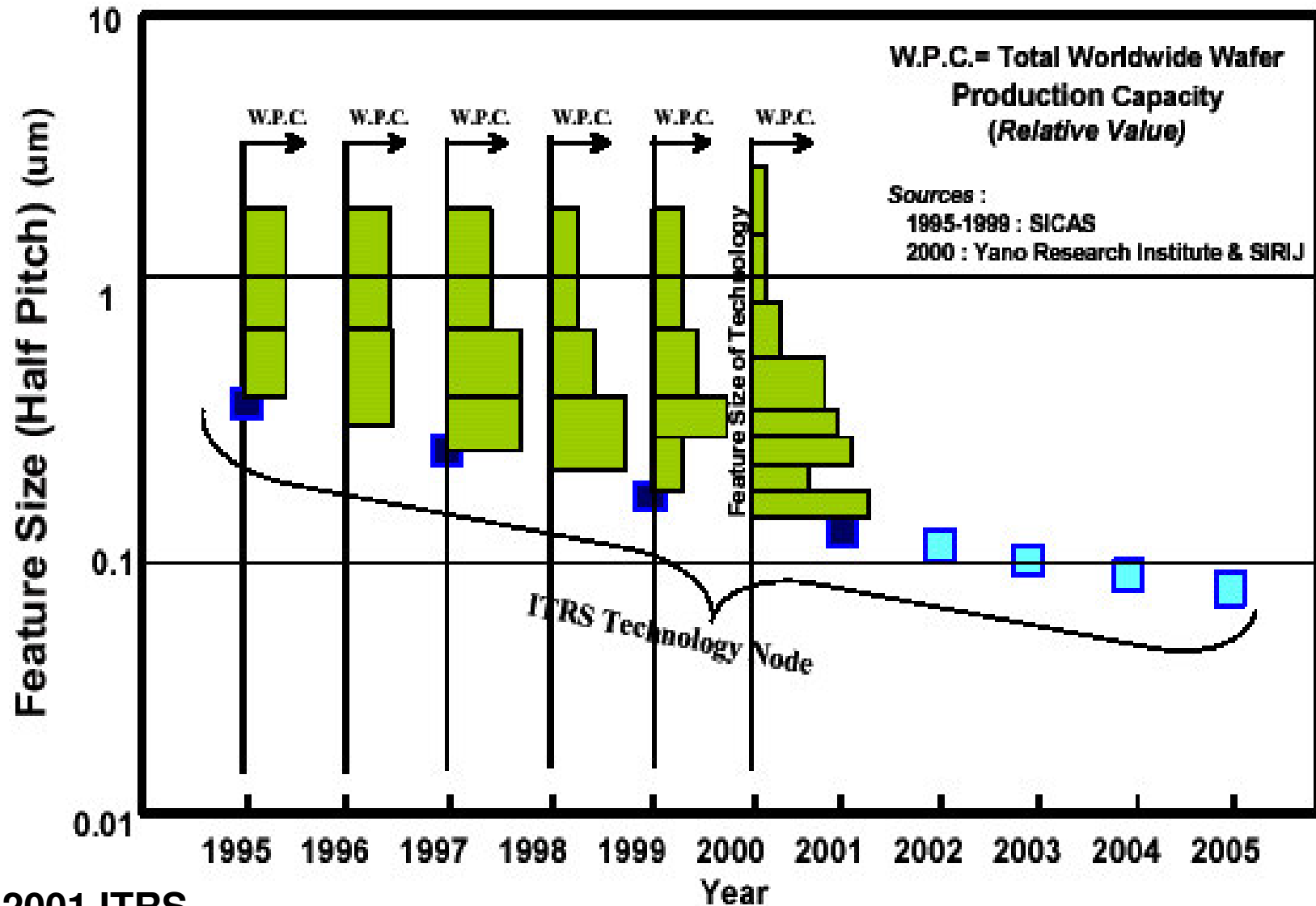
# Custom Design Starts

Gartner Dataquest - September 2001

## Application Specific IC Design Starts



# Not Everything is at the Limit



## 2001 ITRS

# Nanotechnology – The Way Around the Roadblocks?

- ❖ **Patterning: photolithography ⇒ Self assembly**
- ❖ **Materials: mixtures & structures that don't occur in normal chemistry**
- ❖ **Replaces requirement for perfection with fault-tolerance**