

ON-CHIP ESD PROTECTION DESIGN BY MIXED-MODE SIMULATION

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OUTLINE

- **On-Chip ESD Protection: Basics & Solutions**
- **Mixed-Mode ESD Simulation-Design**
- **Practical ESD Design Examples**
- **New Challenges: RF/M-S/Whole-Chip ESD**

Integrated Electronics Laboratory @ IIT

Research Interests:

- **Advanced IC designs:**
 - * Analog/mixed-signal/RF ICs
 - * SoC
- **Advanced ESD Protection for ICs**
- **IC CAD & Modeling**
- **Semiconductor Devices**

CURRENT RESEARCH ACTIVITIES @ IEL

- **Projects:**
 - * Resolution/sampling/power-optimized ADC in SiGe
 - * Multi-mode universal RF SoC ICs in SiGe BiCMOS
 - * Hi-resolution/hi-speed ADC chips in CMOS/BiCMOS
 - * Universal Digital-ready RF SoC ICs in CMOS/BiCMOS
 - * Super-compact cored RF IC inductors
 - * Modeling & CAD for electro-magnetic devices
 - * ASIC interpolator IC for sine/cosine optical encoder
 - * 15kV HBM ESD protection for mixed-signal ICs
 - * ESDcat - whole-chip ESD design verification CAD
 - * Super-compact ESD protection
 - * RF ESD protection in CMOS/BiCMOS
 - * 3D ESD protection simulation-design methodology

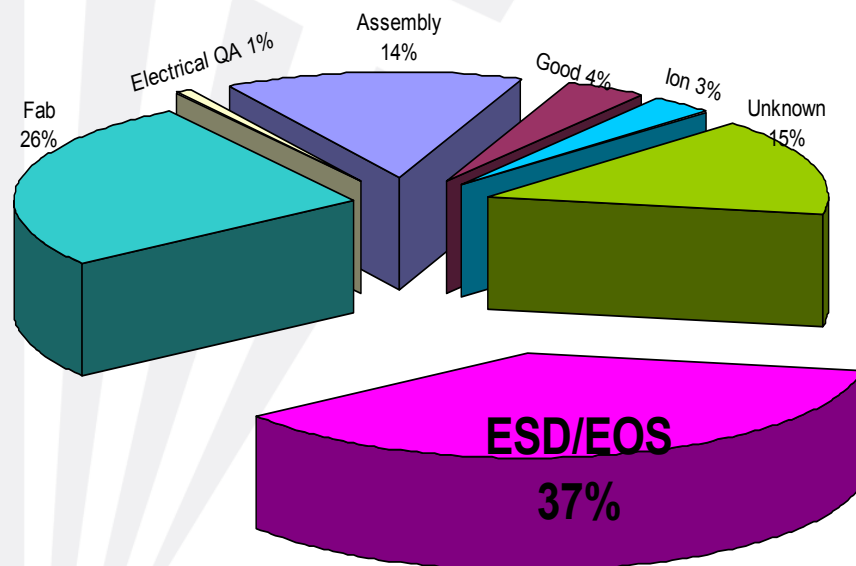
WHAT IS ESD?!

- ESD = Electrostatic Discharge
 - ESD events - transfer of charges between objects
 - Phenomena - super fast & huge I/V-pulses
- ⇒ Cause electronic part (IC) damages

A Multi-B-\$ Problem

- ESD failures - 30%-50% IC field failures
- A killing factor for time-to-market.

Informal ESD Failure Statistics



[1] L. Brown, et al, Electronic Packaging & Production, April 1990.

[2] R. Merrill, et al, EOS/ESD symp., 1993.

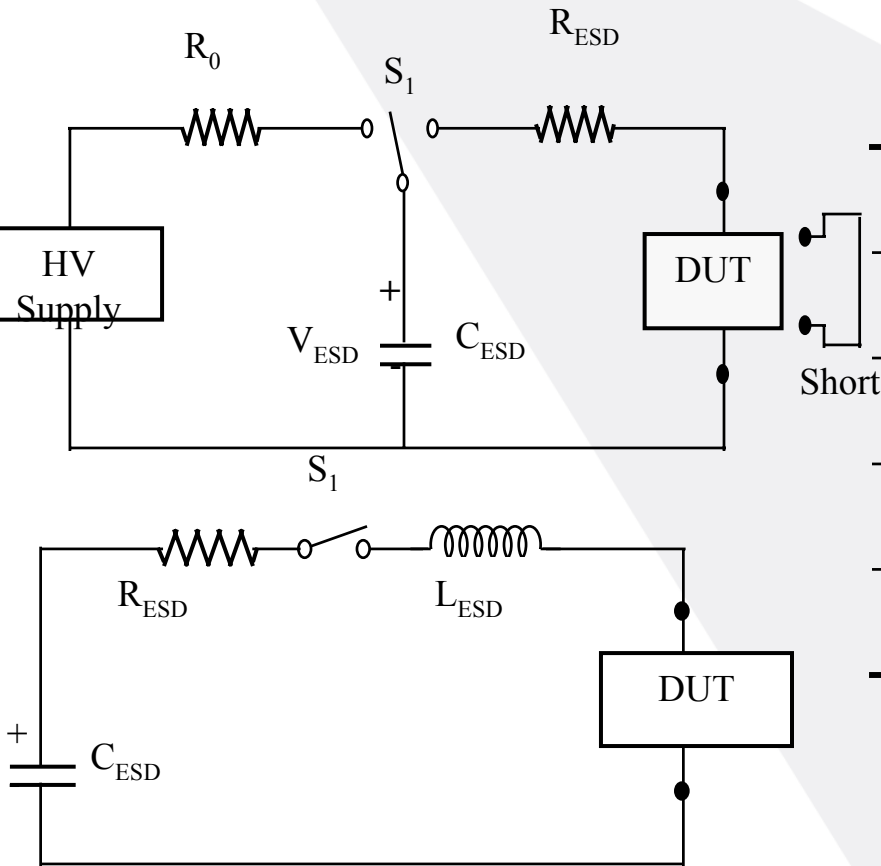
ESD Protection

- Advanced package solutions.
 - Buffers using new anti-ESD materials.
 - Add-on ESD devices.
- **On-Chip ESD protection circuitry for all I/Os of IC chips.**

ESD Test Models

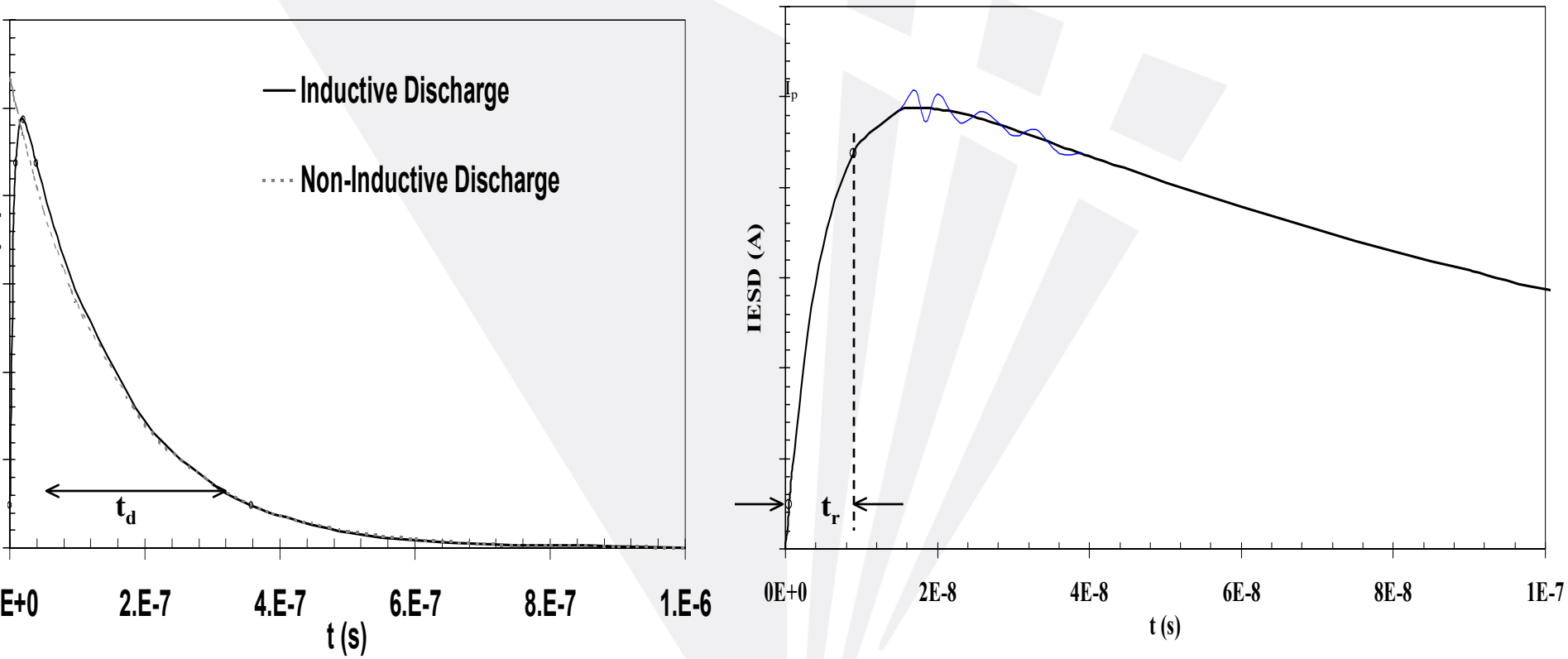
- **HBM** - human body model.
- **MM** - machine model.
- **CDM** - charged device model.
- **IEC** - Int'l Electrotechnical Commission Model
- **TLP** - transmission line pulse model
- **Field Induction.**

HBM ESD Test Model



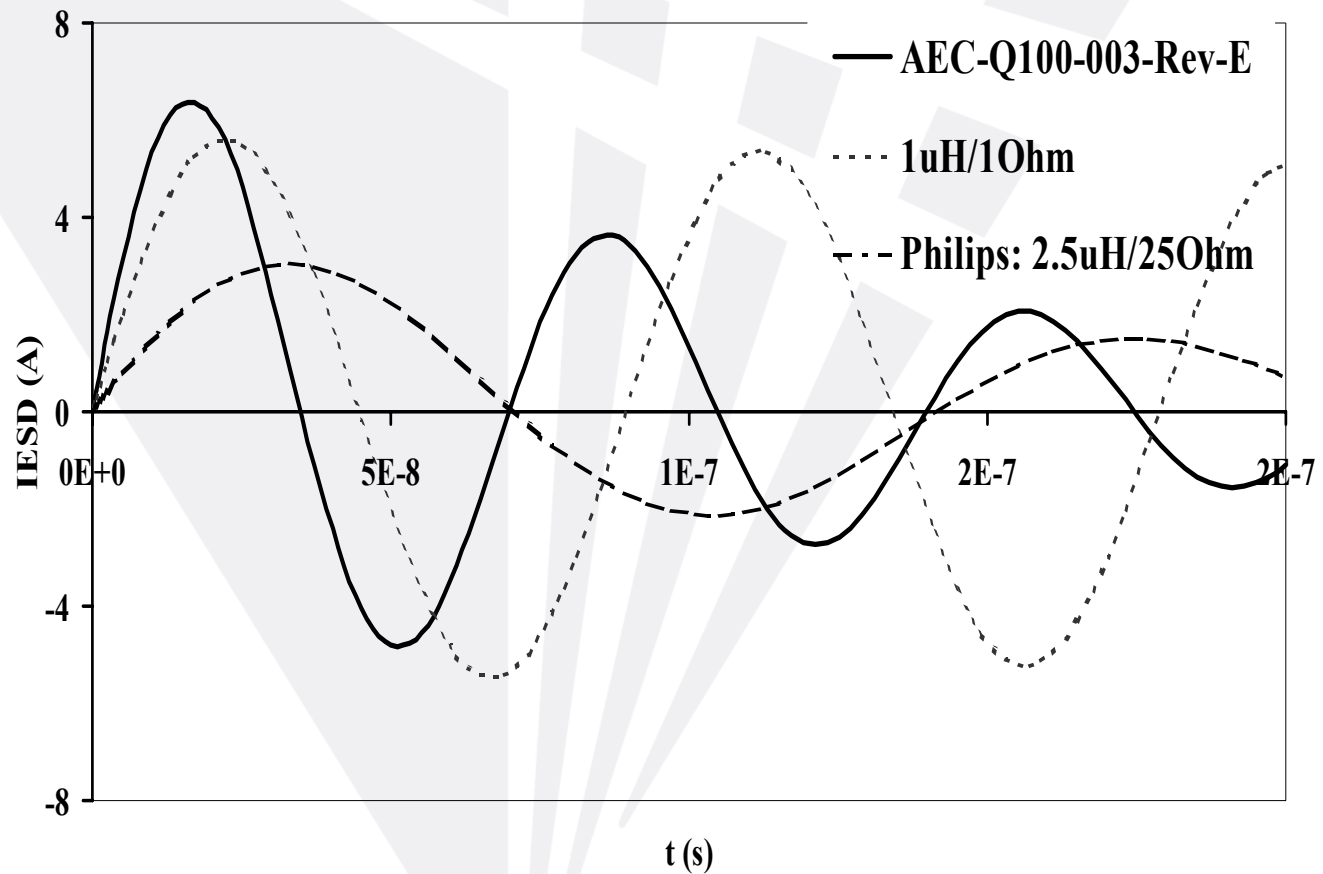
| Elements | Specifications |
|-----------|------------------------------|
| R_0 | $10^6 - 10^7 \Omega$ |
| R_{ESD} | $\sim 1500 \Omega$ |
| C_{ESD} | $\sim 100 \text{pF} \pm 1\%$ |
| L_{ESD} | $\sim 7.5 \mu\text{H}$ |

HBM ESD Pulse Waveform



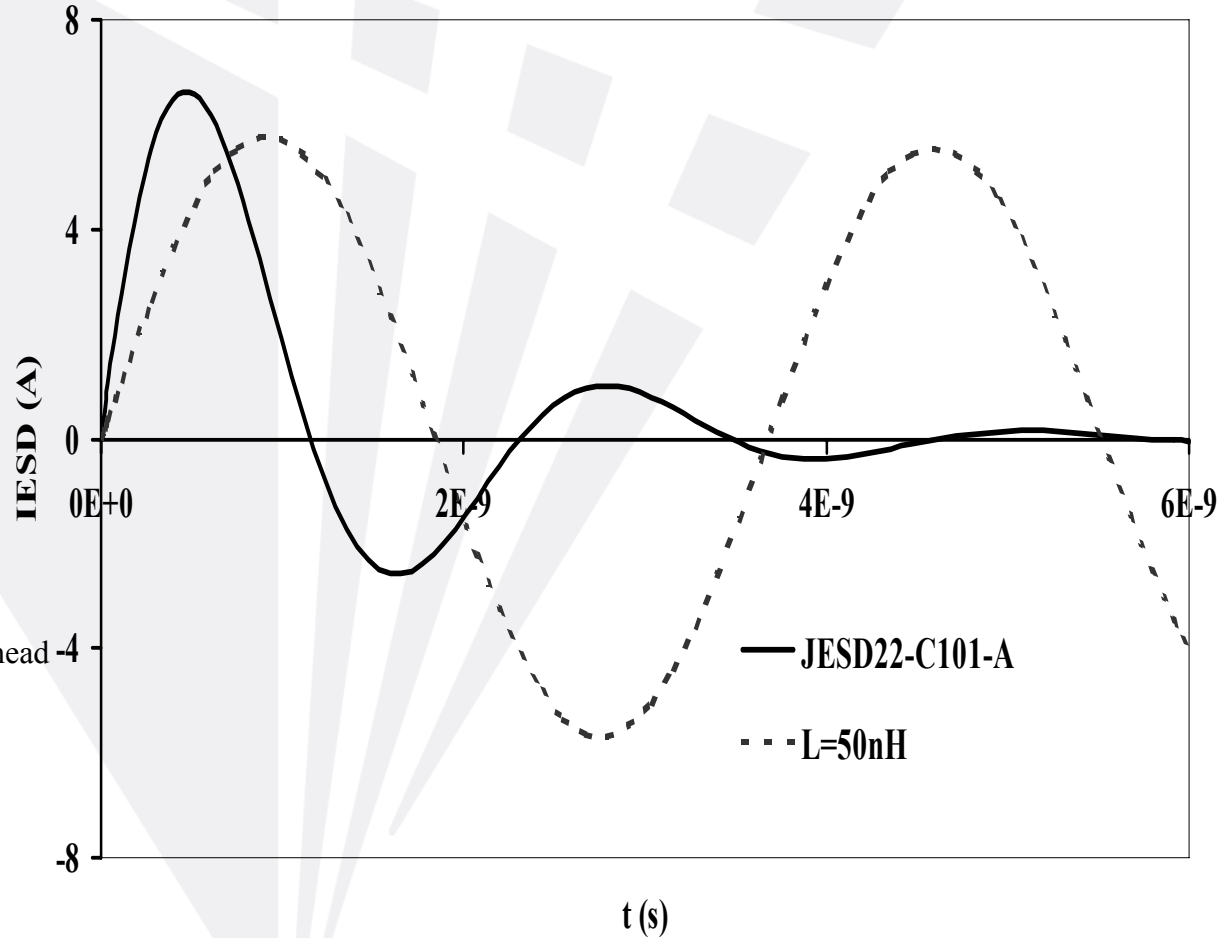
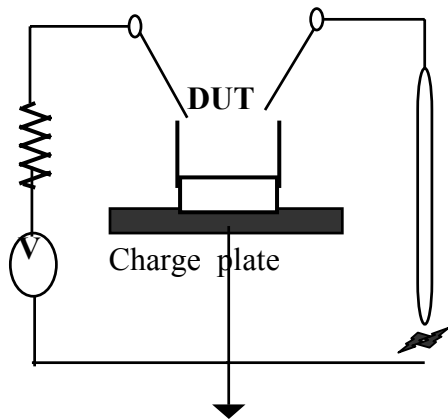
MM ESD Model

- **Oscillatory**
- $C_{ESD} = 200\text{pF}$
- $R_{ESD} \sim 0$
- $L_{ESD} \sim 2.5\mu\text{H}$



CDM ESD Model

- **Oscillatory**
- $C_{ESD} = 6.8\text{pF}$
- $R_{ESD} = 0\sim 25\Omega$
- $L_{ESD} \sim 5\text{-}100\text{nH}$
- $t_r < 1\text{ns}$



IEC ESD Model

- $C_{ESD} = 150\text{pF}$
- $R_{ESD} \sim 330\Omega$
- $L_{ESD} \sim 0$
- $t_r < 1\text{ns}$

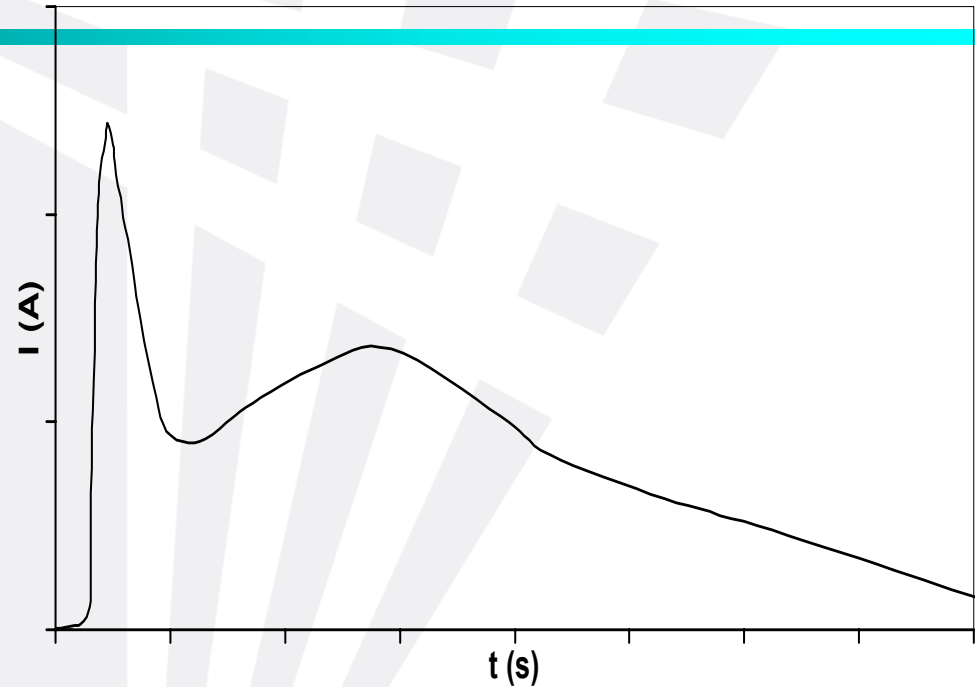
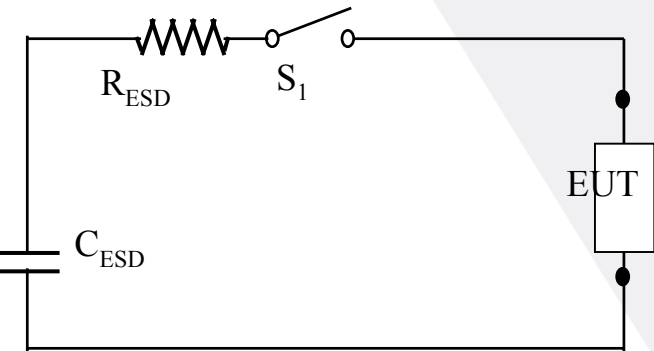
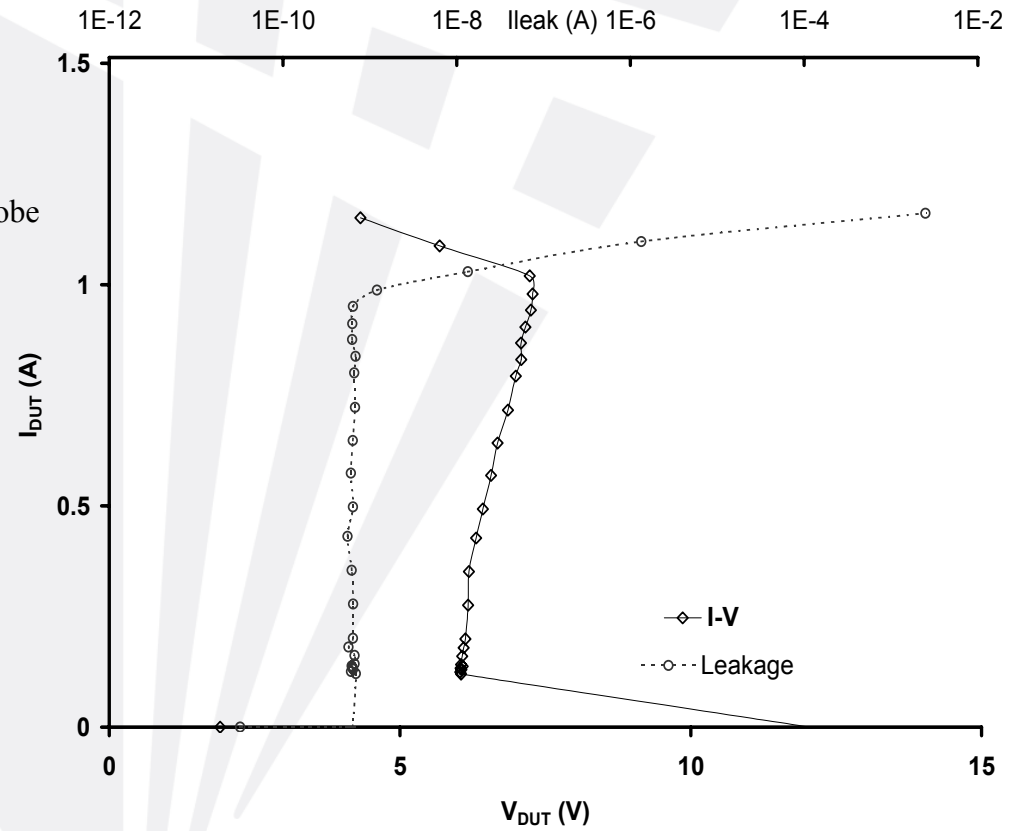
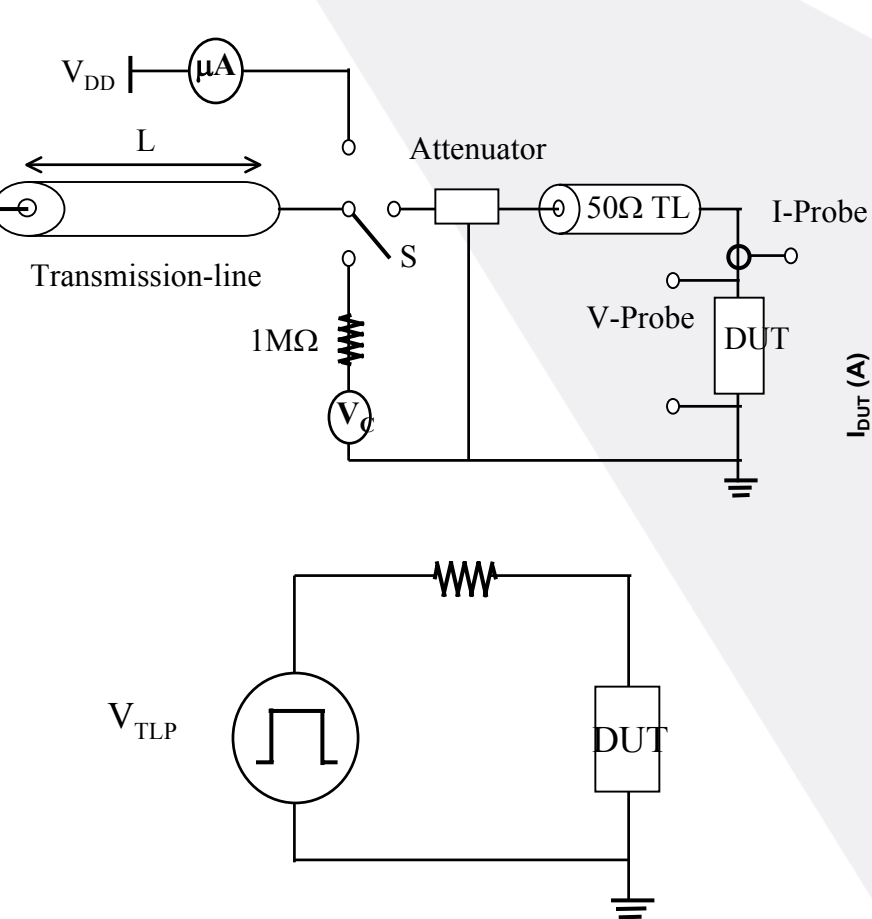


Table III IEC test classification

| Contact discharge | | Air discharge | |
|-------------------|--------------|---------------|--------------|
| Level | Test voltage | Level | Test voltage |
| 1 | 2kV | 1 | 2kV |
| 2 | 4kV | 2 | 4kV |
| 3 | 6kV | 3 | 8kV |
| 4 | 8kV | 4 | 15kV |
| x | open | x | open |

TLP Test Model



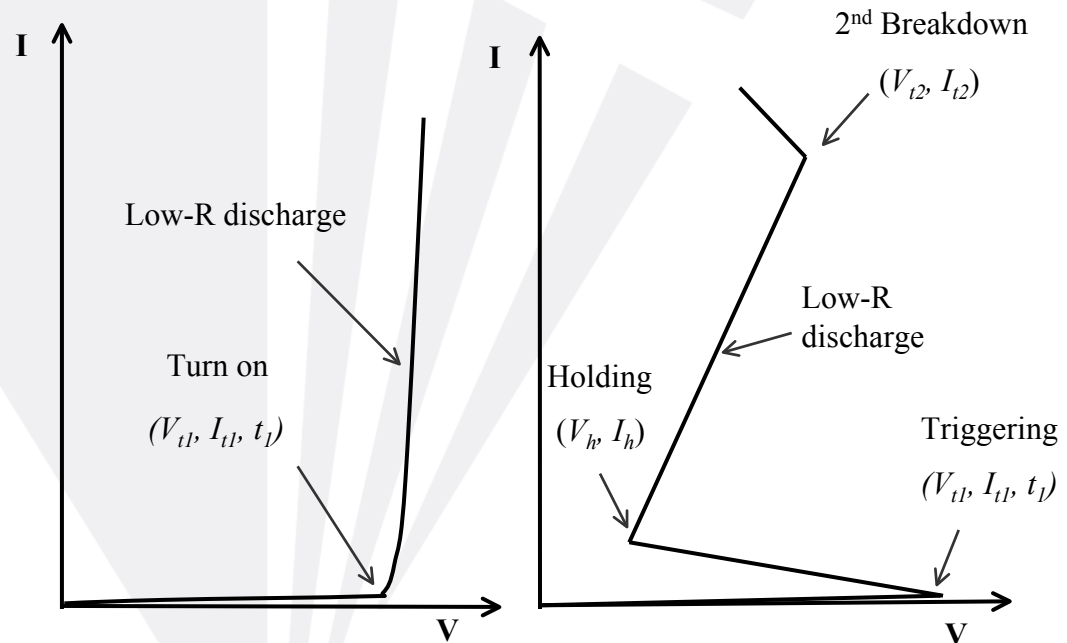
On-Chip ESD Protection: Basics

- **Two types of ESD damages:**
- Thermal damage → heat generation in Si, metal
← high current
- Dielectric rupture ← high electric field
← high voltage

- **Two ESD protection requirements:**
- To discharge hi-current safely,
- To clamp pad voltage to a sufficiently low level.

ESD Protection Mechanisms

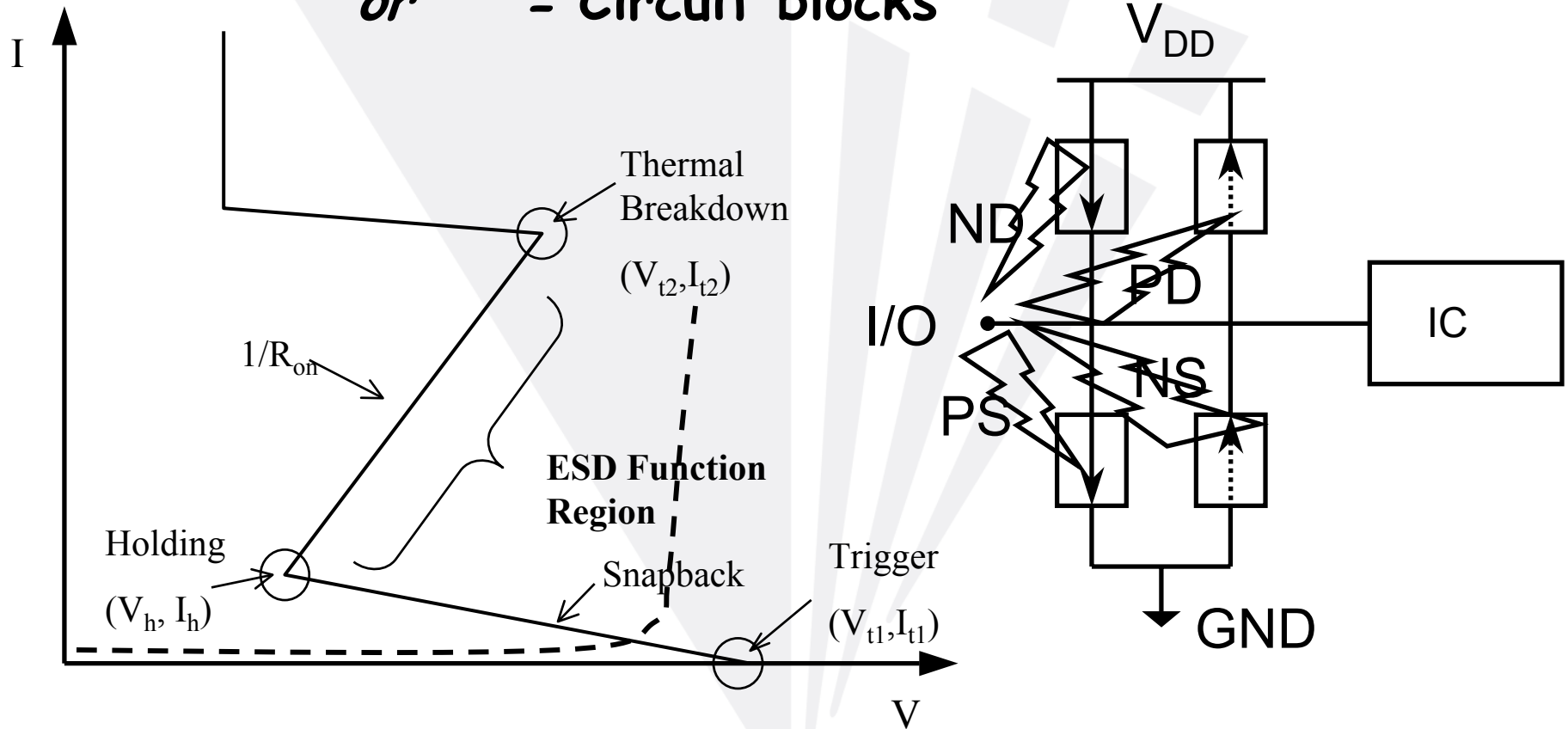
- Two ESD protection mechanisms:
- Simple turn-on I-V,
- Snapback I-V.



- Key parameters:
- (V_{t1}, I_{t1}, t_1) , (V_h, I_h) , (V_{t2}, I_{t2}) , etc.

A Complete ESD Protection Scheme

- ESD protection = Devices: Diodes, BJT, MOS, SCR...;
or = Circuit blocks

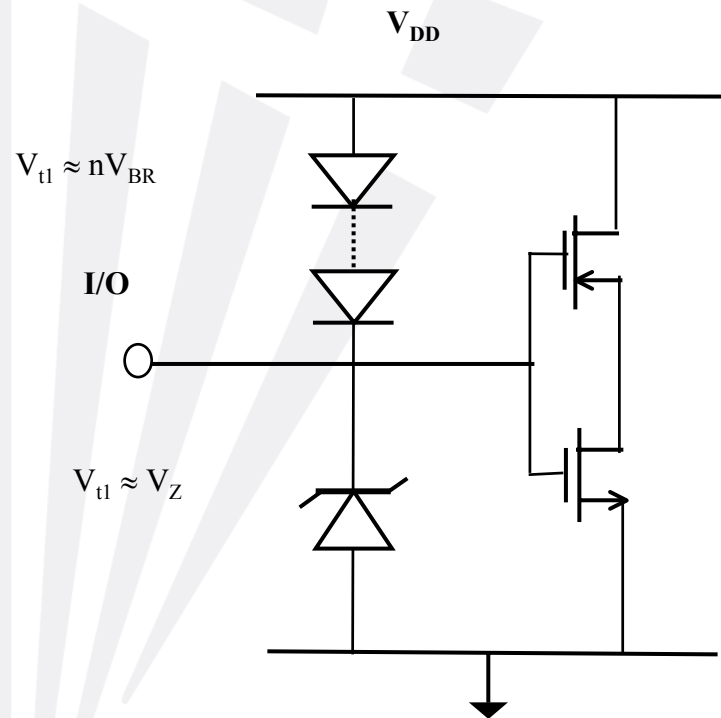


Diodes as ESD Protection

- Diode ESD protection: Forward or Reverse,
- Hi-current mode,

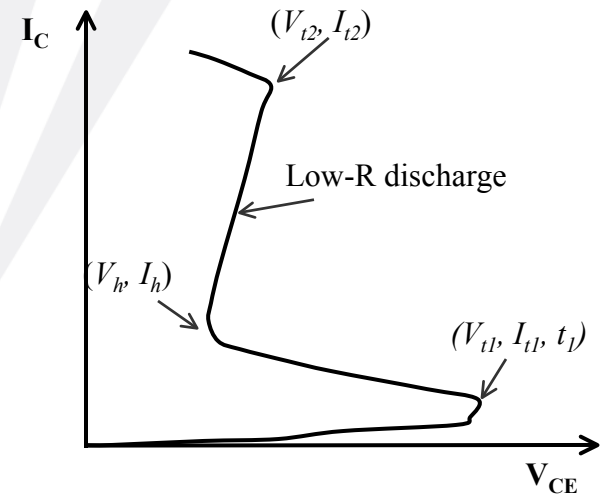
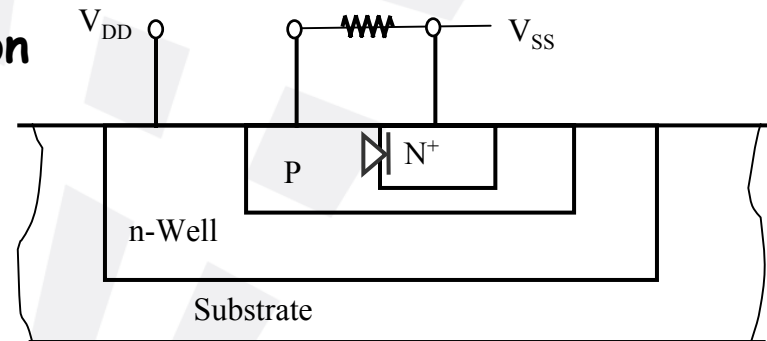
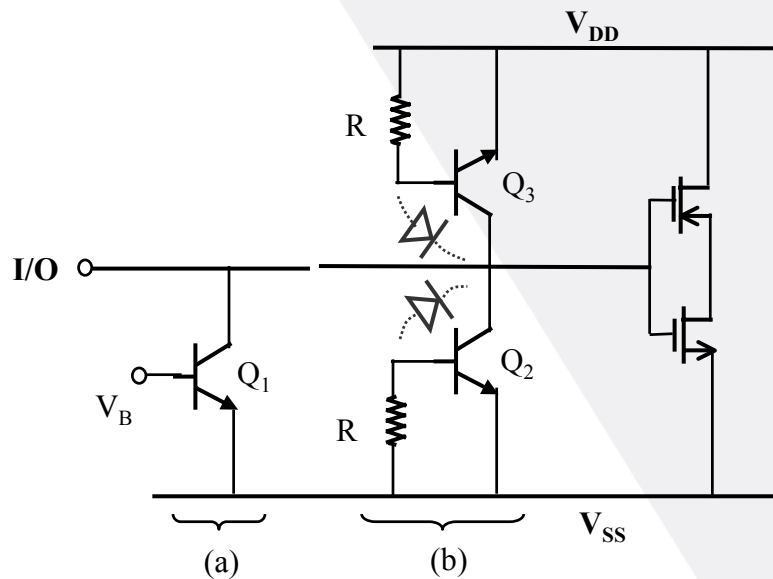
$$i_D \propto e^{\frac{v_D}{2V_T}}$$

- Forward diode strings,
- Zener diodes



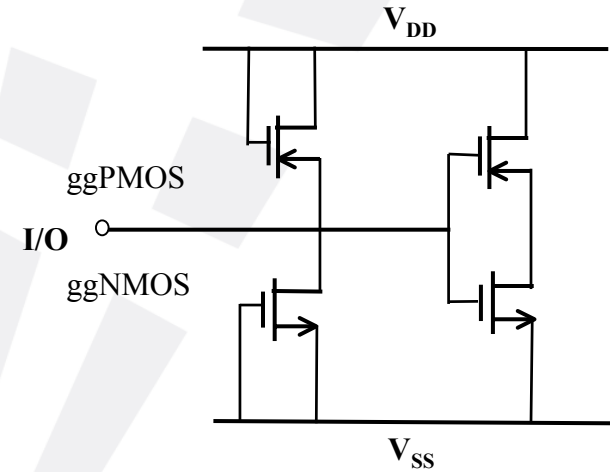
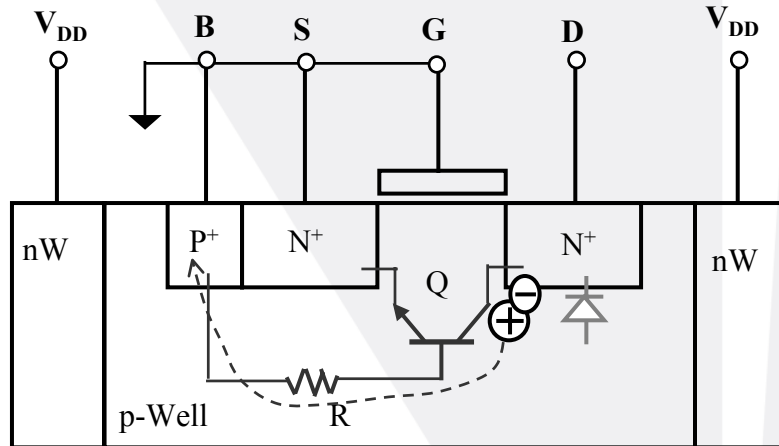
BJTs for ESD Protection

- BJT in hi-injection mode in ESD operation

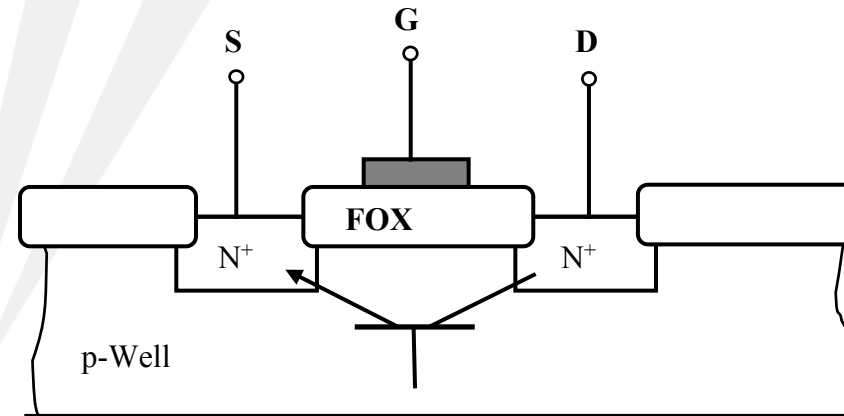
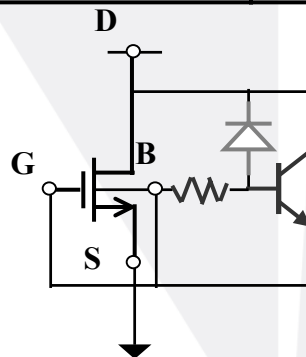


MOSFETs for Protection: ggMOS

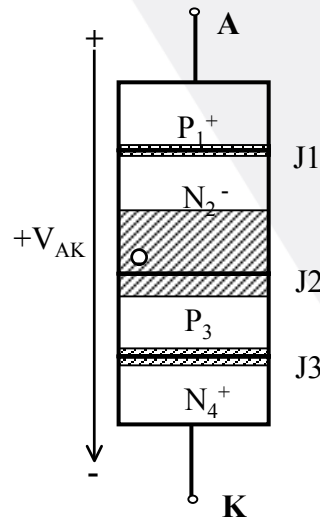
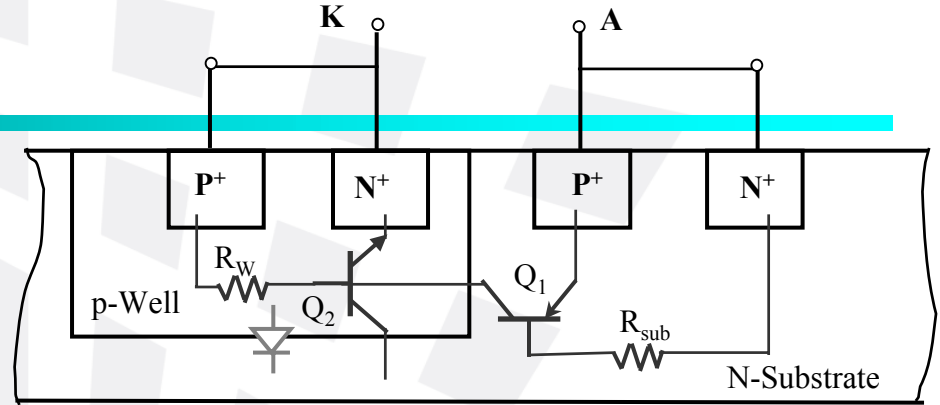
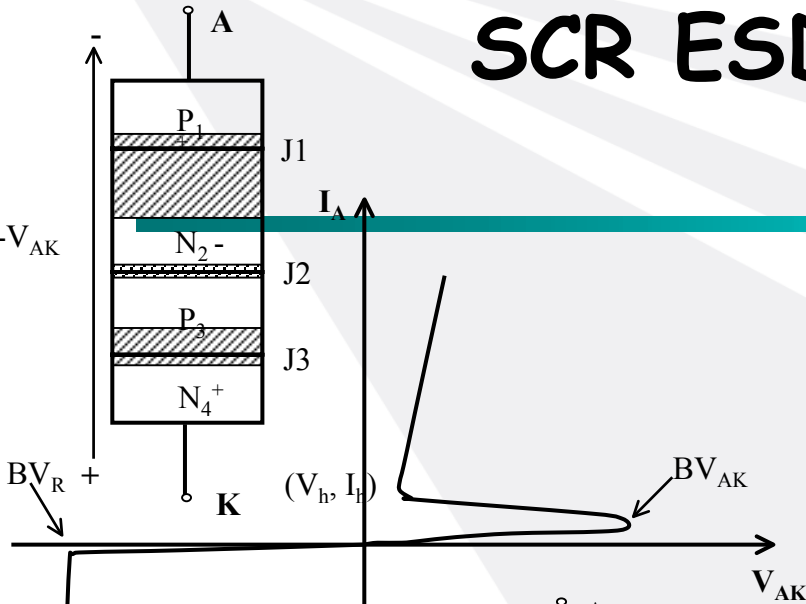
- Grounded-gate NMOS ESD protection device



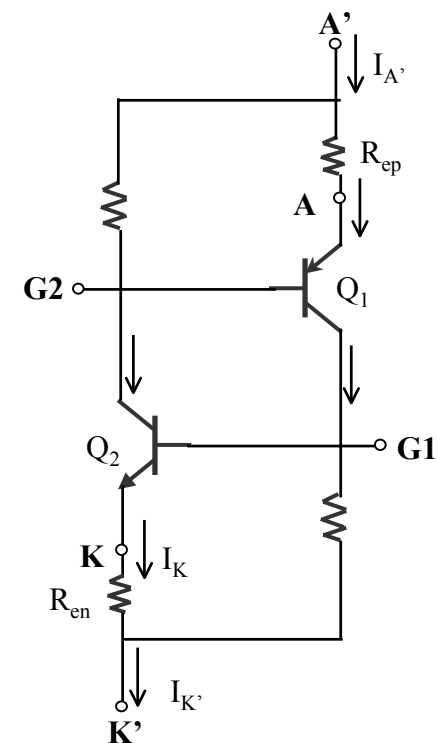
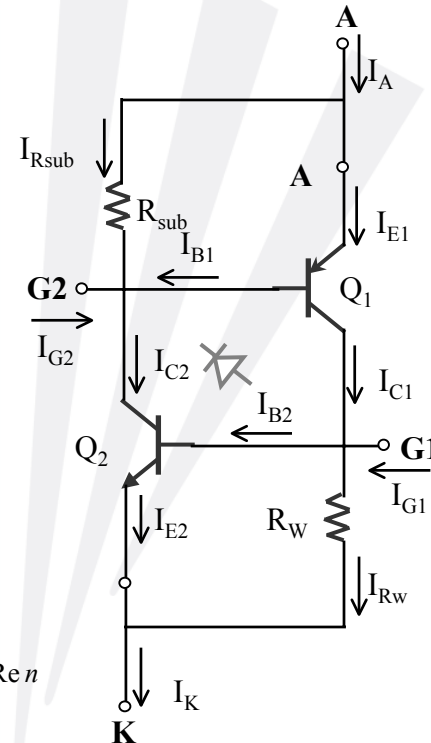
- Thick-oxide NMOS:



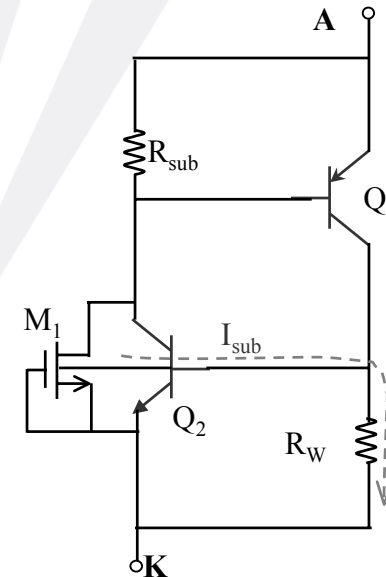
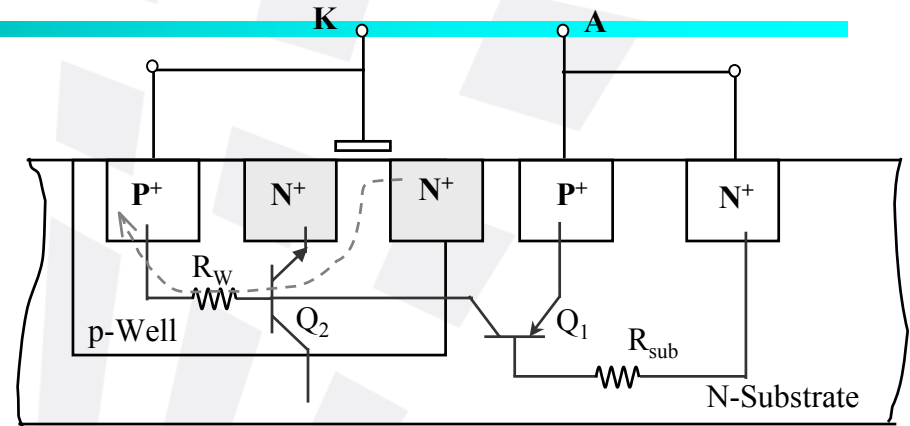
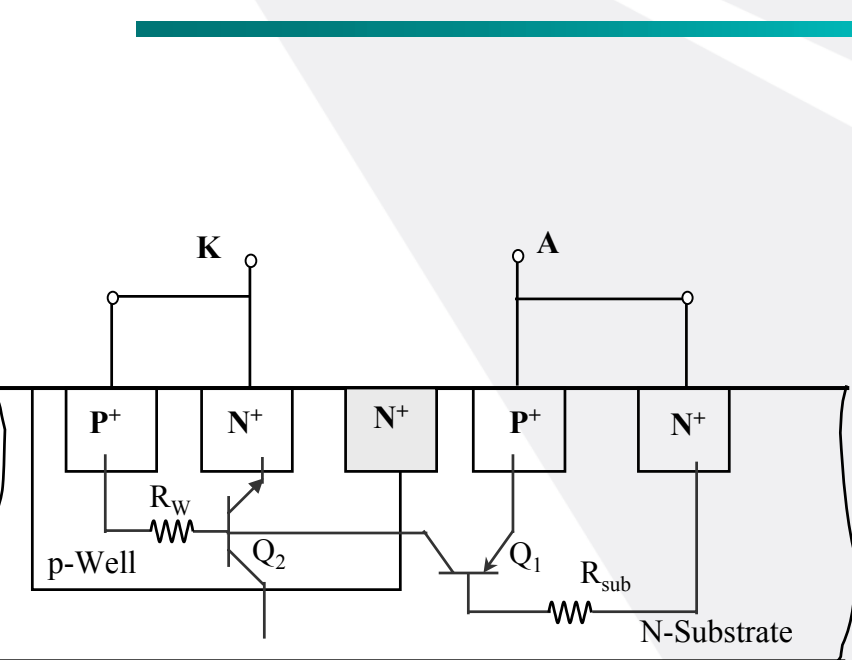
SCR ESD Protection Structures



$$BV_{AK} \approx BV_{DJ_2} \left(1 - \alpha_1 \frac{I_A}{I} - \alpha_2 \frac{I_K}{I}\right)^{1/n} + V_{Rep} + V_{Ren}$$



MVSCR/LVSCR ESD Protection



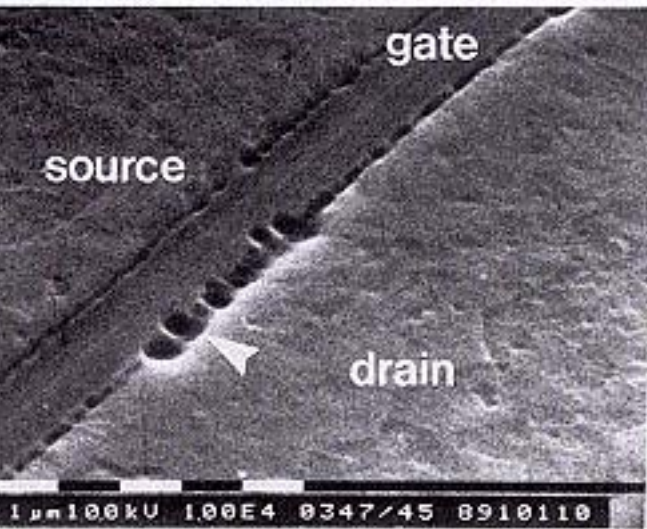
ESD Failure Analysis

- **Catastrophic failure → destroying devices.**
 - * **Thermal breakdown: Si, metal interconnects**
 - * **Dielectric rupture: MOS gate oxide**

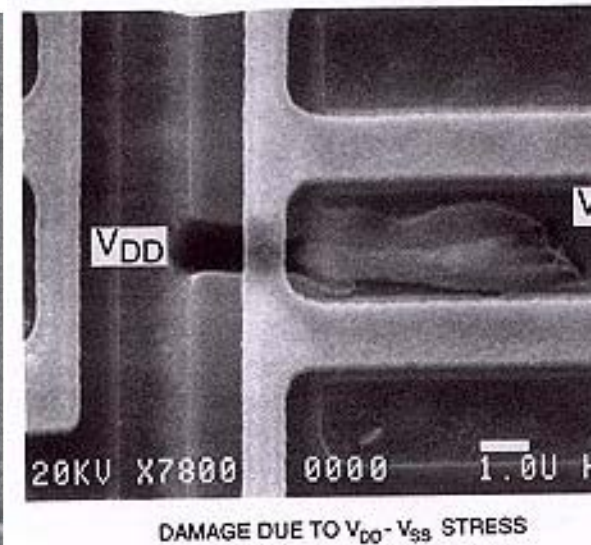
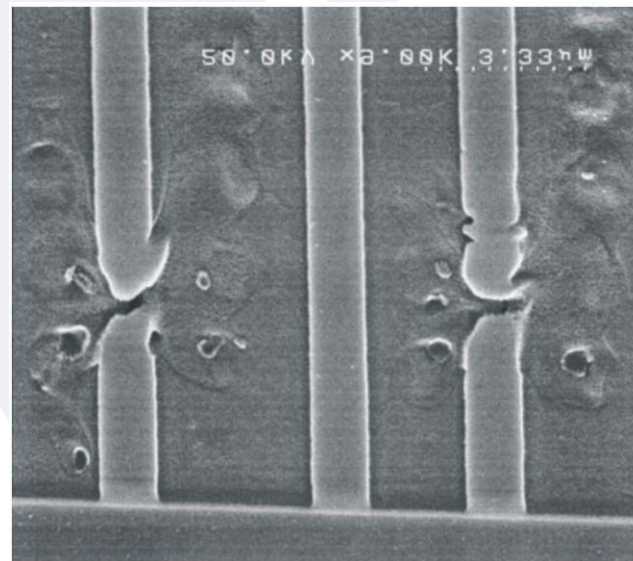
- **Latent defects → degradation.**
 - * **Increased leakage**
 - * **Lifetime problem**
 - * **Unknown mechanisms**

ESD Failure Signatures

effects at D/G diffusion edge



V_{DD}-V_{SS} stressing



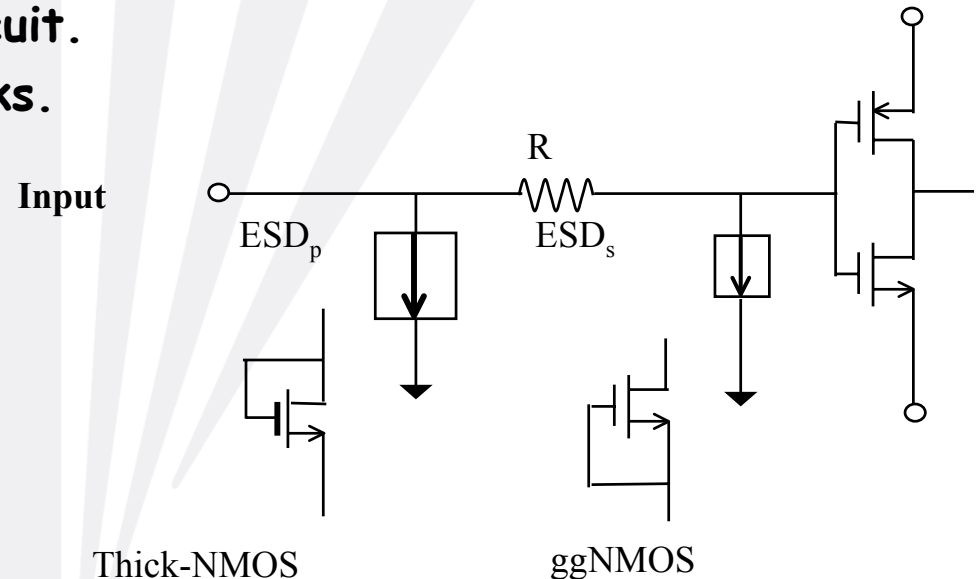
D-S local defect in fingers

ESD Protection Circuits

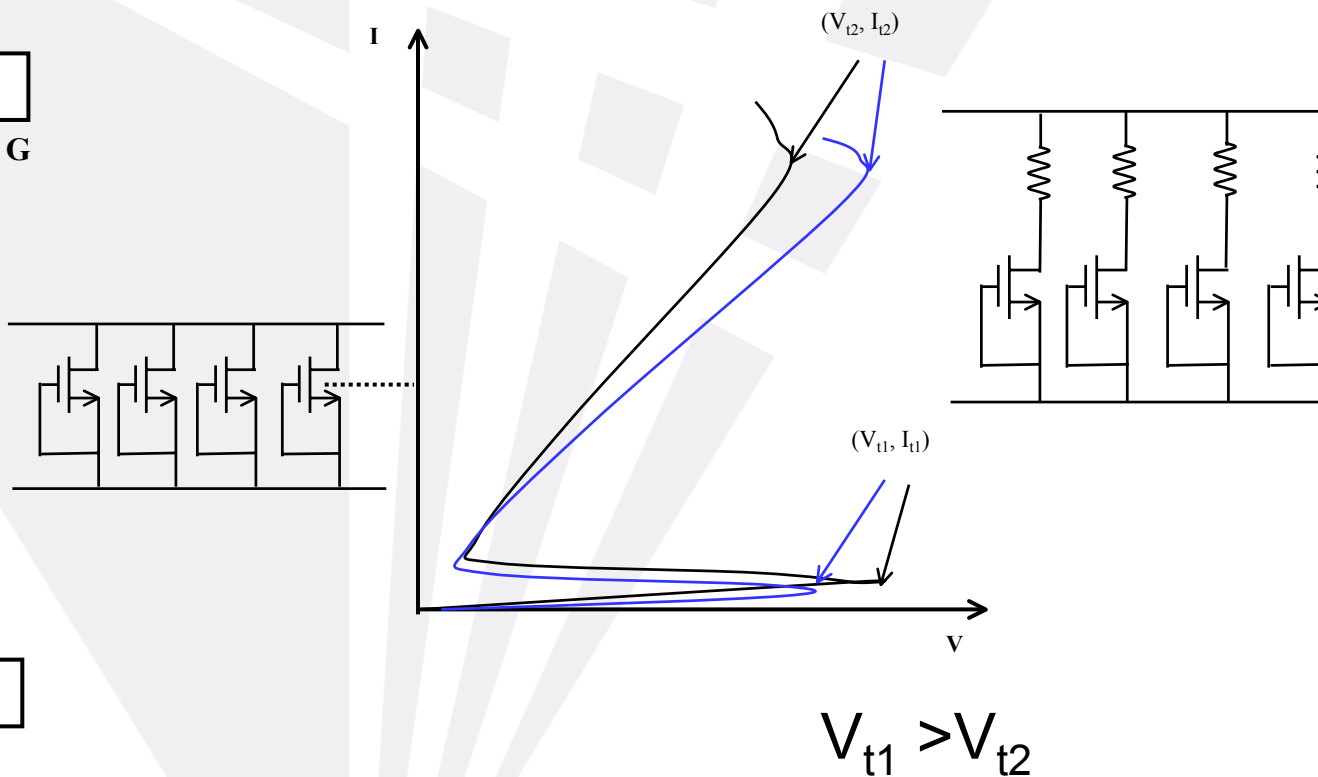
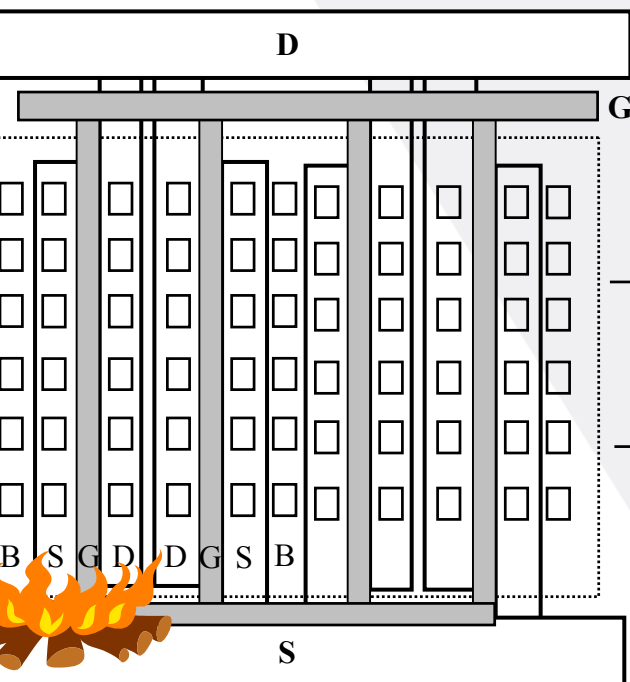
- ESD protection goes beyond single-device solutions,
- Complex ESD protection circuits are used in modern IC designs,
- To meet unique need of different circuit blocks on a chip,
- To take full use of modern IV technologies: BiCMOS, RF, Hi-V, SiGe, SOI, etc.

I/O ESD Protection Circuits

- **A primary-secondary protection scheme**
- Primary unit: takes most ESD current, low- V_h , but $V_{t1} \sim$ high,
- Secondary unit: lower V_{t1} , handle low ESD pulse,
- Isolation-R: V-build-up after 2nd one ON, to turn on 1st one; prevent current flowing into internal circuit.
- Any reasonable combination works.

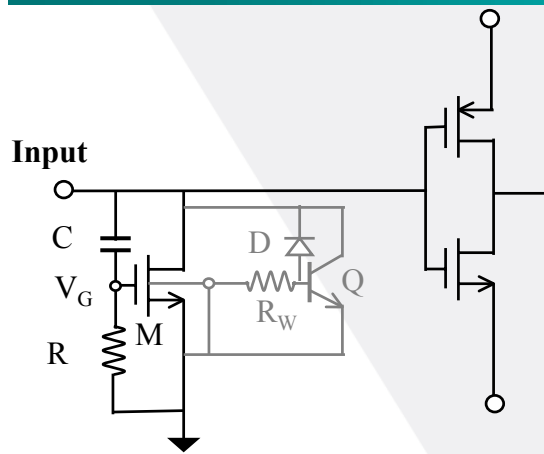


Multi-finger ggNMOS ESD Protection

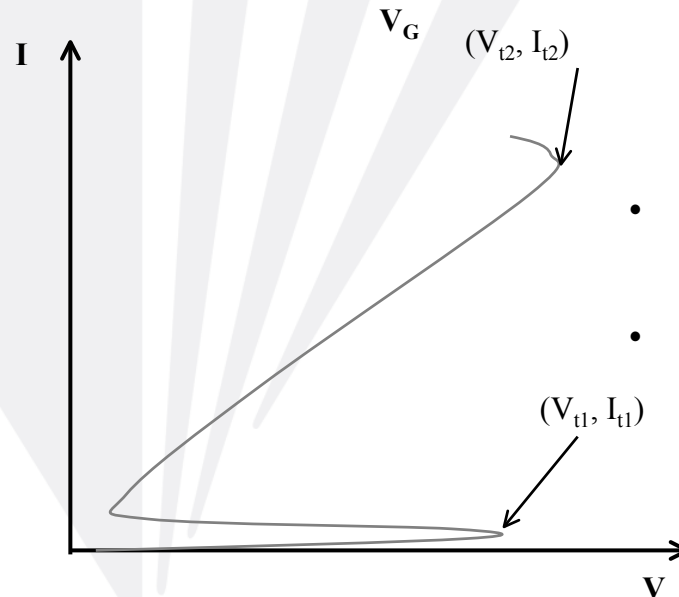
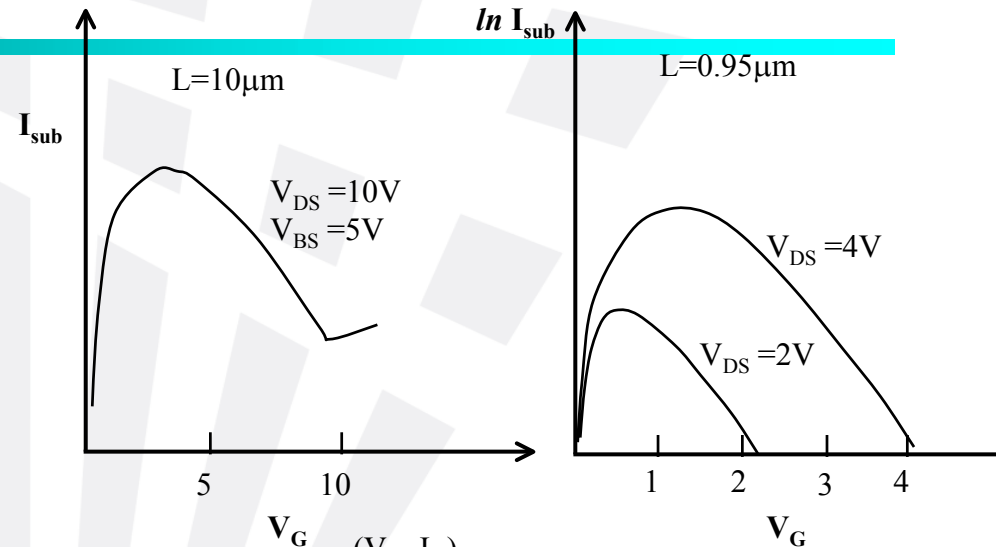
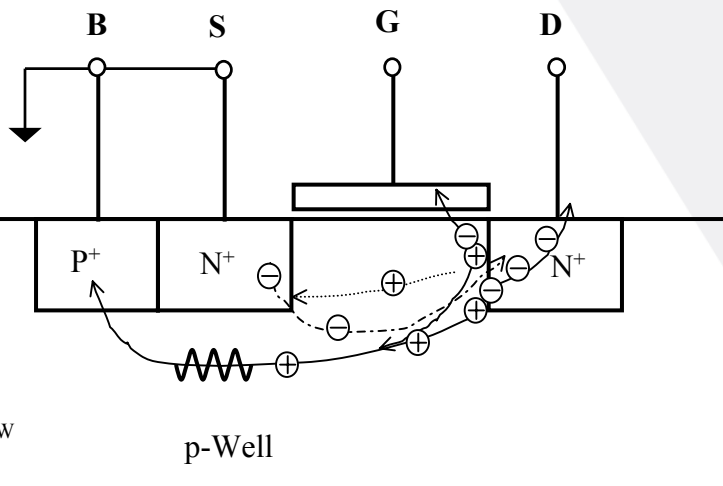


- Issue: non-uniform turn-on → lower protection than designed
- Solution 1: using Ballasting -R,
- Solution 2: make $V_{t1} < V_{t2}$

Gate-coupled NMOS (gcNMOS)

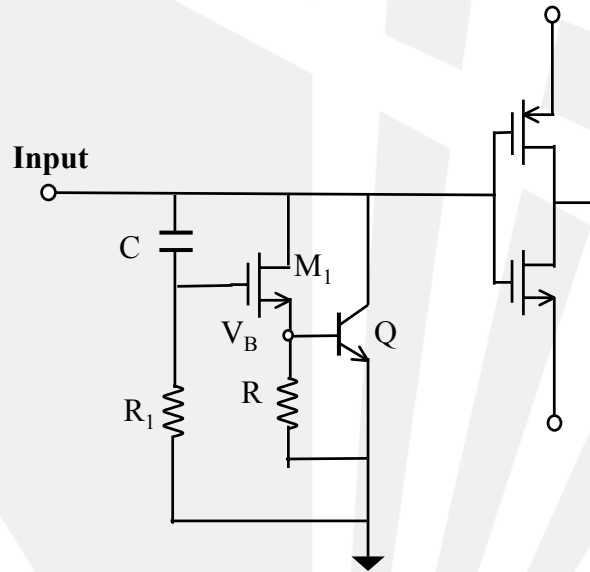
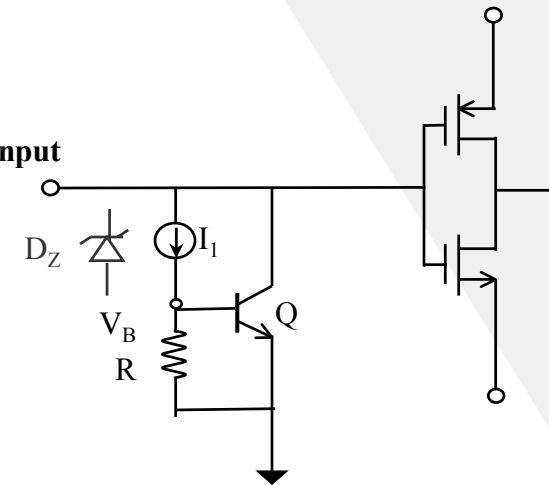


gcNMOS



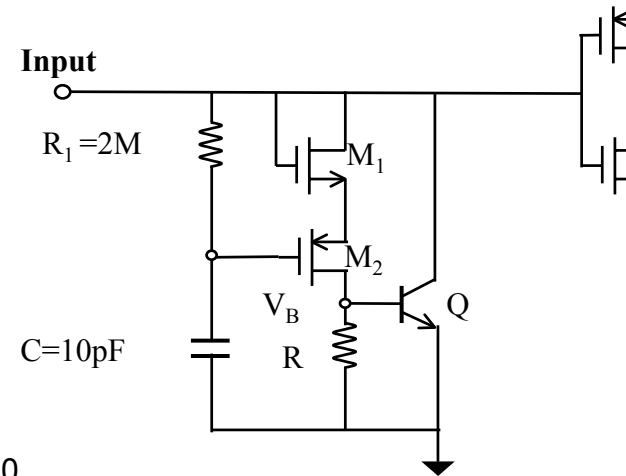
- $V_g \Rightarrow$ Hot carriers
 $\Rightarrow I_{sub} \Rightarrow V_{t1} < V_{t2}$
- But $V_g < BV_g$

BJT ESD Protection Cirucits



gcNMOS-triggered BJT
 $C_{gs} \rightarrow$ bad RC timing
 \rightarrow mis-triggering?

Add M2 to break the path

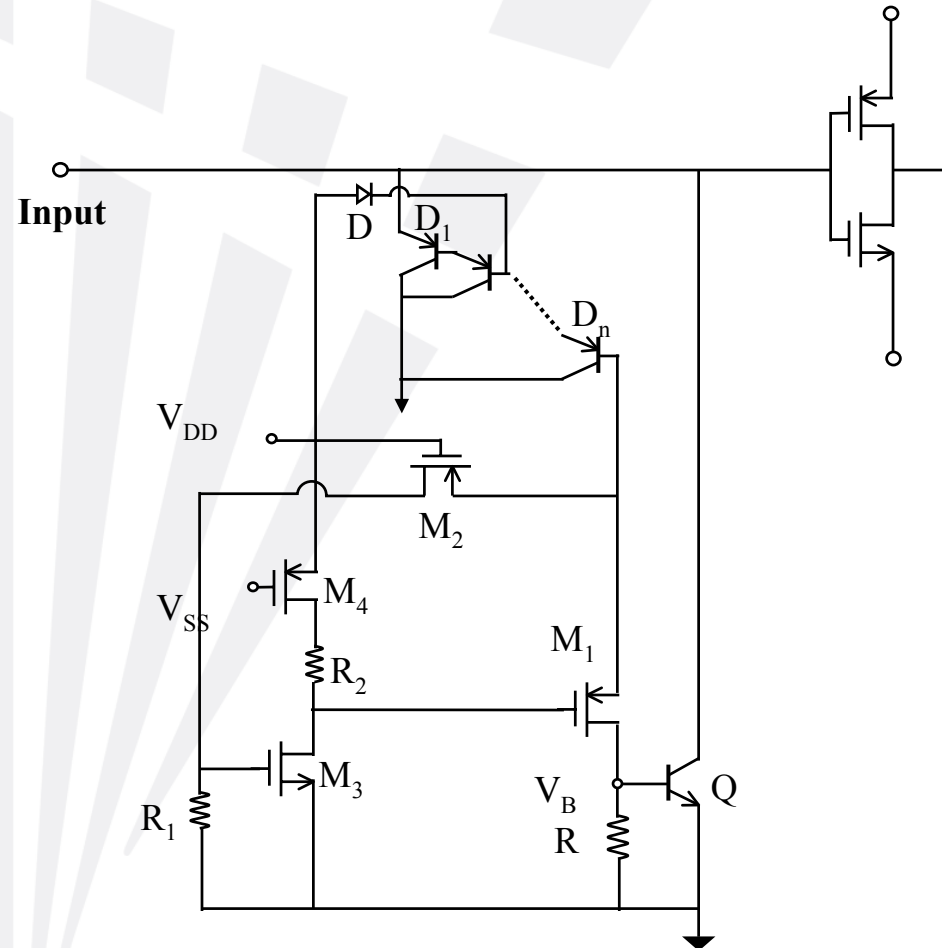


Ref: Tandan, N., "ESD Trigger Circuit", *Proc. 16th EOS/ESD Symp.*, 1994, pp.120

A complex CMOS trigger BJT circuit

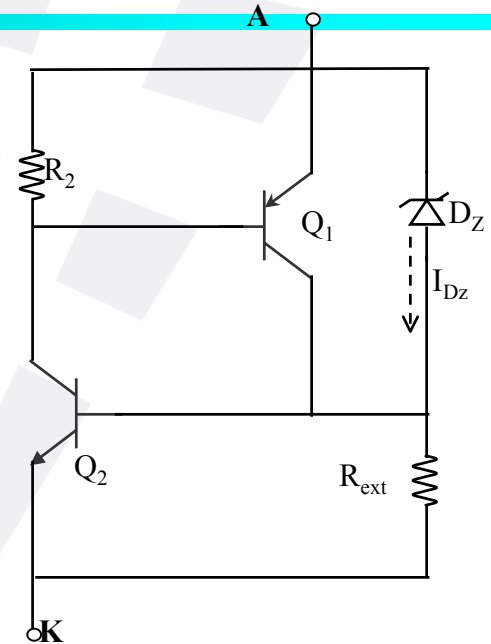
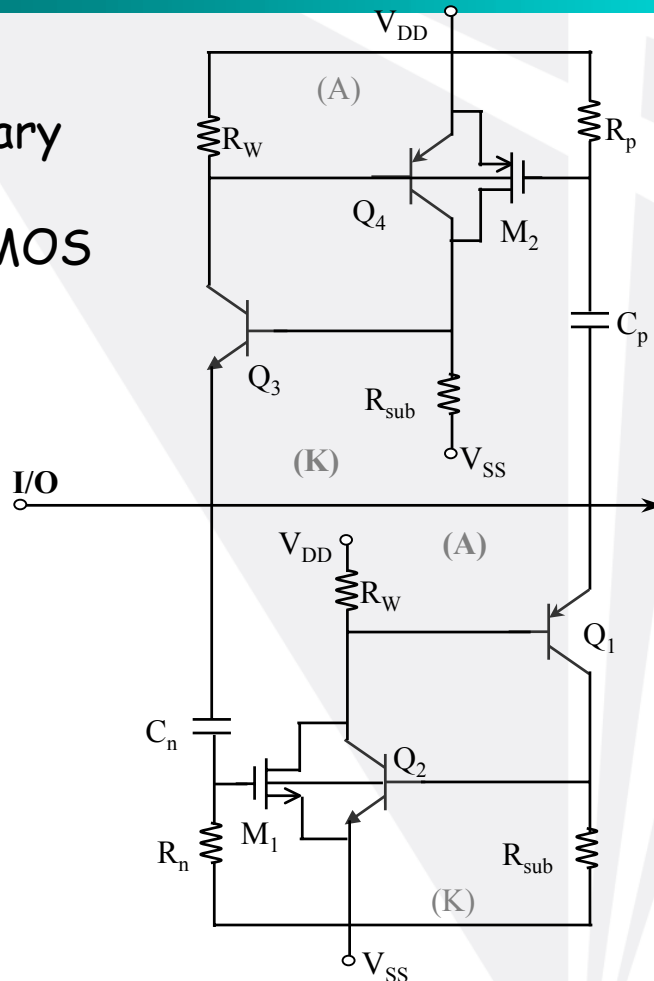
- Zener-D not available in CMOS
- D-string = external-I to BJT
- M1=isolation w/o ESD; ON at ESD
- +ESD: M2=On, M2+R → M3=On
- → M1 = On
- → trigger BJT

Ref: J, Smith, *Proc. EOS/ESD*, p63, 1998.



SCR ESD Protection Circuits

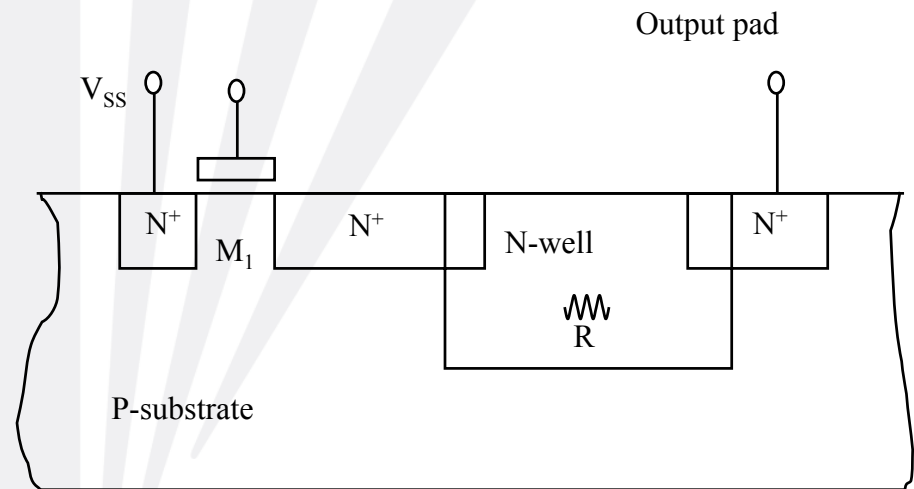
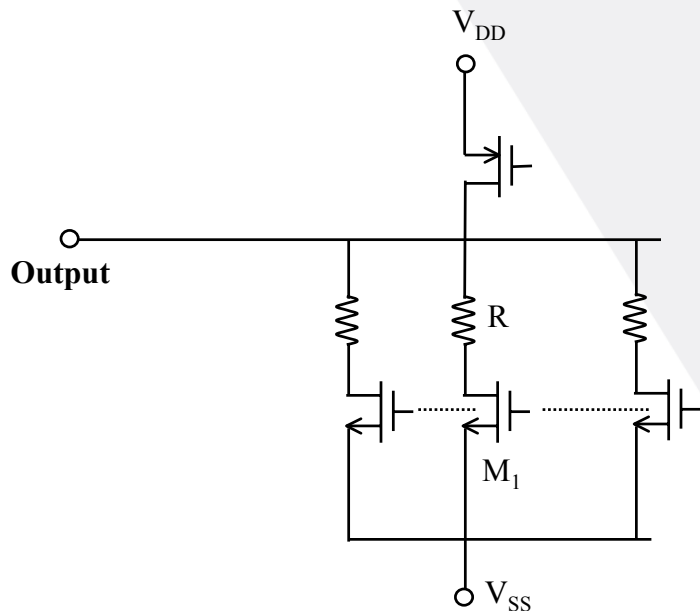
A complementary LVSCR circuit:
gcNMOS/gcPMOS triggering



Zener-D triggered
LV SCR circuit

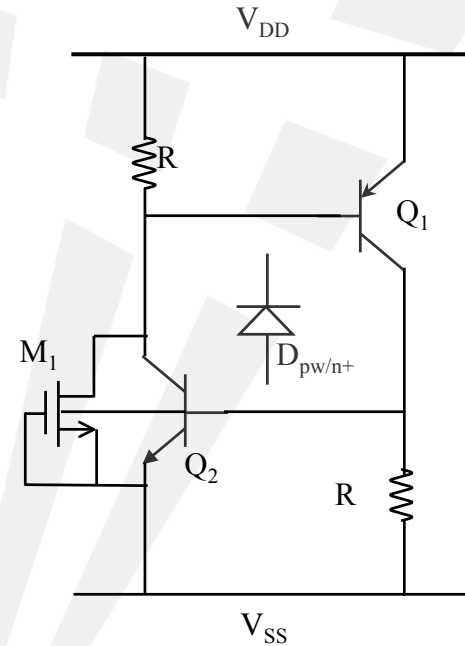
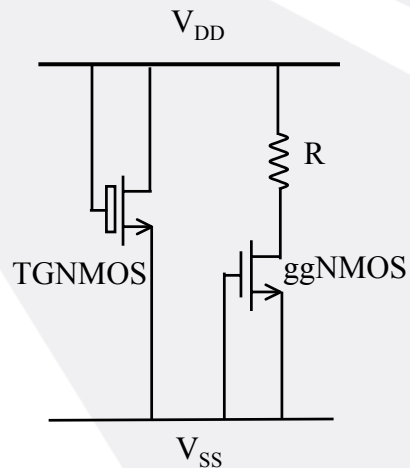
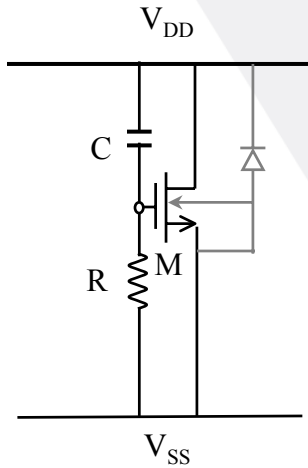
Output Buffer Self-Protection

- Output buffer transistors \Rightarrow ESD protection,
- buffers functionality \sim ESD trade-off,
- Don't use gcNMOS: it alters buffer!
- Use ballasting-R for uniformity,
- Ballasting-R = drain extension region



Ref: D. Scott, et al, "Circuit to Improve Electrostatic Discharge Protection", U.S. Patent, No. 5,019,888, 1991.

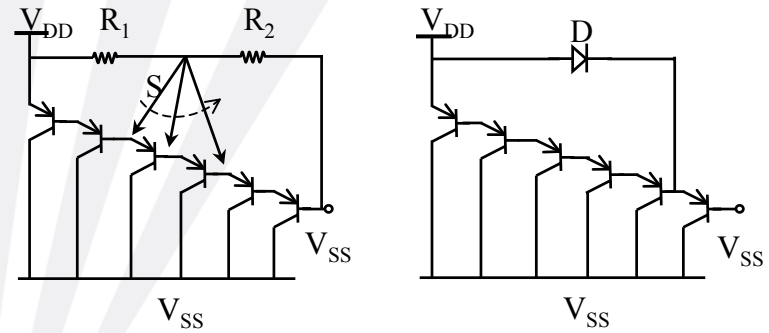
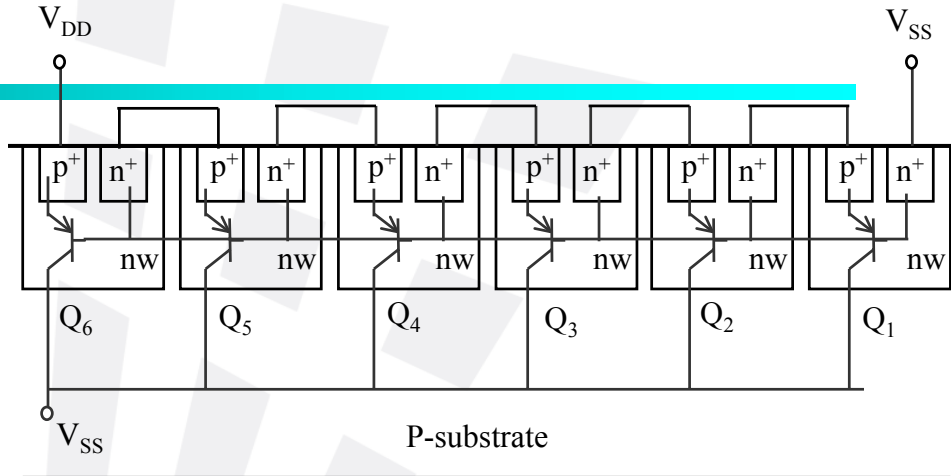
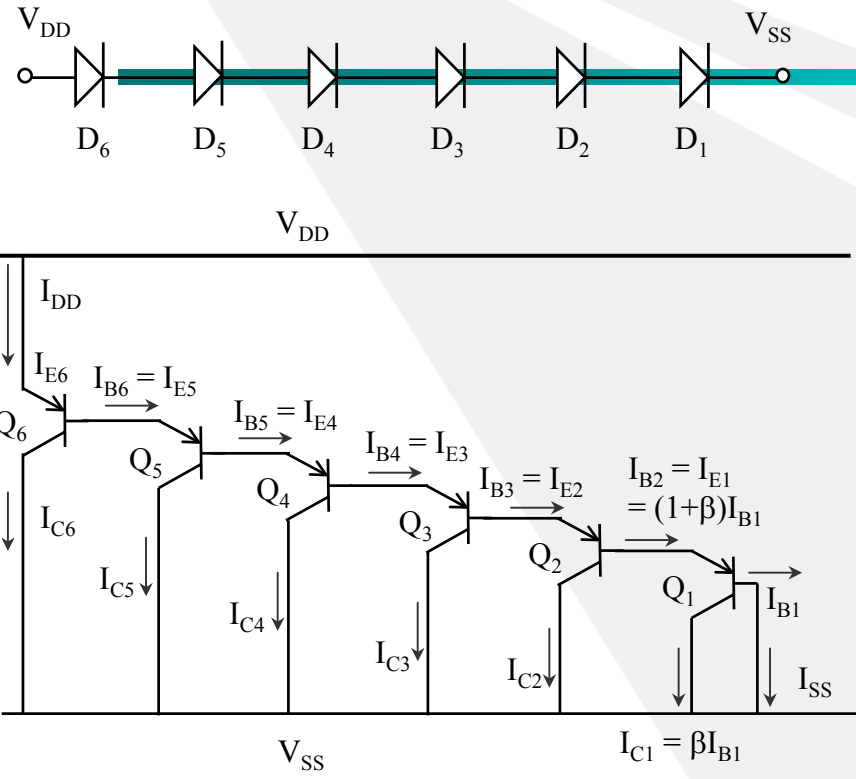
Power Clamps



NMOS clamps

NMOS-triggered
SCR clamp

Diode-string Power Clamp



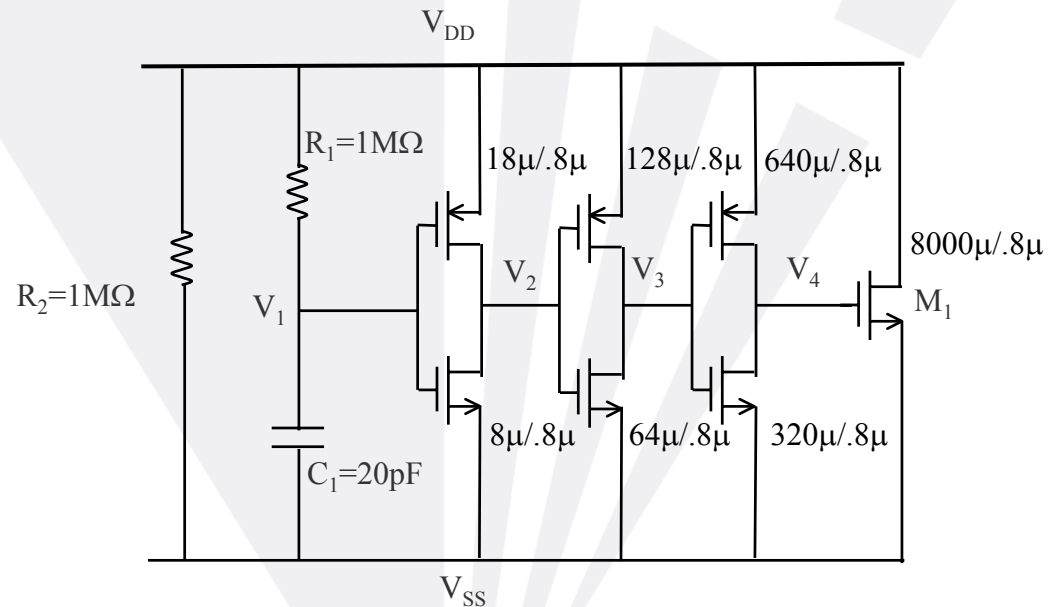
- Design trade-off:
- Darlington amplification: $\text{Hi-}\beta \rightarrow \text{lower } V_{t1}$,
- $\text{Hi-}\beta \rightarrow \text{low } R_{on}$,

$$V_{t1} = \sum_{i=1}^m V_{Di} = mV_D - \frac{m(m-1)}{2} nV_T \ln(1 + \beta)$$

$$R_{on} = R_{i6} \approx r_e + \frac{R_{i5} + R_W}{1 + \beta} = r_e \sum_{a=0}^5 \frac{1}{(1 + \beta)^a} + R_W \sum_{b=1}^6 \frac{1}{(1 + \beta)^b}$$

NMOS Switch as Power Clamp

- Advantage: all normal device operation → good for Spice simulation,
- Disadvantage: need large NMOS/PMOS size,



Ref: Merrill, R. and Issaq, E., "ESD Protection Methodology", 15th EOS/ESD Symp., 1993, pp.233.

Challenges in ESD Design

- Lack of well-developed ESD theory
- *Trial-&Error* ESD design approaches dominate:
 - * Experience + Si iterations
 - * Lack of ESD simulation & design methodology
 - * Average 3 iterations for experienced designers

Challenges

- **Common mistake - design portability.**
- **Costly, time-consuming, tedious.**
- **What does an IC designer want?**

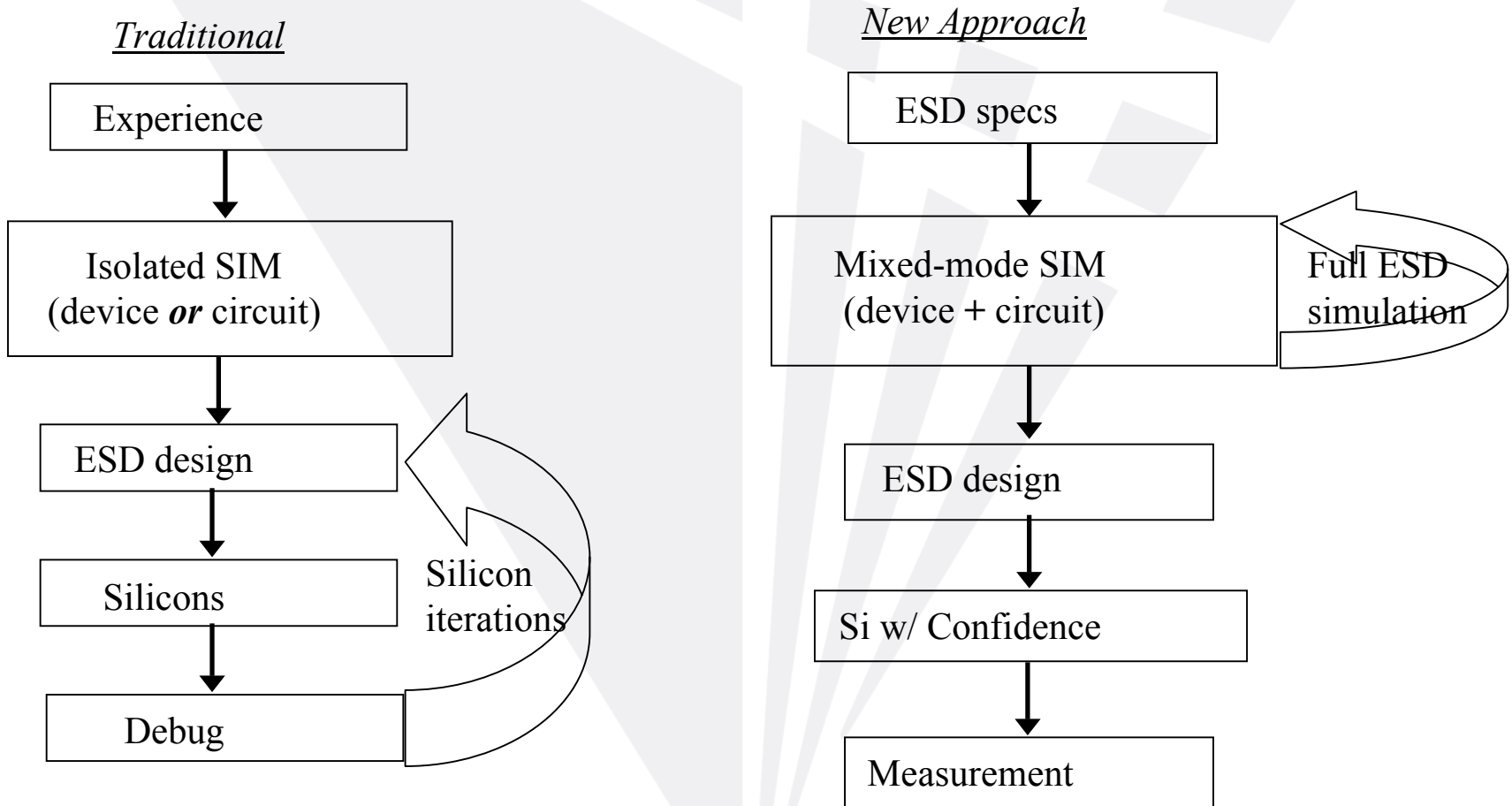
➤ **ESD forward design methodology → prediction by CAD**

➤ **Full-chip ESD design verification →
ESD-circuit interactions.**

New Mixed-mode ESD Simulation- Design Methodology

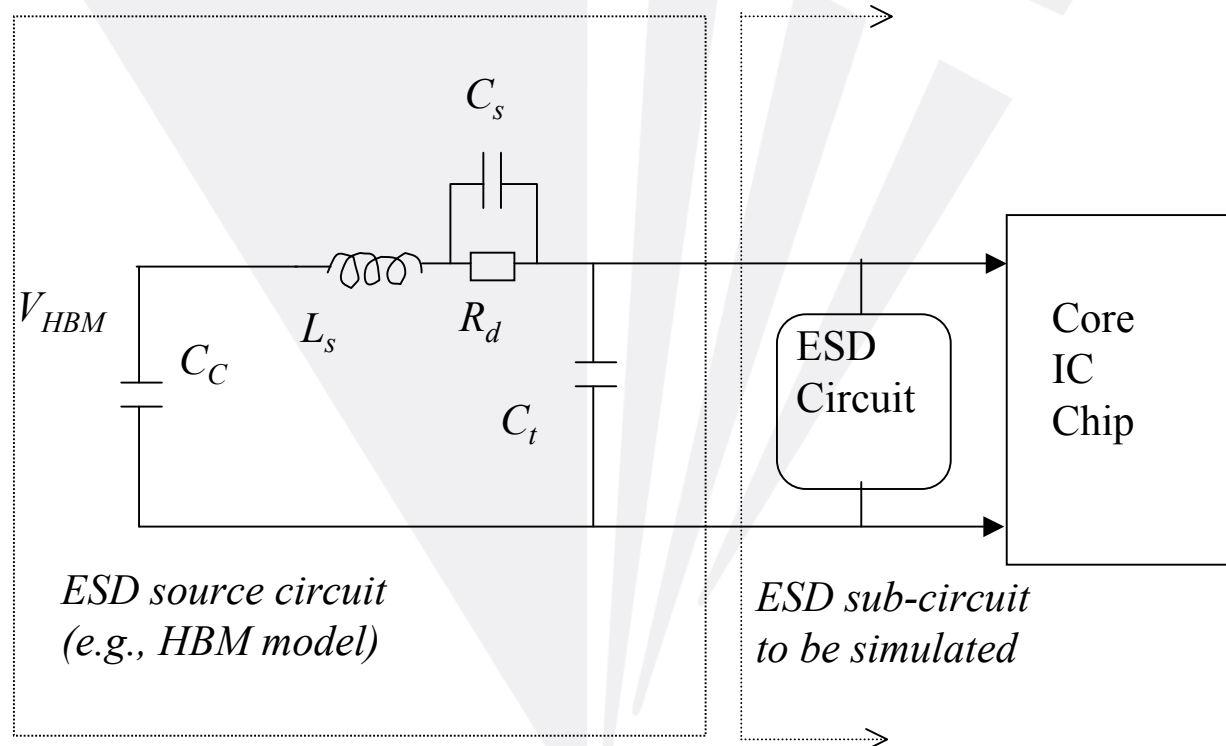
- **Mixed-mode ESD simulation:**
 - * Electro-thermal coupling
 - * Process-Device-circuit-layout coupling
- **ESD design prediction (forward design), not analysis (backward approach).**

ESD Design Method: New ~ Old

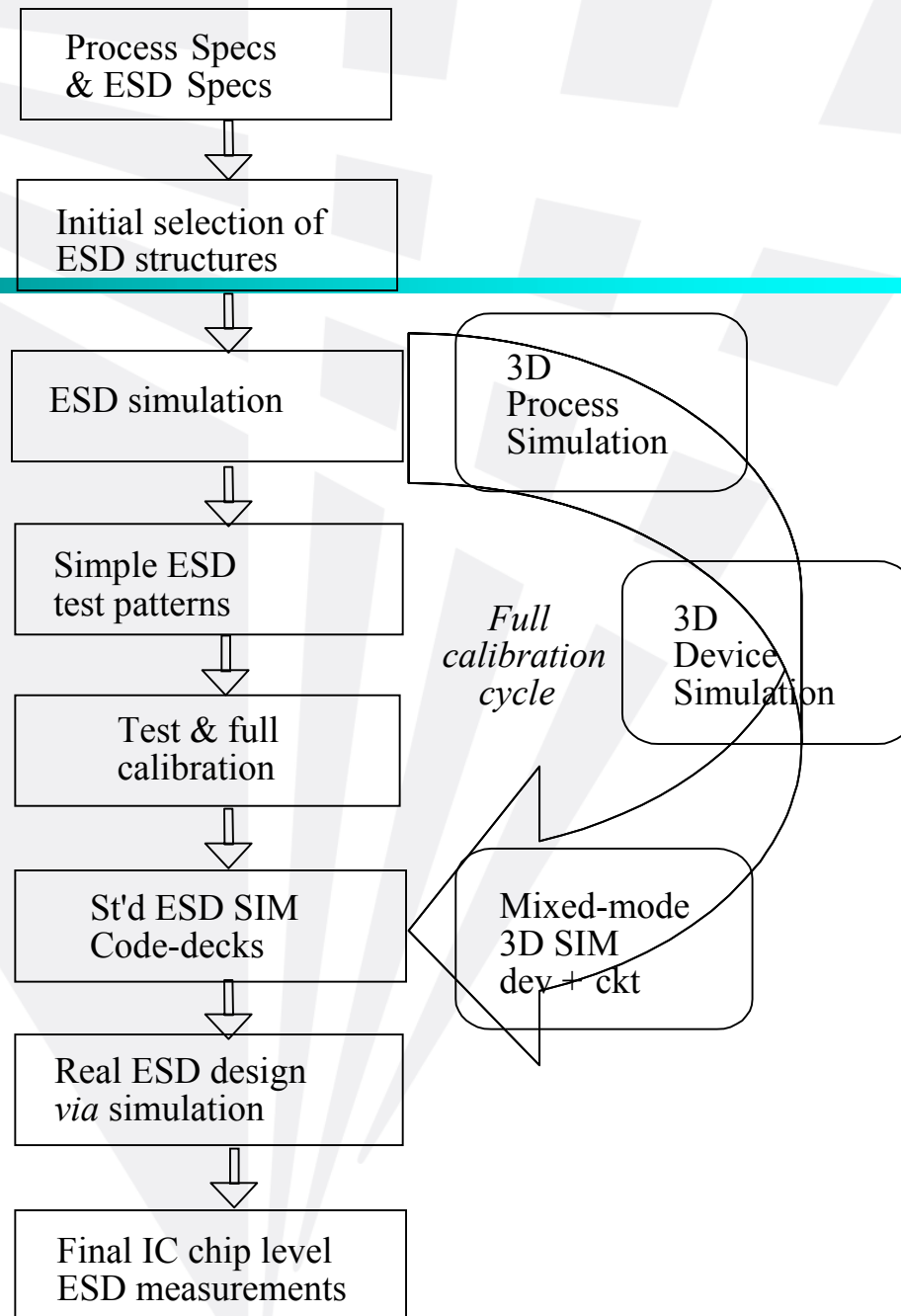


Mixed-Mode ESD Simulation Schematic

- Device-circuit coupling
- No assumption



• Design flow



ESD Simulation Capabilities

- **Steady State Analysis:** V_{t1} , I_{t1} , V_h , I_h , etc.
- **Actual Transient ESD Event Simulation:** V_{t1} , I_{t1} , V_{t2} , I_{t2} , t_1 , ESDV, etc.
- **Failure Analysis Capabilities**
 - * Currents & heat flow in protection circuitry - Si
 - * Currents & heat flow in metals
 - * Failure defects -- melting point, latent failures, etc.
- **Integration of ESD & process development.**

What's Critical in ESD Simulation?

Calibration

Calibration!!

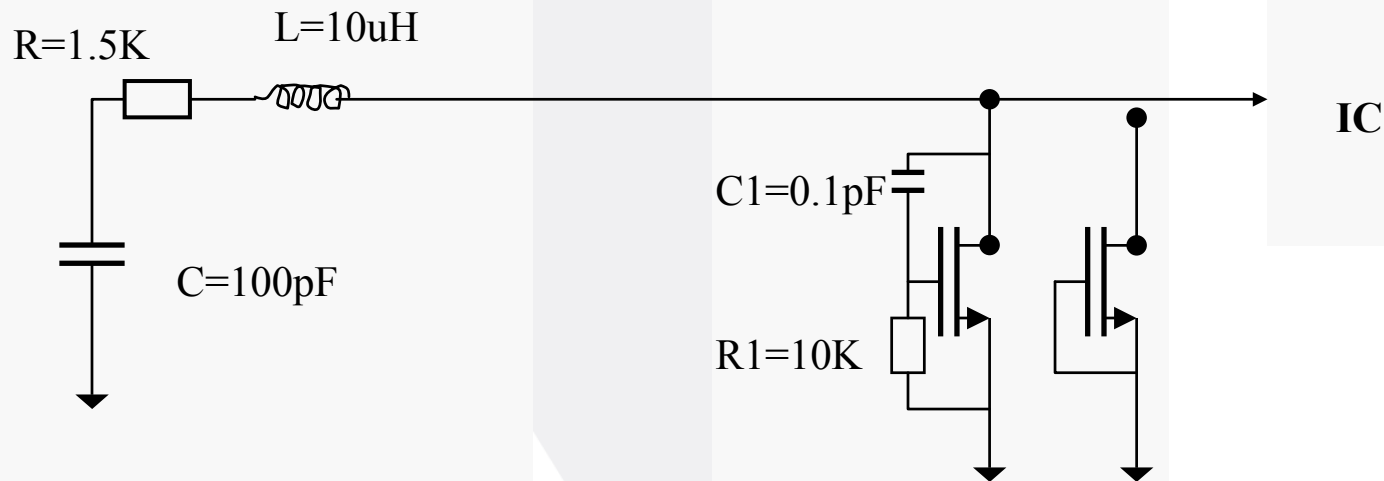
CALIBRATION!!!

- **To avoid garbage-in garbage-out**

Example 1: NMOS ESD Protection in 0.8μ CMOS

- **gGNMOS, gCNMOS**

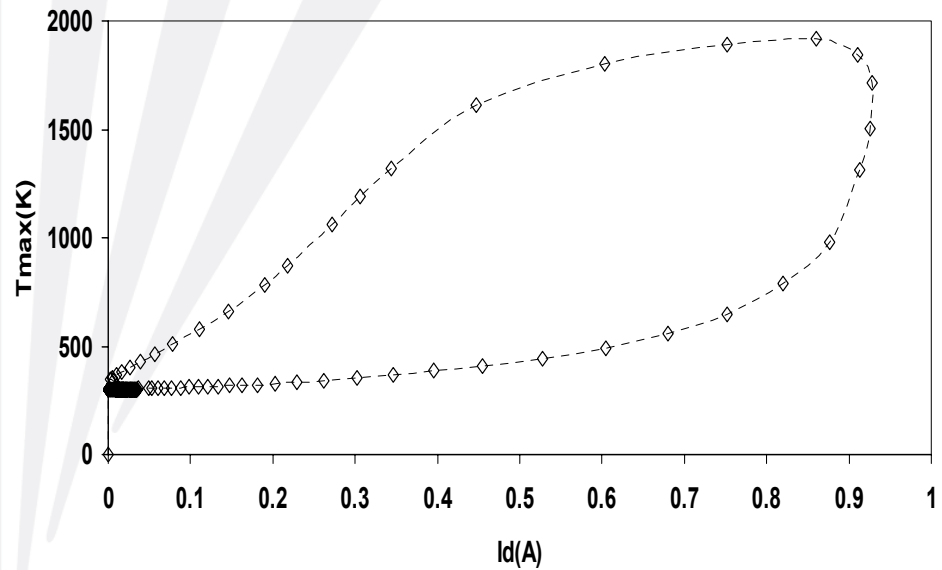
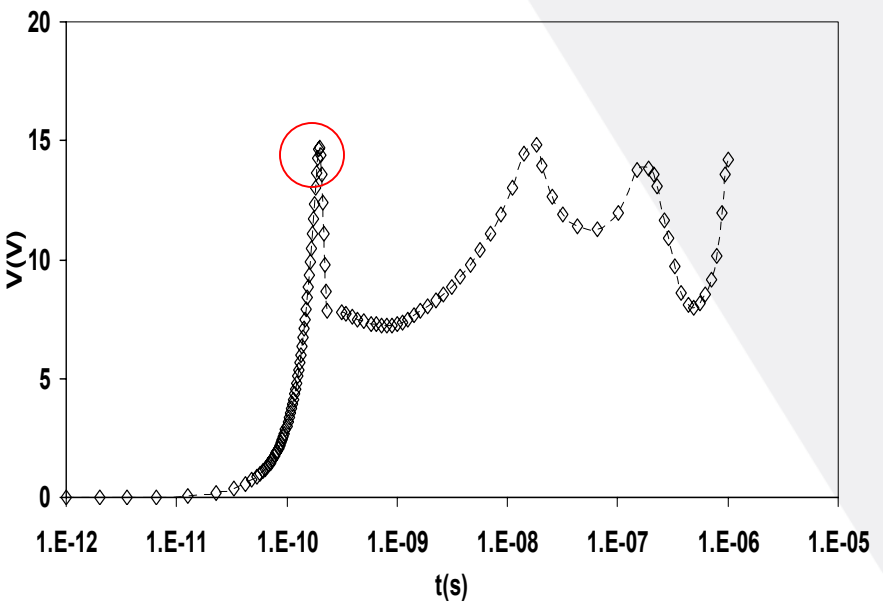
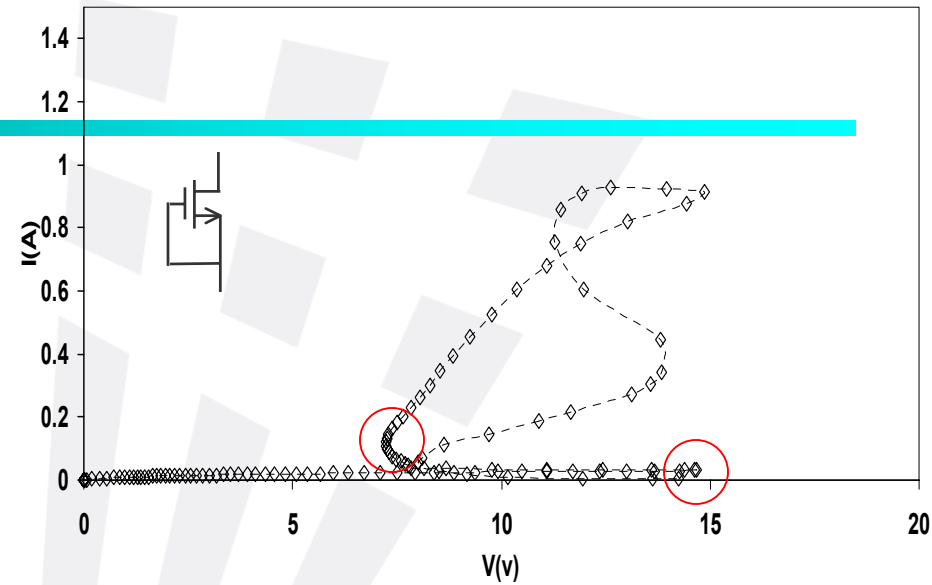
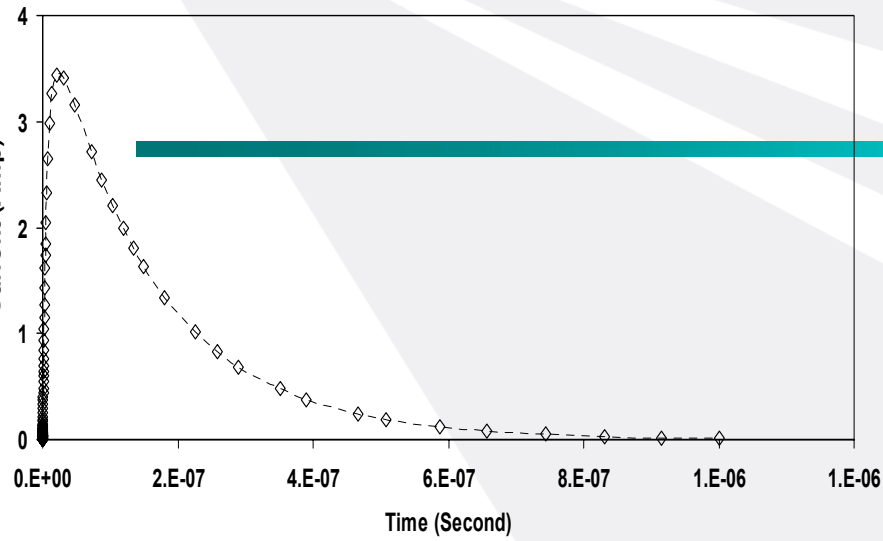
HBM Model



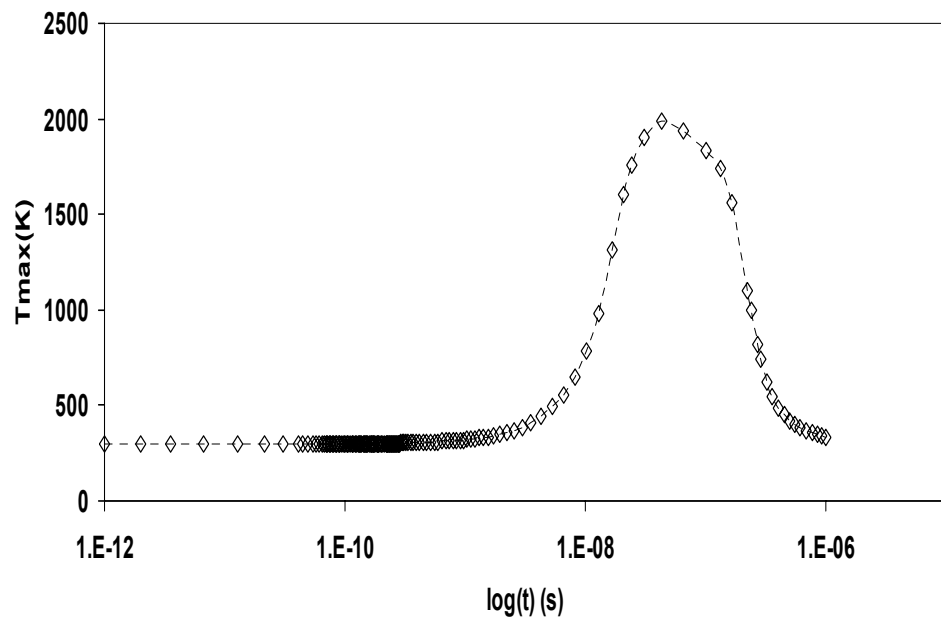
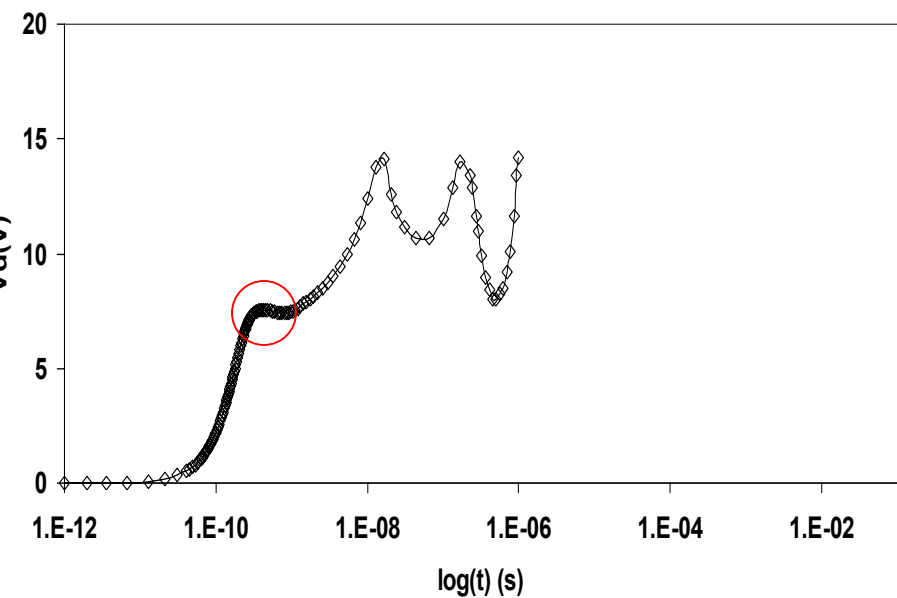
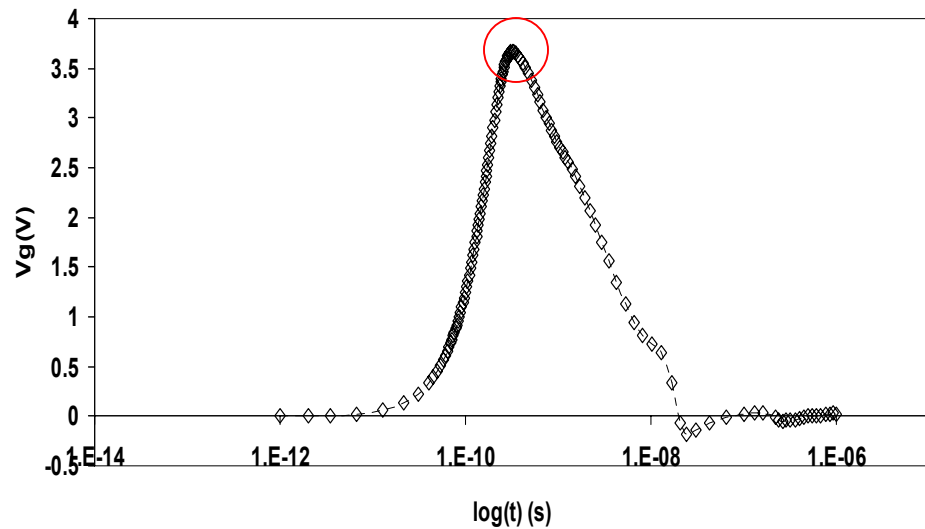
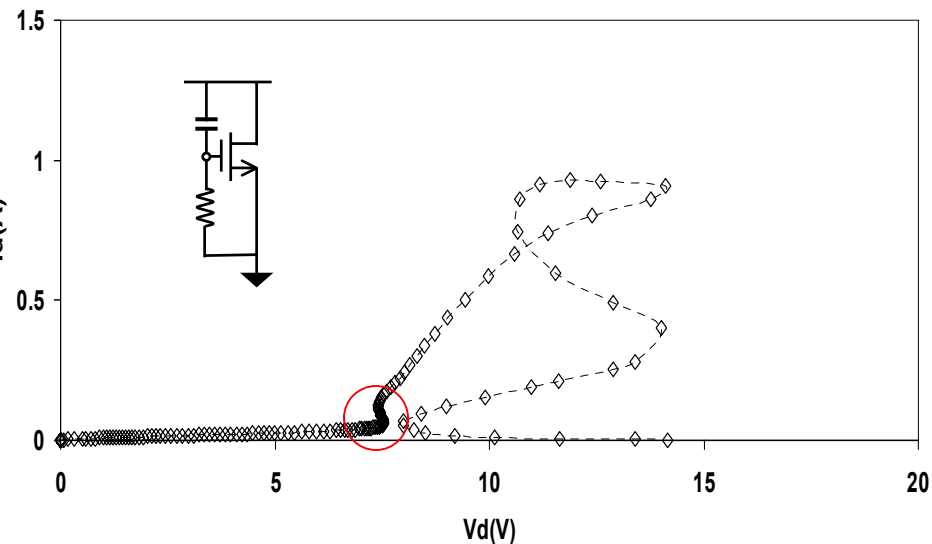
[1] A. Wang, et al, "A study of NMOS behavior under ESD stress: simulation and characterization", *Microelectronics Reliability*, v38, Pergamon, 1998, pp1183-1186.

[2] H. Feng, "A Mixed-Mode Simulation-Design Methodology For On-Chip ESD Protection Design", *MS Thesis*, IIT, 2001.

GGNMOS (SCGS=2um, DCGS=4um, W=100um)



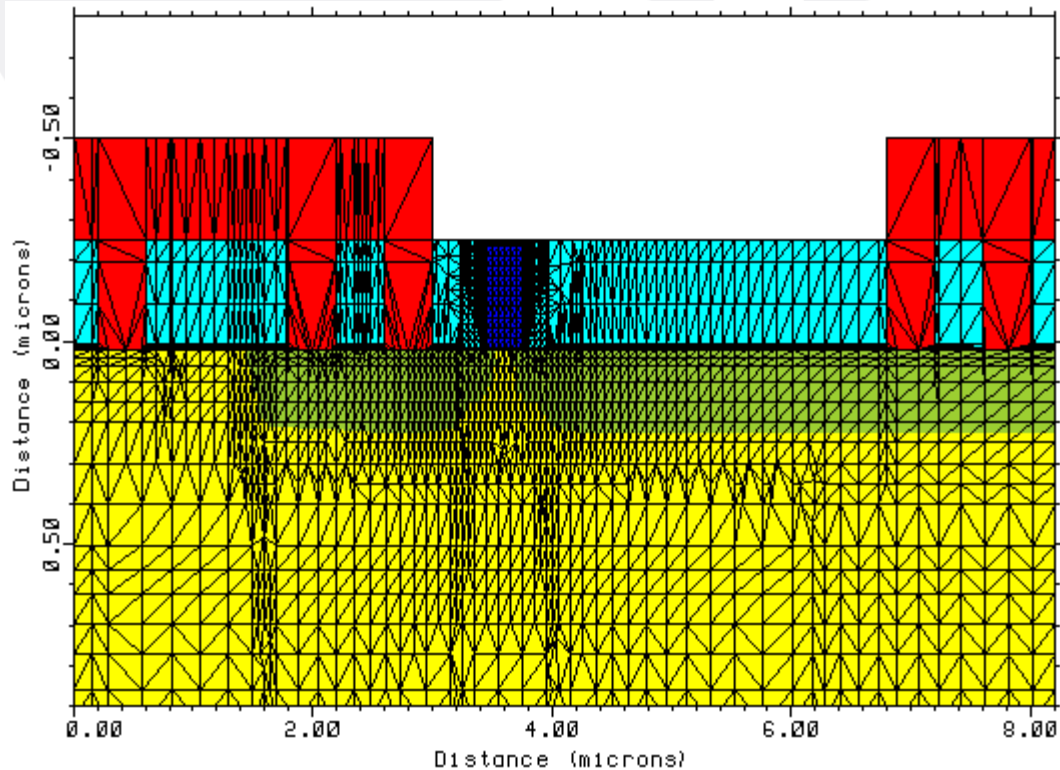
GCNMOS (SCGS=2 μ m, DCGS=4 μ m, W=100 μ m)



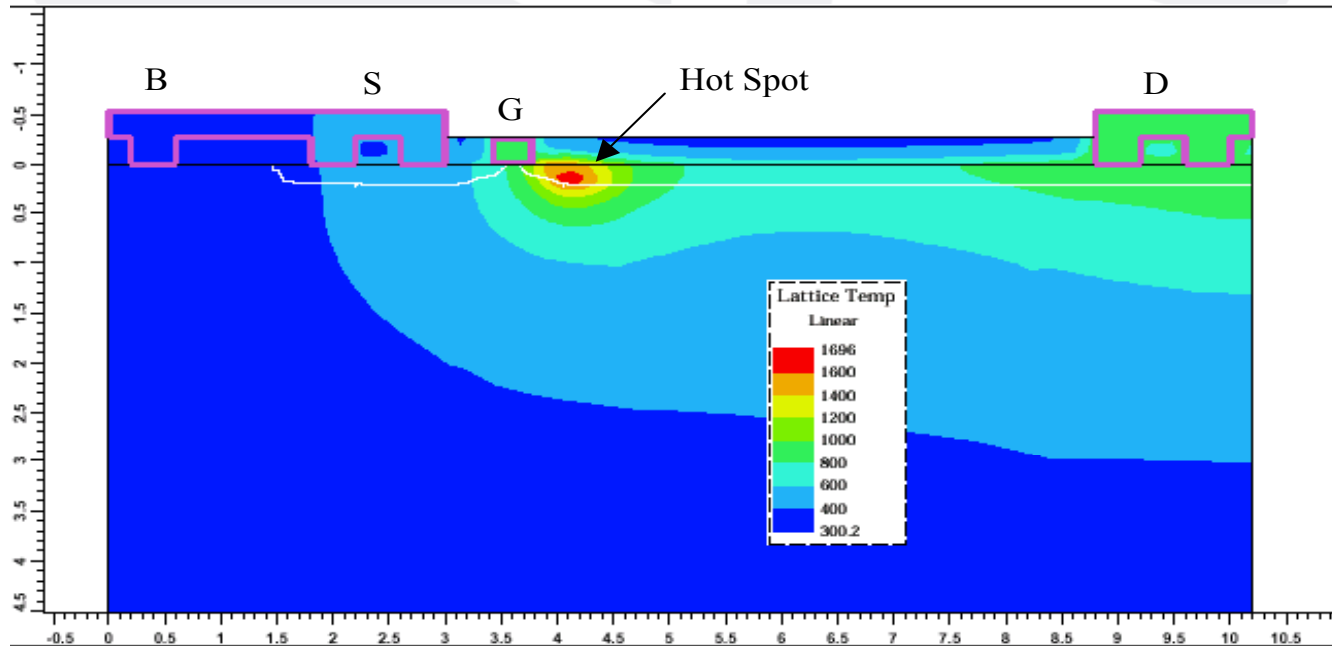
Example 1: Data

| | GGNMOS | | GCNMOS | |
|-------------|--------|-------|--------|------|
| | SIM. | TEST | SIM. | TEST |
| $V_{t1}(V)$ | 14.68 | 12.56 | 7.54 | 6.66 |
| $t_1(ns)$ | 0.2 | - | 0.42 | - |
| $V_h(V)$ | 6.92 | 6.48 | 7.41 | 6.08 |
| $V_G(V)$ | - | - | 3.67 | - |
| $t_G (ns)$ | - | - | 0.32 | - |

Example 2: ggNMOS ESD in 0.35u CMOS

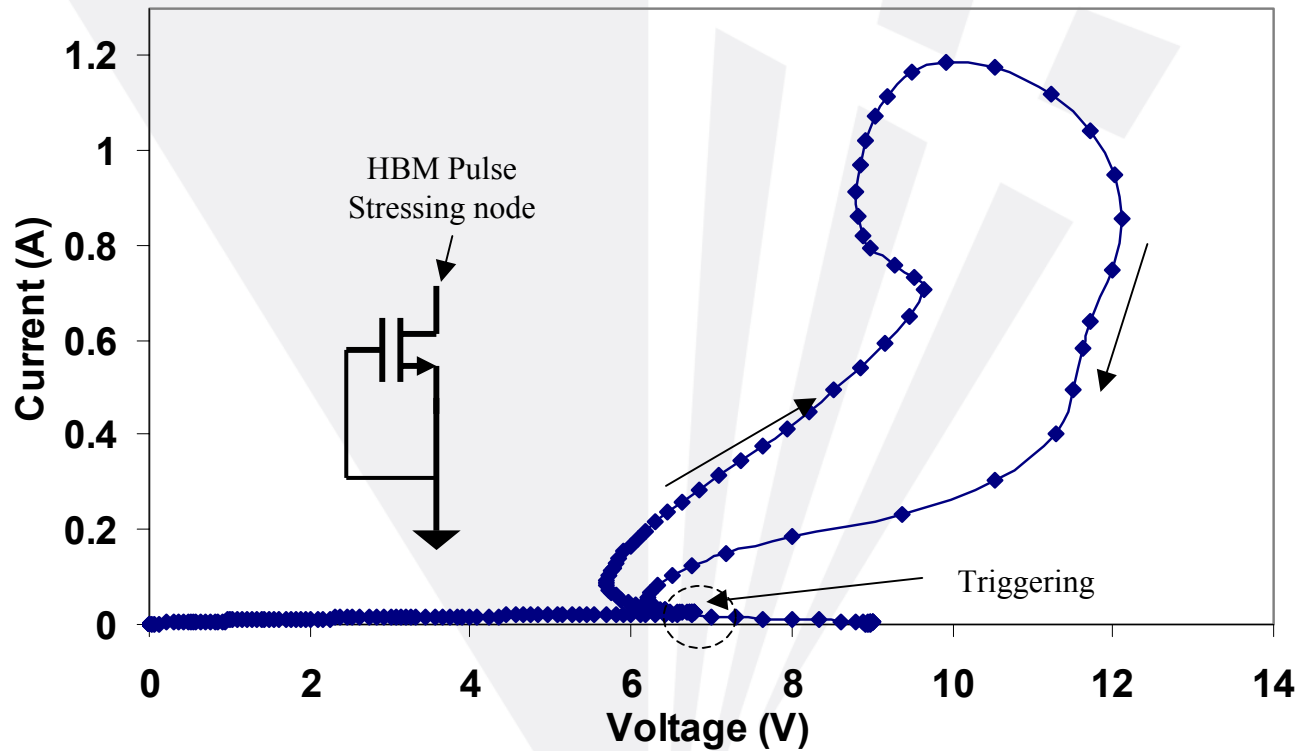


ggNMOS ESD Structure under Stress



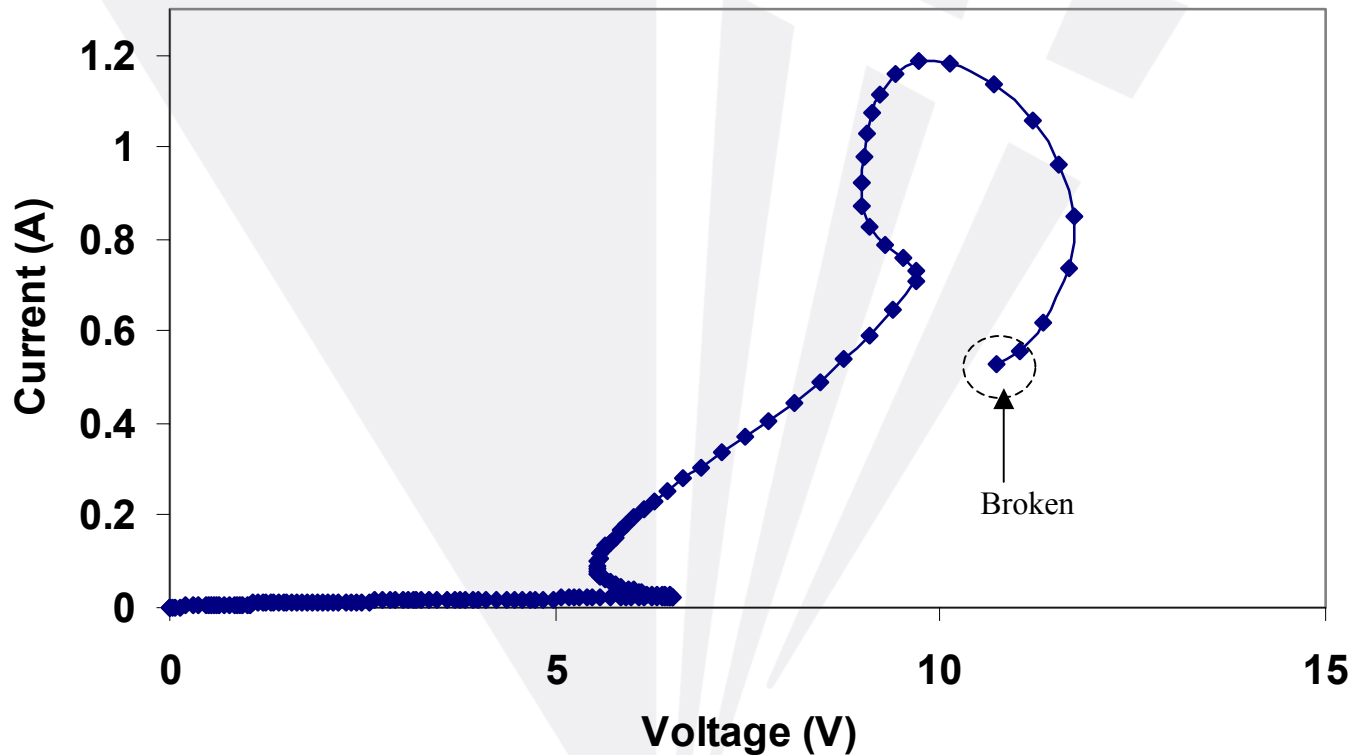
ggNMOS ESD Simulation: Passed

HBM 2kv ggNMOS (80um/0.4um) -- Passed



ggNMOS ESD Simulation: Failed

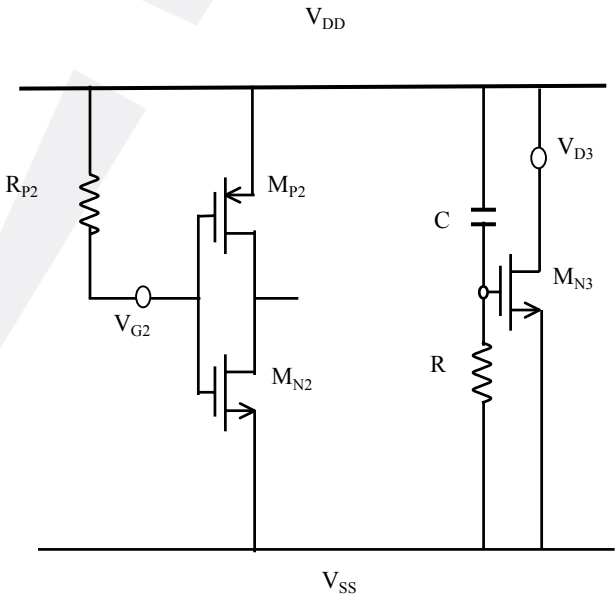
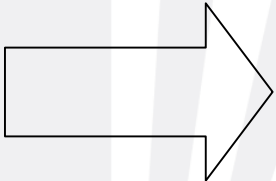
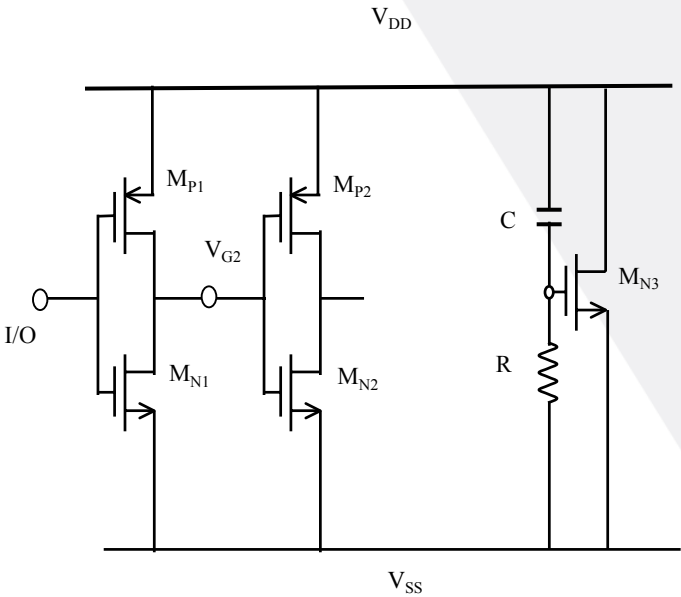
HBM 2kv ggNMOS (w < 80um) -- Failed



Example 3: Circuit+gcNMOS Clamp in 0.35μ CMOS

A circuit block of 2 inverters in parallel with a gcNMOS power clamp

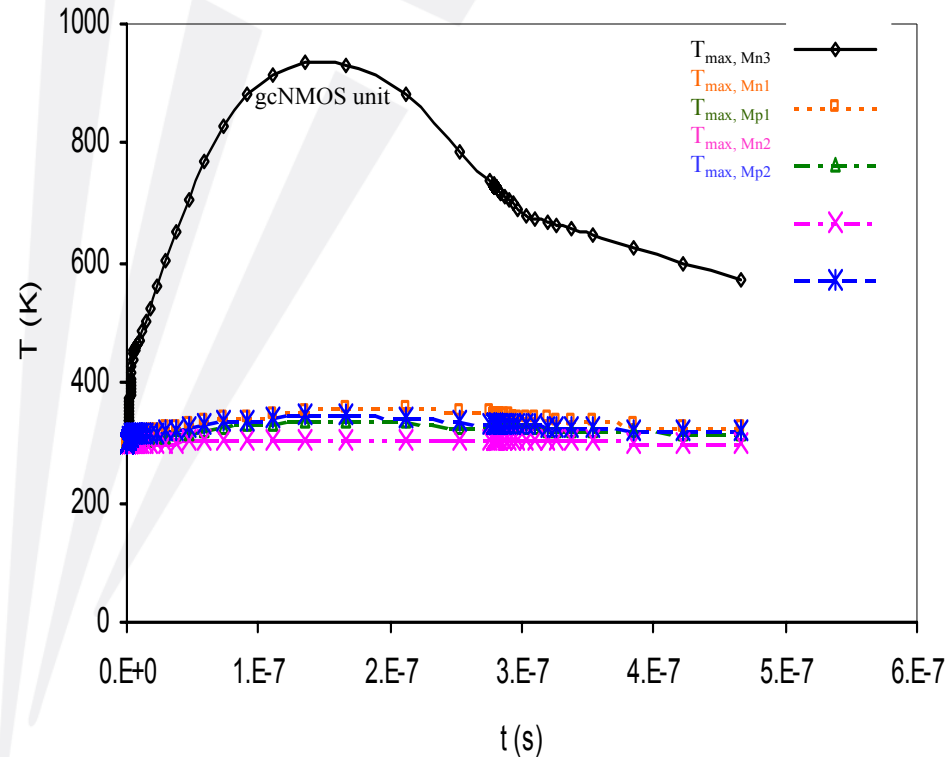
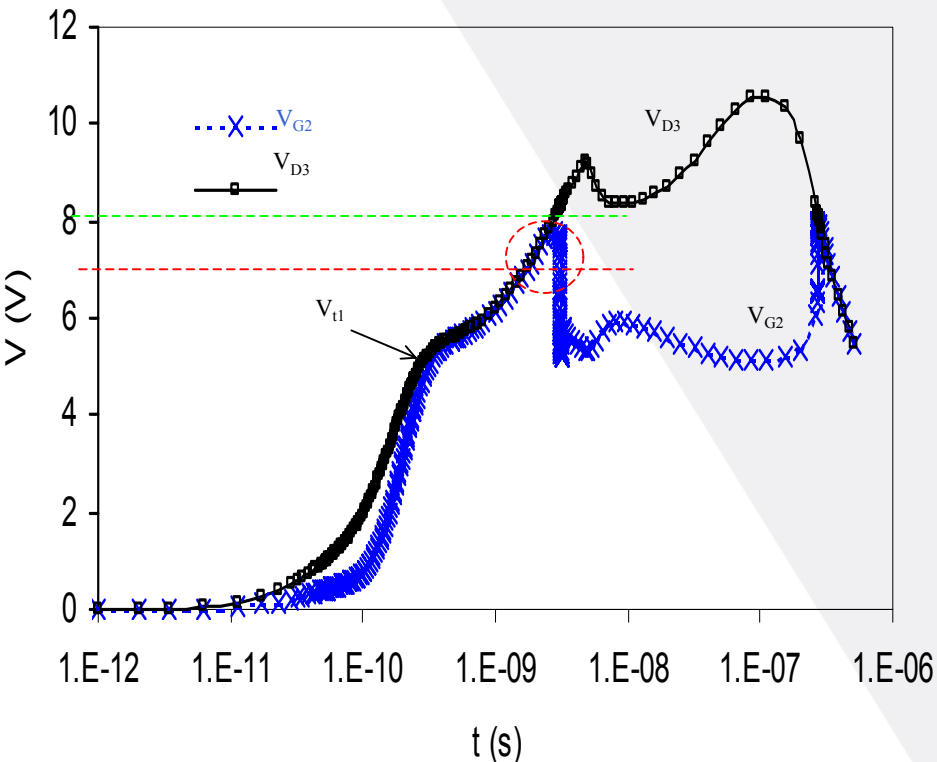
Equivalent circuit at input = L:
ESD defect M_{n2} gate?
($BV_G = 8V$)



Ref: H. Feng, "A Mixed-Mode Simulation-Design Methodology For On-Chip ESD Protection Design", *MS Thesis*, IIT, 2001.

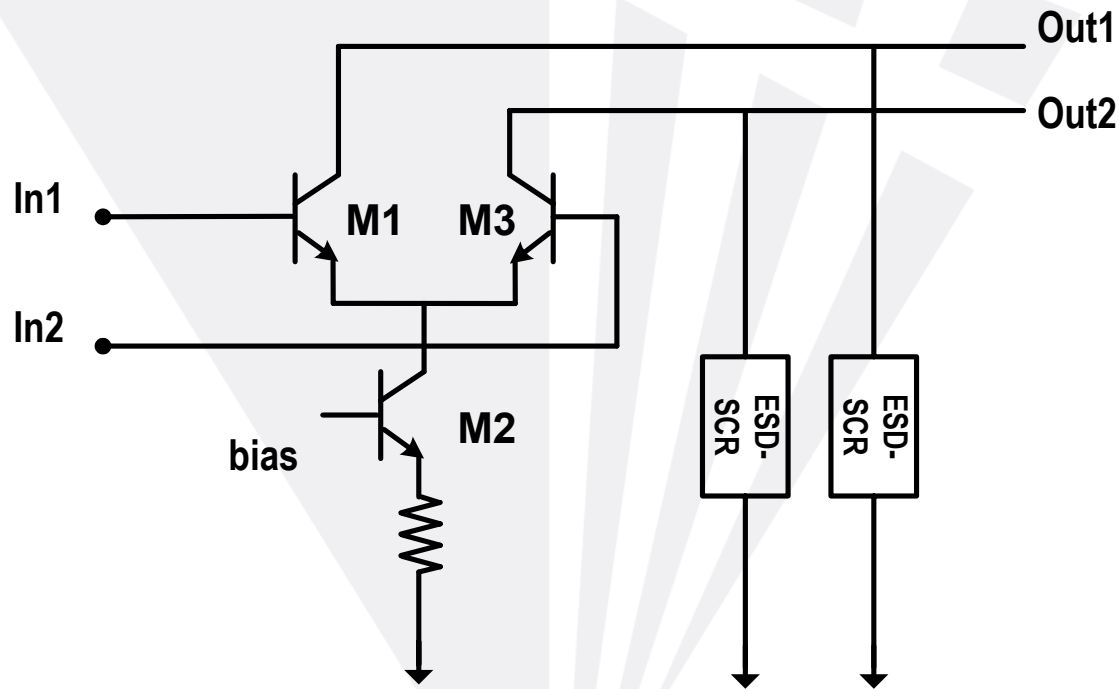
Example 3 Simulation

- $V_{t1} < 6V$,
- Potential risk of $V_G \sim BV_G$ very briefly,
- Hot M_{n3} : gcNMOS works.



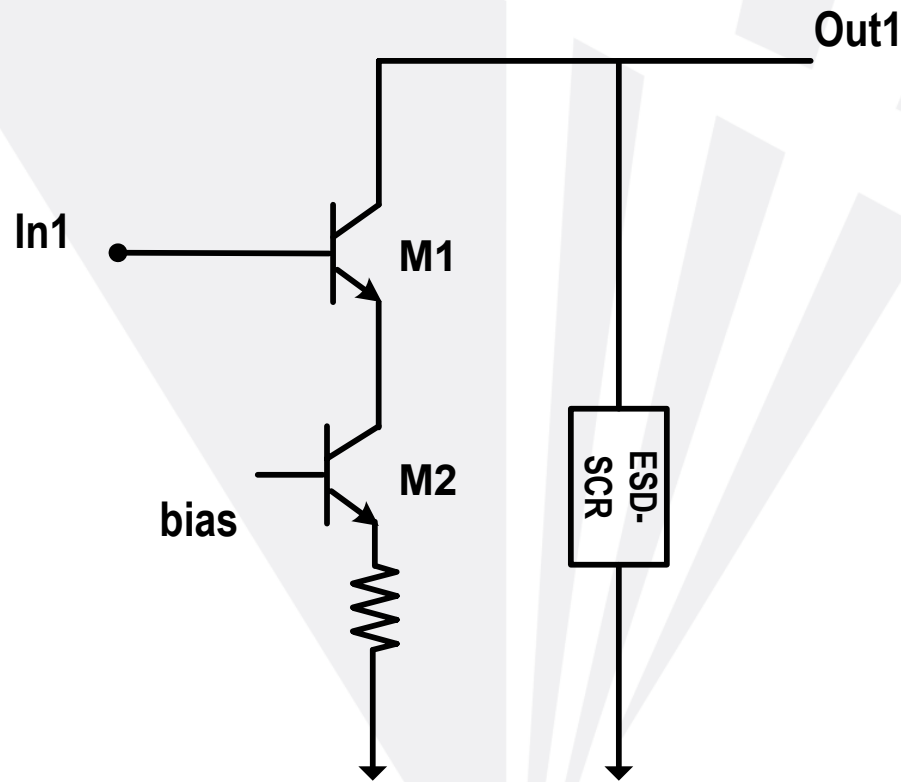
Example 5: Output ESD Protection

- Differential output buffer with open collectors
- SCR ESD protection

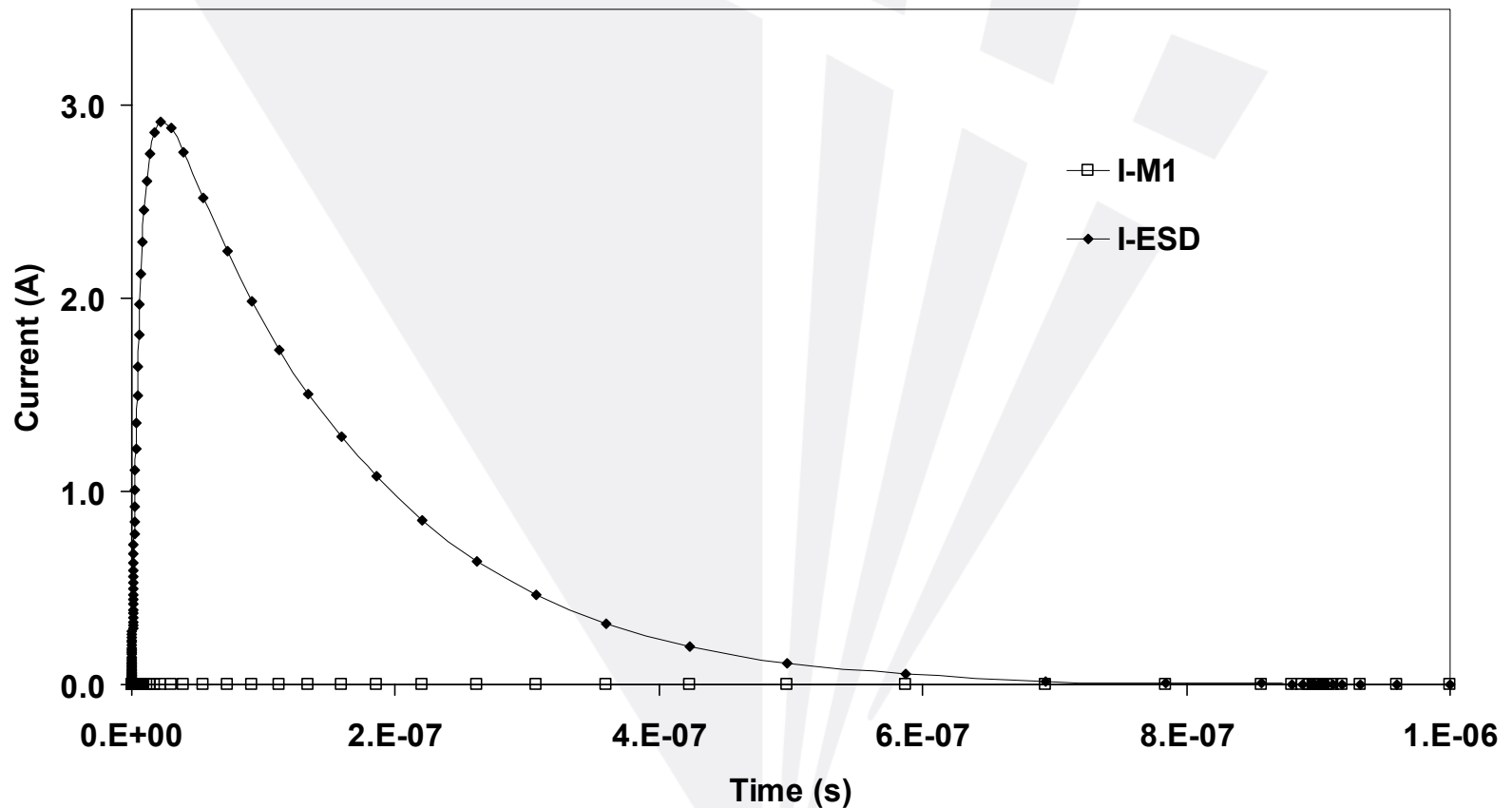


Ref: H. Feng, et al, In press, IEEE JSSC, 2003.

Example 5 ESD Simulation Topology

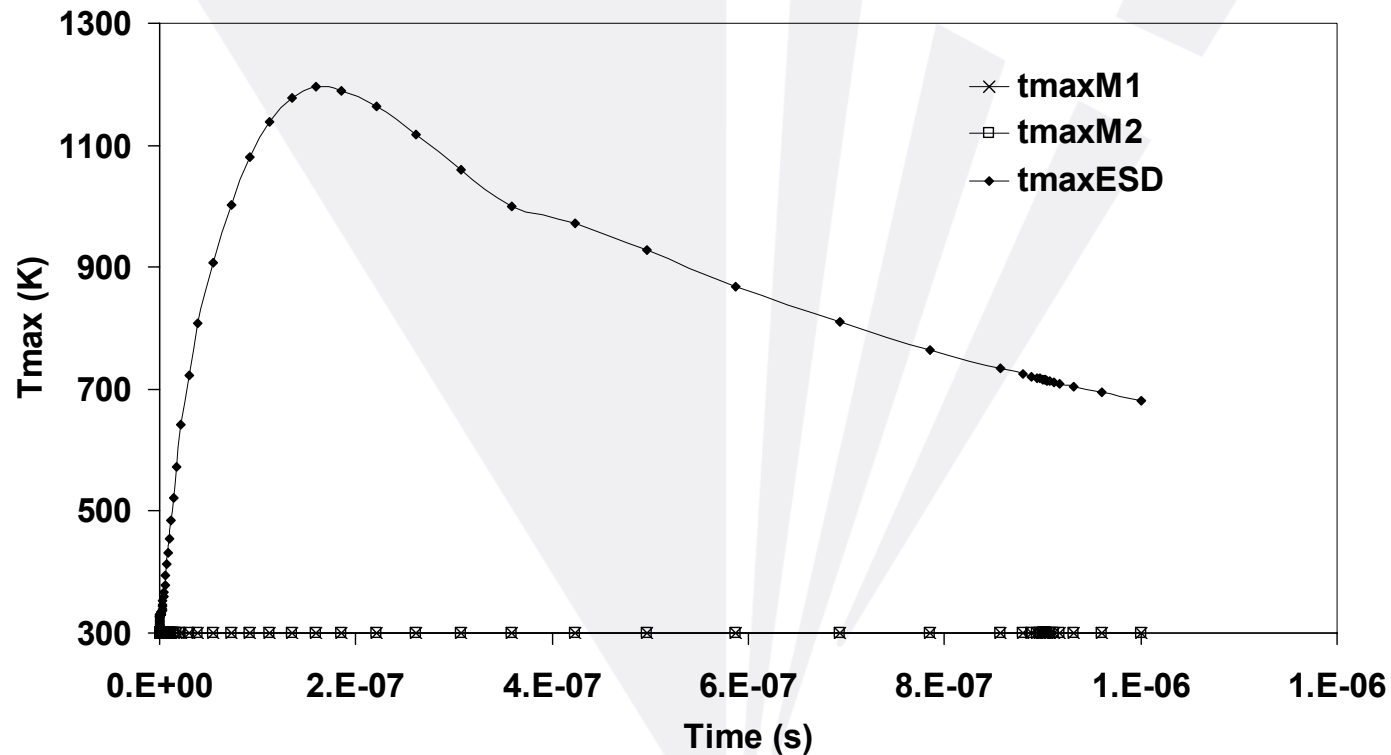


~100% ESD Current Discharges into SCR ESD



T_{max} in Each Devices under ESD

- ESD heat generation in SCR ESD device only



NEW ESD DESIGN CHALLENGES

Emerging ESD protection design concerns:

- RF ESD protection: What's unique?
- ESD protection for mixed-signal ICs
- Whole-chip ESD protection design
- Full-chip ESD protection design verification by CAD

RF ESD?

Some theories to define the RF ESD phenomena & problems

Need to define RF ESD characterizing parameters

To design RF ESD protection circuits by ESD simulation

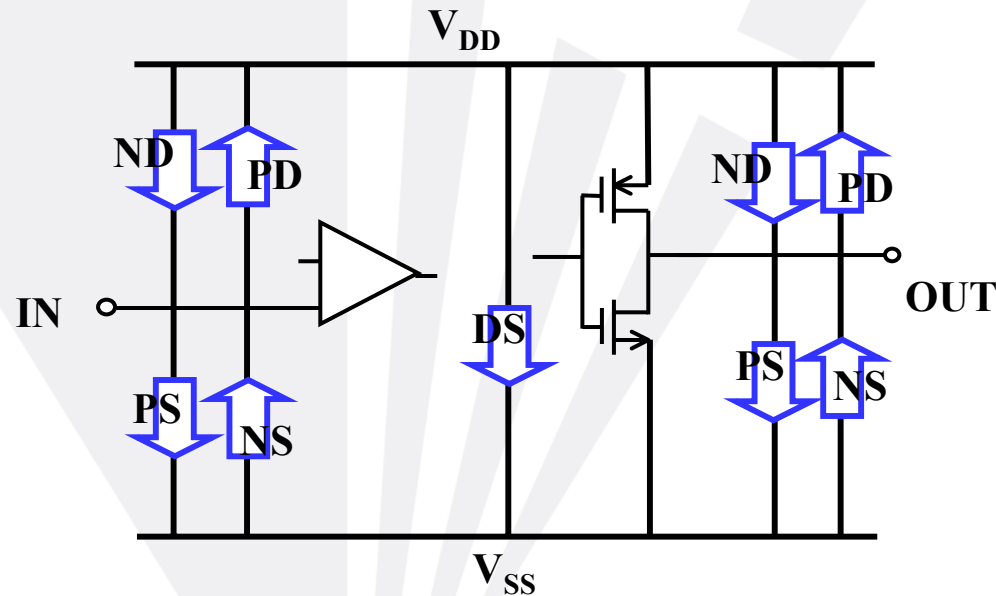
To perform RF ESD design verification

Need to characterize your designs by testing

To balance Specs for RF ESD protection and the circuits.

Full ESD protection scheme

- Multiple units for ND, PD, NS, PS, DS & SD ESD protection
- Large sizes



➤ **Problem: too much parasitics \Rightarrow intolerant to RF ICs.**

ESD-Circuit Interactions

• Circuit-to-ESD Influences

- ESD protection may be affected by the core circuits protected,
- Weak discharge links in core IC - Early ESD Failure.
- **Unique Challenge 1: ESD Mis-Triggering by fast RF/M-S signals (dV/dt , dI/dt)**

• ESD-to-Circuit Influences

- ❖ ESD-induced parasitic C_{ESD} (200fF - pF) & R_{ESD} ,
- $C_{ESD} R_{ESD}$ delay \Rightarrow signal integrity, clock corruption, ...
- $C_{ESD} \Rightarrow$ loading effect, Z-matching, power efficiency, BW, ...
- ΔC_{ESD} , $\Delta R_{ESD} \sim$ frequency, biasing, T, ...
- **Unique Challenge 2: including C_{ESD} in RF IC design,**
- ❖ ESD-Induced Parasitics: Noises
- Substrate noise-coupling effects due to C_{ESD}
- Self-generated noises by ESD units
- **Unique Challenge 3: ESD noise effects into RF ICs?**

Local-Optimization for Mixed-Signal ESD

- One global ESD triggering, V_{t1} , does NOT fit whole chip,
 - Multi- $V_{DD}/V_{SS} \Rightarrow$ locally-optimized V_{t1} for different I/Os,
 - Need a safety margin for V_{t1} :
 - V_{t1} of 5V fits $V_{DD}=3.3V$ blocks,
 - V_{t1} of 23V good for $V_{DD}=15V$ blocks.
- **Challenge:** multi- V_{t1} ESD design in RF/M-S ICs
- \Rightarrow whole-chip ESD design optimization,
 - \Rightarrow not quite unique for RF ESD

ESD-to-Circuit Influences

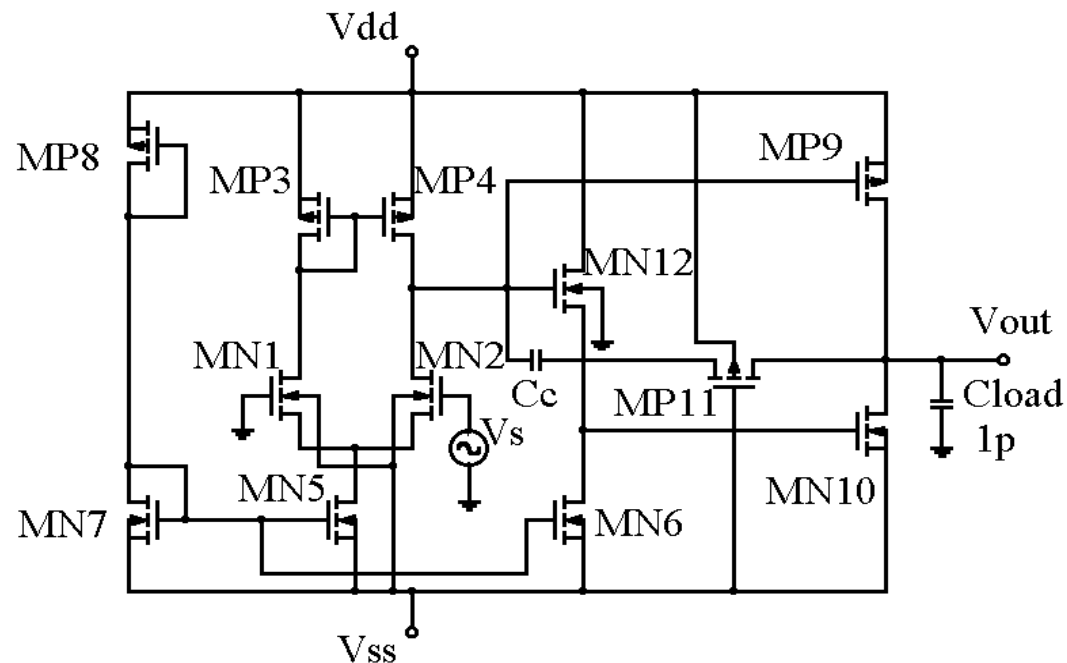
Let data speak:

- o Three different types of ESD protection structures: ESD1, ESD2 & ESD3,
- o Three RF blocks: a 4GHz ring oscillator, a bluetooth LNA & a hi-speed Op Amp.
- o Fabricated in 6M 0.18 μ m CMOS with Al/Cu interconnects

| ESD types | | ESD1 | | ESD2 | | ESD3 | |
|-------------------|----------|------|------|-------|-------|-------|-------|
| C_{ESD} (pF) | C_{Si} | 0.54 | | 0.09 | | 0.07 | |
| | C_M | Cu | Al | Cu | Al | Cu | Al |
| | | 0.30 | 0.43 | 0.029 | 0.041 | 0.019 | 0.028 |

Hi-speed Op Amp: General SPEC's

An Op Amp in $0.18\mu\text{m}$ CMOS,
Design SPECs:
Power: 0.43mW ,
Slew rate: 116mV/ns ,
Settling time: 3.7ns at 1%,
Output swing: 0.96 at 80% gain,
BW: 121MHz

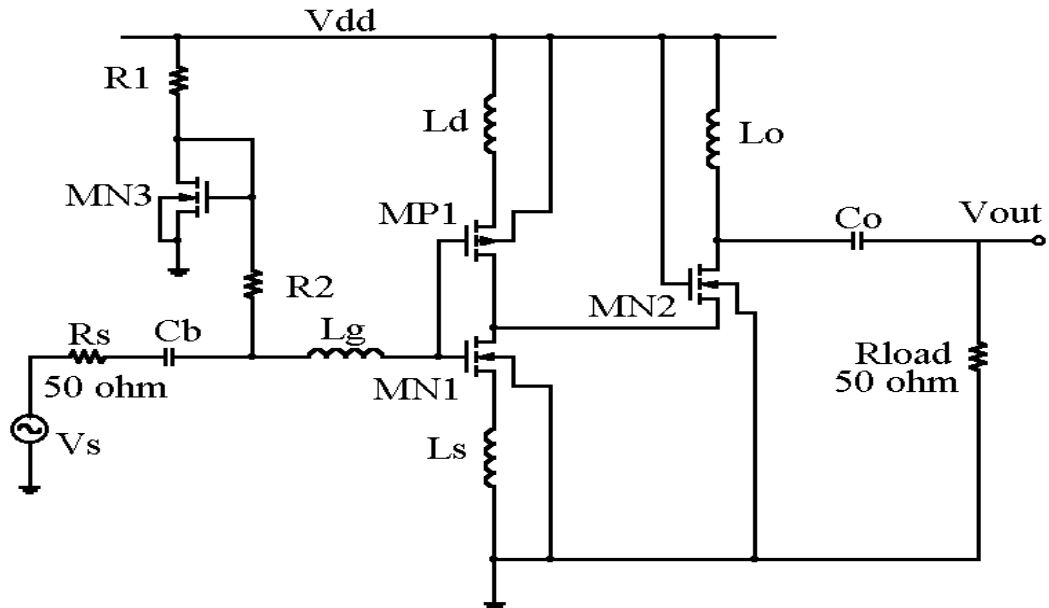


Strong $C_{ESD} \sim$ SEPCs Correlation!

| Specs | No C_{ESD} | ESD1 | ESD2 | ESD3 |
|--------------------|--------------|----------------------------|-------|--------|
| f_T (MHz) | 120.7 | -38.7% | -8.9% | -7% |
| | | Recovery | | |
| | | → + 81.9% (+83.5% in Cu) → | | |
| Phase Margin | 70.1° | -14.4% | -2.0% | -1.6% |
| | | Recovery | | |
| | | → + 88.9% (+90.3% in Cu) → | | |
| Slew rate (mV/ns) | 115.9 | -30.1% | -5.2% | -4.1% |
| | | Recovery | | |
| | | → + 86.4% (+88.7% in Cu) → | | |
| t_{set} (ns, 1%) | 3.77 | -353% | -102% | -89.7% |
| | | Recovery | | |
| | | → +74.6% (+76.9% in Cu) → | | |

ESD Noise Effects by LNA

- A Bluetooth LNA in $0.18\mu\text{m}$ CMOS,
- Design SPECS:
on-chip 50Ω matching at I/O,
center freq: 2.4GHz ,
 $\text{NF}=1.76\text{dB}$,
 $P=24\text{mW}$ in 3.3V ,
 $S_{21}=23.4\text{dB}$,
 $S_{11}=-34.5\text{dB}$,
 $S_{22}=-47.7\text{dB}$,
 $S_{12}=-39.6\text{dB}$



How ESD Structures Affect NF?

| ESD Protection Type | NF (dB) | Degradation |
|---------------------|---------|-------------|
| No ESD | 1.7582 | - |
| ESD1 | 1.8247 | 3.78% |
| ESD2 | 1.7596 | 0.08% |
| ESD3 | 1.7586 | 0.02% |

- **Strong influences of ESD protection structures on noise performance**

RF ESD Protection Solutions

- RF ESD protection still in the problem-shaping phase!
- No all-fit & well-argued RF ESD solution yet.
- Any ESD protection \Rightarrow RF ESD
given ESD-Circuit interactions $\downarrow\downarrow\downarrow$

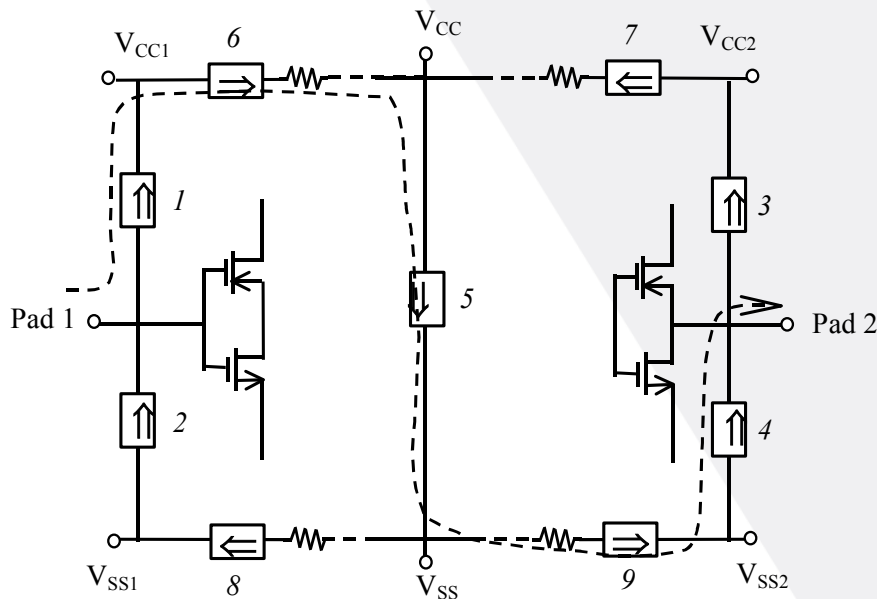
➤ Goal for RF ESD \Rightarrow ANY NOVEL structures:

- o Ultra-fast ESD switching,
- o Novel triggering mechanisms,
- o Hi-ESDV/Si ratio,
- o Small size,
- o Low-parasitics,
- o Multiple-mode ESD protection,

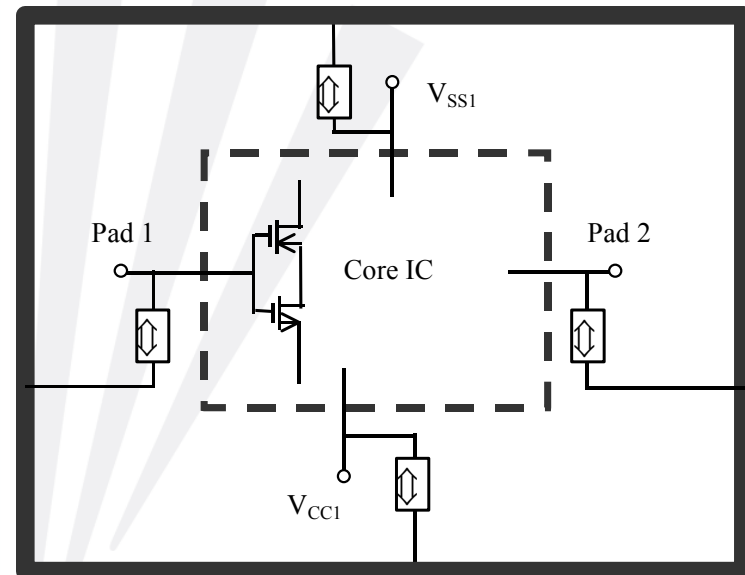
Whole-Chip ESD Protection

- Ensure a discharging path between ANY two pads.
- Consider possible internal weak-leak as shunting-channels
- Estimate the worst-case discharge-path impedance

A pad + Clamp Scheme;



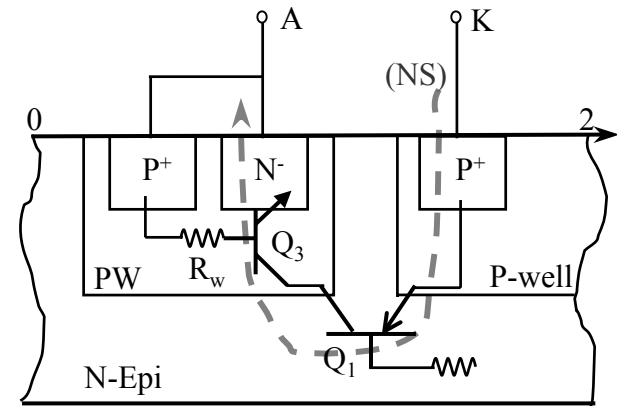
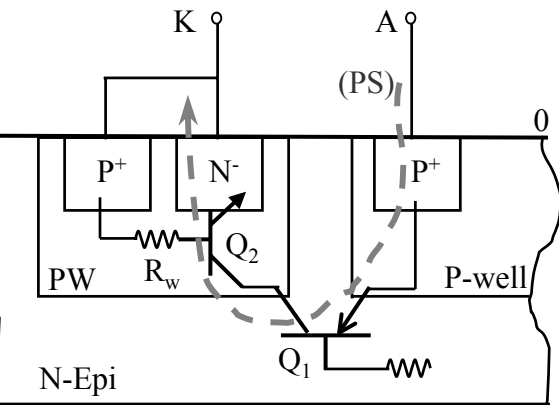
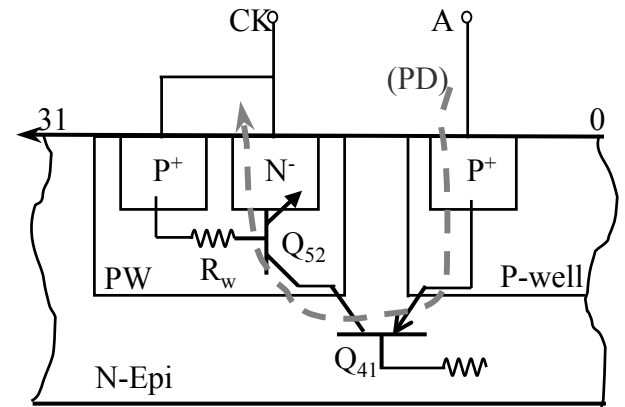
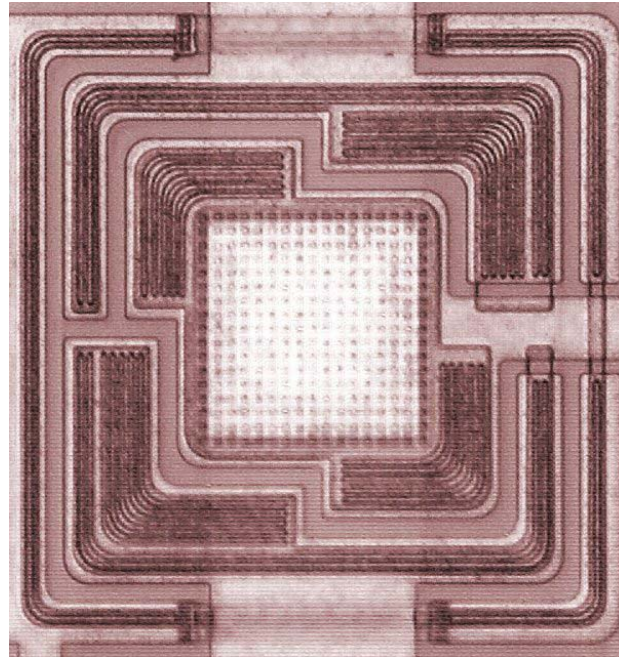
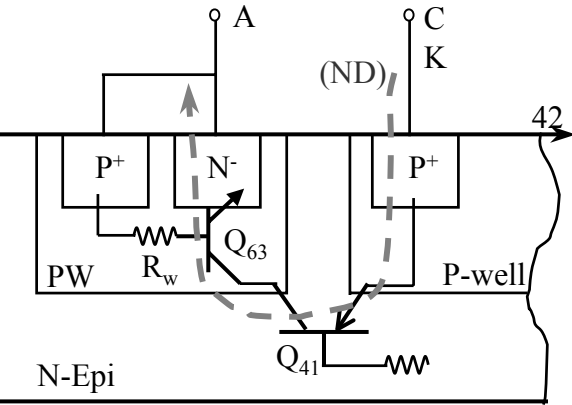
A common ESD bus scheme



Global ESD Bus

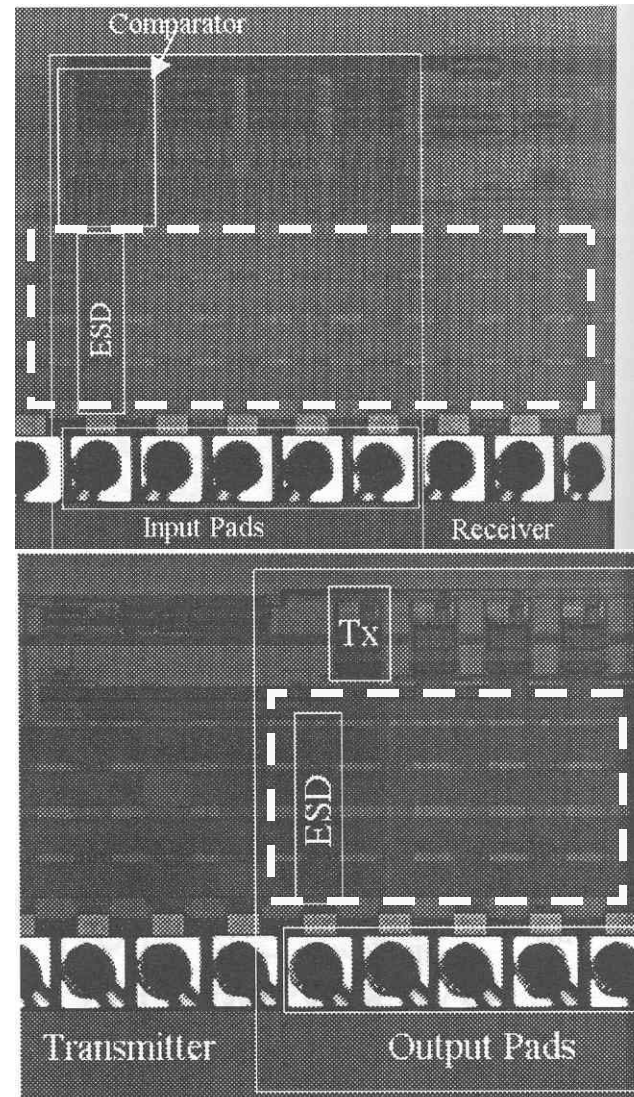
Ref: A. Wang, *On-Chip ESD Protection for Integrated Circuits*, Kluwer Academic Publishers, ISBN: 0-7923-7684-1, 2002.

Nice: Pad-oriented Compact ESD Protection



All-mode protection,
Under-pad!

Why Bother These Exotic Design?!



Ref: Hatori, et al, Proc. IEEE CICC 2001, pp501.

Future Work on ESD Protection

- A 3D mixed-mode ESD simulation-design methodology
- Full-chip ESD verification tool:
ESDExtractor → ESDInspector (smart checking) → ESDZapper → ESDSimulator → ESDcat
- Hi-I ESD Device Modeling: P-SWM model for geometry
- More on ESD-Circuit Interactions
- Novel low-parasitic compact ESD protection
- Super-GHz RF ESD protection
- ESD for Wide-bandgaps, GaN..
- Nano-ESD protection
- Emerging apps.....

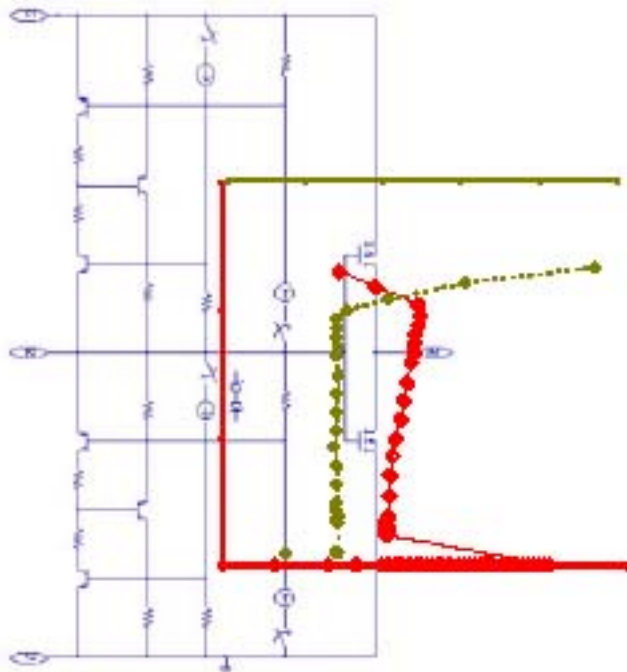
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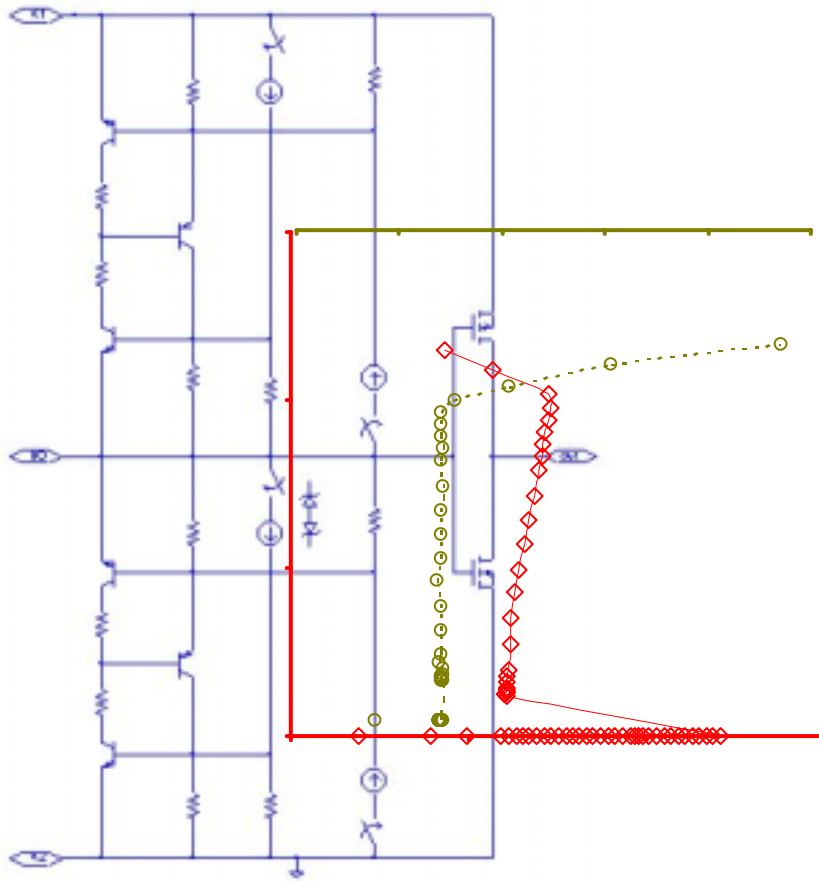


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This comprehensive and insightful book discusses ESD protection circuit design problem: designer's perspective. *On-Chip ESD Protection for Integrated Circuits: An IC Design Per* provides both fundamental and advanced materials needed by a circuit designer for design protection circuits, including:

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- ESD failure analysis, protection devices, and protection of sub-circuits
- Whole-chip ESD protection and ESD-to-circuit interactions
- Advanced low-parasitic compact ESD protection structures for RF and mixed-signal
- Mixed-mode ESD simulation-design methodologies for design prediction ESD-to-circuit interactions, and more!

Many real world ESD protection circuit design examples are provided. The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field.


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On-Chip ESD Protection for Integrated Circuits
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by
Albert Z.H. Wang
Illinois Institute of Technology, Chicago, USA

Dedication. Acknowledgements. Preface. **1.** Introduction. **2.** ESD Test Models. **3.** ESD Protection Device Solutions. **4.** ESD Protection Circuit Solutions. **5.** Advanced ESD Protection; Mixed and Whole-Chip ESD Protection. **6.** ESD Failure Analysis and Modeling. **7.** Layout and Test Influences on ESD Protection Circuit Design. **8.** ESD Simulation-Design Methodologies. **9.** Circuit Interactions. **10.** Conclusion Remarks and Future Work. **Appendix A:** Summary of Standards. References. **Appendix B:** Commercial ESD Testing Systems. **Appendix C:** ESD Protection Circuit Design Checklist. Index.

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On-Chip ESD Protection for Integrated Circuits

An IC Design Perspective

by
Albert Z.H. Wang

Illinois Institute of Technology, Chicago, USA

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AND COMPUTER SCIENCE 663

This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer's perspective. *On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective* provides both fundamental and advanced materials needed by a circuit designer for designing ESD protection circuits, including:

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Many real world ESD protection circuit design examples are provided. The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field.

Contents

Dedication. Acknowledgements. Preface. 1. Introduction. 2. ESD Test Models. 3. ESD Protection Device Solutions. 4. ESD Protection Circuit Solutions. 5. Advanced ESD Protection; Mixed-Signal, RF and Whole-Chip ESD Protection. 6. ESD Failure Analysis and Modeling. 7. Layout and Technology Influences on ESD Protection Circuit Design. 8. ESD Simulation-Design Methodologies. 9. ESD - Circuit Interactions. 10. Conclusion Remarks and Future Work. **Appendix A:** Summary for ESD Test Standards. References. **Appendix B:** Commercial ESD Testing Systems. **Appendix C:** ESD Protection Circuit Design Checklist. Index.

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