

Analog Front End Design For ADSL

R. K. Hester

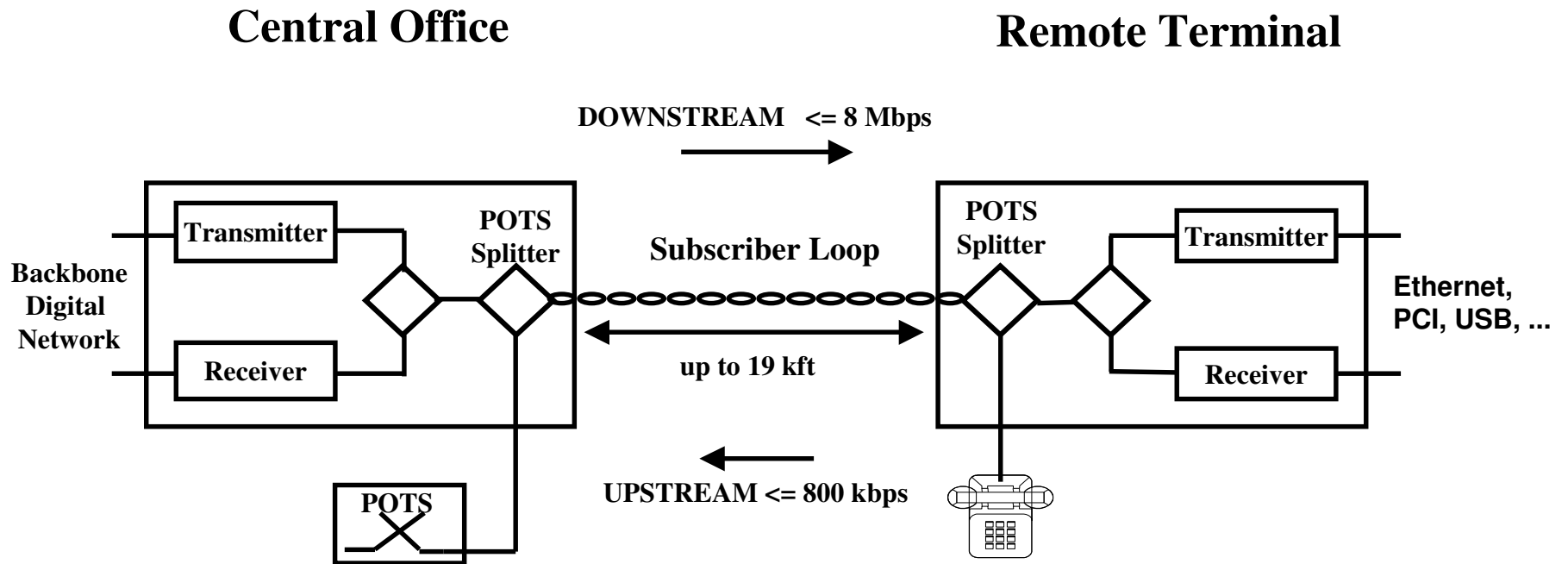
Texas Instruments Incorporated

Dallas, Texas, USA

Outline

- **Canonical ADSL System Diagram**
- **Signal Characteristics**
- **Impairments**
- **Line Coupling Circuits**
- **Transmitter Design**
- **Receiver Design**

ADSL System



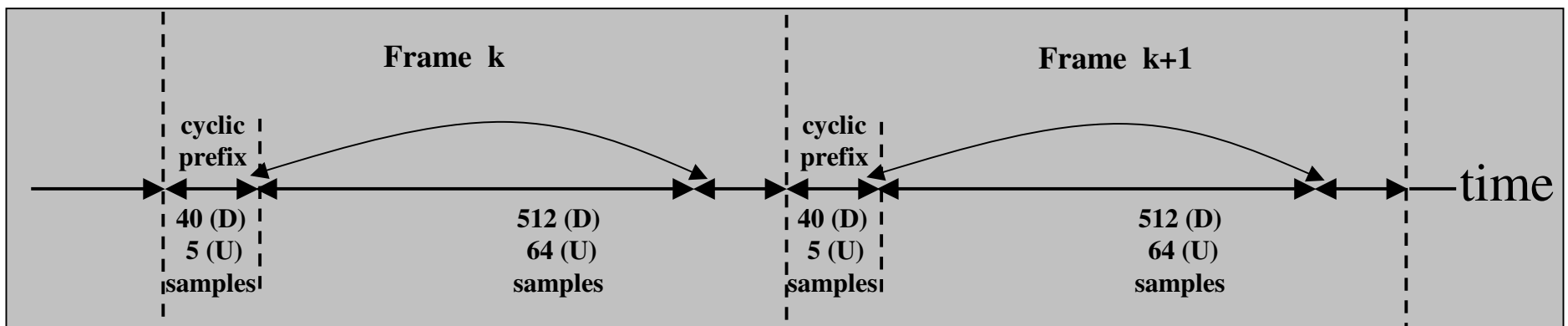
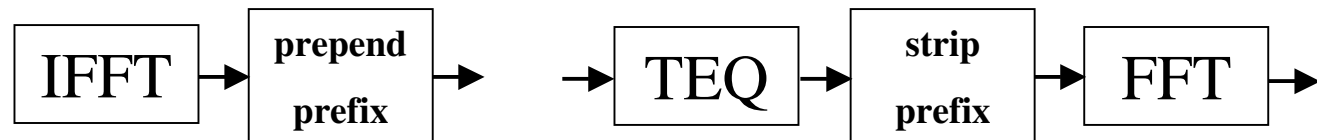
Unlike V.xx dial-up modems, the signal is not terminated by a voice-band line card

Signal Characteristics

- **DMT modulation**
- **Frequency plan**
- **Capacity**
- **Peak-to-Average Ratio and BER**
- **Continuous-time/Discrete-time PSD**

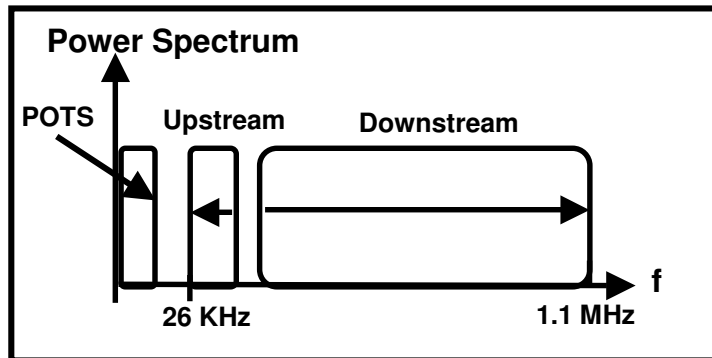
Discrete Multi-Tone Signaling (ODFM)

- Employs many narrow-band (4.3125 kHz) sub-carriers
- Low baud frequency (4 kHz)
- Data dynamically assigned to sub-carrier according to SNR
- IFFT/FFT used to modulate/demodulate in blocks

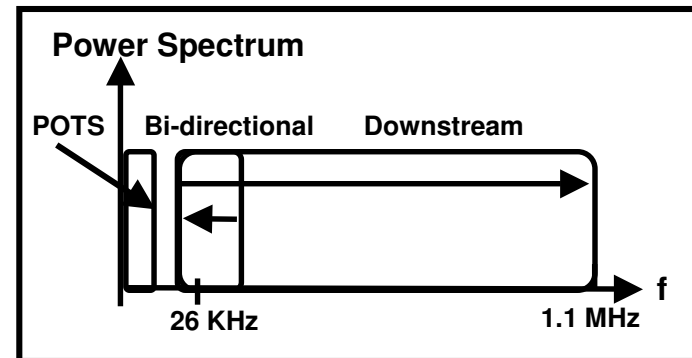


Frequency Plan

Frequency Division Duplexed

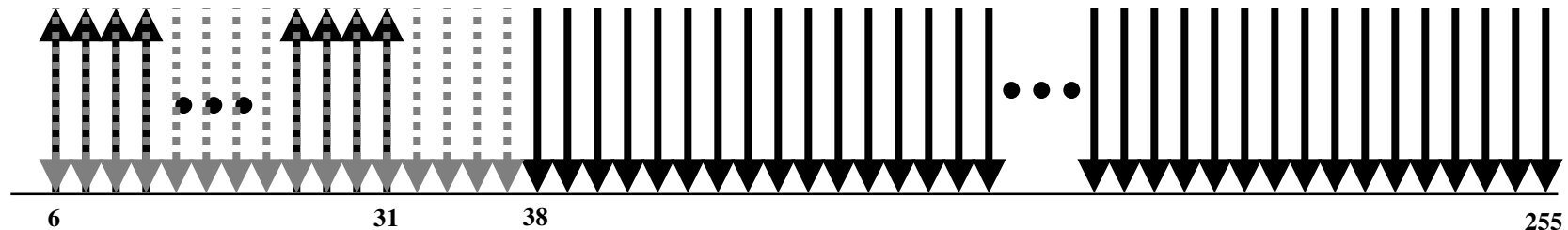


Echo-Cancelled



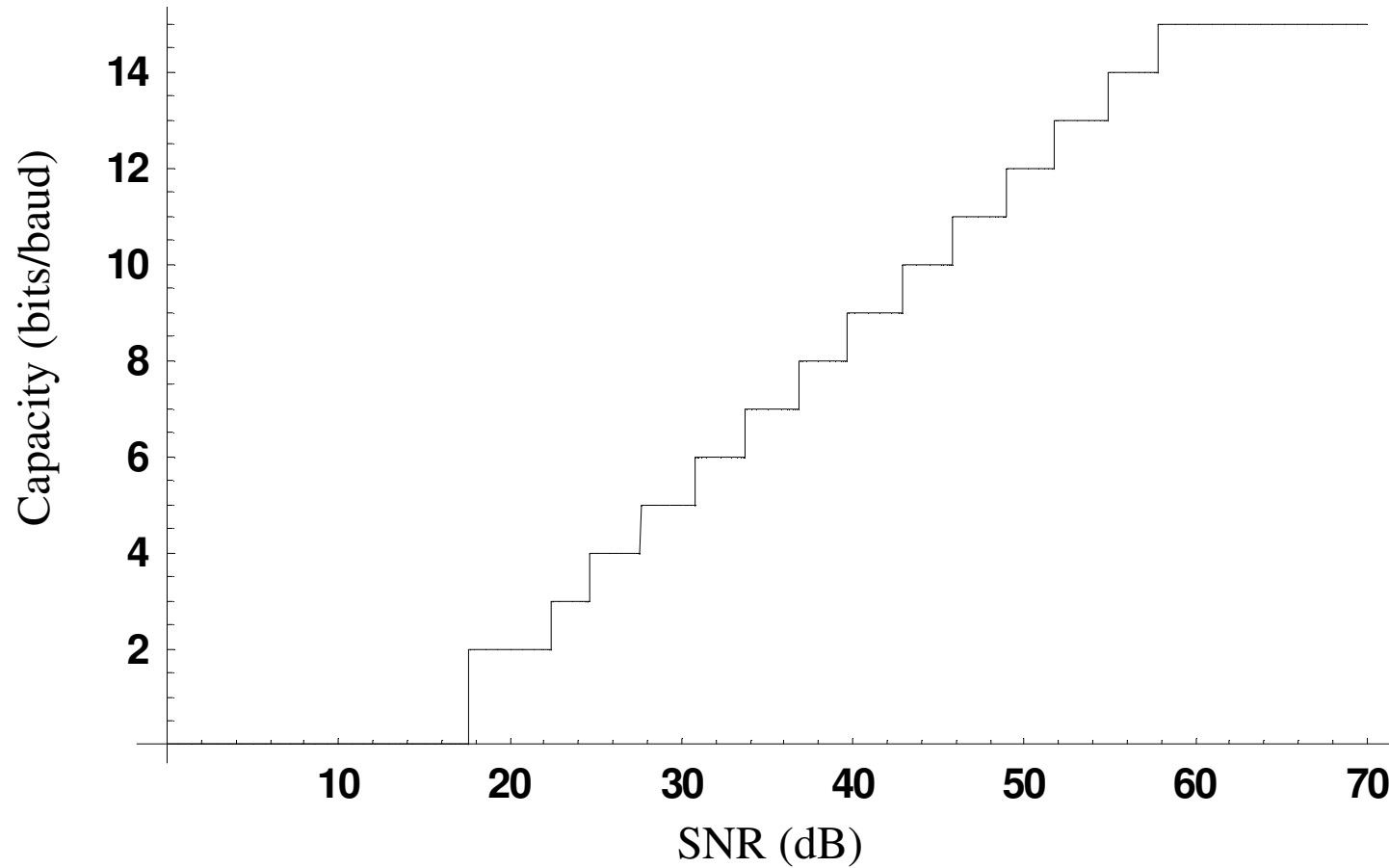
ITU G.hs training protocol guarantees FDD-EC modem interoperability

Annex A Frequency Plan Example

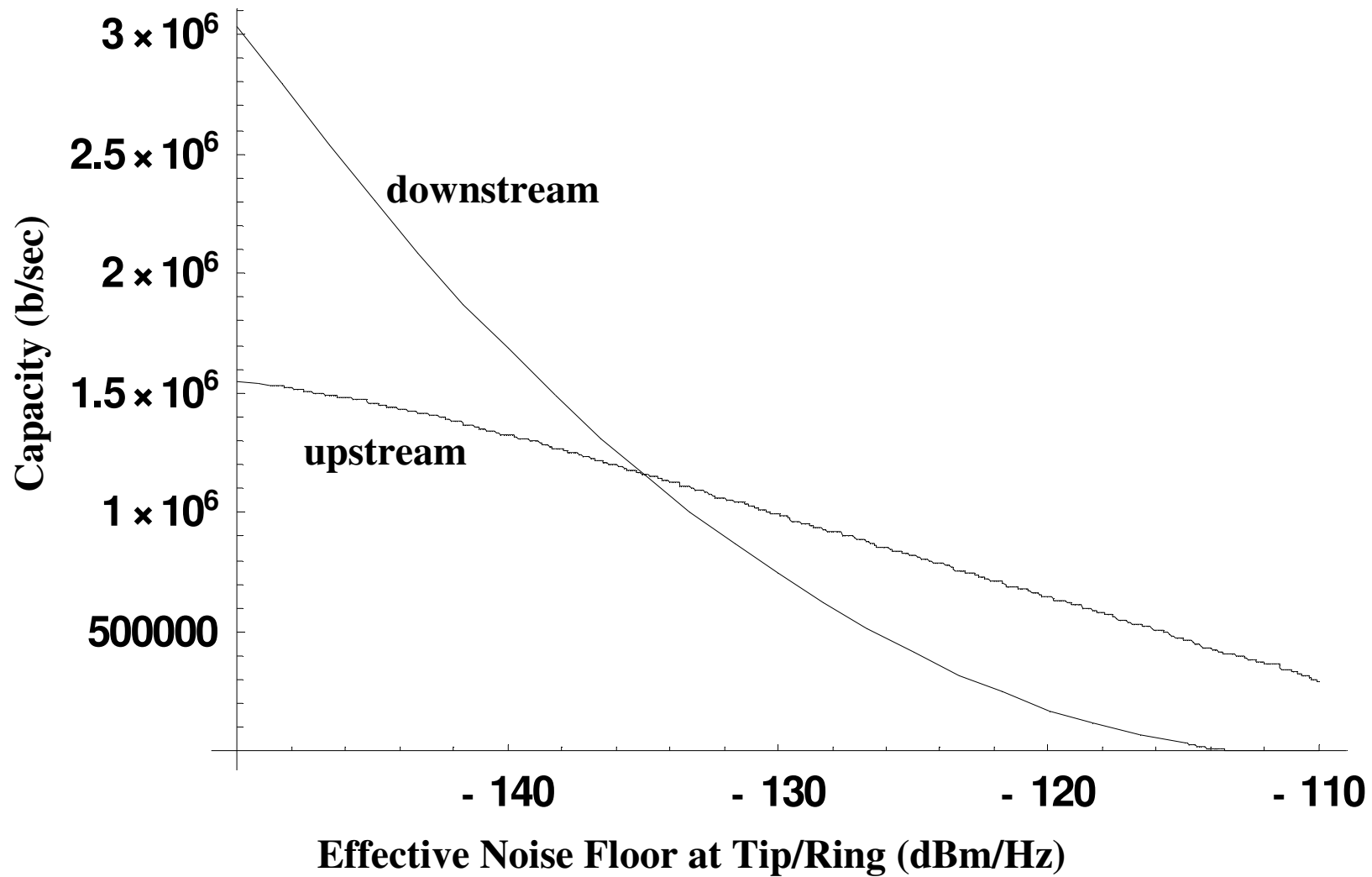


- Sub-carrier frequencies: $n \cdot 4.3125$ kHz
 - Upstream $n = 6, \dots, 31$
 - Echo-canceling downstream $n = 6, \dots, 255$
 - Frequency division downstream $n = 33, \dots, 255$
- Modulation: 4QAM ... 32768QAM
- Subcarrier data rate capacity: 2-15 bits per baud period

Subcarrier Capacity versus SNR



Maximum 15kft 26awg Data Rate Capacity

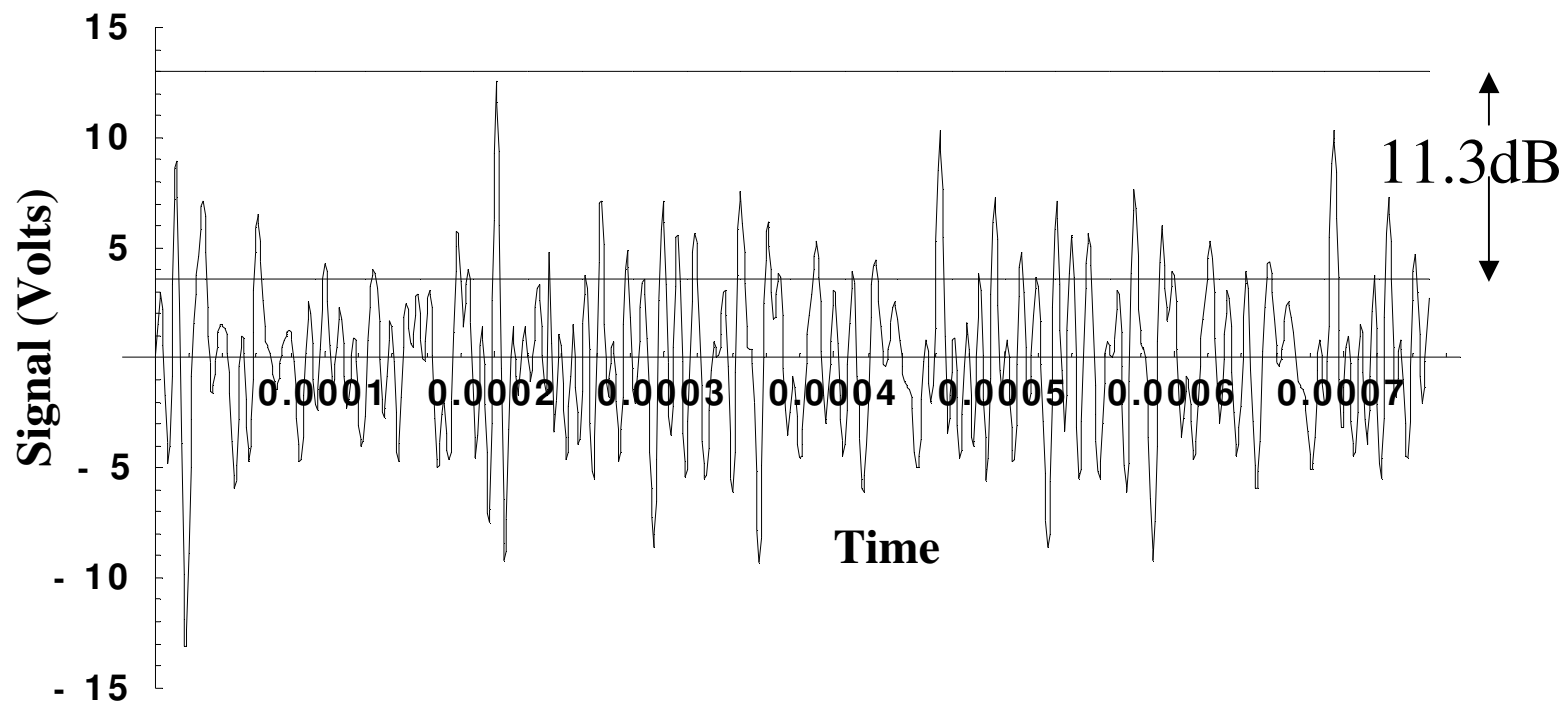


More on Frequency Plan

<u>Annex</u>	<u>Upstream</u>	<u>Downstream</u>
• A (POTS)	6 – 31	6 (33) – 255
• A+	6 – 31	6 (33) – 511
• B (ISDN)	29 – 63	29 (60) – 255
• B+	29 – 63	29 (60) – 511
• C (TCM-ISDN)	33 – 63	33 – 255
• H (TCM-ISDN)	6 – 255	6 – 255
• I	1 – 31	1 – 255
• J	1 – 31 (63)	1 – 255

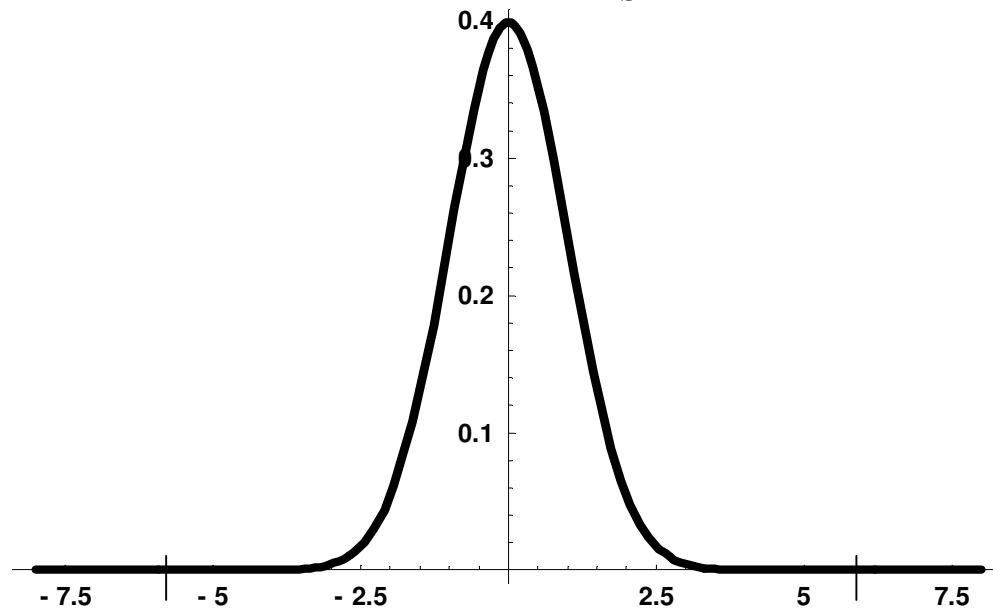
Peak-to-RMS Ratio

- Subcarriers are statistically independent, so sum of N has Gaussian probability distribution in time-domain, where variance is $0.43152 * N \text{ volt}^2$.
- When $N=250$, the RMS signal is 3.28V, and a 16dB peak-to-RMS ratio corresponds to 41.4 V_{pp}.

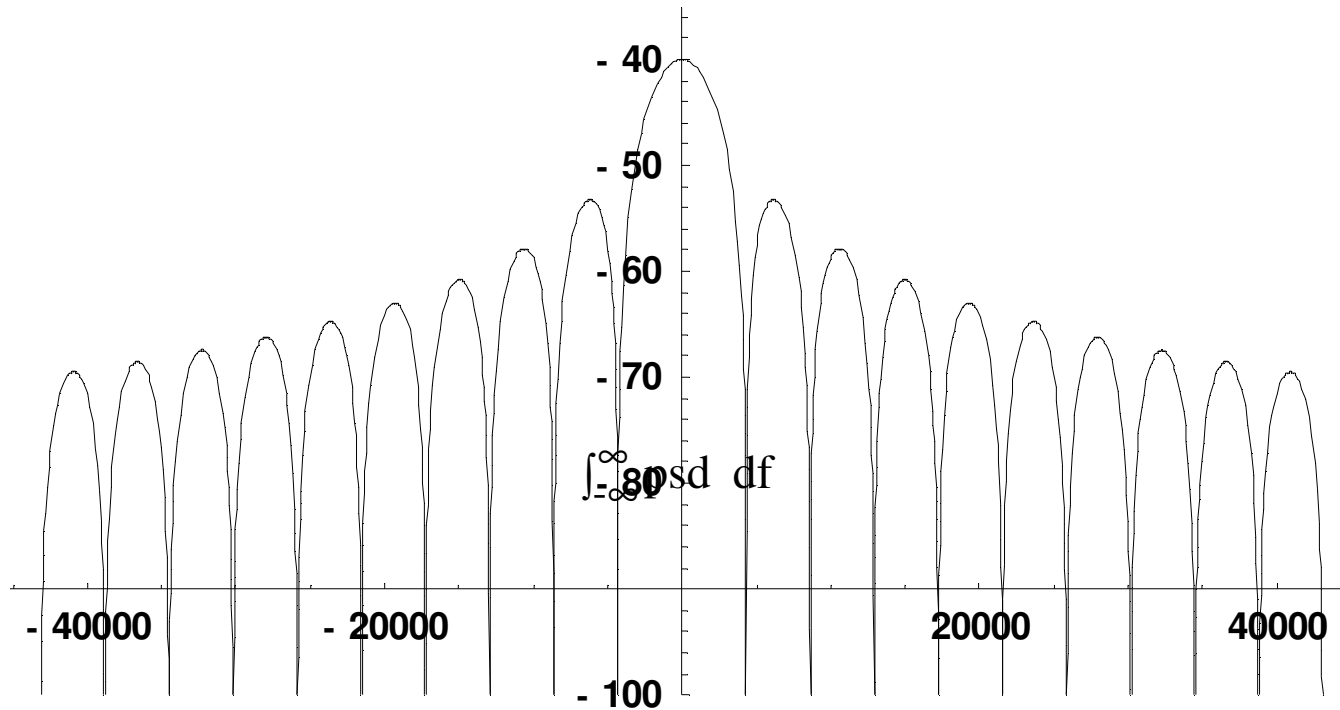


Gaussian Signal Statistics

- Sub-carriers are statistically independent, so sum of N sub-carriers has Gaussian probability (central limits theorem)
- Signal clipping, either analog or digital, transmitter or receiver, wrecks SNR and creates transmission errors
- Must support signal swing that corresponds to desired bit error rate
- 16dB peak-to-RMS ratio (peaks to $6.3 V_{\text{RMS}}$) corresponds to a 10^{-7} BER.



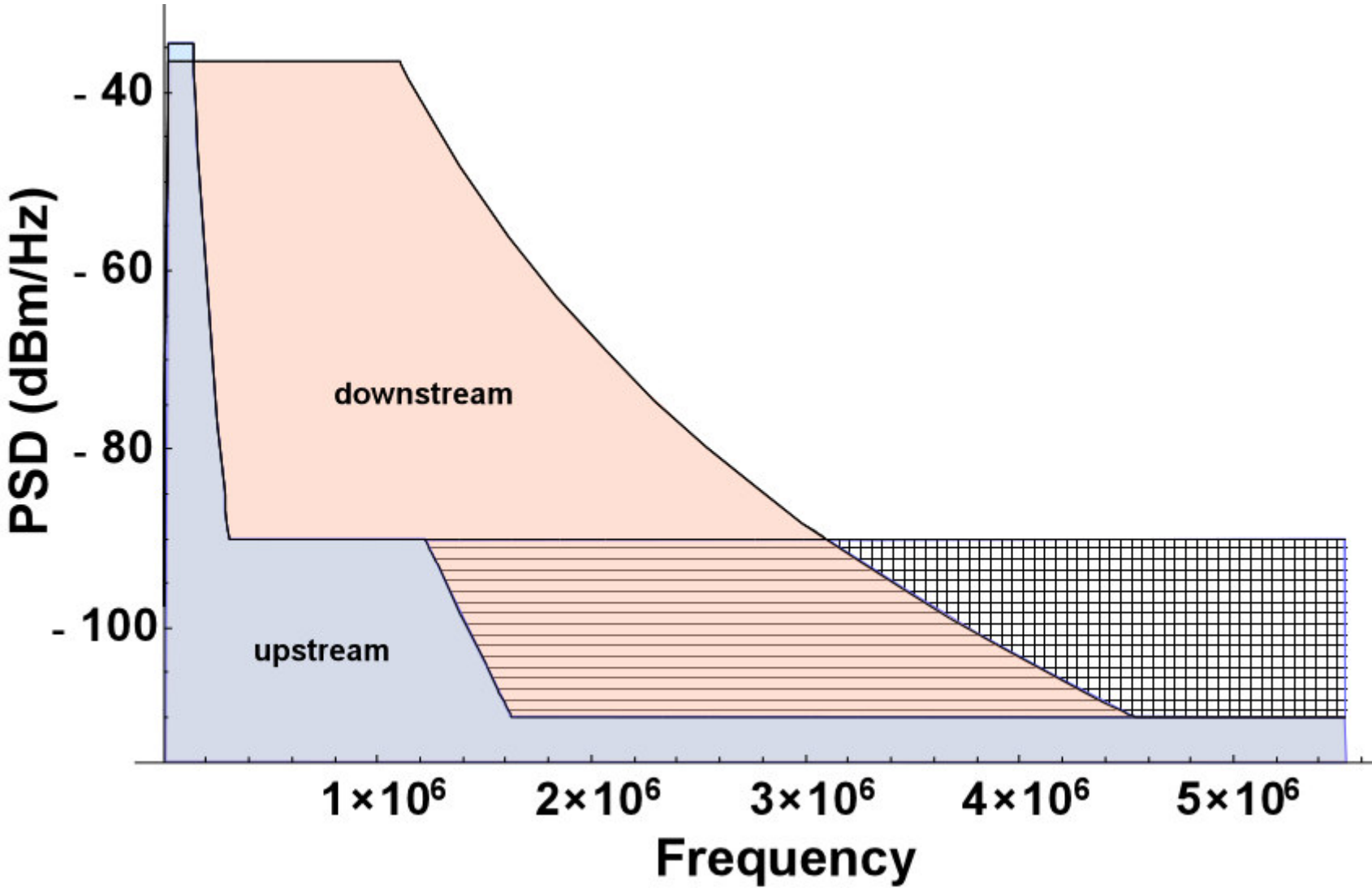
Sub-Carrier Power Spectral Density (dBm/Hz)



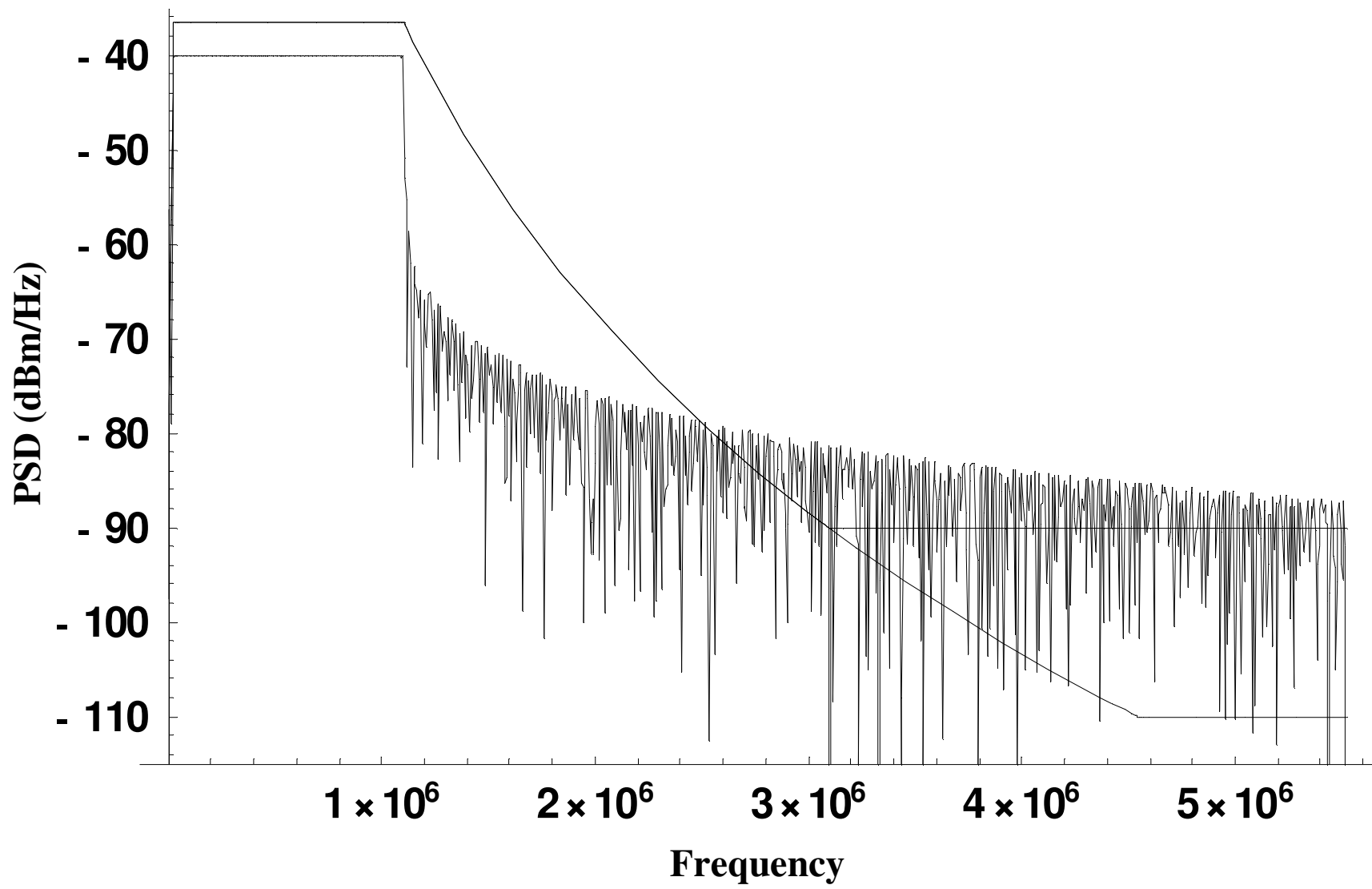
$$\text{Sub-carrier Power} = \int_{-\infty}^{\infty} psd df$$

$$= -3.65\text{dBm} (432\mu\text{W}) \text{ downstream and } -1.65\text{dBm} (544\mu\text{W}) \text{ upstream.}$$

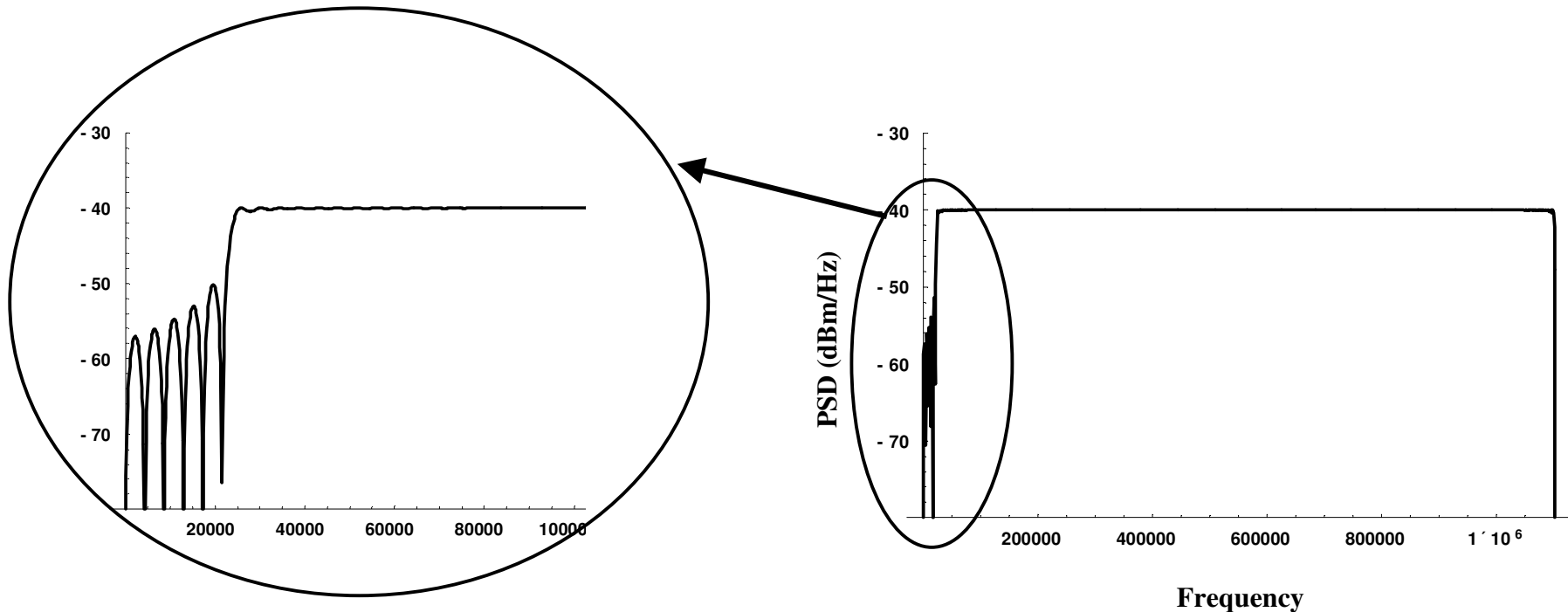
ITU/ANSI PSD Masks



Downstream PSD With Continuous Time Sub-Carrier Generation

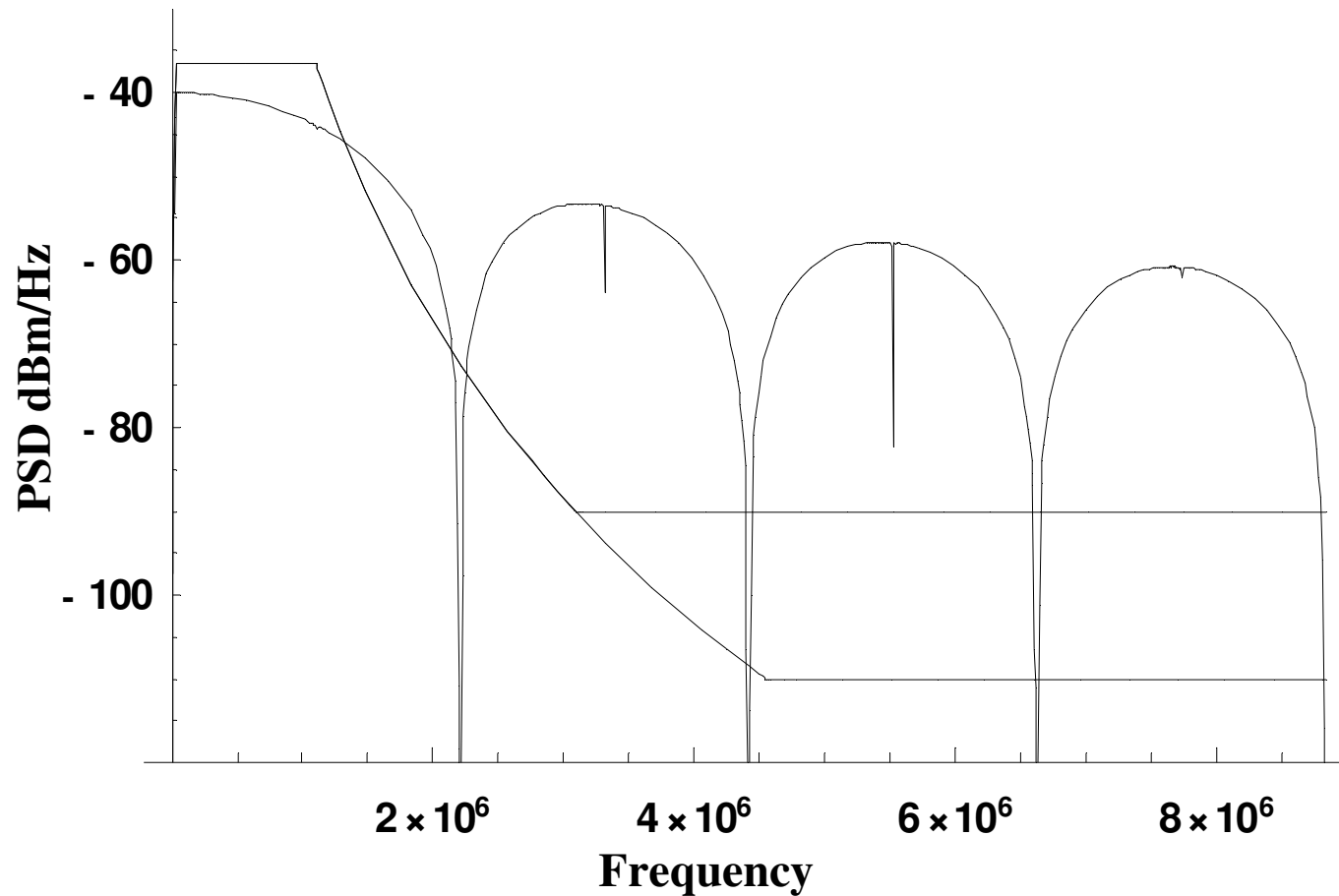


DSP Transmitter Signal (Minimum Sample Rate)



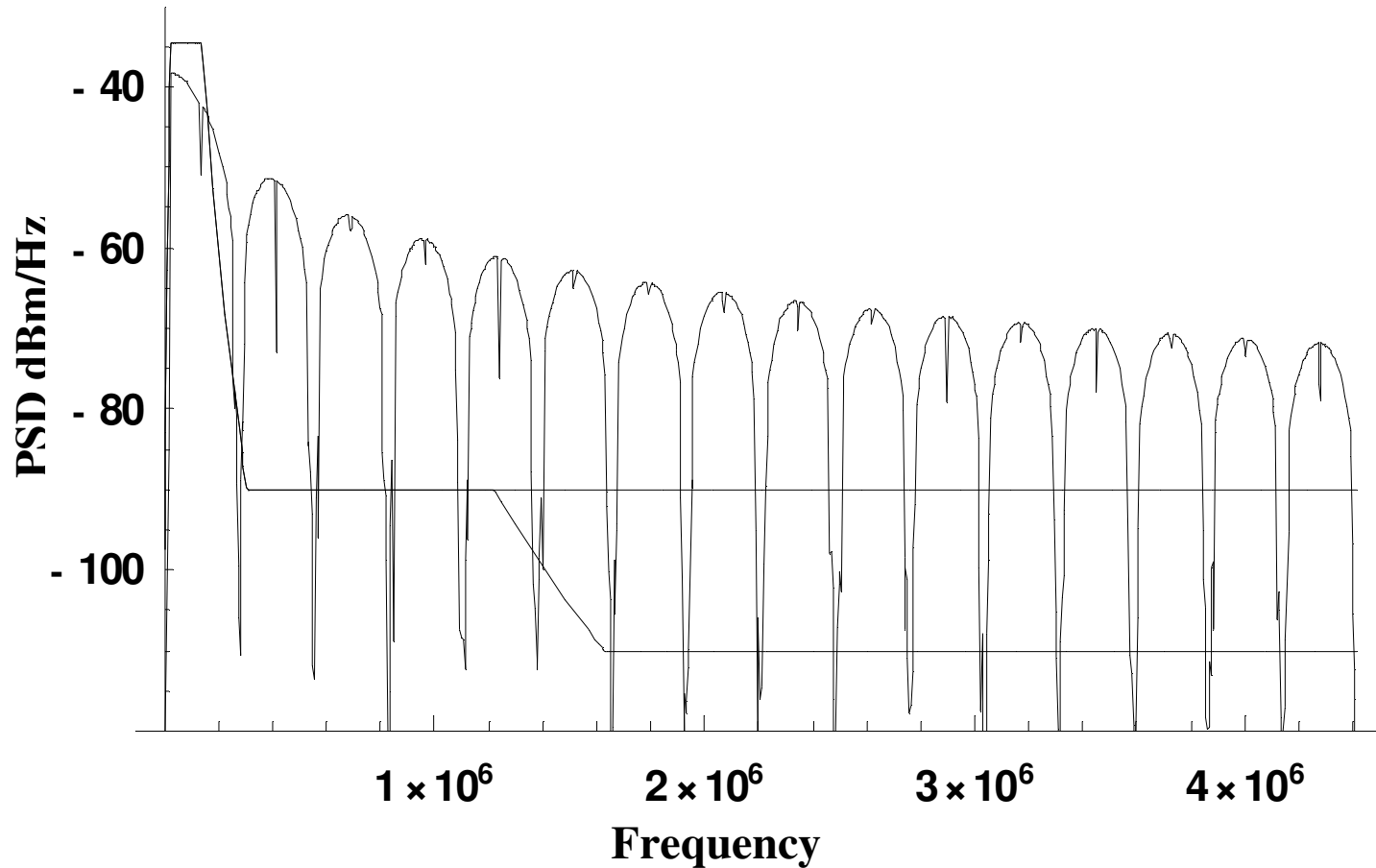
- **Minimum Annex A downstream 256-point IFFT with 4312.5Hz resolution (one bin per subcarrier) produces 2208kS/sec sample rate.**
- **Minimum Annex A upstream 32-point IFFT with 4312.5Hz resolution (one bin per subcarrier) produces 276kS/sec sample rate.**

Downstream PSD With Minimum Sample Rate



- Conversion of downstream signal to continuous-time at 2208kS/sec produces in-band droop and significant standard's non-compliance.

Upstream PSD With Minimum Sample Rate (276kS/sec)

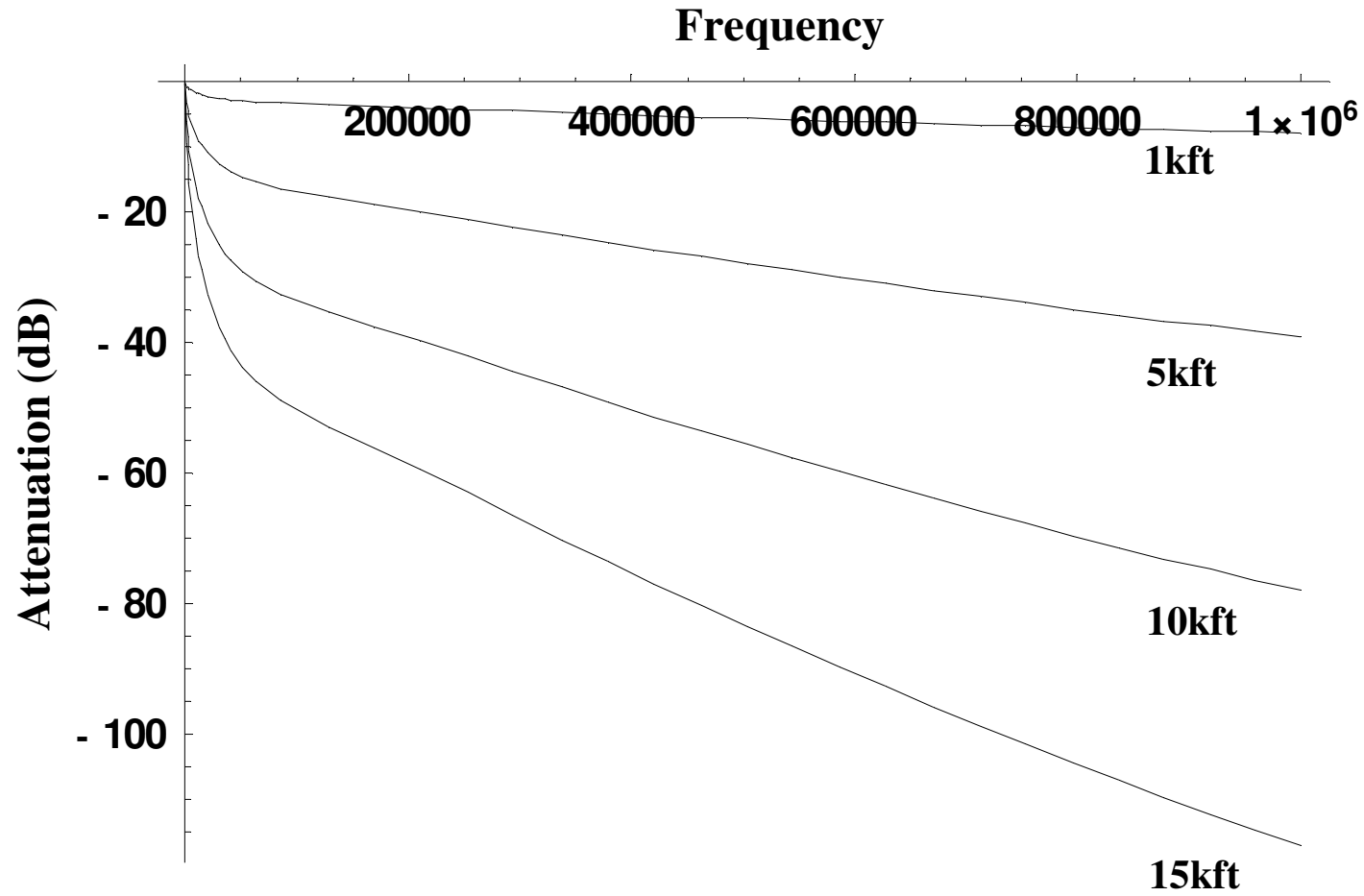


- Conversion of upstream signal to continuous-time at 276kS/sec produces in-band droop and significant standard's non-compliance.

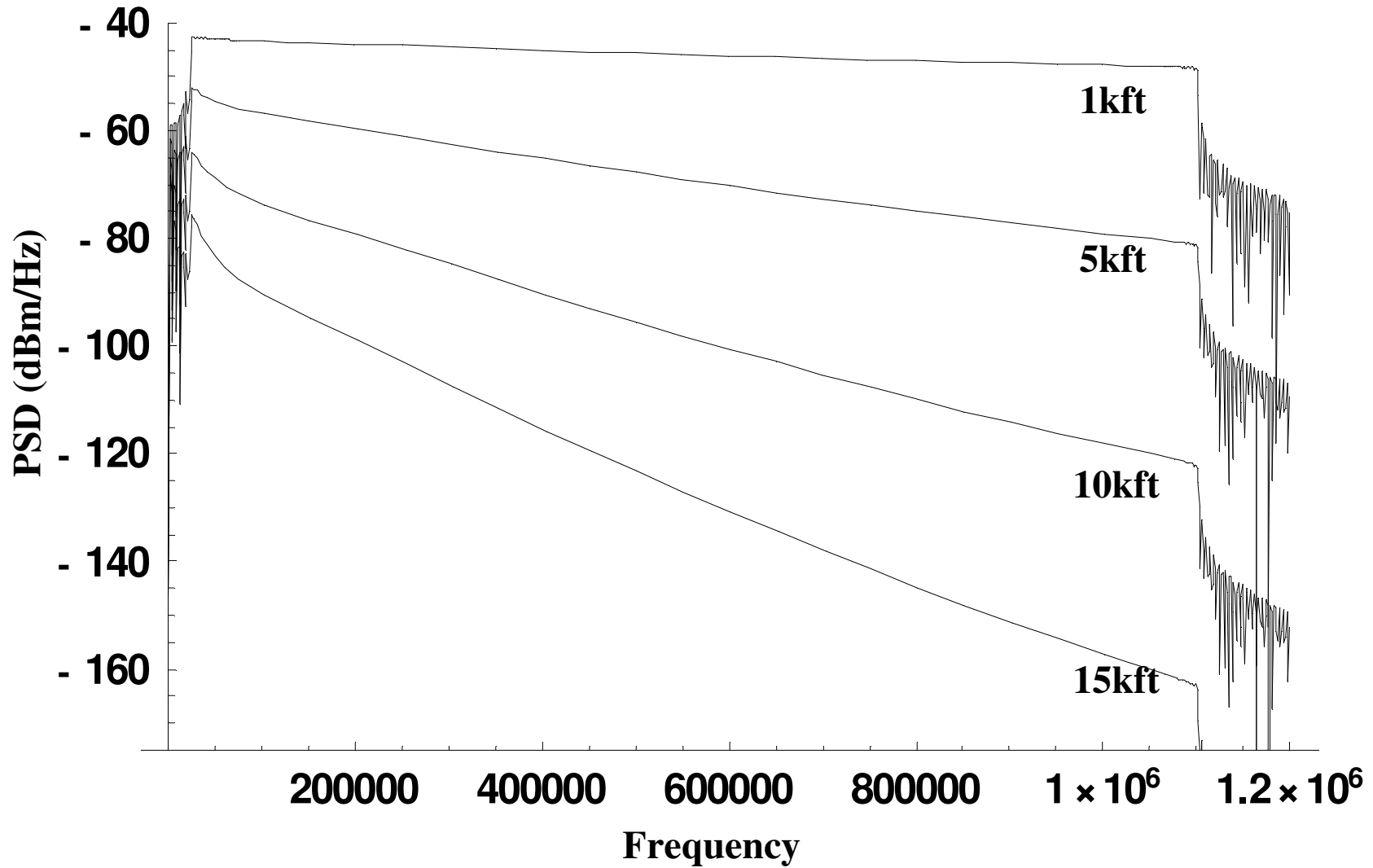
Impairments

- **Loop attenuation**
- **Loop variability**
- **Crosstalk**

26awg Loop Attenuation

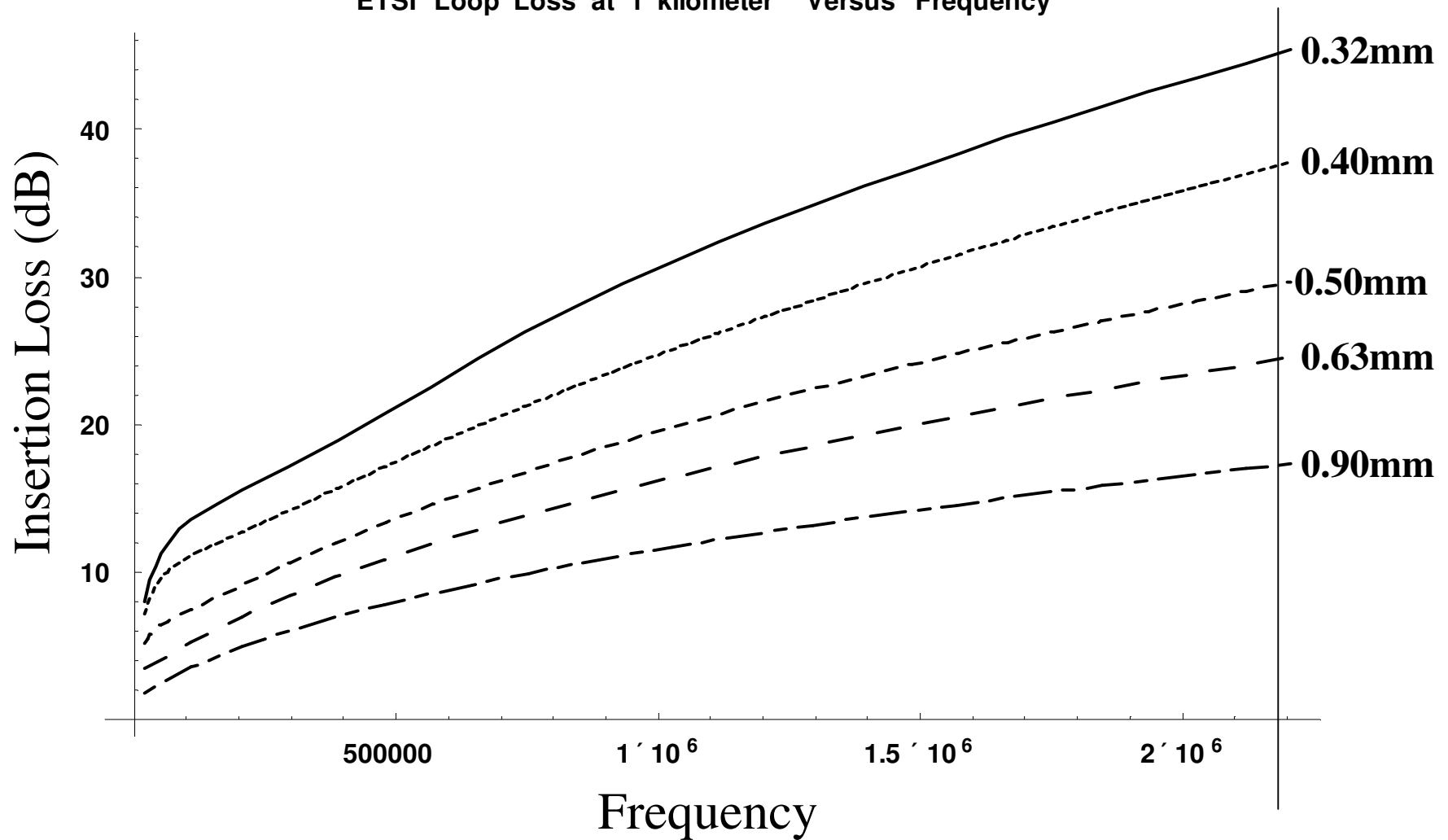


Downstream PSD on 26awg Loops

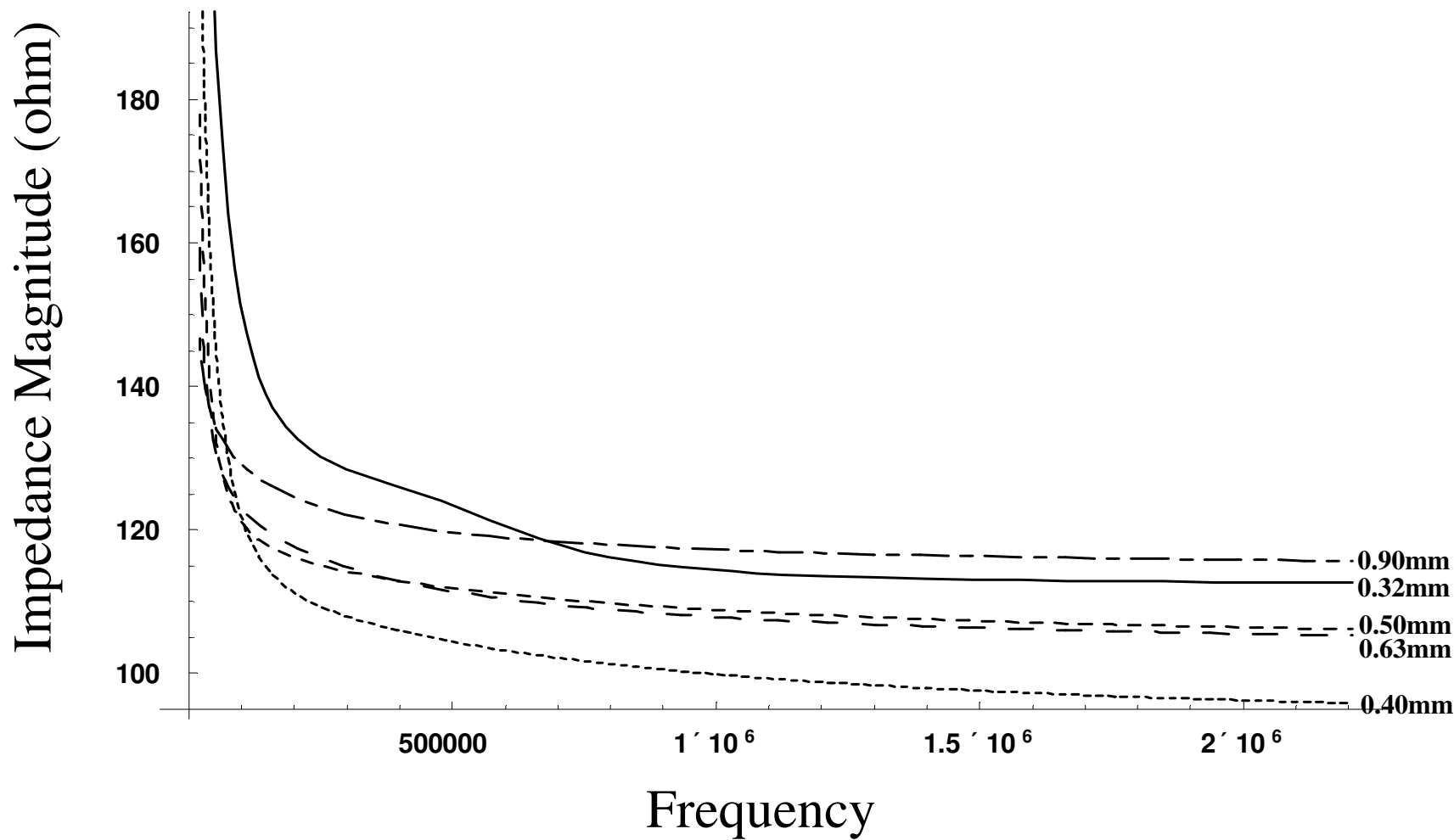


Loop Variability

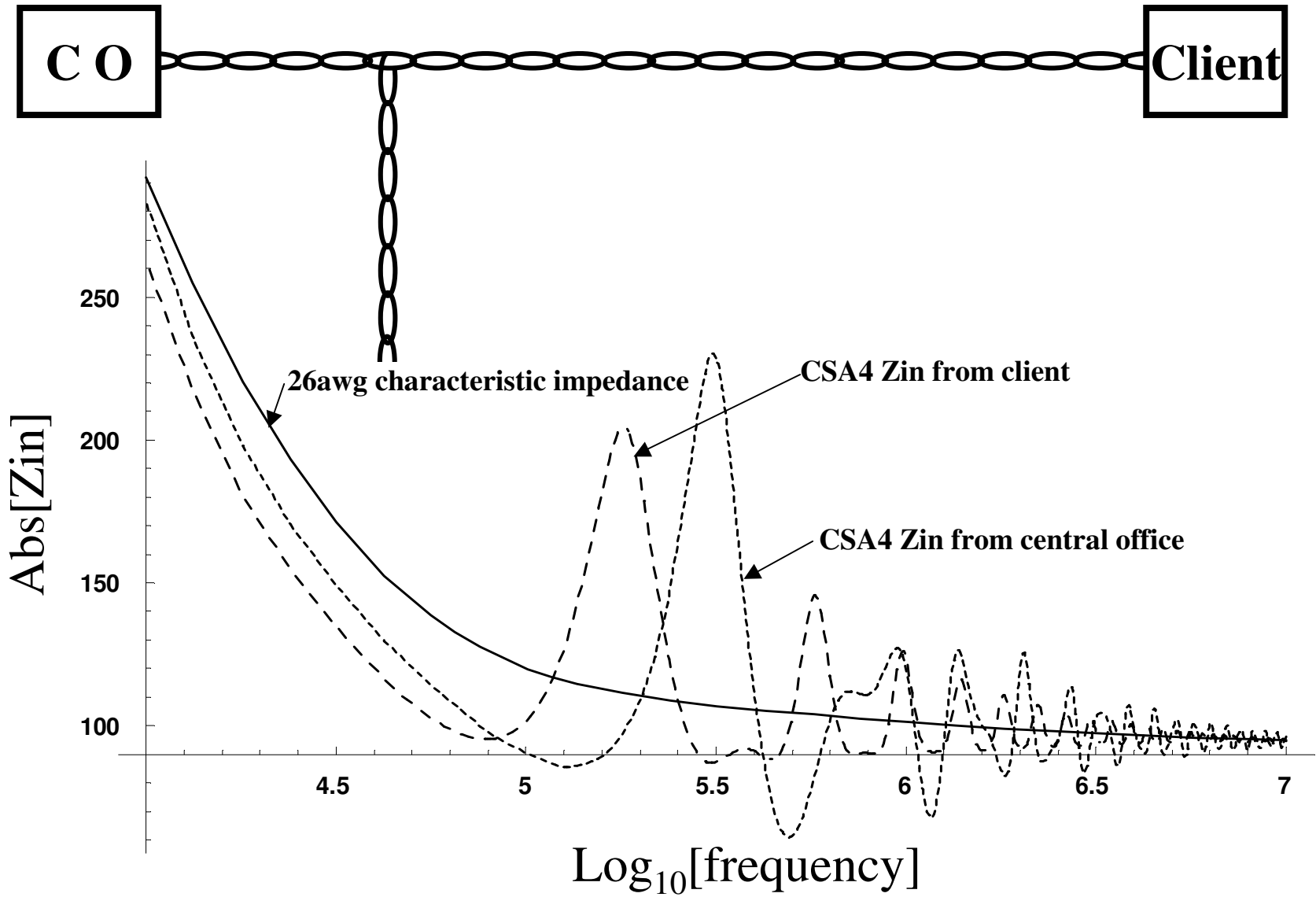
ETSI Loop Loss at 1 kilometer Versus Frequency



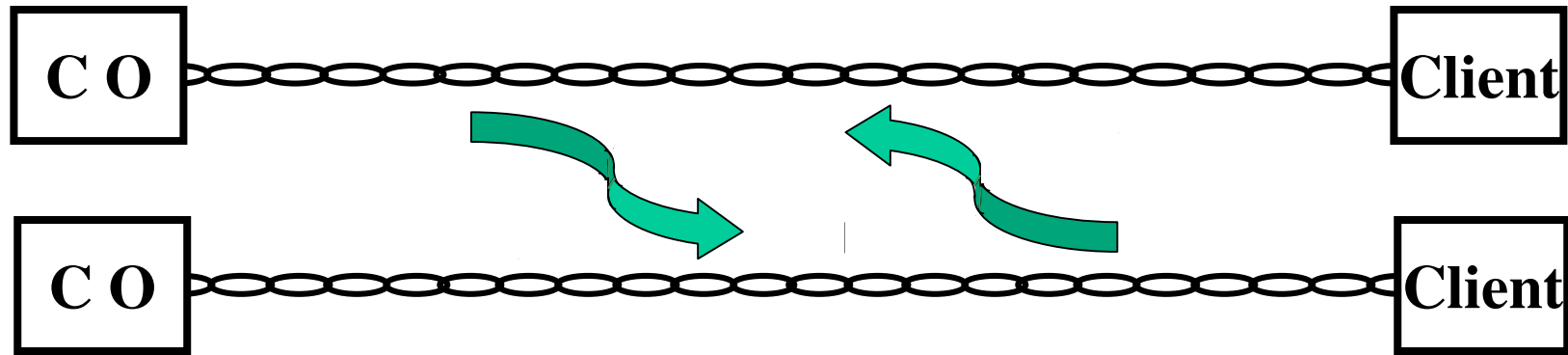
Loop Impedance



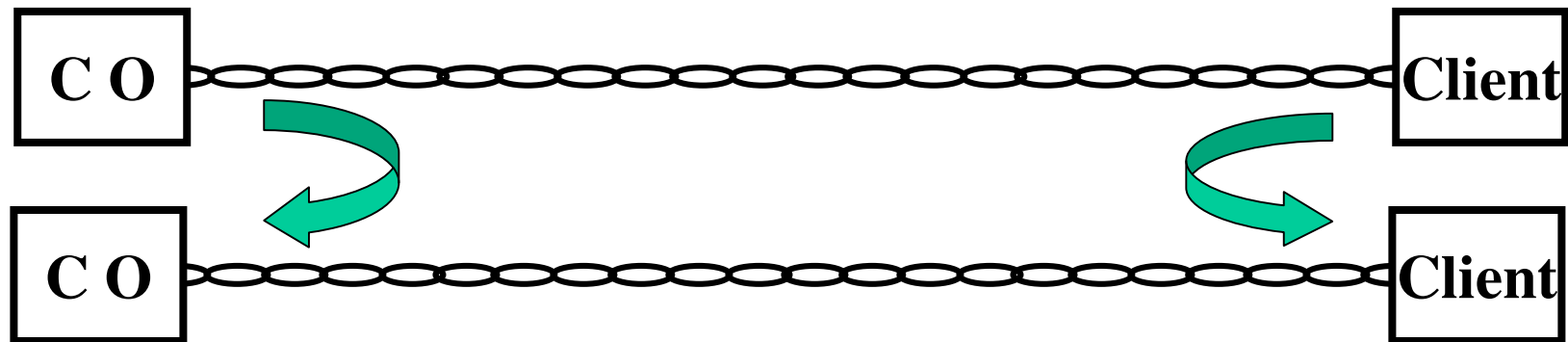
Bridged Taps



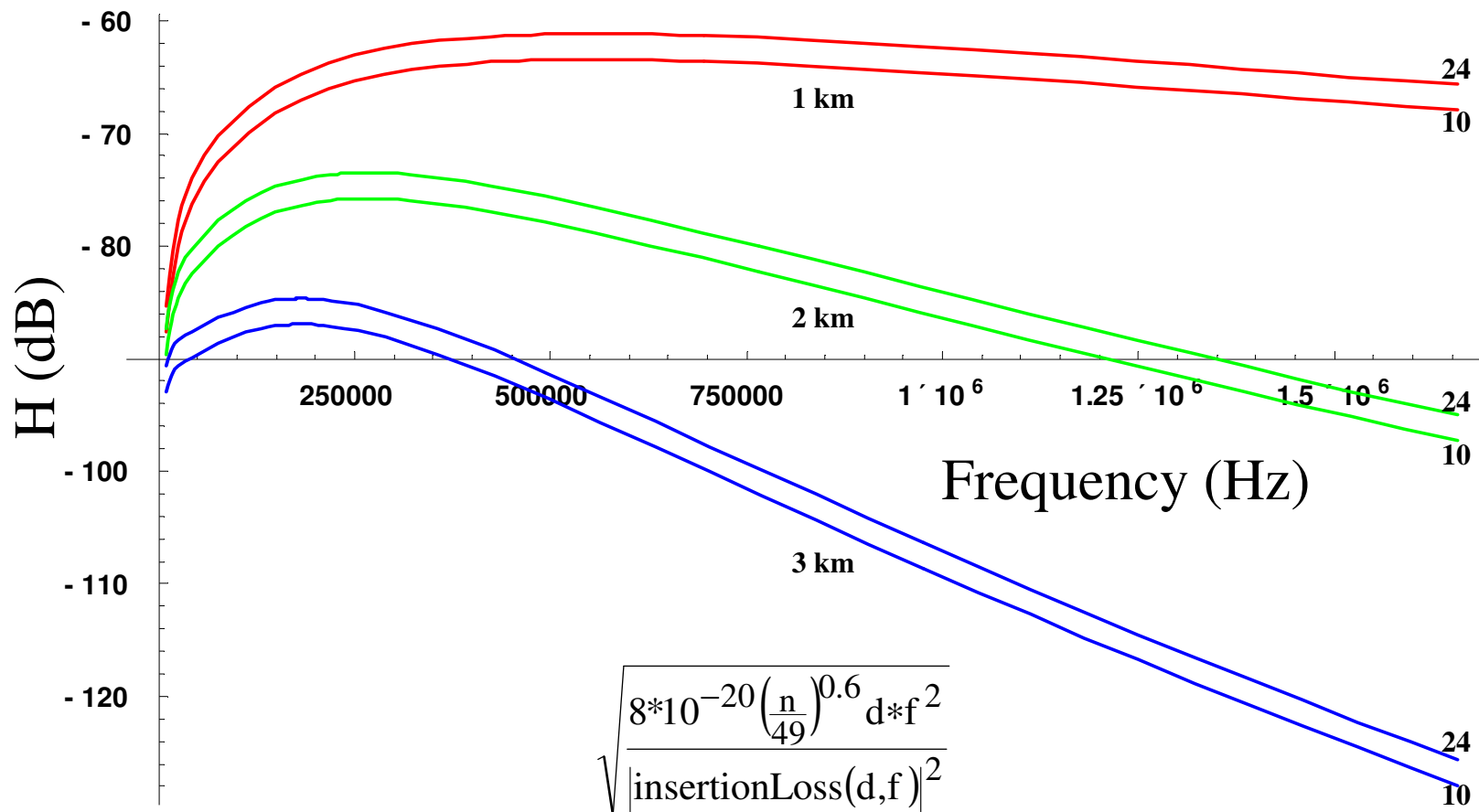
Far End Cross Talk (FEXT)



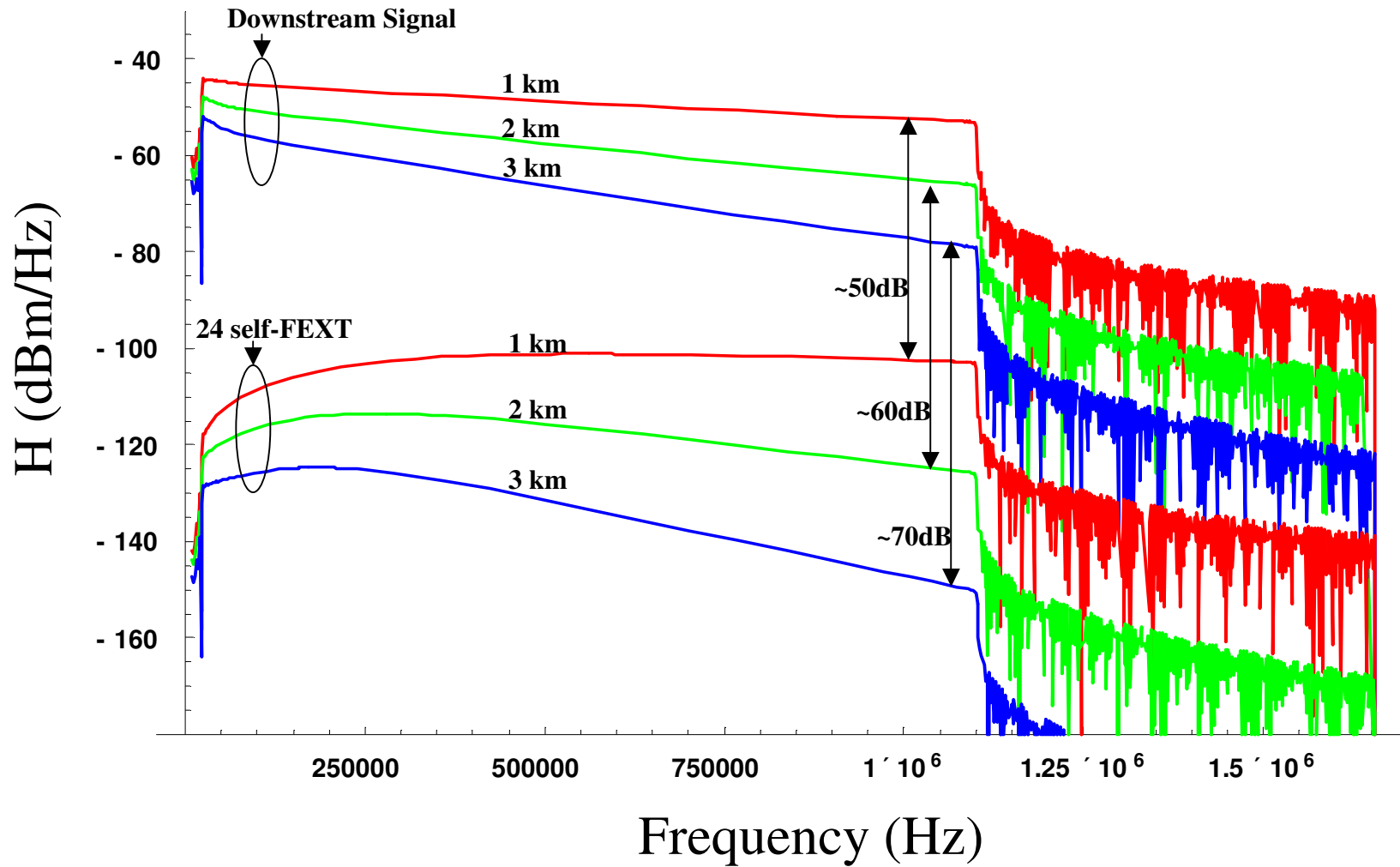
Near End Cross Talk (NEXT)



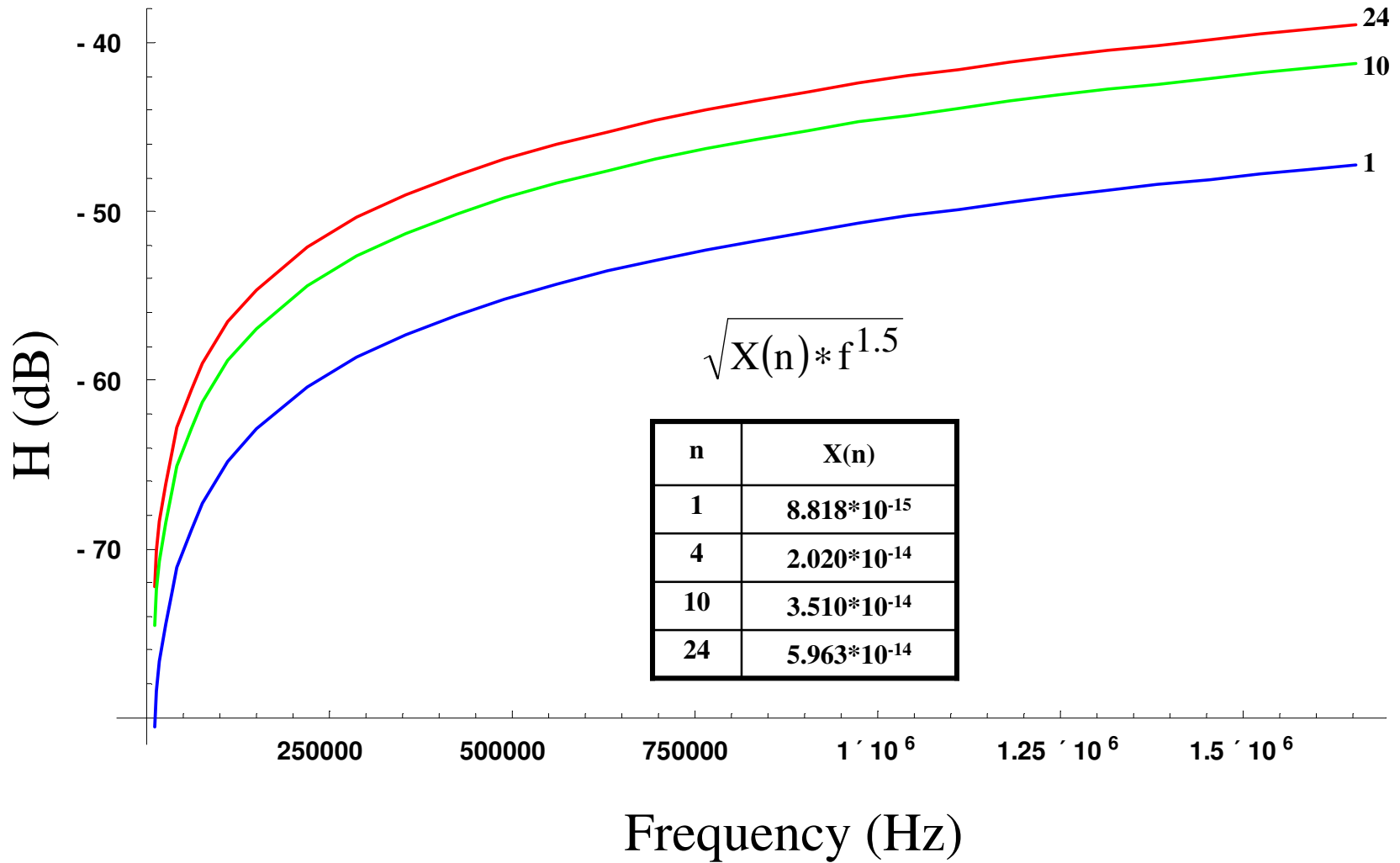
Far End Crosstalk Transfer Function (FEXT)



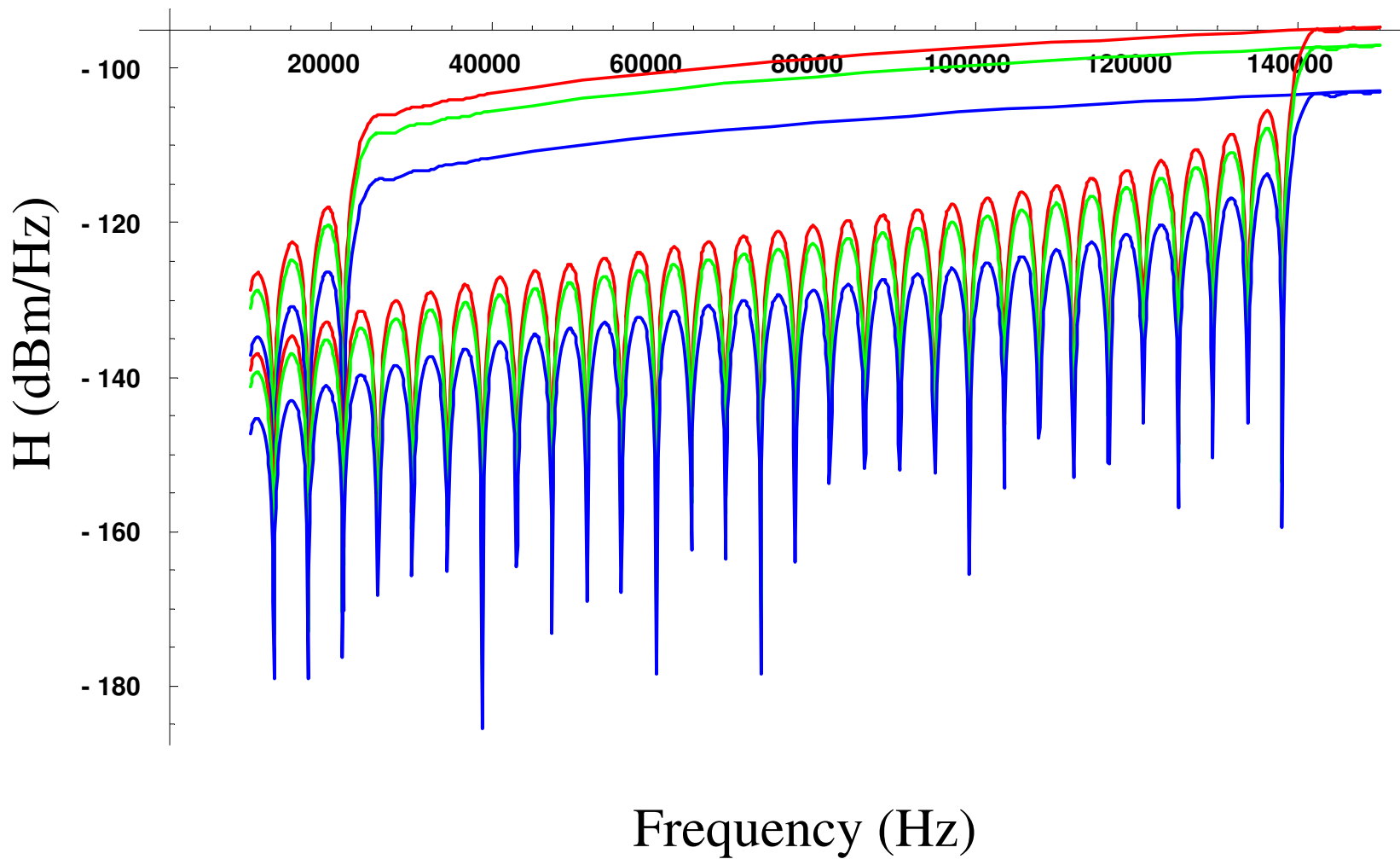
24-Self FEXT Example



Near End Crosstalk Transfer Function (NEXT)



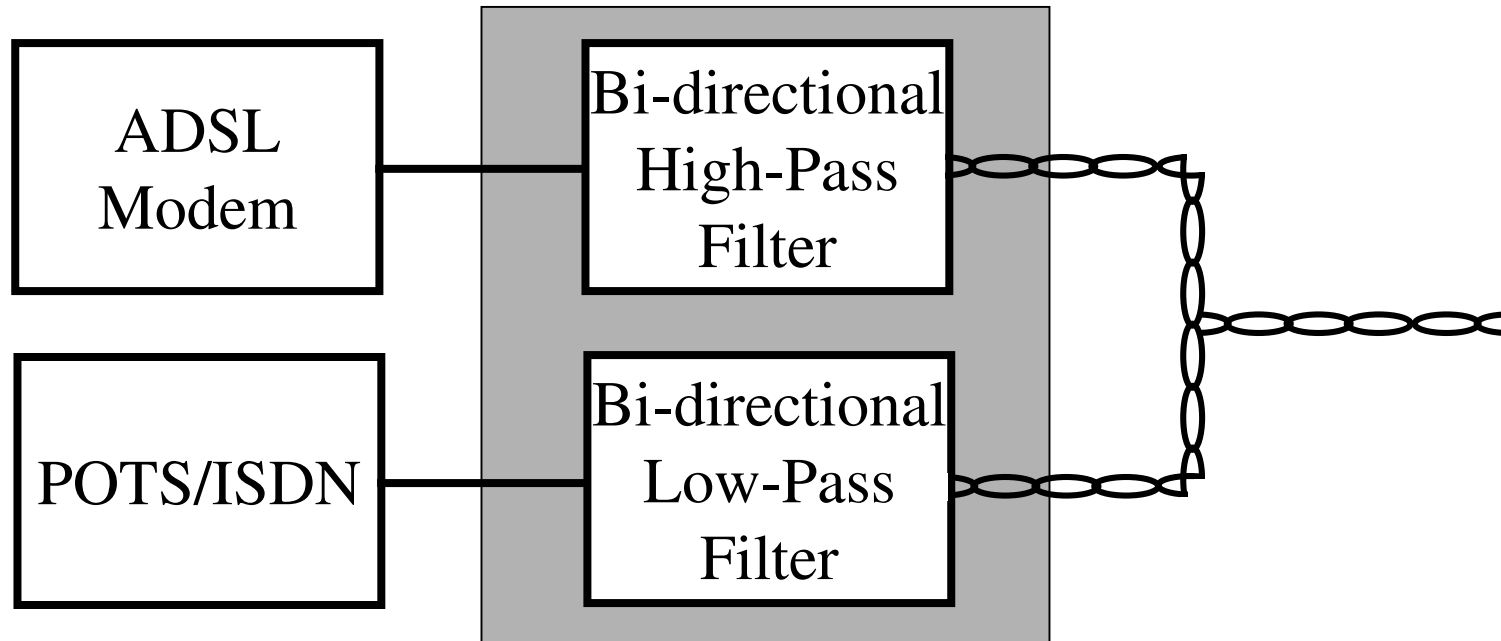
1-, 10- and 24-Self NEXT Example



Line Coupling Circuit

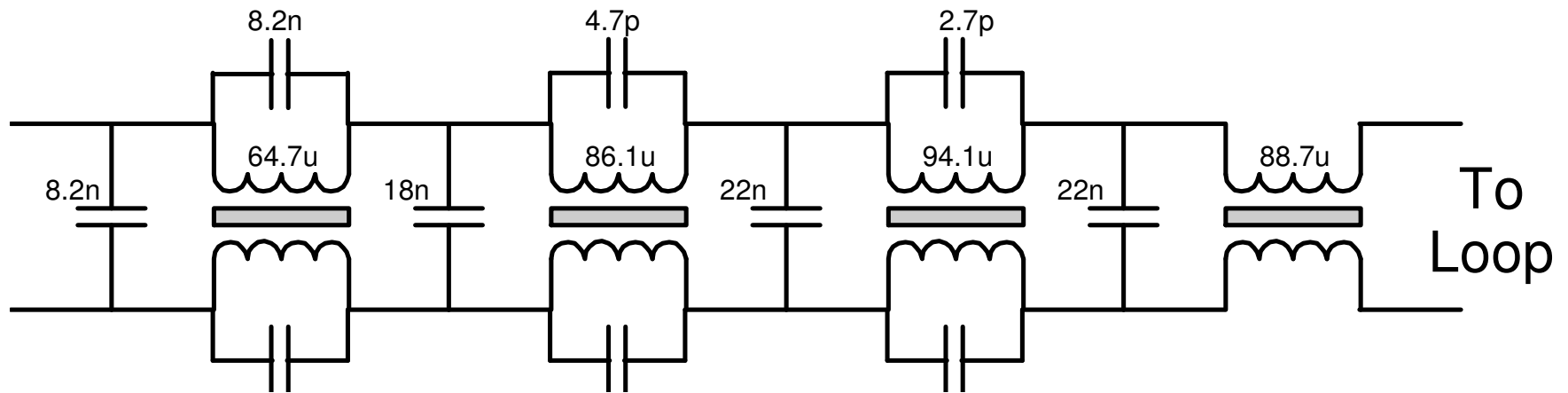
- **Splitter**
- **Active termination**
- **Hybrid**

Splitter



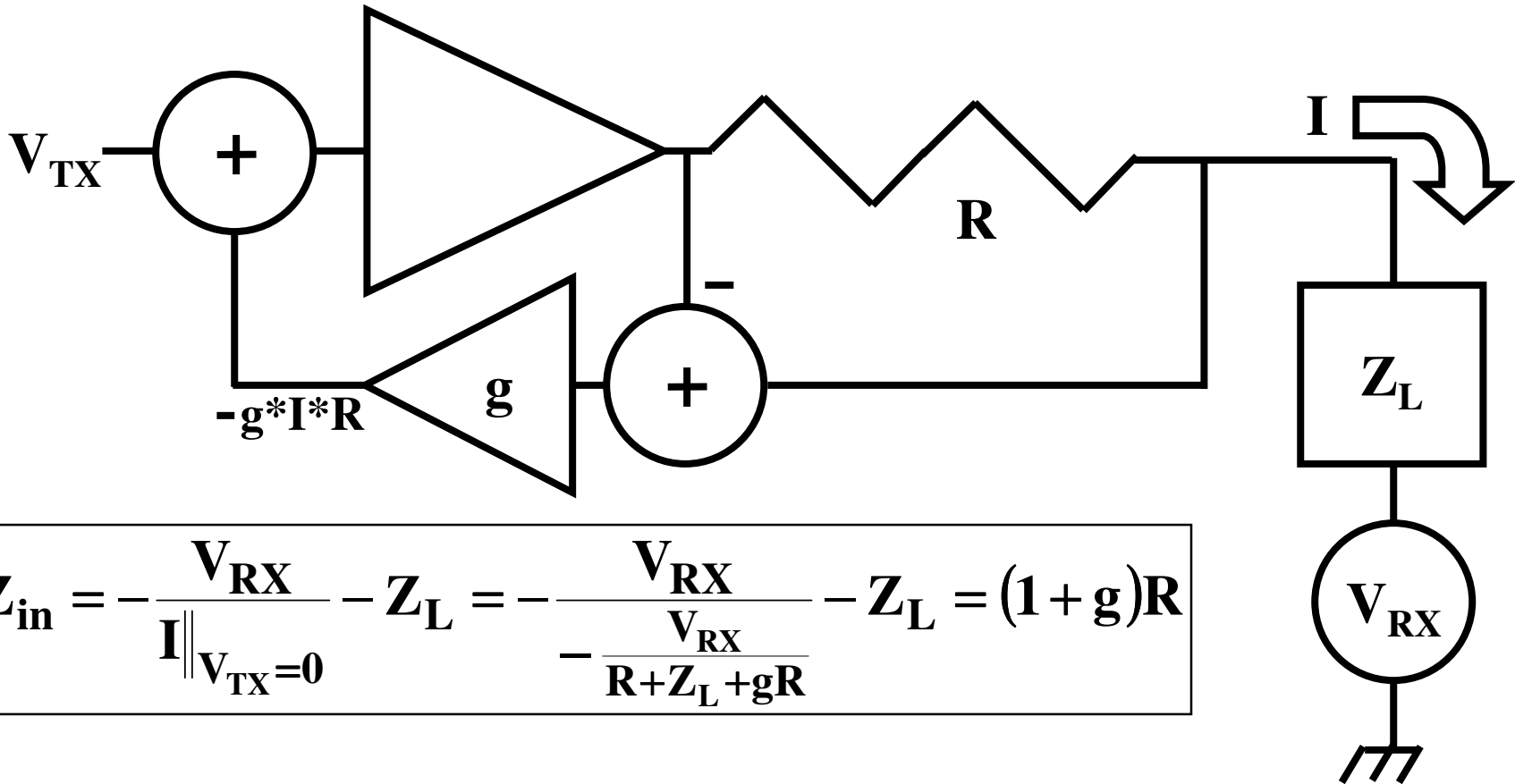
- In the POTS/ISDN frequency band, the high-pass, generally built into modem transformer circuit, presents high impedance to loop and reduces ADSL modem-generated noise.
- In the ADSL frequency band, the low-pass presents high impedance to loop and reduces POTS/ISDN-generated noise.

Annex B Splitter Low-Pass Example



- **Very high quality (low distortion) components are required**
- **DC current feed (POTS) may not saturate transformers**
- **Cost is high, both the bill of materials and the PCB area**

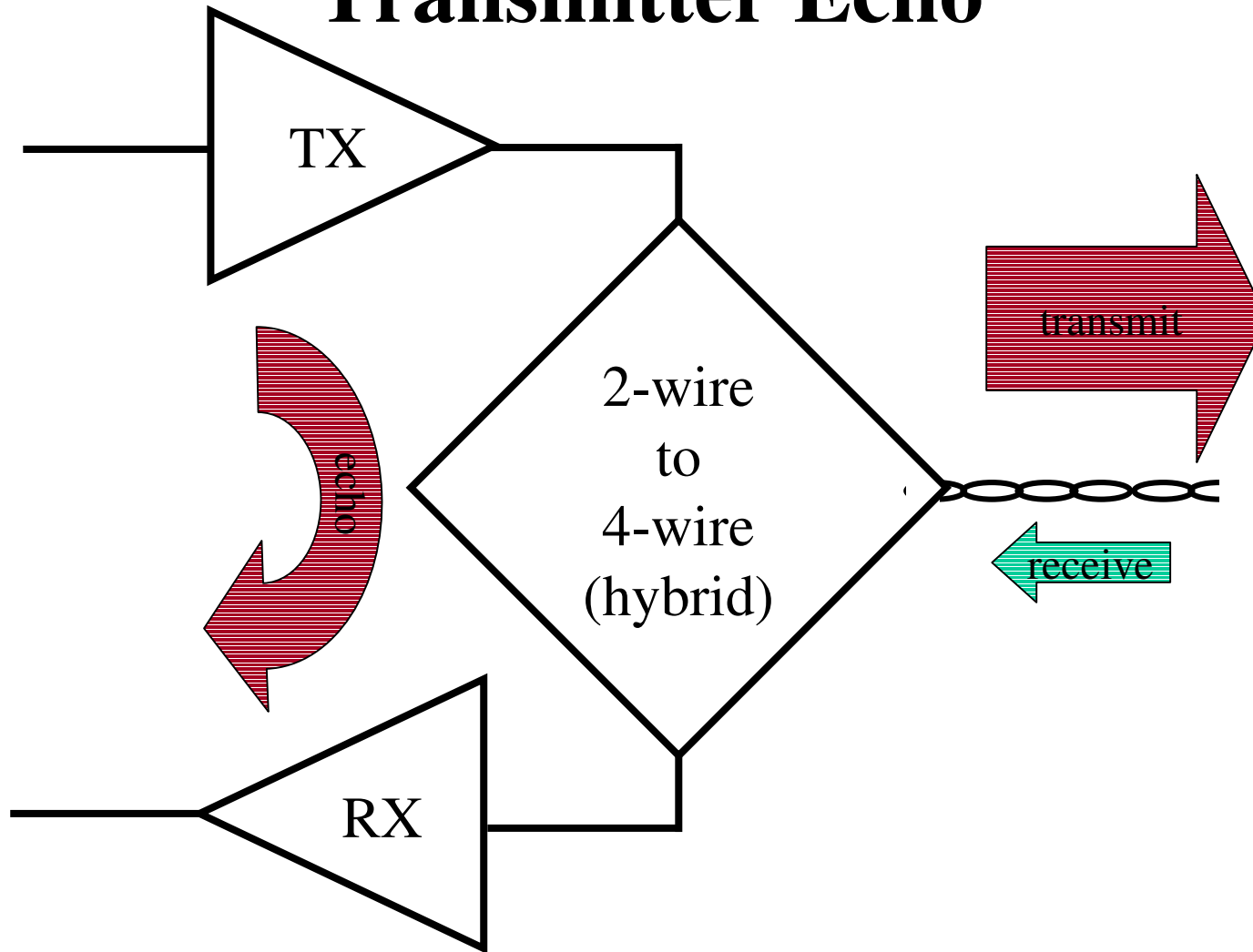
Active Termination



$$Z_{in} = -\frac{V_{RX}}{I \Big|_{V_{TX}=0}} - Z_L = -\frac{V_{RX}}{-\frac{V_{RX}}{R+Z_L+gR}} - Z_L = (1+g)R$$

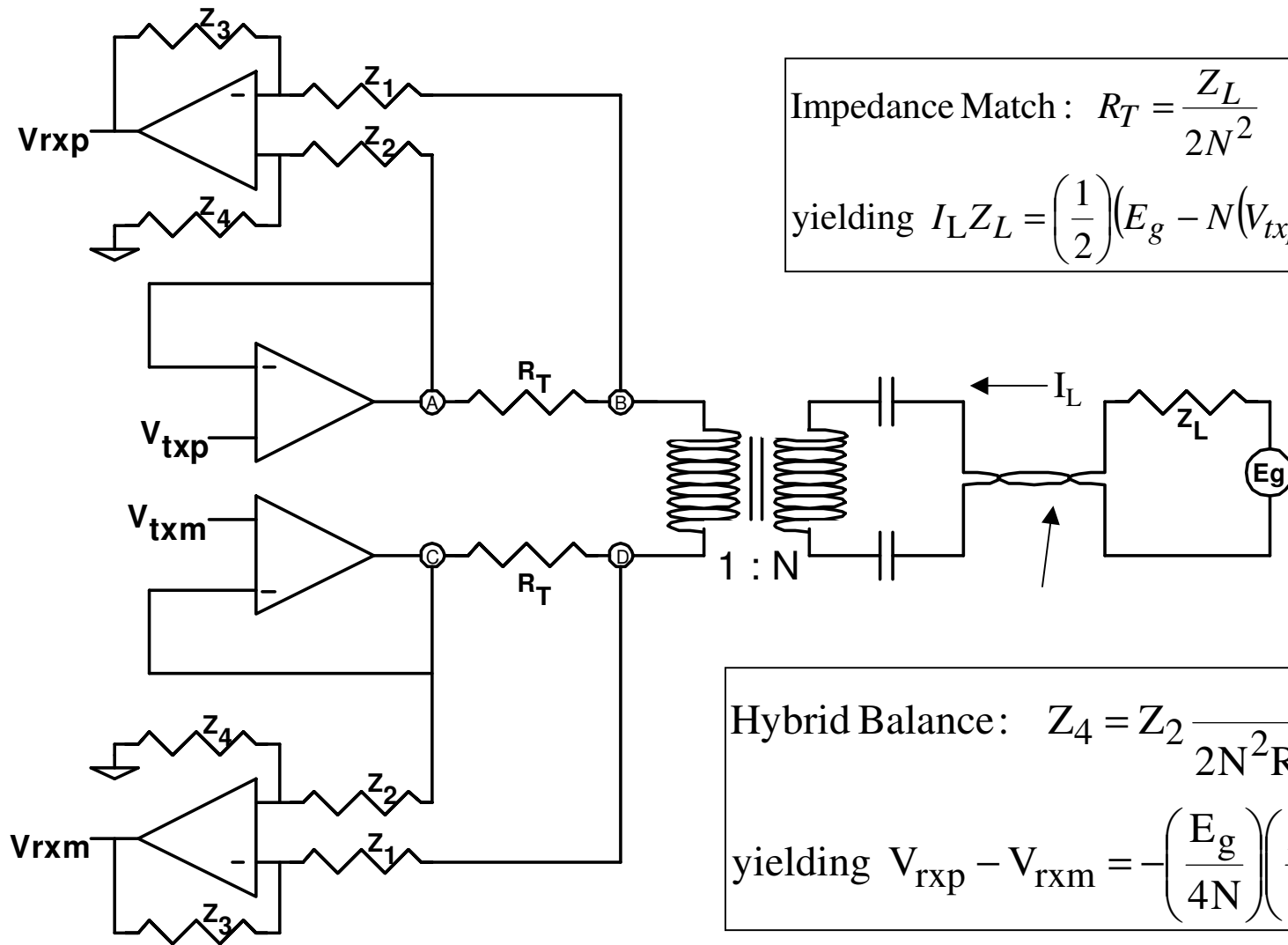
- Reduces driver power supply voltage requirement
- Downside: Reduces receiver gain by $20\text{Log}_{10}[(1+g)]$

Transmitter Echo



On long loops, the echo power is greater than the receive power

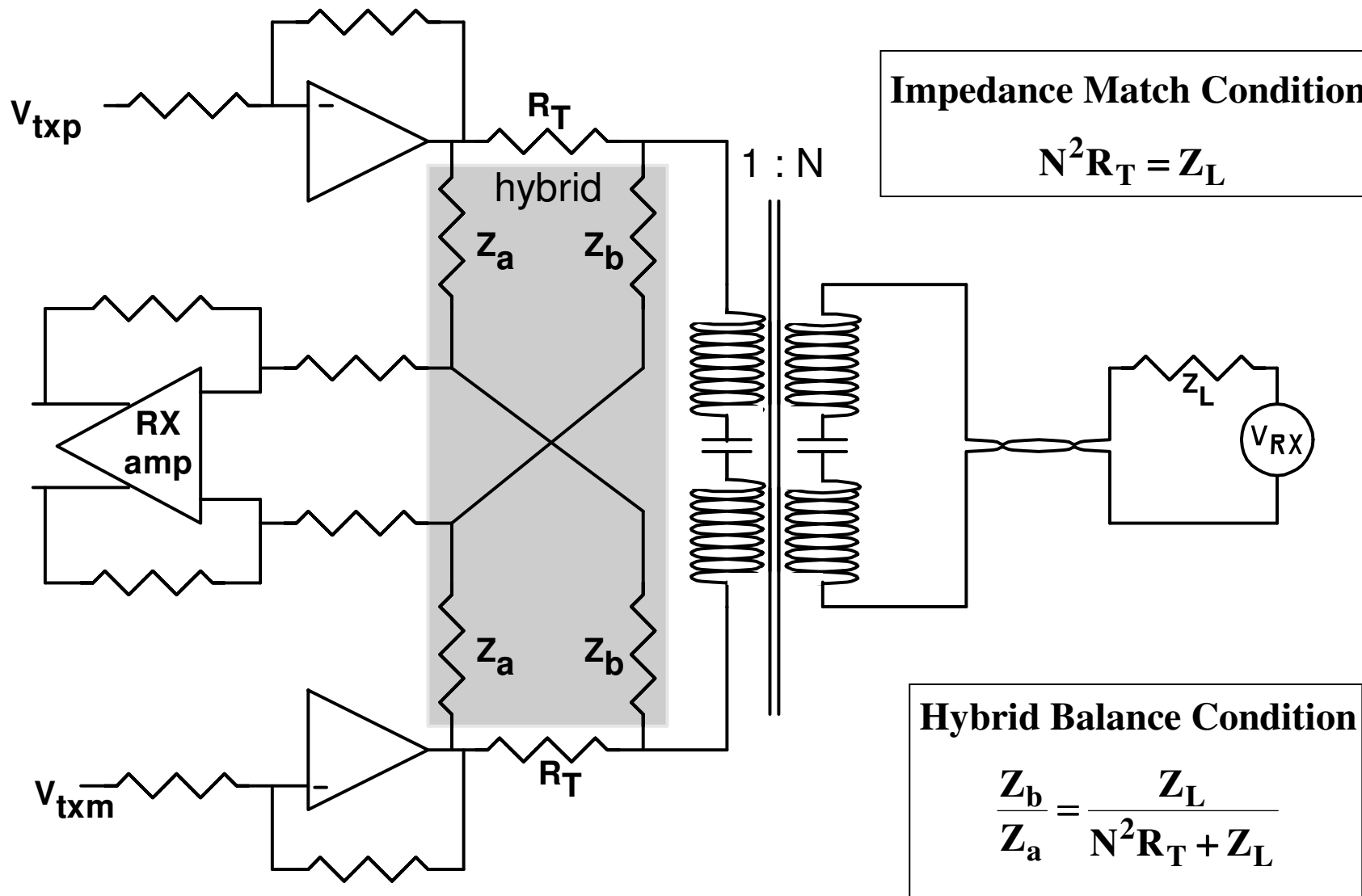
2nd Order High-Pass with Passive Termination and Hybrid



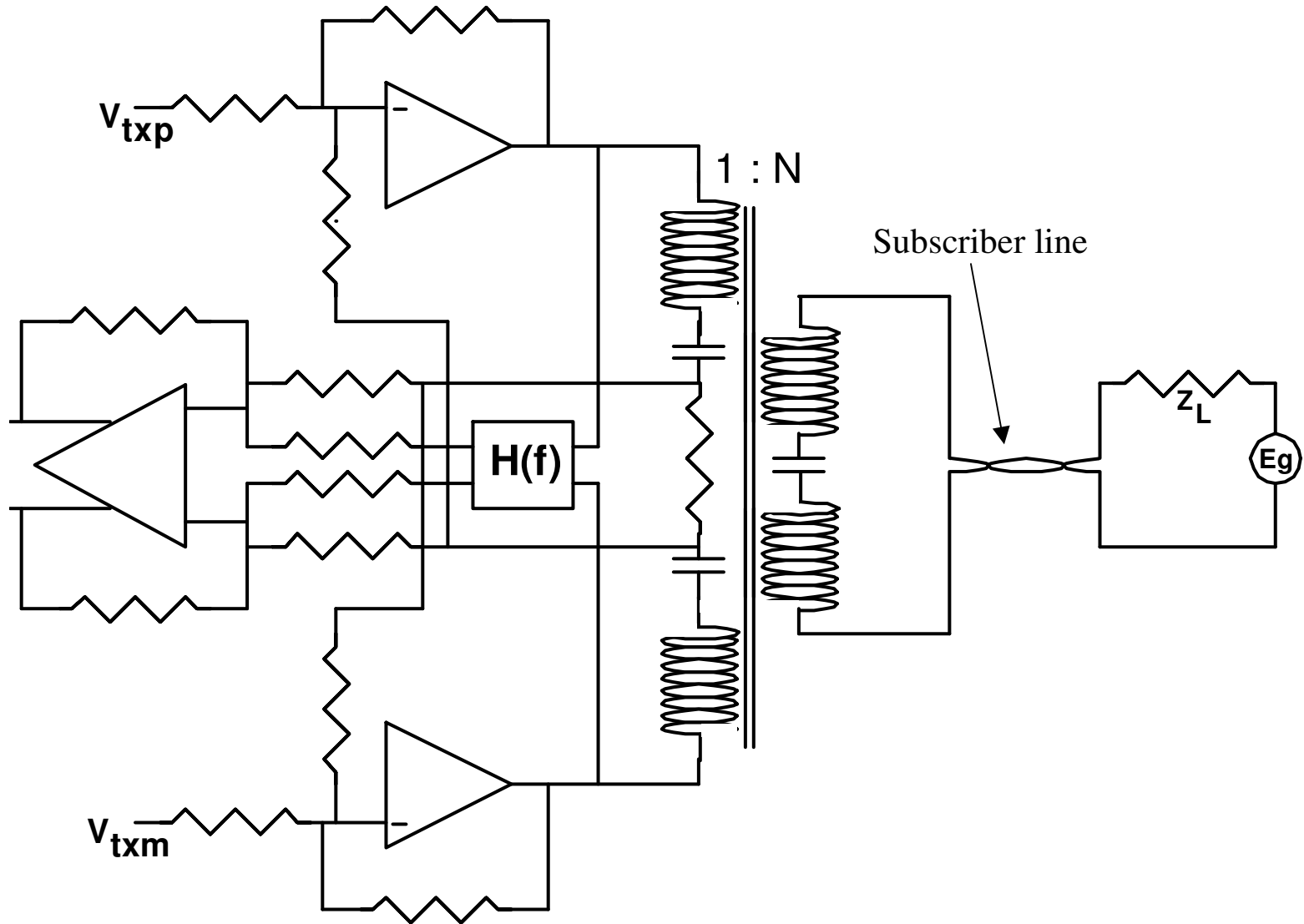
Impedance Match: $R_T = \frac{Z_L}{2N^2}$
 yielding $I_L Z_L = \left(\frac{1}{2}\right)(E_g - N(V_{txp} - V_{txm}))$

Hybrid Balance: $Z_4 = Z_2 \frac{Z_3 Z_L}{2N^2 R_T (Z_1 + Z_3) + Z_L}$
 yielding $V_{rxp} - V_{rxm} = -\left(\frac{E_g}{4N}\right)\left(\frac{Z_3}{Z_1}\right)$

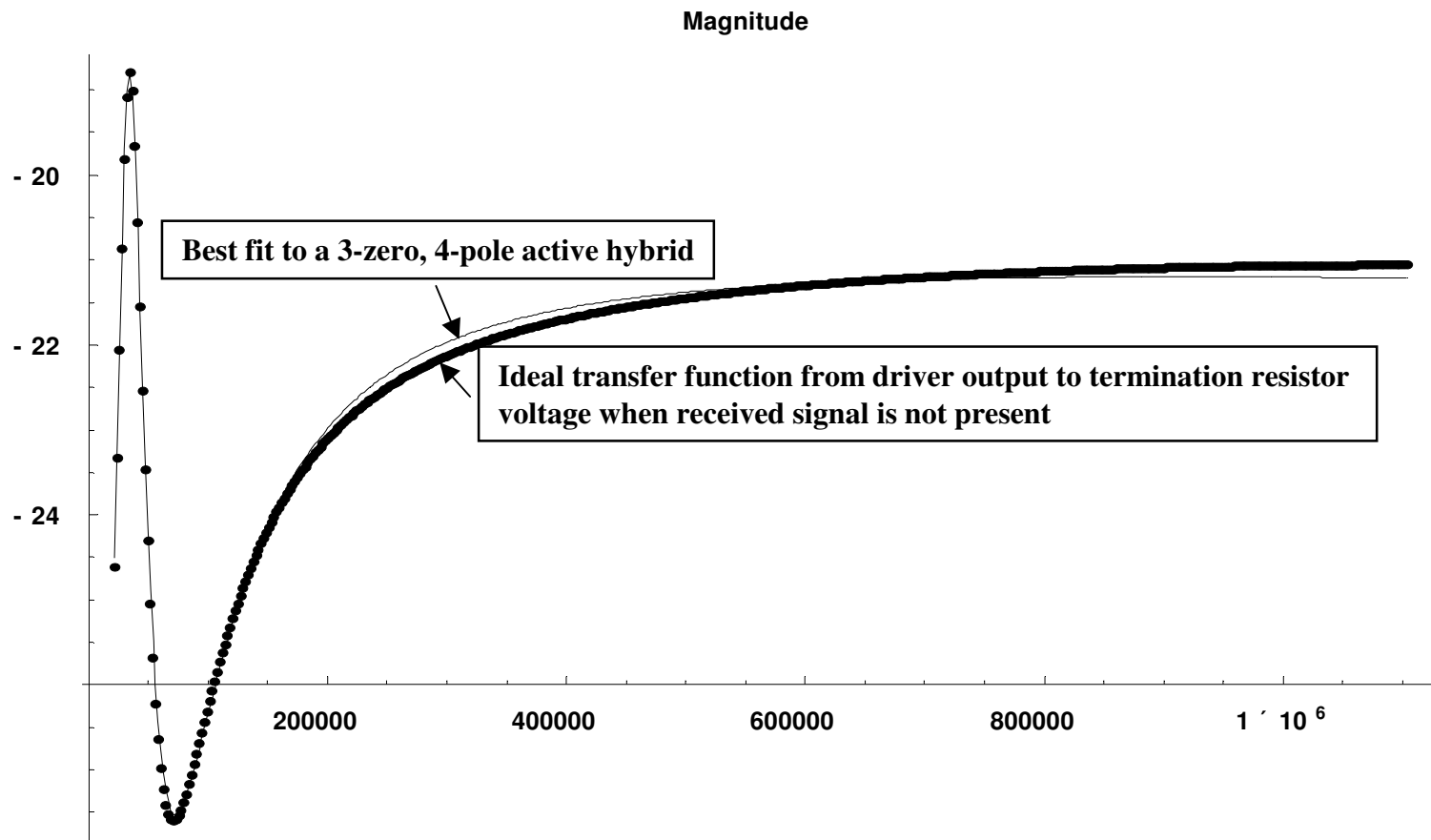
3rd Order High-Pass With Passive Termination and Hybrid



3rd Order High-Pass With Active Termination and Hybrid



Active Hybrid Transfer Function



Hybrid Rejection Definitions

$$R_H(\text{exp}) = 20\text{Log}_{10} \left[\frac{\text{transmitter signal at tip/ring}}{\text{transmitter signal at receiver amplifier output}} \right]$$

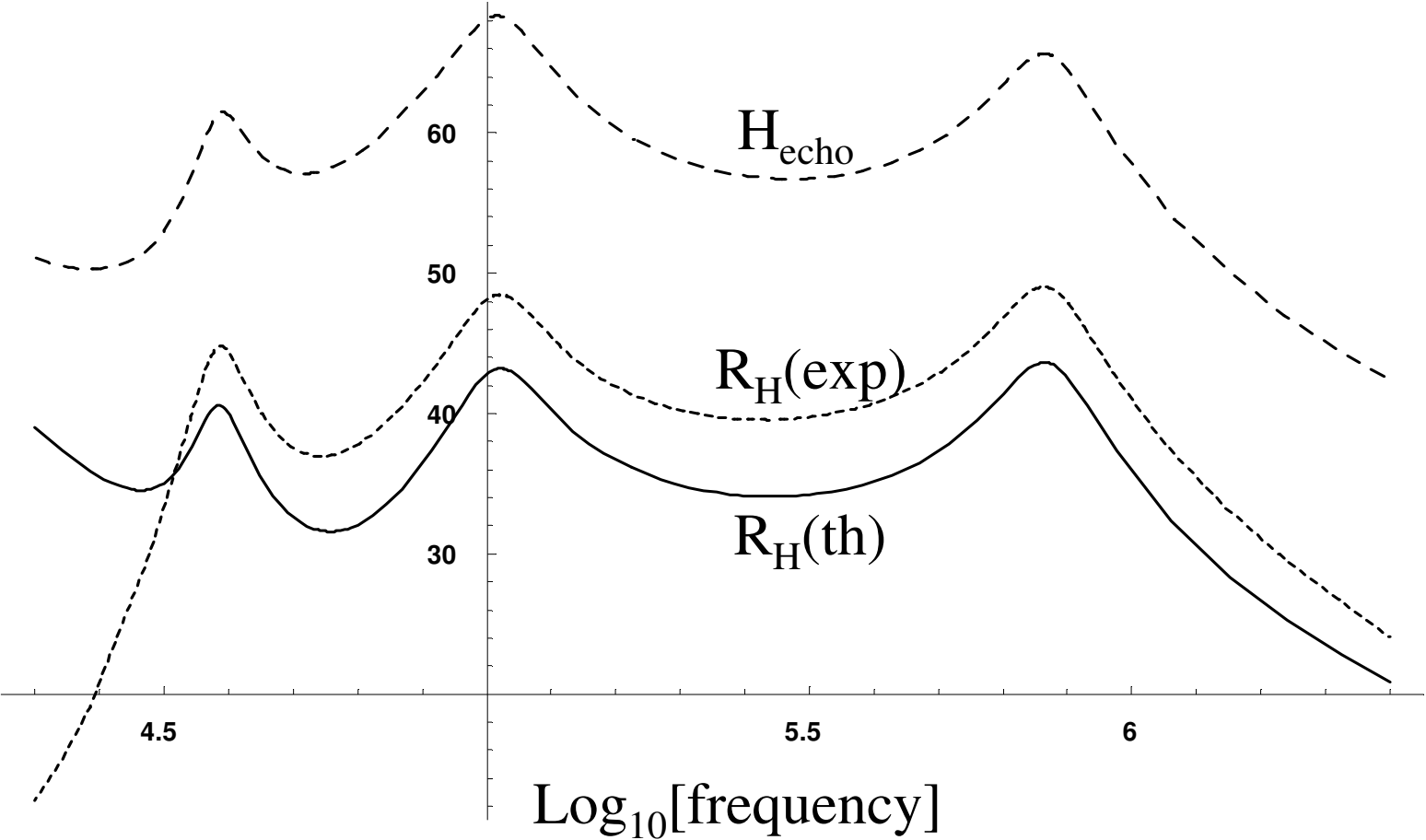
received signal gain from tip/ring to receiver amplifier output

$$R_H(\text{th}) = 20\text{Log}_{10} \left[\frac{\text{transmitter signal at tip/ring when hybrid is removed}}{\text{transmitter signal at tip/ring when hybrid is present}} \right]$$

Echo Response

$$H_{\text{Echo}} = 20\text{Log}_{10} \left[\frac{\text{transmitter signal at driver output}}{\text{transmitter signal at receiver amplifier}} \right]$$

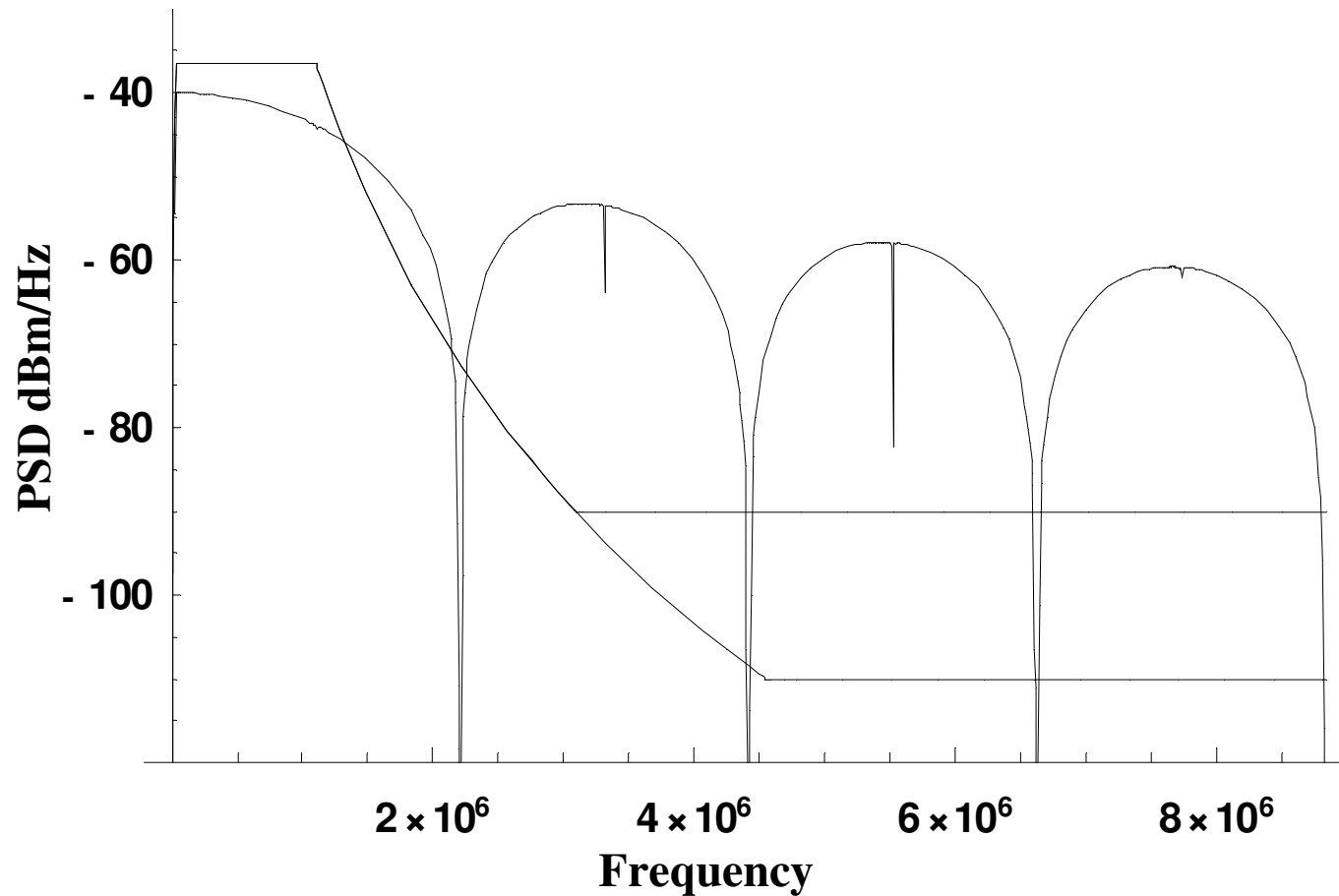
Hybrid Rejection Example



Transmitter Signal Path

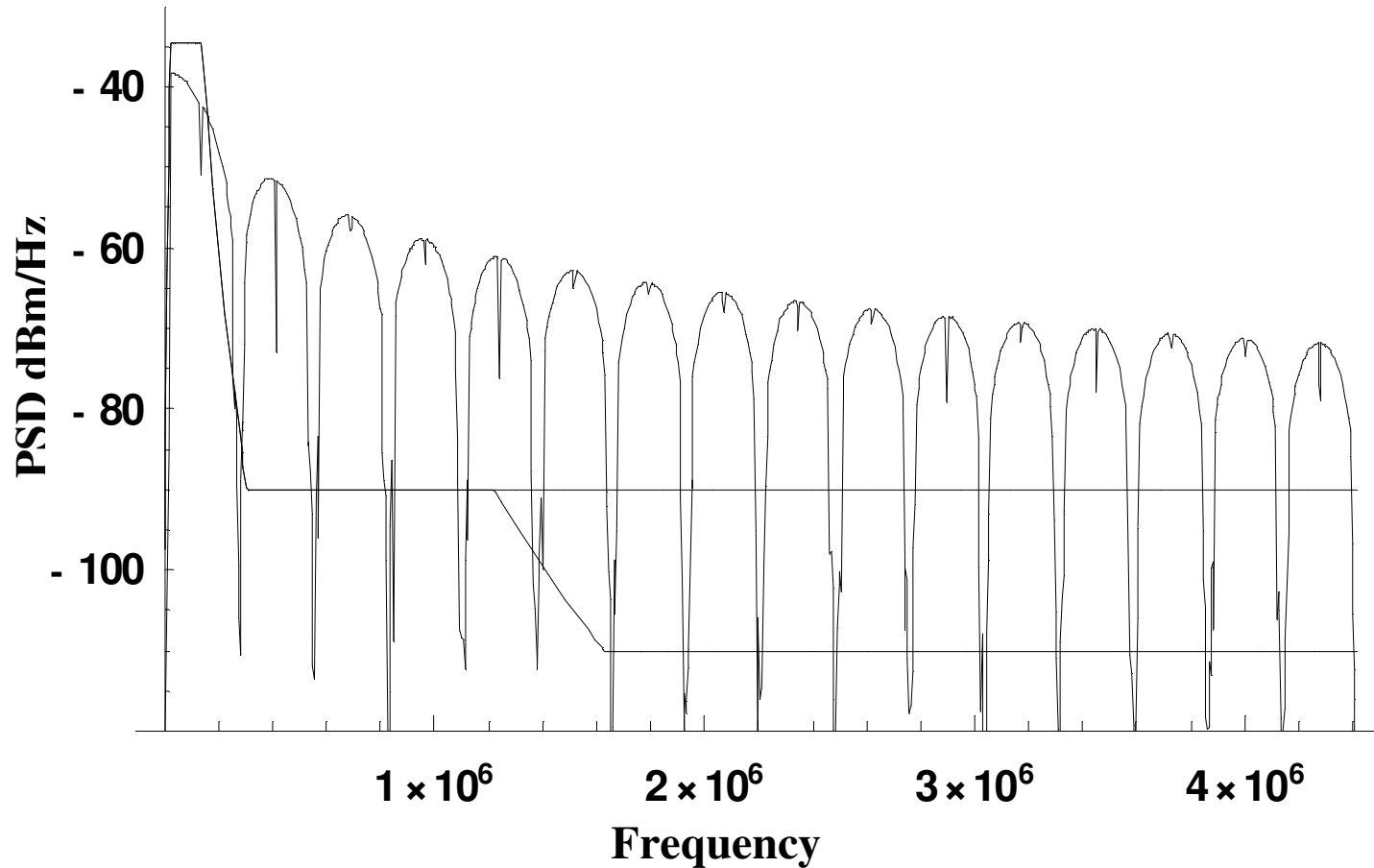
- **Over-sampling**
- **Managing PAR**
- **MTPR requirement**
- **Line Drivers**

Downstream PSD With Minimum Sample Rate



- Conversion of downstream signal to continuous-time at 2208kS/sec produces in-band droop and significant standard's non-compliance.

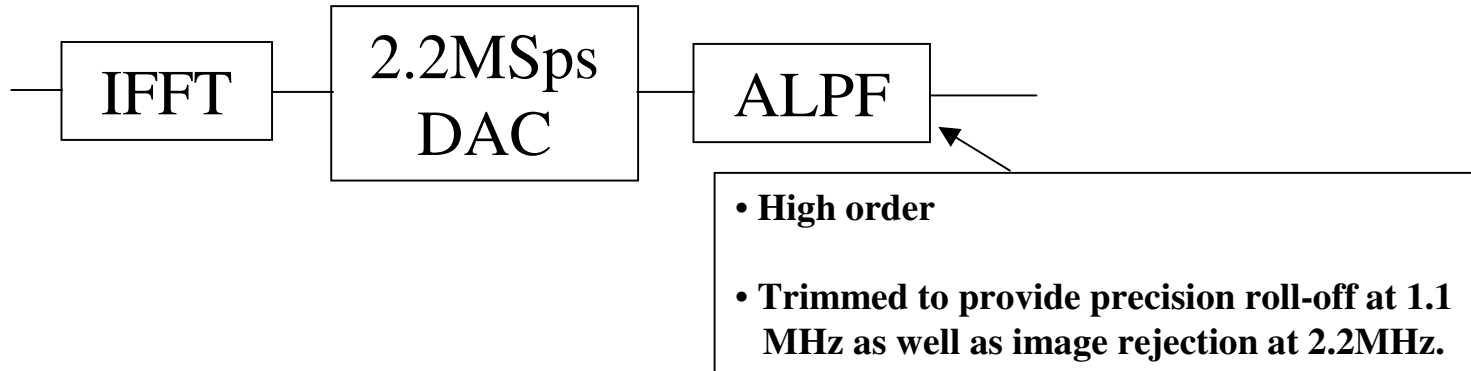
Upstream PSD With Minimum Sample Rate (276kS/sec)



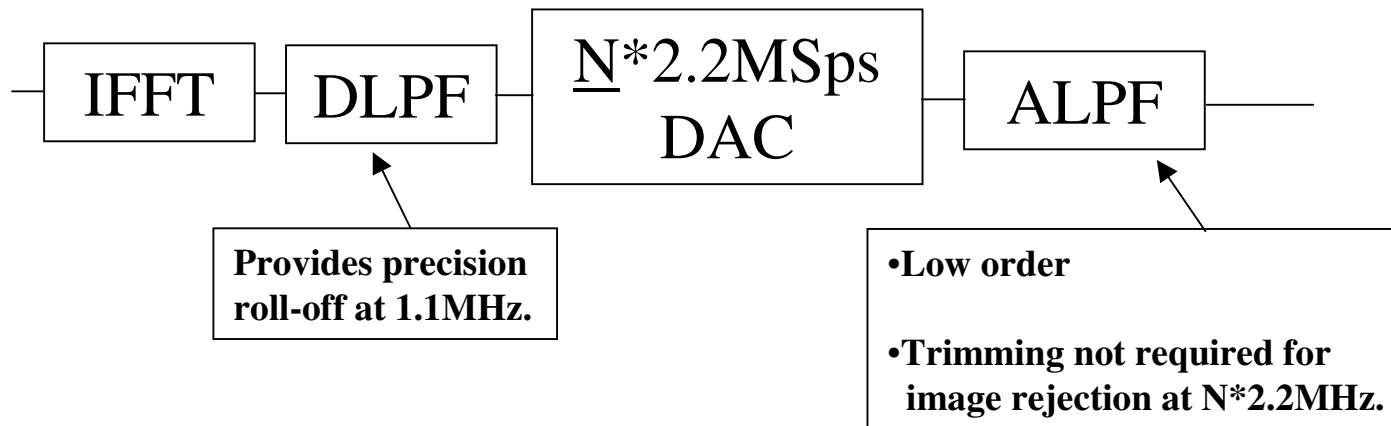
- Conversion of upstream signal to continuous-time at 276kS/sec produces in-band droop and significant standard's non-compliance.

Low-Pass Reconstruction Filter Architectures

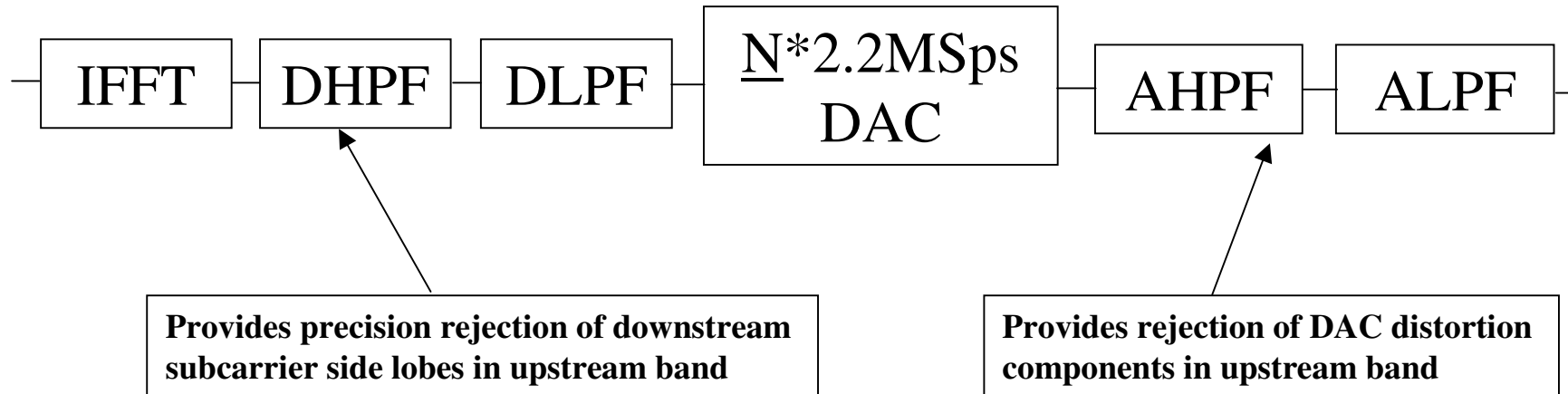
(A) Nyquist rate DAC (Analog filter)



(B) Over-sampled DAC (Digital/Analog filter combination)

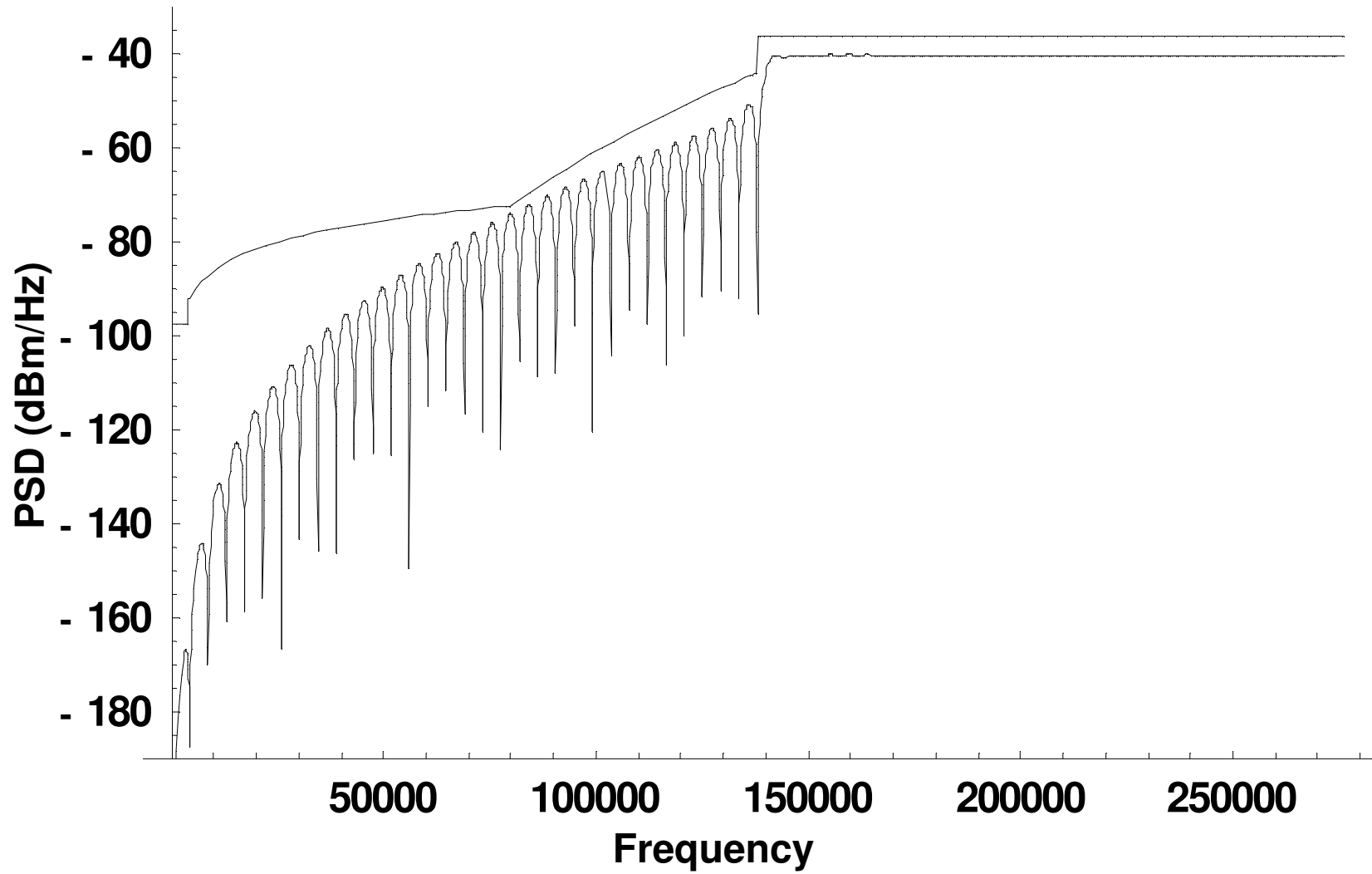


Helping Out the Central Office Hybrid

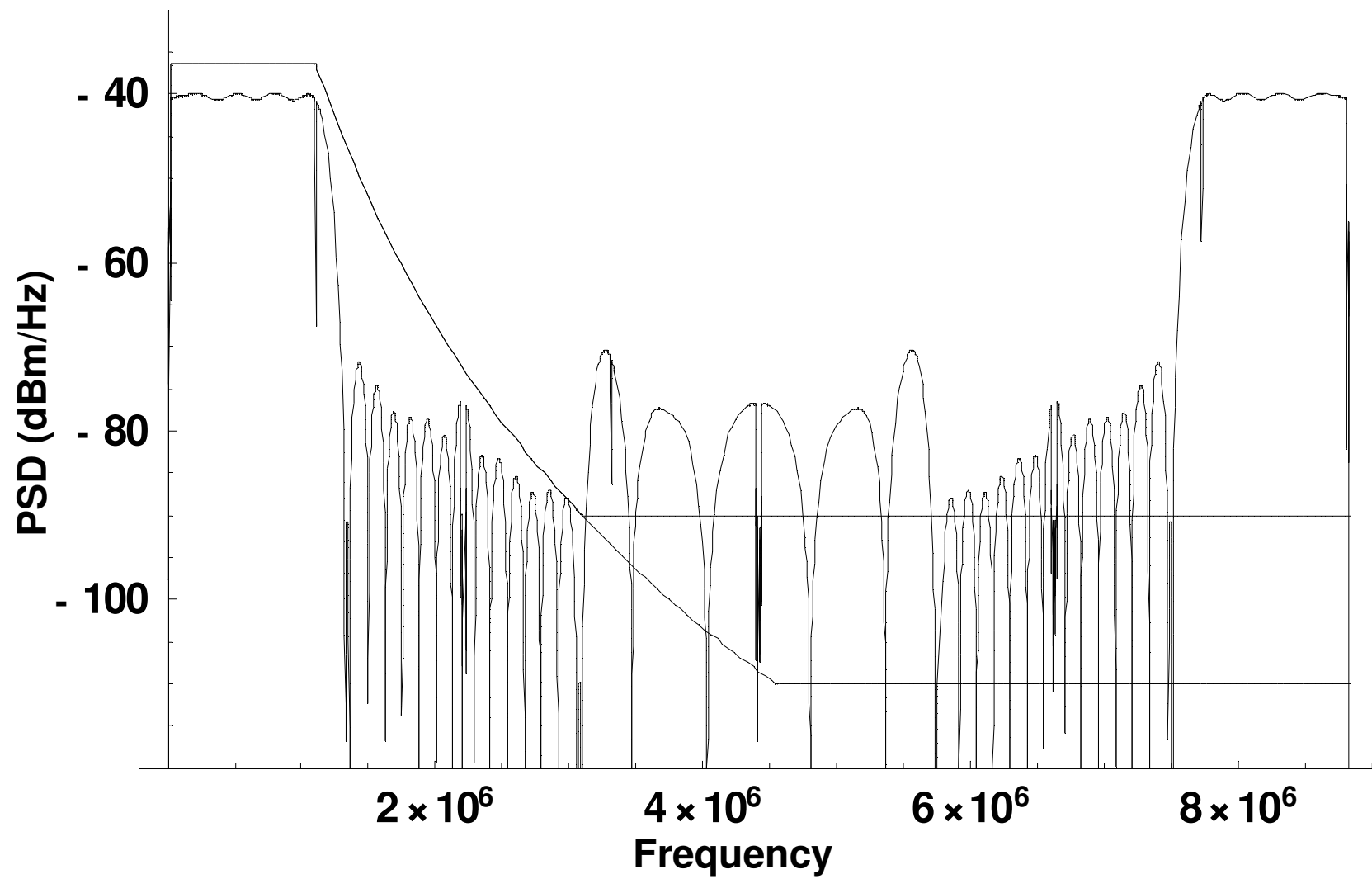


Digital High-Pass Output Spectrum

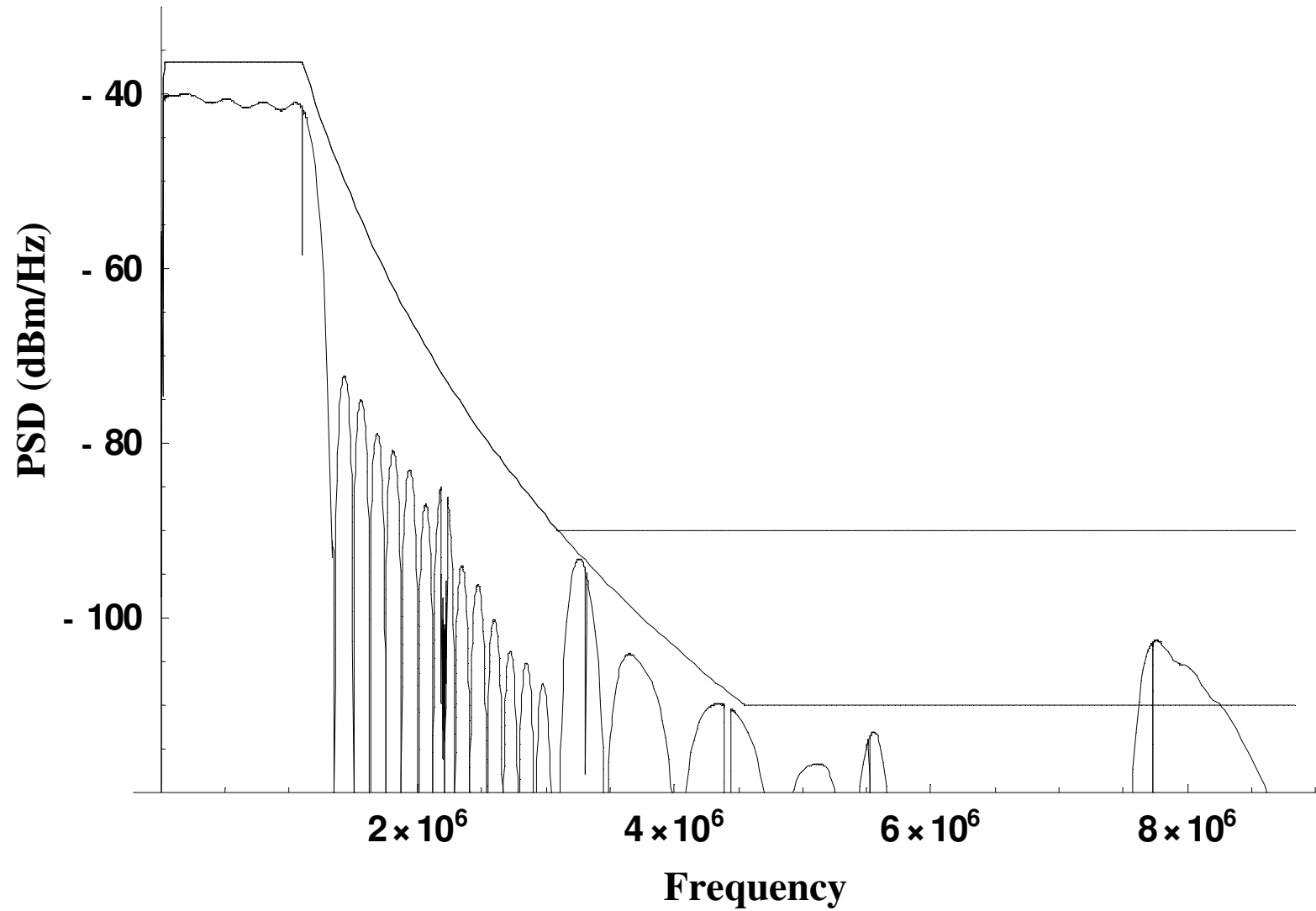
(downstream bin 32-255 employed)



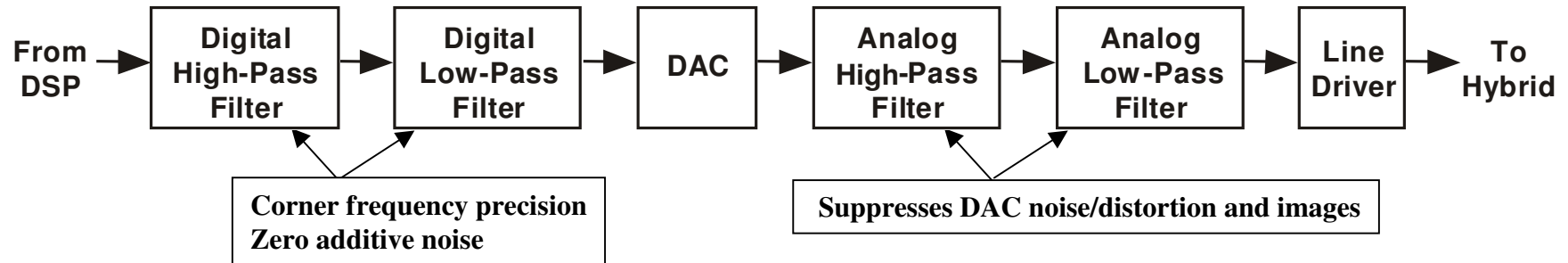
Digital Low-Pass Filter Output Spectrum



Analog Low-Pass Filter Output Spectrum



Transmitter Template



- **DHPF**

- High order DHPF is critical to downstream transmitter signal suppression in FDD modems
- Reduced-NEXT compliance in echo-canceling modems employing non-overlapping spectra

- **DLPF**

- High order is critical to upstream transmitter signal suppression in FDD modems
- Interpolating stages increase sample rate, reducing signal droop and relaxing analog low-pass

- **DAC**

- Precision (<12 effective bits) depends upon analog filtering, hybrid rejection and receiver sensitivity

- **AHPF**

- Suppresses DAC noise/distortion in upstream band in FDD central office modems.

- **ALPF**

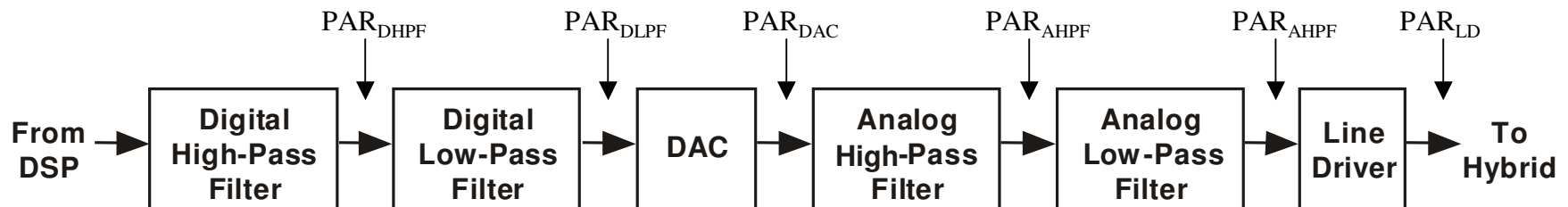
- Eliminates signal images centered at multiples of DAC sample rate.
- Suppresses DAC noise/distortion in downstream band in FDD client modems.

- **Line Driver**

- High voltage technology.
- Very low distortion required.

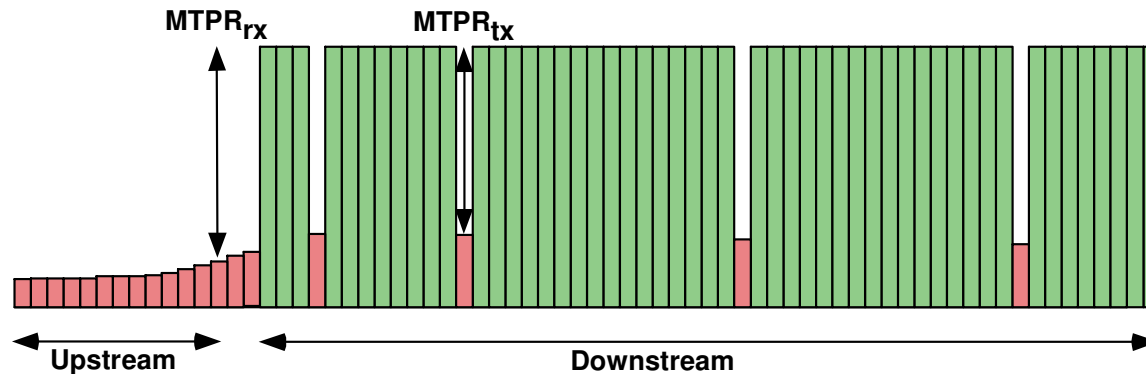
Managing Peak Signal to Average Signal Ratio

- Bit Error Rate is proportional to the frequency of signal clipping
- Clipping rate of gaussian signal is determined by PAR
- PAR is determined by circuit NOT a property of signal
- Managing PAR in digital or analog domains – node by node
 - Usually desirable to limit the number of clipping nodes to one (driver)
 - For given signal swing (volts or bits), PAR is increased (decreased) by decreasing (increasing) signal power
 - For given signal power, PAR is increased (decreased) by increasing (decreasing) swing (volts or bits)



Missing Tone Power Ratio Test

- Equivalent of spurious free dynamic range in narrow band systems



FDD (EC) Central Office Example (frequency-independent echo response)

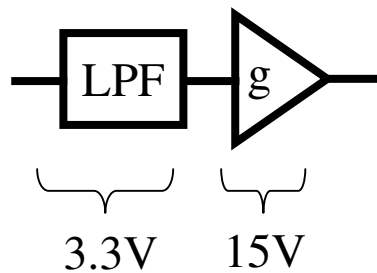
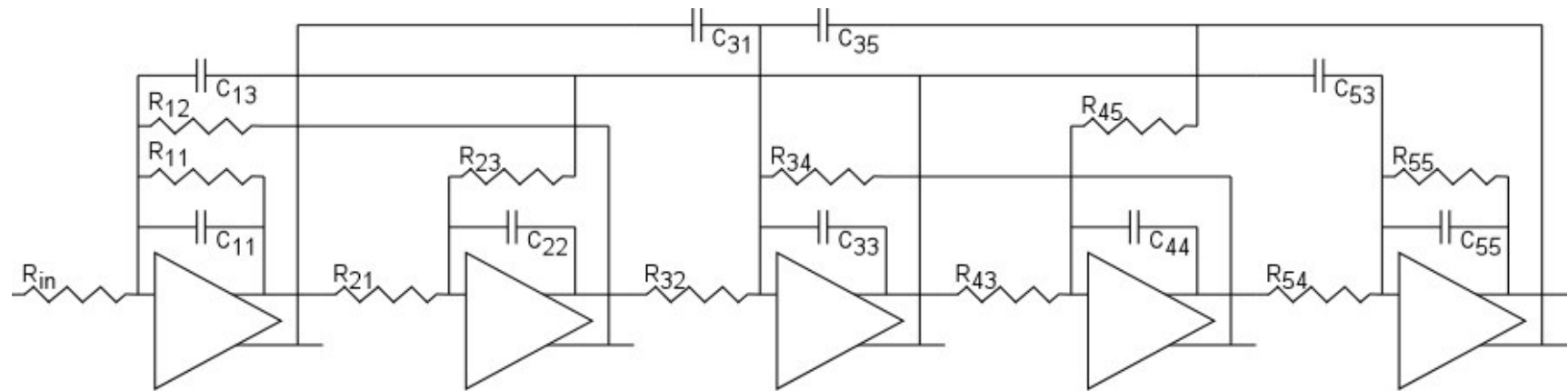
$MTPR_{tx}=65$ (75)

$MTPR_{rx}=75$ (75)

Virtue of High Voltage IC Processes

Client Reconstruction Low-Pass Filter Example

(138kHz corner frequency, -140dBm/Hz noise in downstream band)



3.3V Process

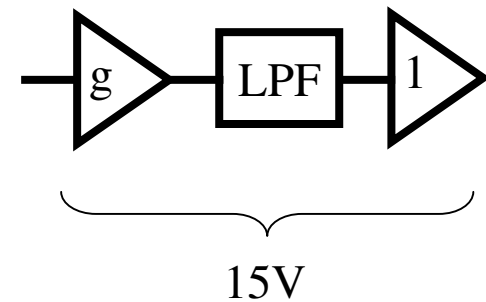
C11= 89.6pF
 C13= 428.pF
 C22= 1157pF
 C33= 3292pF
 C31= 358.pF
 C35= 1142pF
 C44= 7122pF
 C55= 10351pF
 C53= 5710pF

total = 29.6nF

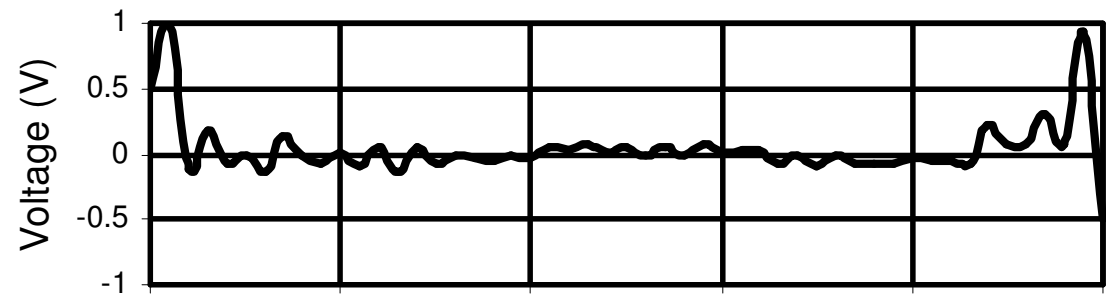
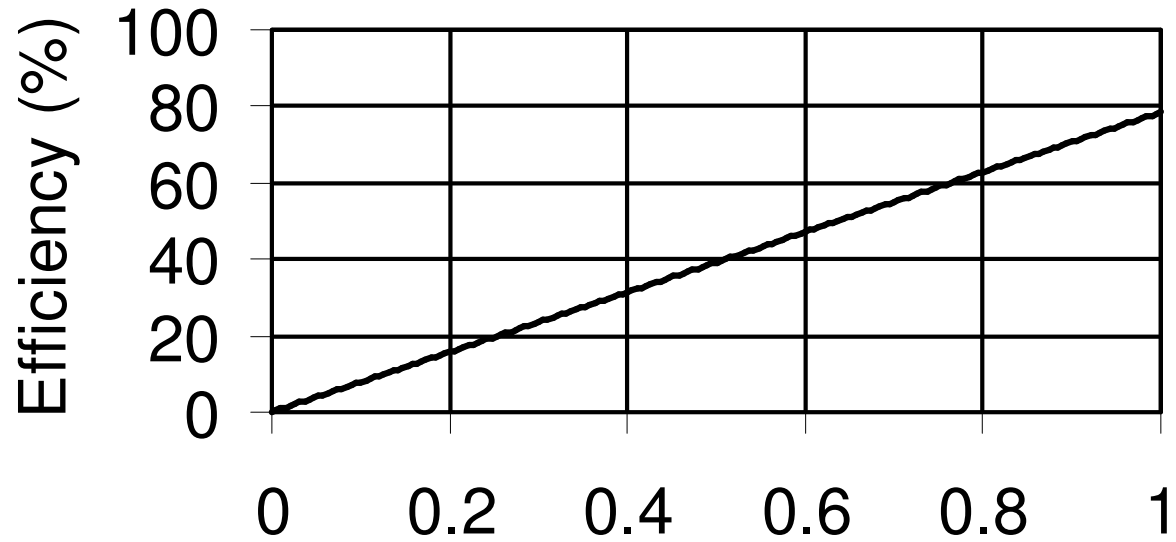
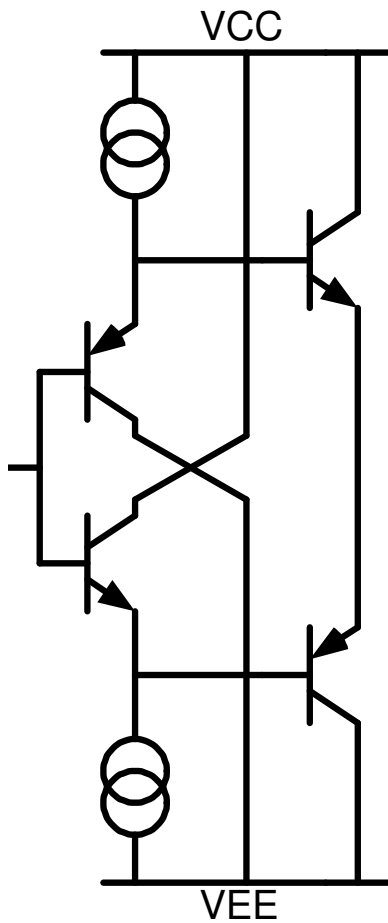
15V Process

C11= 2.36pF
 C13= 11.3pF
 C22= 30.4pF
 C33= 86.6pF
 C31= 9.43pF
 C35= 30.0pF
 C44= 187.pF
 C55= 272.pF
 C53= 150.pF

total = 779pF

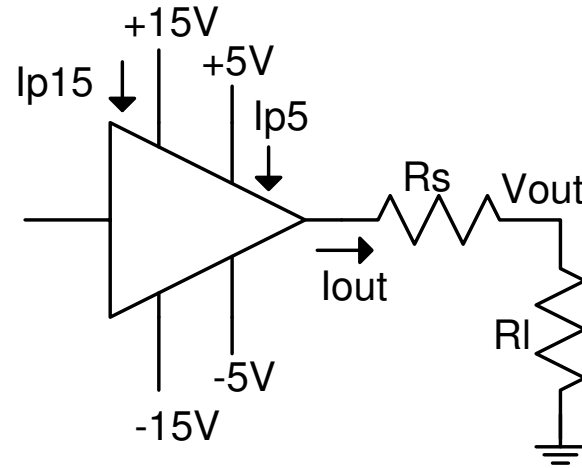


Class AB Output Stage

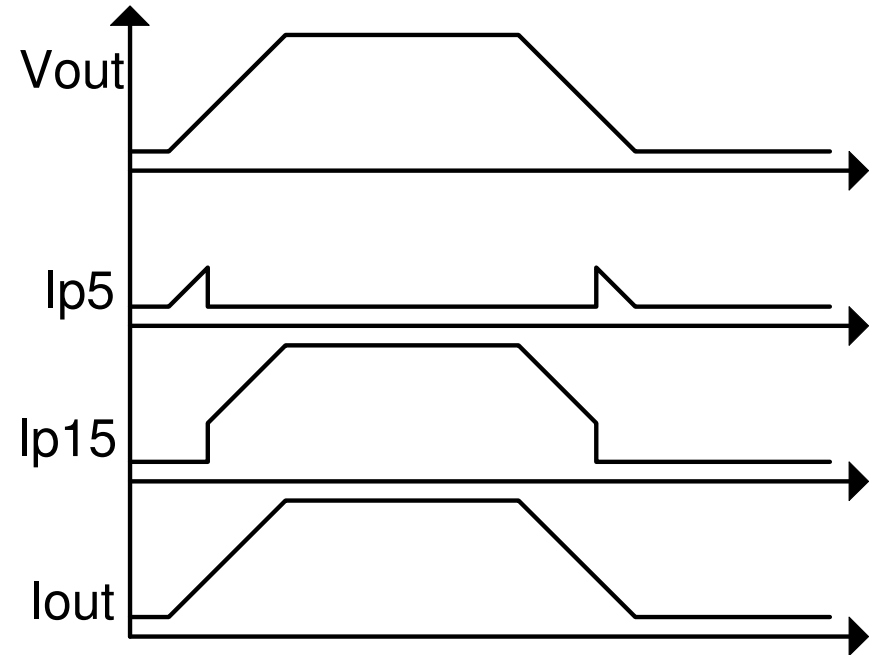


Time
<20% efficiency

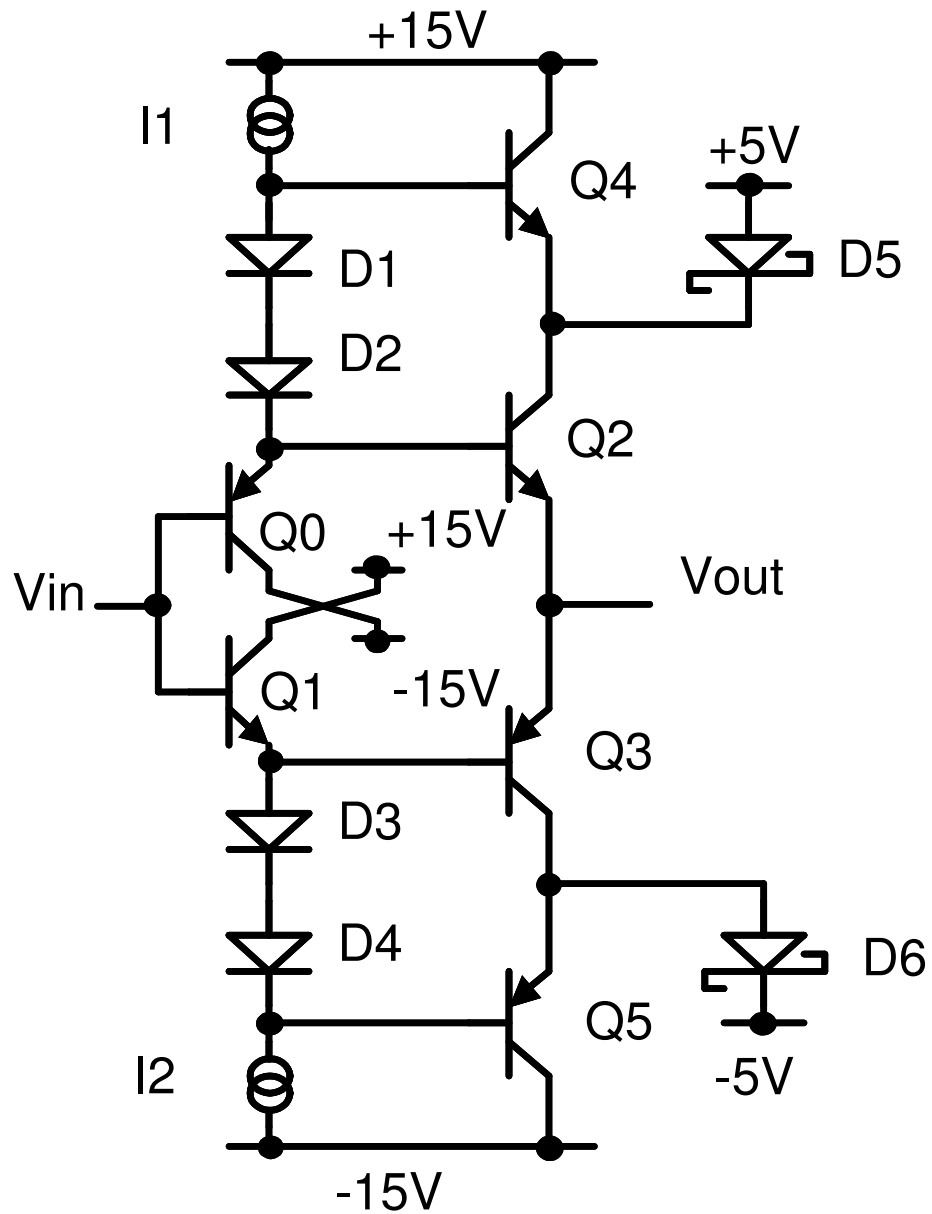
Class G Topology



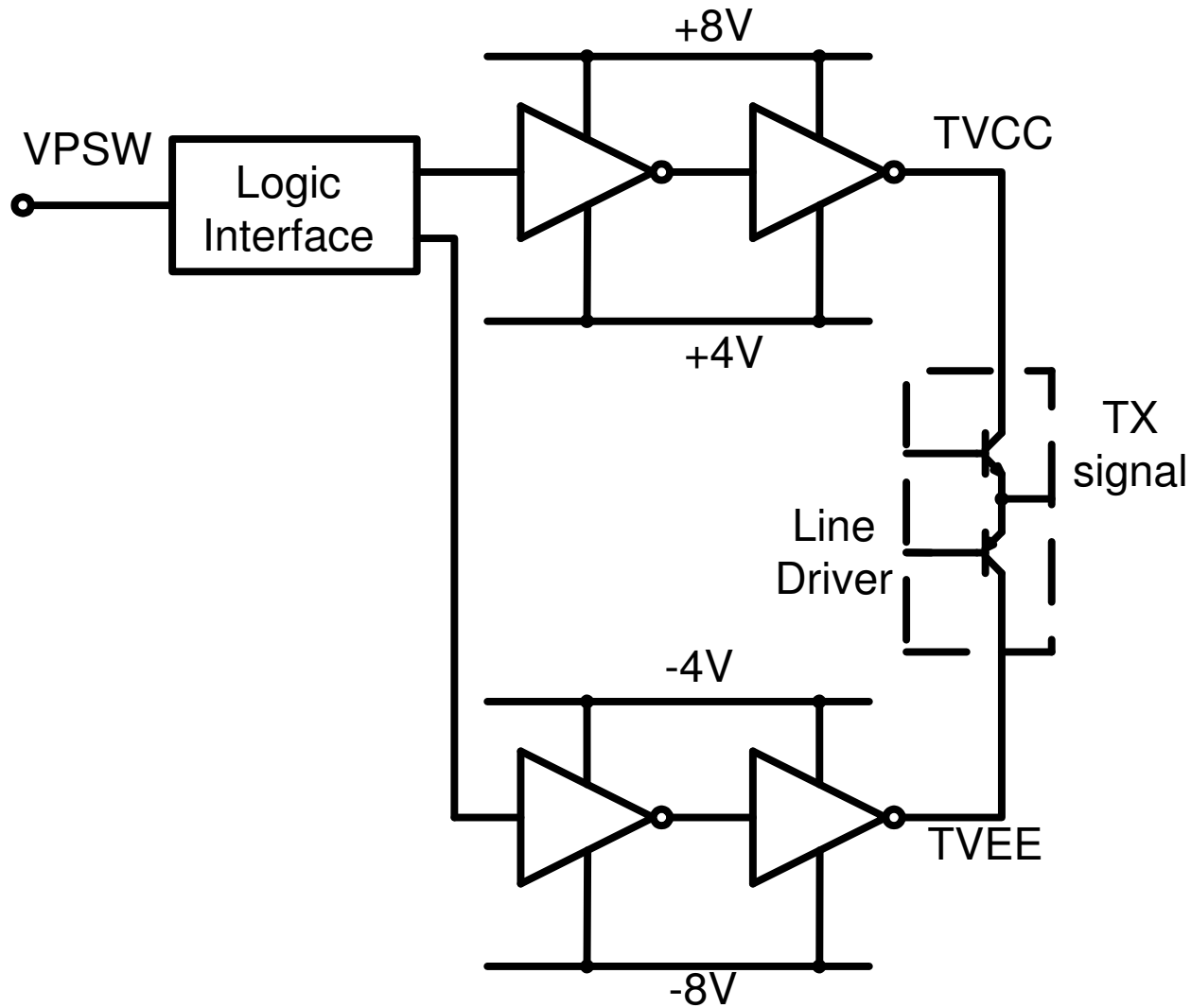
- **Multiple supply output stage**
- **For V_{OUT} low, current comes from +5 V**
- **For V_{OUT} high, current comes from +15 V**
- **Current is mostly drawn from low supply**
- **Challenge in DSL is low distortion at 1 MHz**



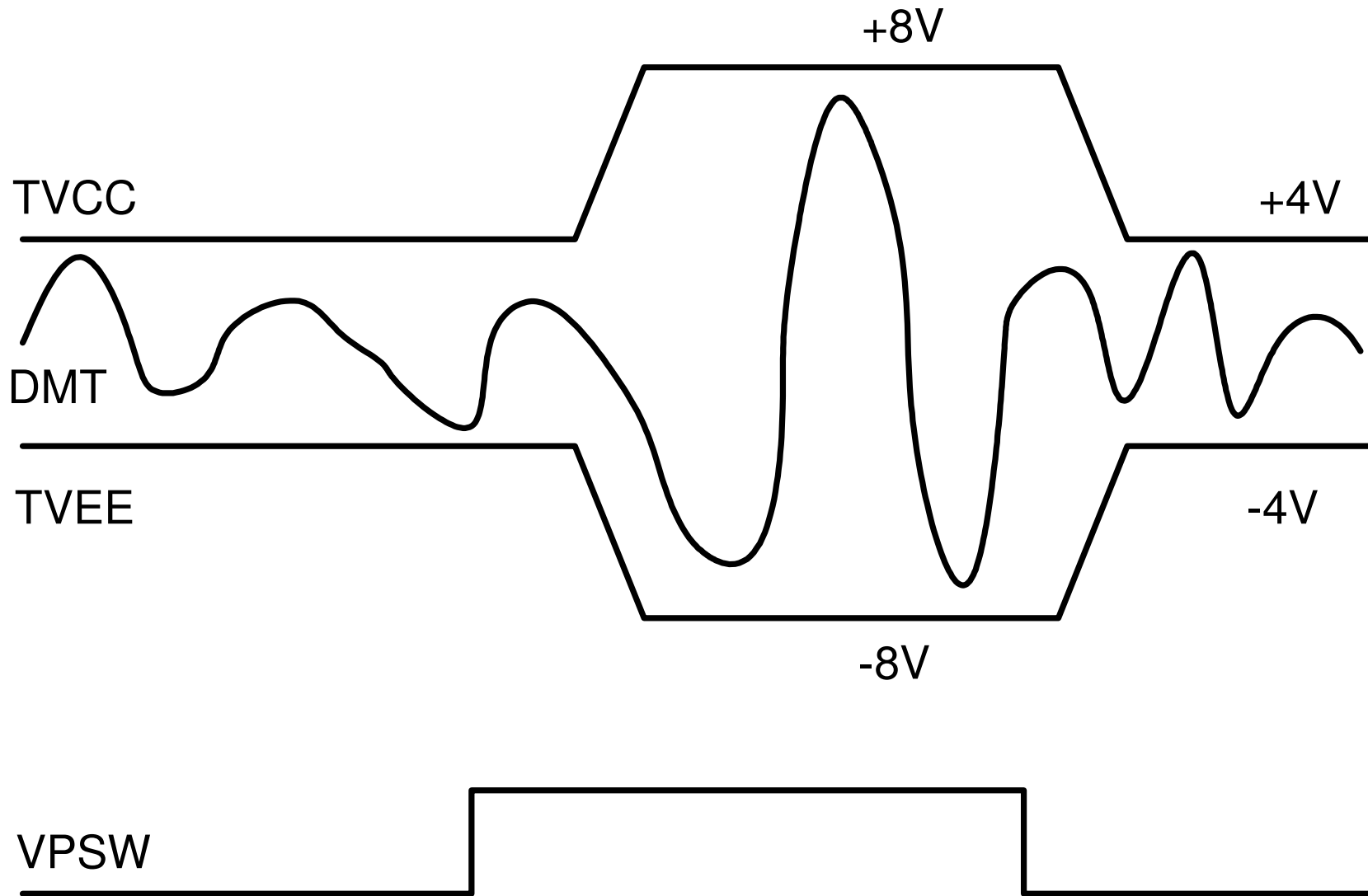
Continuous Class G Circuit



“Zero Overhead” Class G Concept – Block Diagram



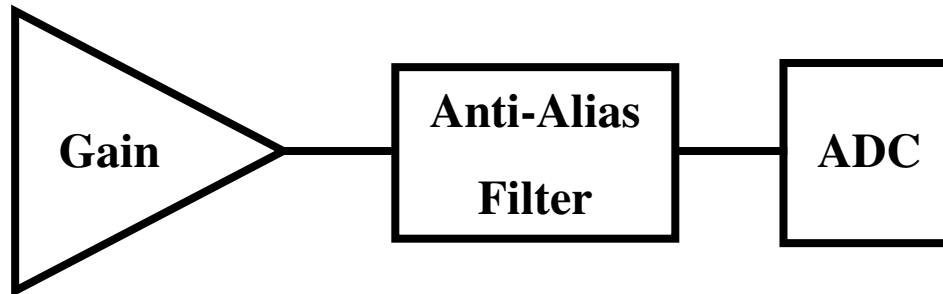
“Zero Overhead” Class G Concept - Waveforms



ZOCG Design Challenges

- Peak prediction
 - Analog signal blocks change peak positions and magnitudes
- Low voltage drop switches
 - Mus swing as close as possible to the rail
- Shoot through currents
 - Must minimize the time that switches to both supplies are on
- Switching edge coupling
 - Changing supply AC can couple into signal output

Receiver Signal Path

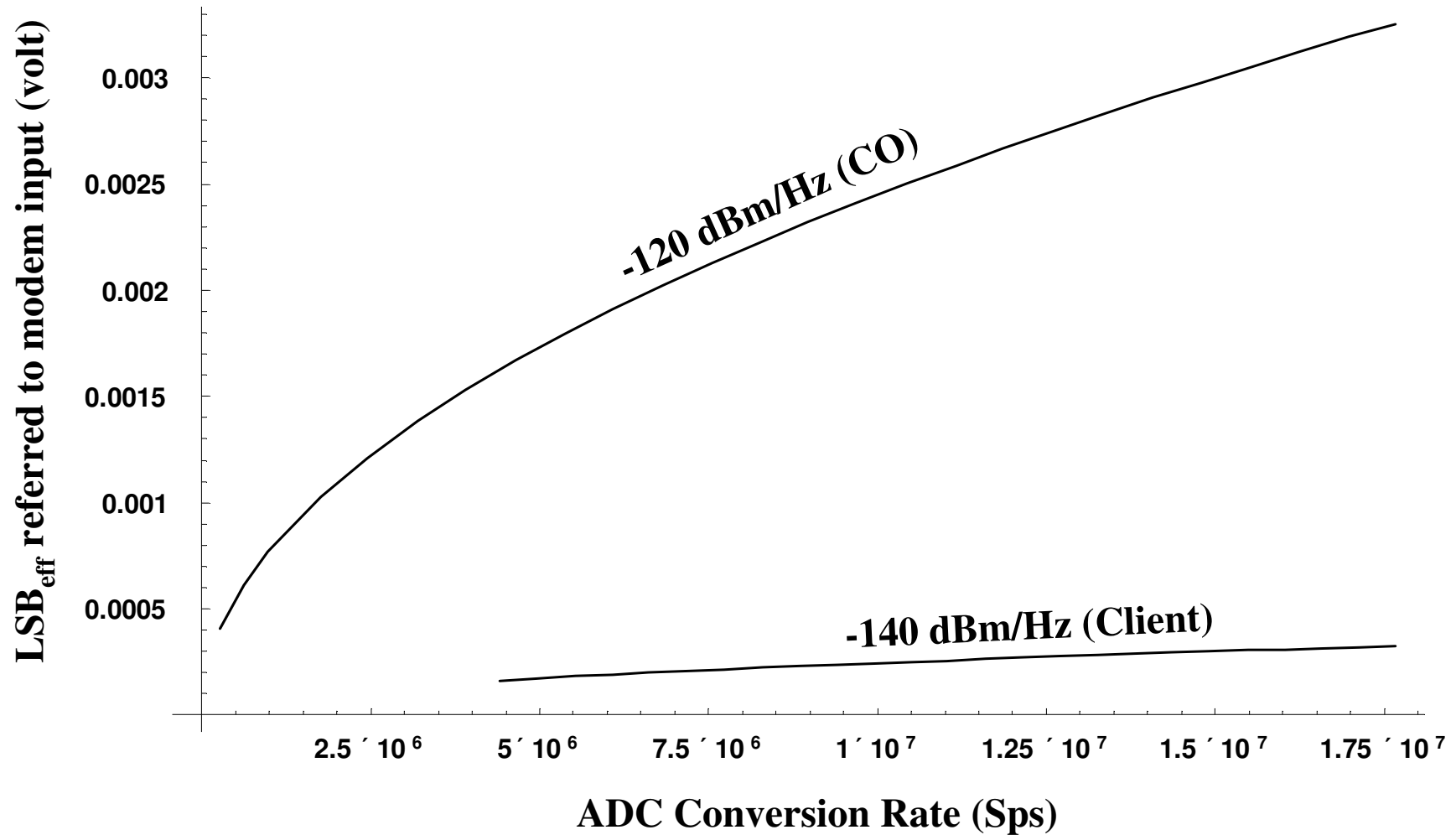


- **Signals**
- **Minimizing ADC requirements**
- **ADC precision**
- **PAR management**

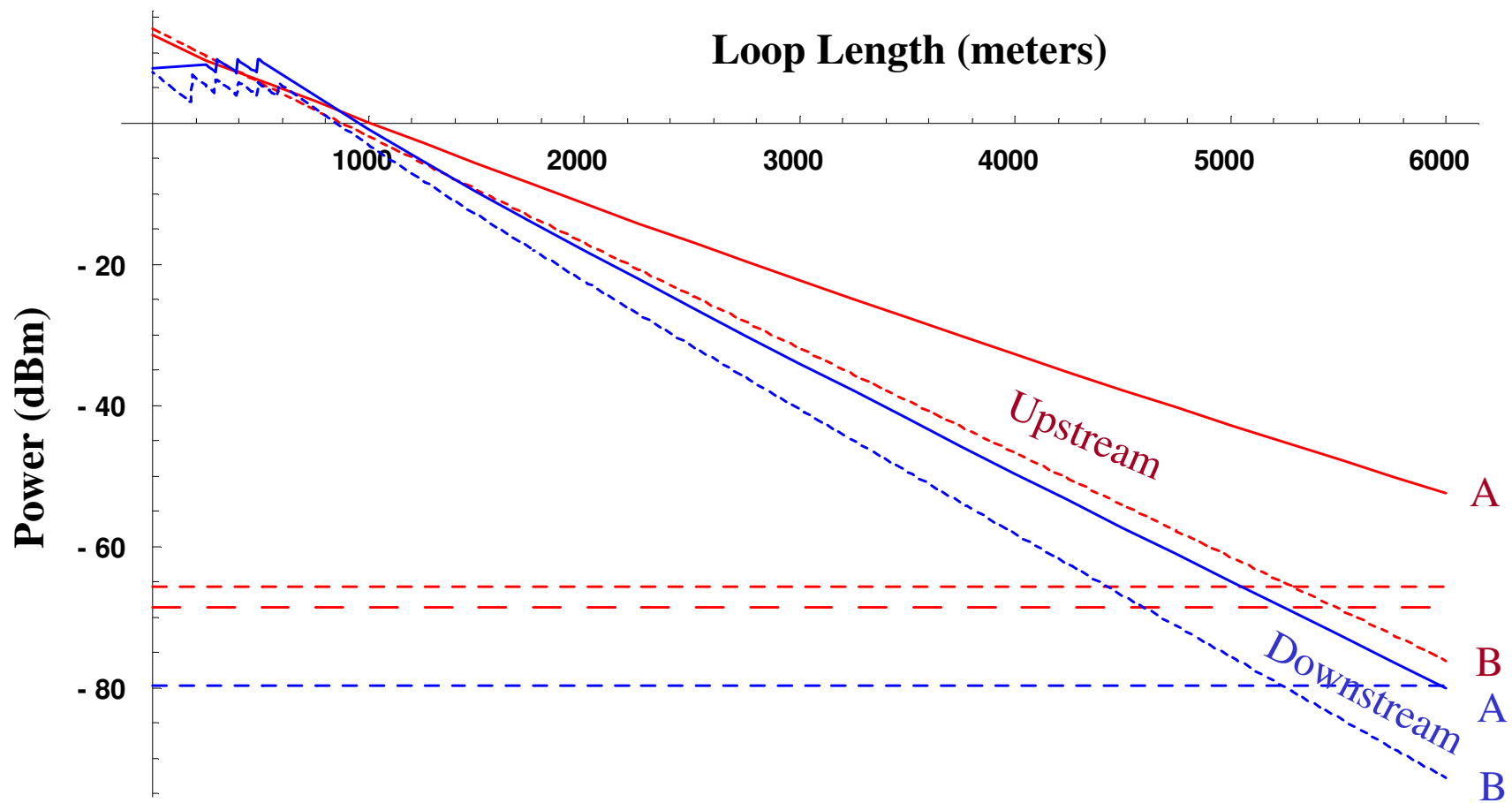
Receiver Noise/Distortion Floor

- **Inherent loop noise**
 - **Loop impedance is ~100 ohms, corresponding to <-173 dBm/Hz**
 - **Measured loop noise is usually in the neighborhood of -140 dBm/Hz**
 - **Central office noise is much higher**
 - **ISDN, T1, SHDSL,**
- **Typical noise floor targets for ADSL front ends**
 - **Central office: <-120 dBm/Hz at loop**
 - **Client: <-145 dBm/Hz at loop**

ADC Resolution Versus Conversion Rate

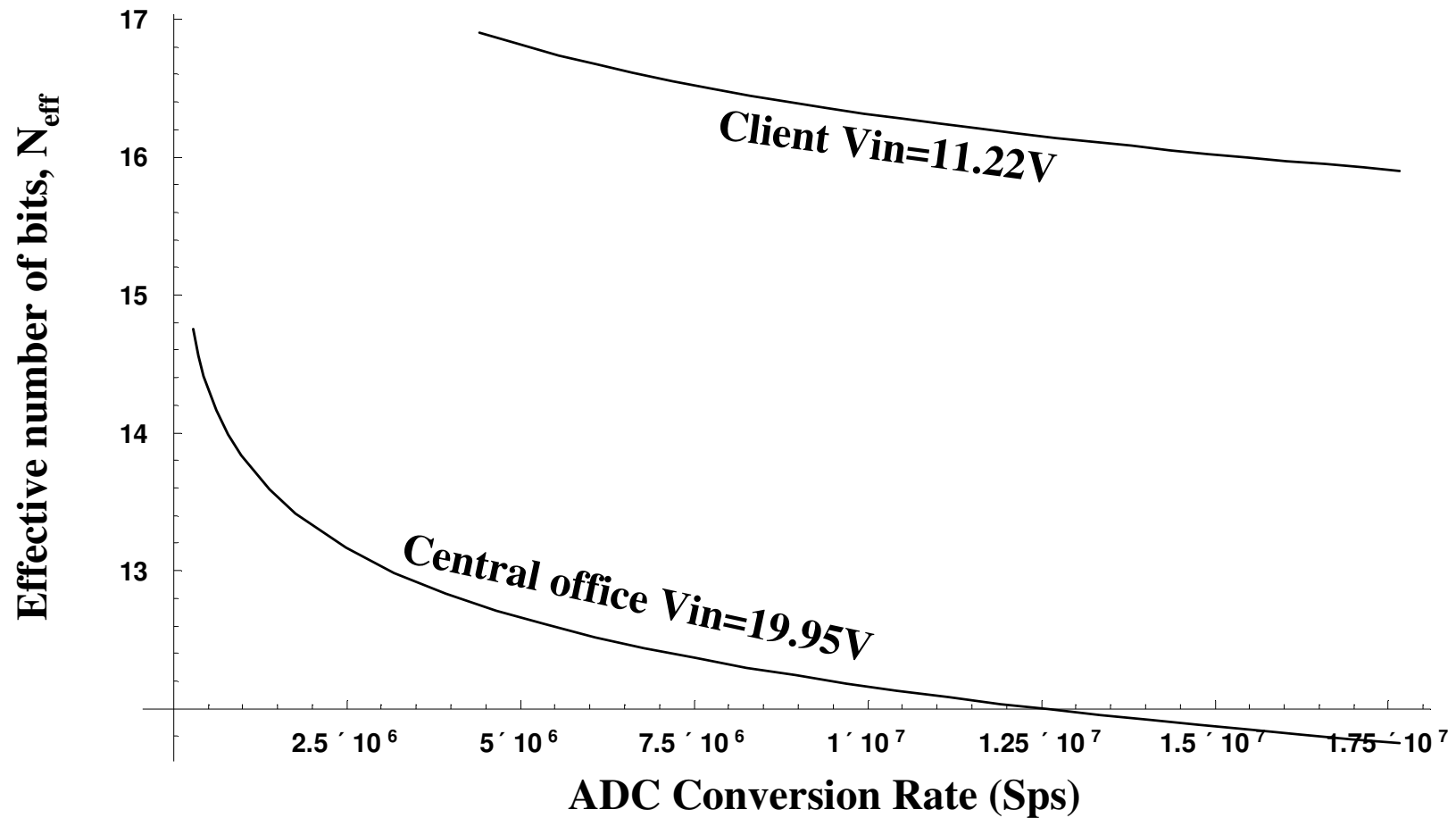


Signal Power Reaching Receiver



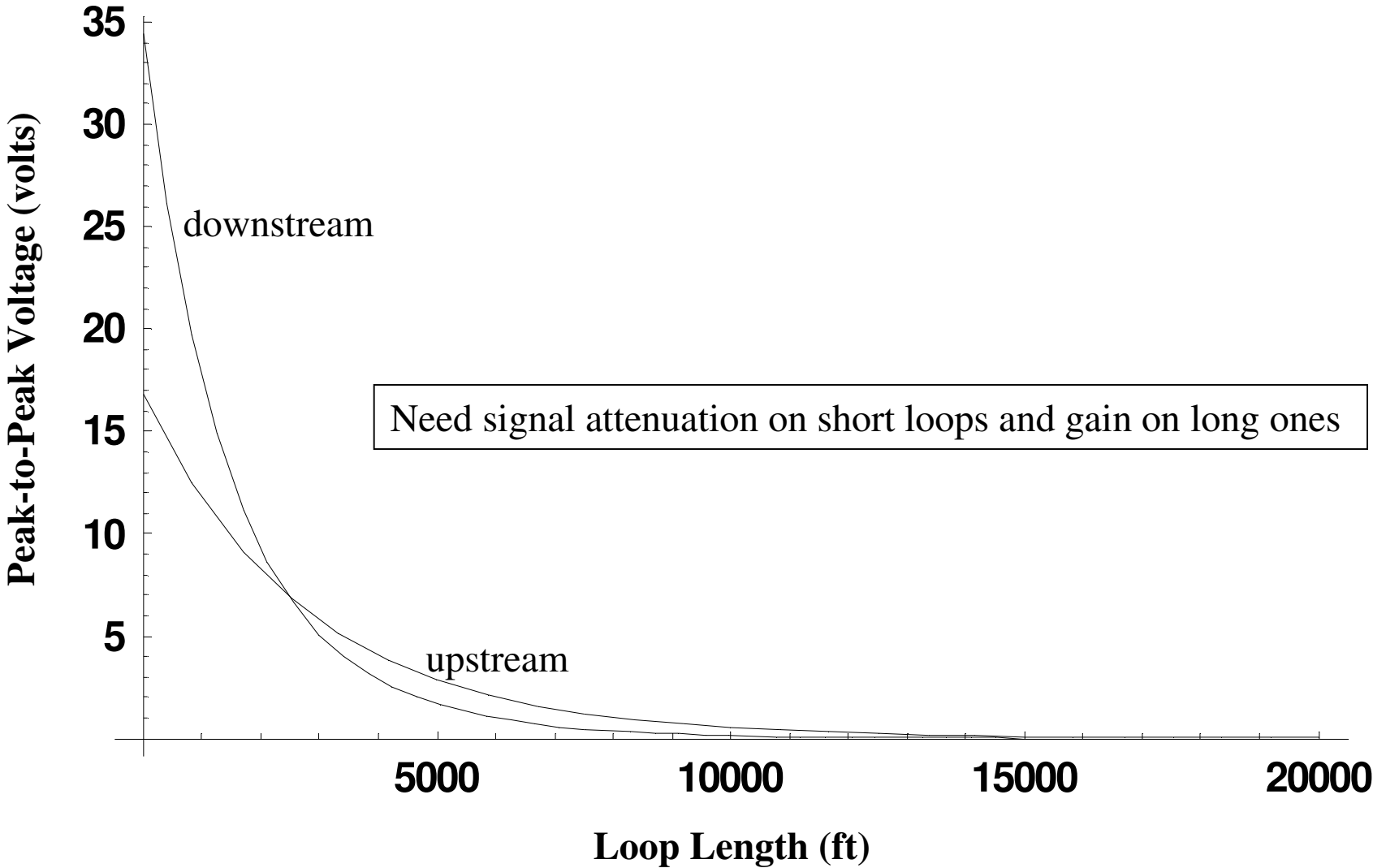
Largest voltage on null loop: 11.2Vpp at client and 19.95Vpp at central office

Minimum ADC N_{eff} versus Conversion Rate

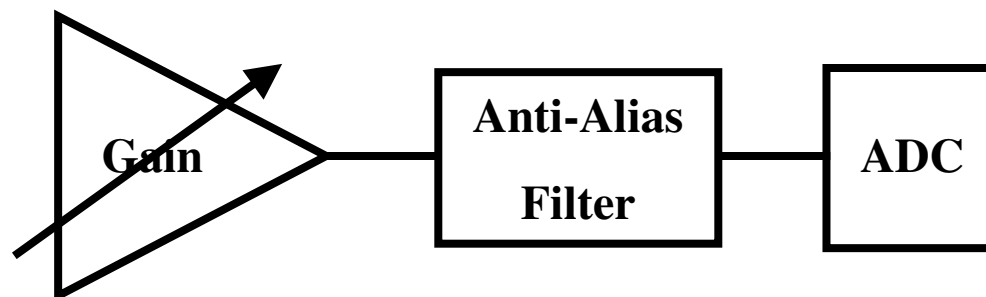


- Input voltages are too high to integrate – must reduce gain from loop to ADC
- Reducing channel gain drives ADC lsb too small

Received Input Peak-to-Peak Voltage versus Loop Length

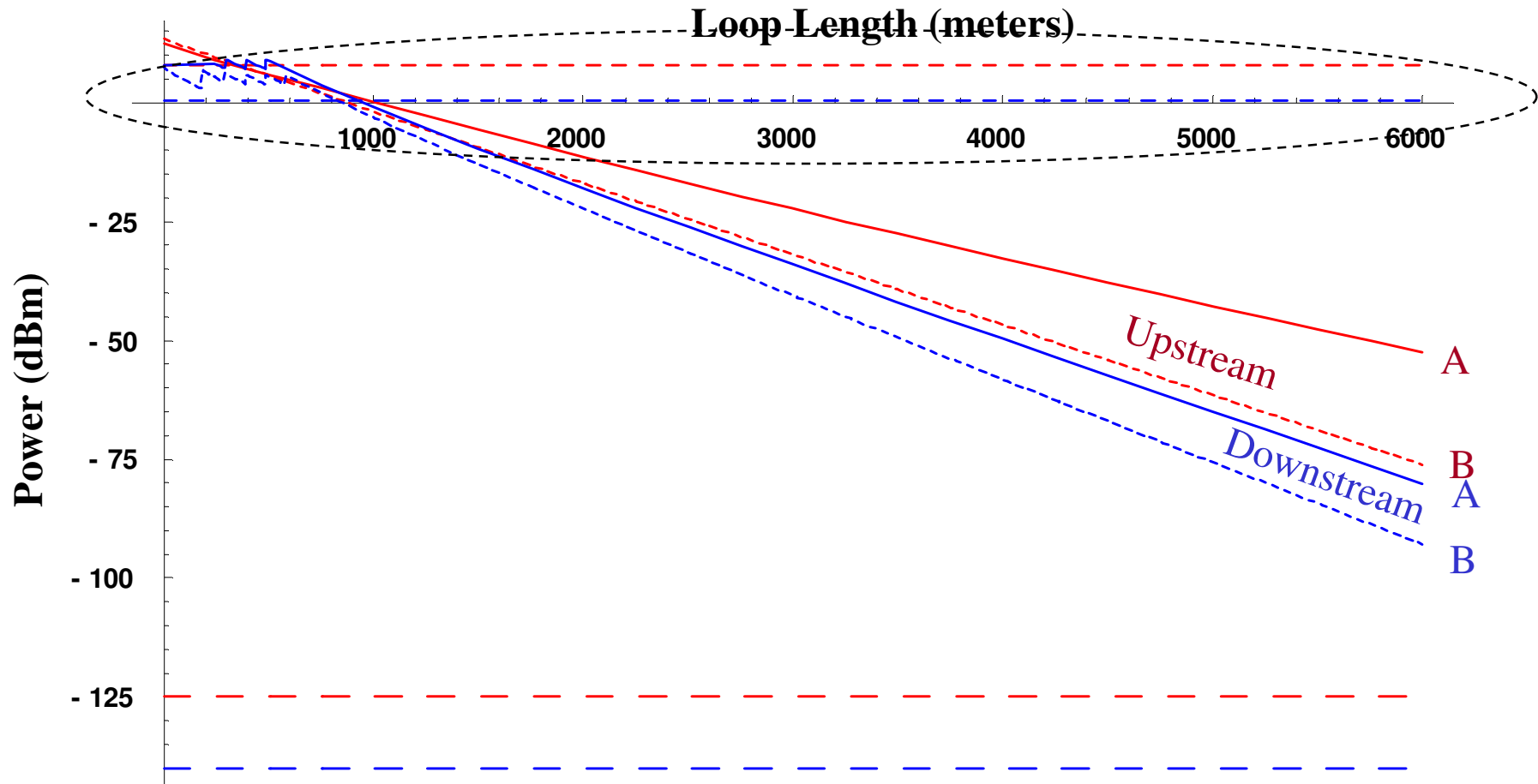


Programmable Gain to the Rescue



- The noise floor targets were set using loop noise measurements, and represent reasonable goals for long loops where signals are small
- On short loops we only need noise floors sufficient to handle 15 bits per subcarrier, $12.5N_{eff}$
- Use programmable gain to increase the channel gain for small signals from long loop
 - gives low channel gain when signals are large
 - gives high channel gain when signals are small
- Remaining problem: the echo

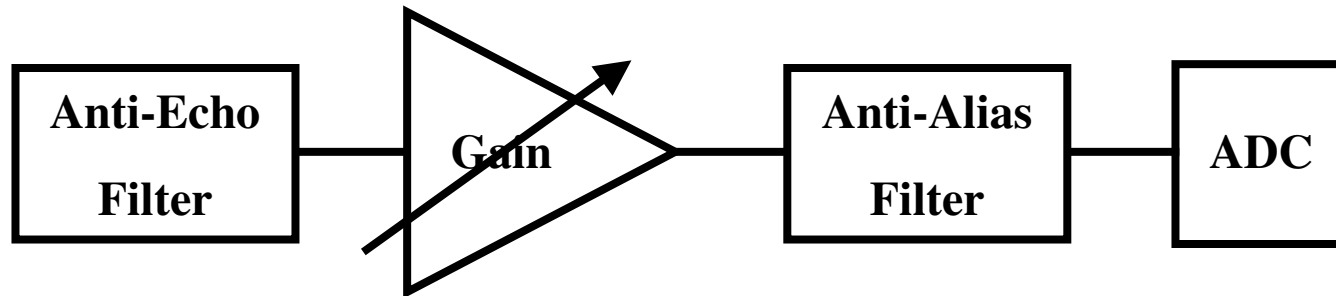
Total Signal Power at Receiver



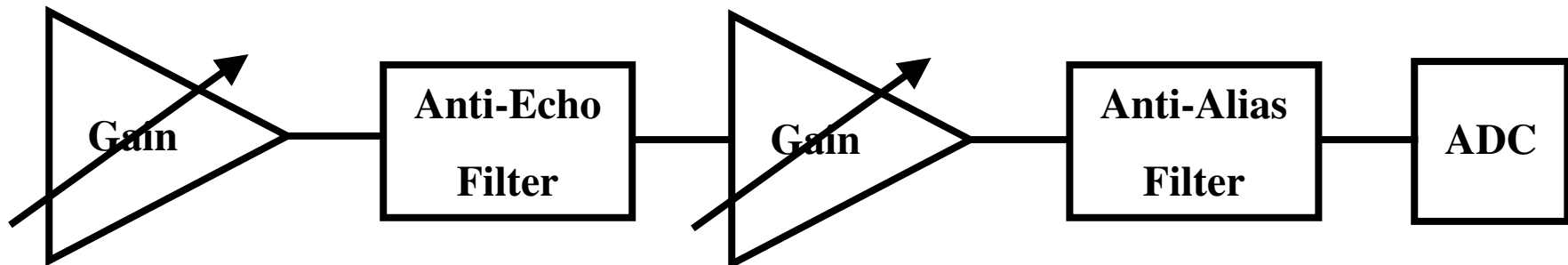
Largest voltage on null loop: 11.2Vpp at client and 19.95Vpp at central office

Killing the Echo

- Better

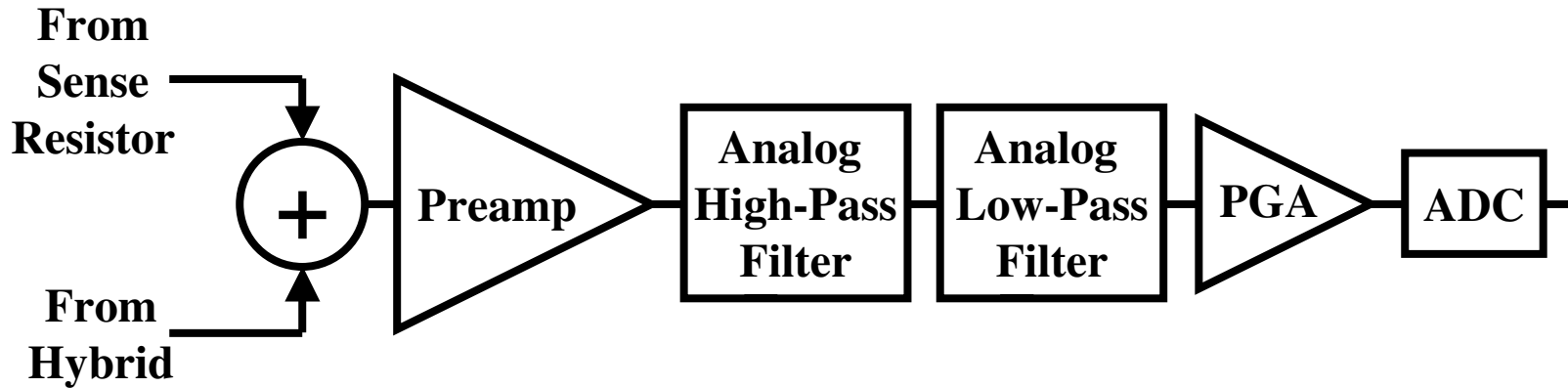


- Best

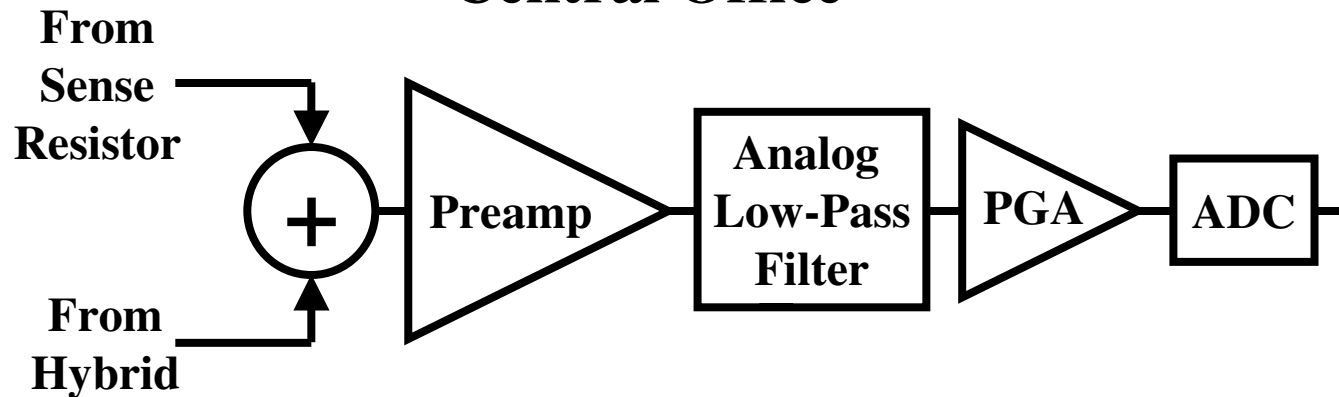


Receiver Architectures

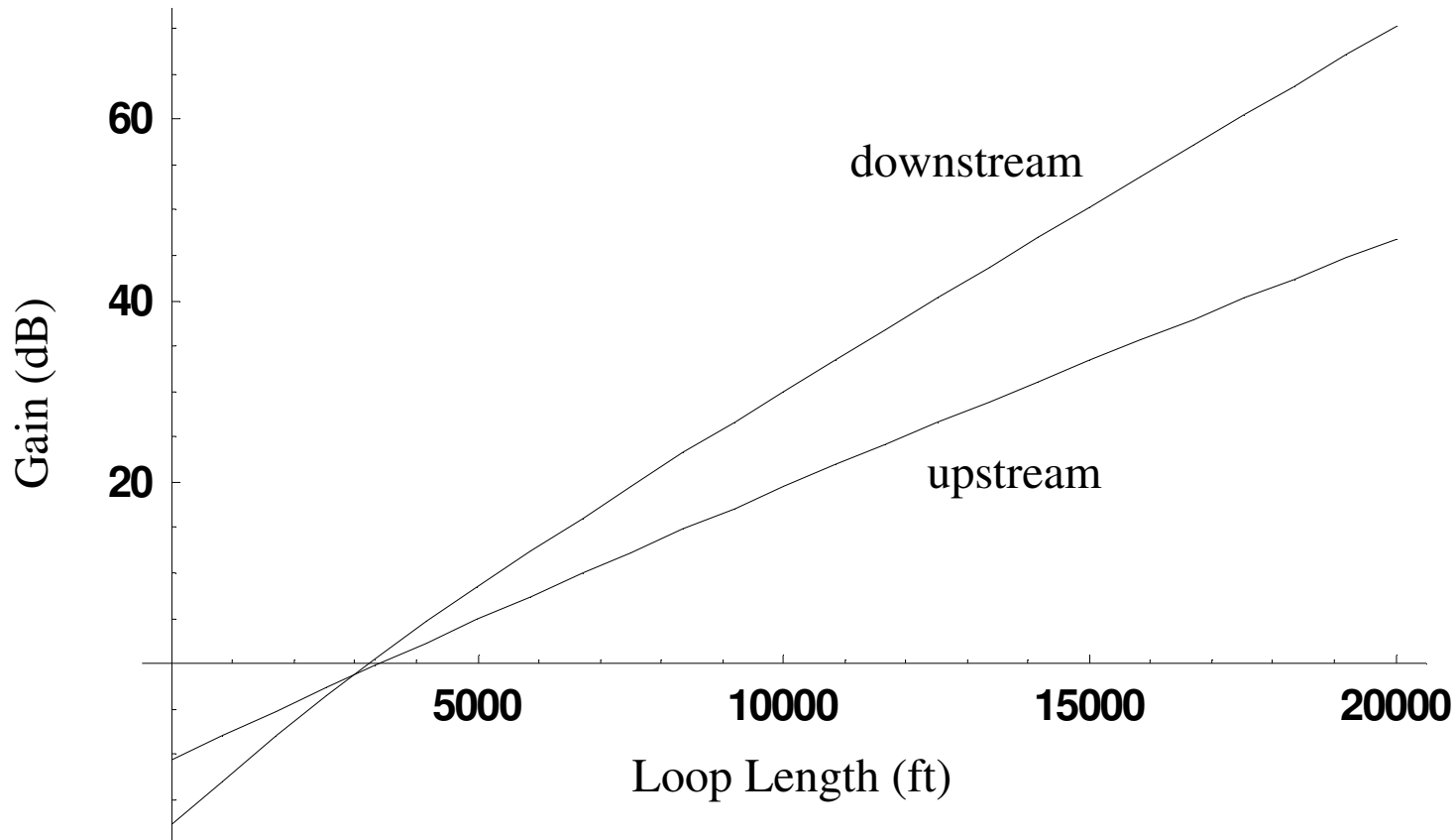
Client



Central Office

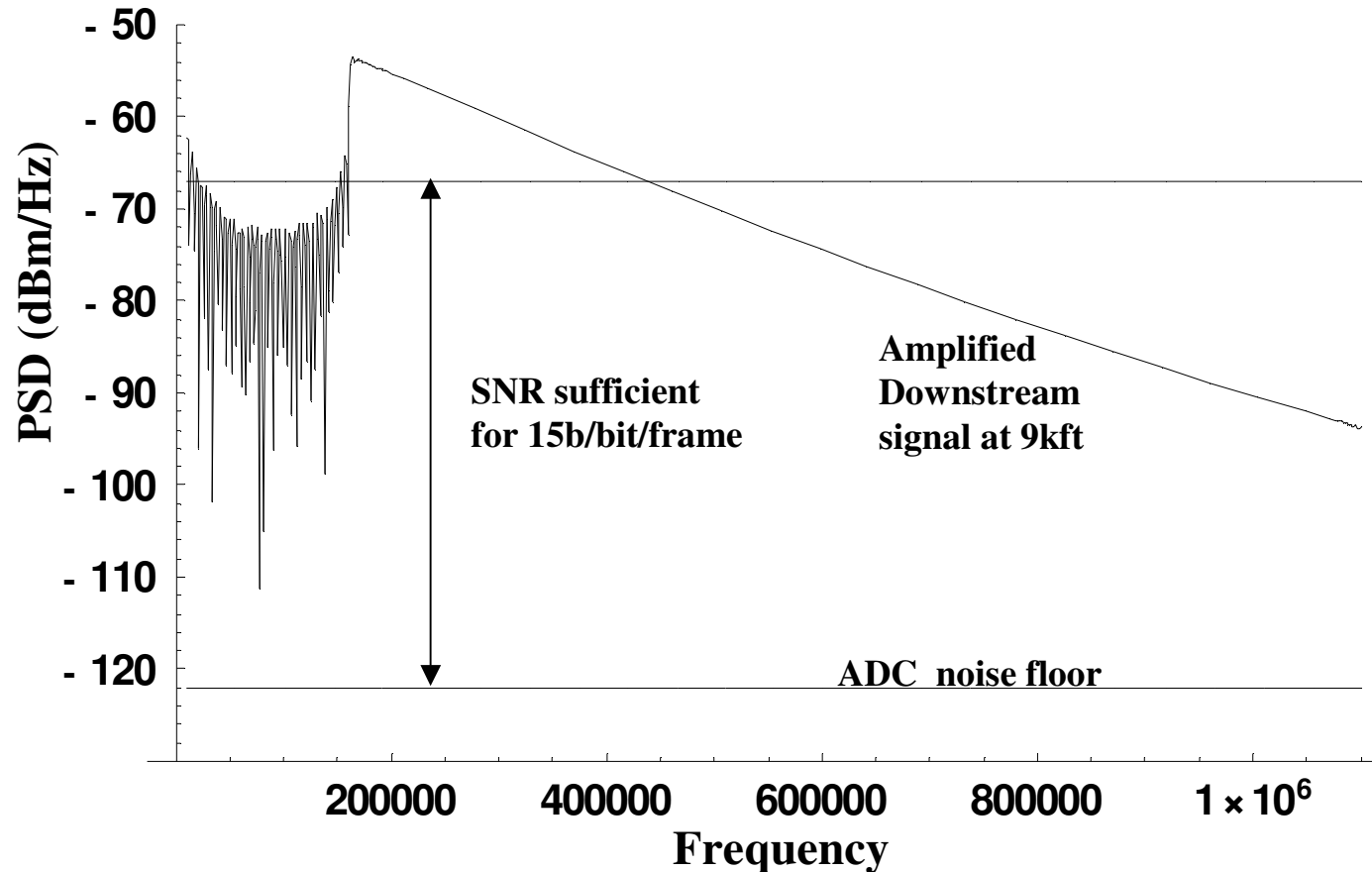


Receiver Programmable Gain



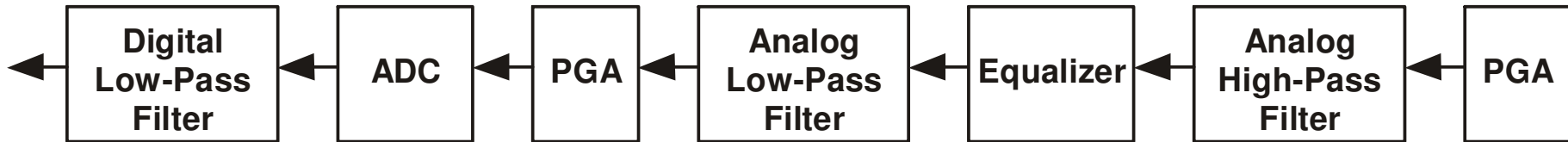
- Receiver gain improves SNR only when the ADC quantization noise is dominant.
- Typically 20 dB gain will amplify the receiver analog noise above the ADC noise. Additional gain will not improve the SNR, so the typical programmable gain range is ~ -20dB to +20dB at the remote terminal and ~ -12dB to +20dB at the central office.

Equalization



- Equalization is frequency dependent gain
- Improves data rate when
 - SNR is limited by noise source subsequent to equalizer
 - Low-Frequency subcarrier SNR exceeds that required to support 15b/frame
- Programmable gain should follow equalizer

Generic Template



- **AHPF**

- In client FDD modems, it may reject virtually all of the upstream echo power and enable higher PGA gain.
- Frequently employed in Annex B central office modem to reject ISDN power in front of PGA.

- **Equalizer**

- Provides frequency dependent gain to amplify weak high-frequency subcarriers above ADC noise.
- Not useful in central office receiver

- **ALPF**

- Provides anti-alias filtering for ADC.
- In central office FDD modems, it also rejects upstream echo and enables higher PGA gain.

- **PGAs**

- Placed both before and after filters when echo is rejected by integrated filter.

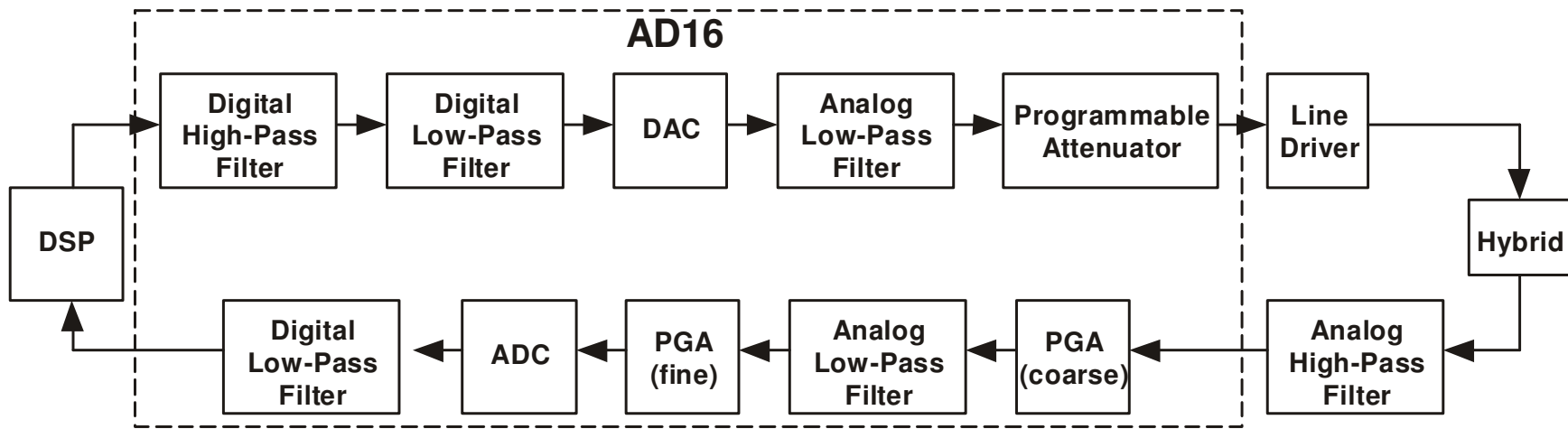
- **ADC**

- Resolution depends upon duplexing, EC being more demanding than FDD because echo power is dominant on long loops.

- **DLPF**

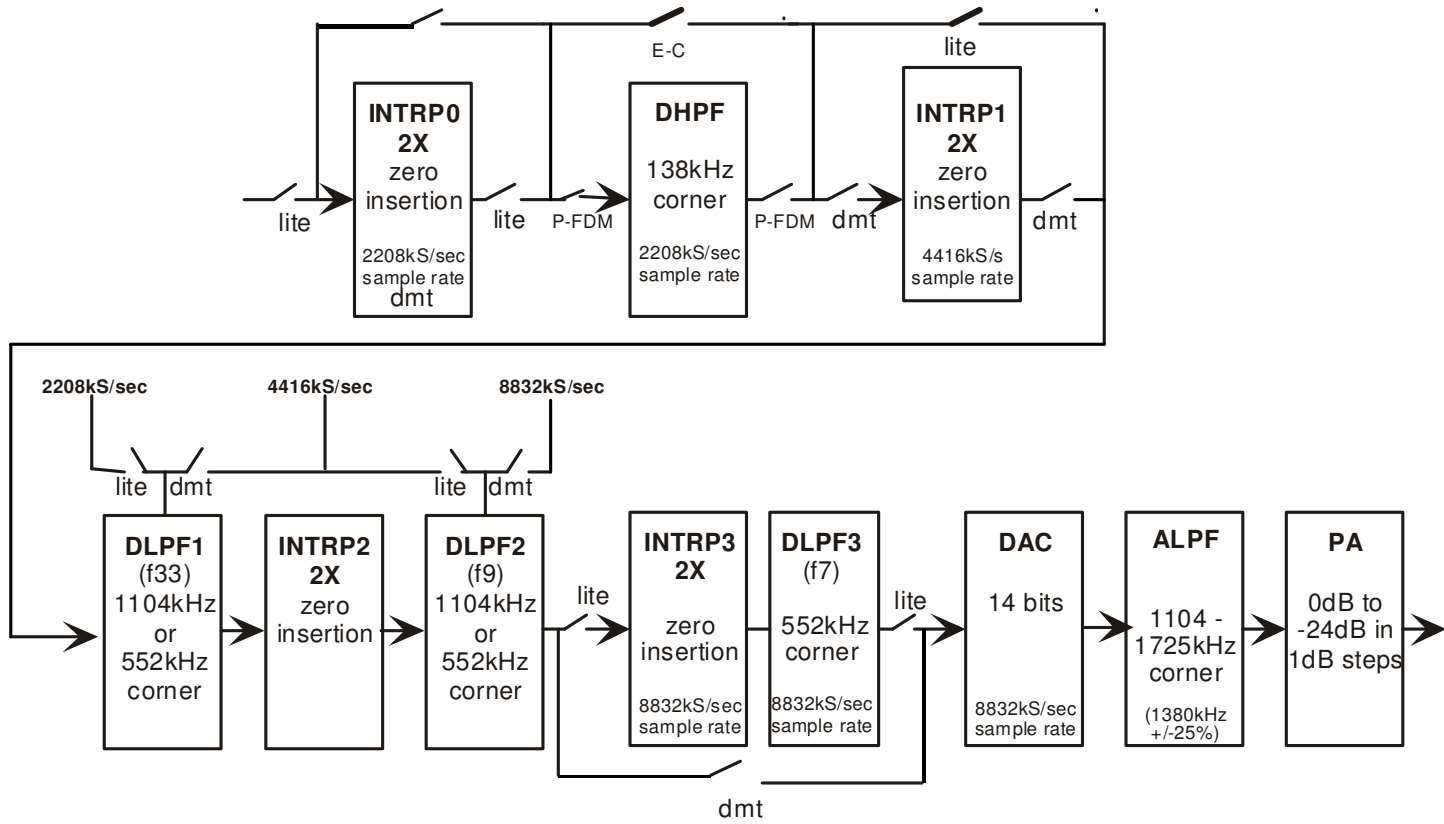
- Decimates sample rate to that of FFT.

Design Example: Echo-Canceling Central Office Modem

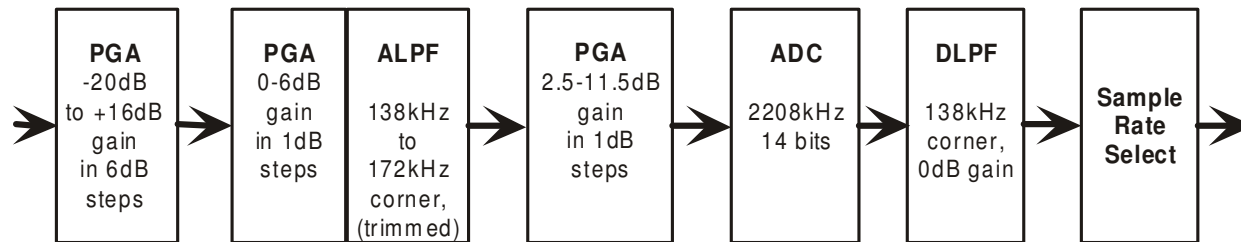


- **Deviations from generic topologies**
 - Analog transmitter high-pass deleted to support echo cancellation
 - Programmable attenuator added to support power cutback on short loops
 - Programmable gain amplifiers precede and follow receiver analog low-pass to adjust signal to 3V_{pp} before non-overlapping portion of echo is removed
 - Equalizer is not necessary on central office receivers
- **DSP sample rates**
 - 2208kS/sec transmitter in full rate mode and 1104kS/sec in “lite” mode
 - 276kS/sec receiver

AD16

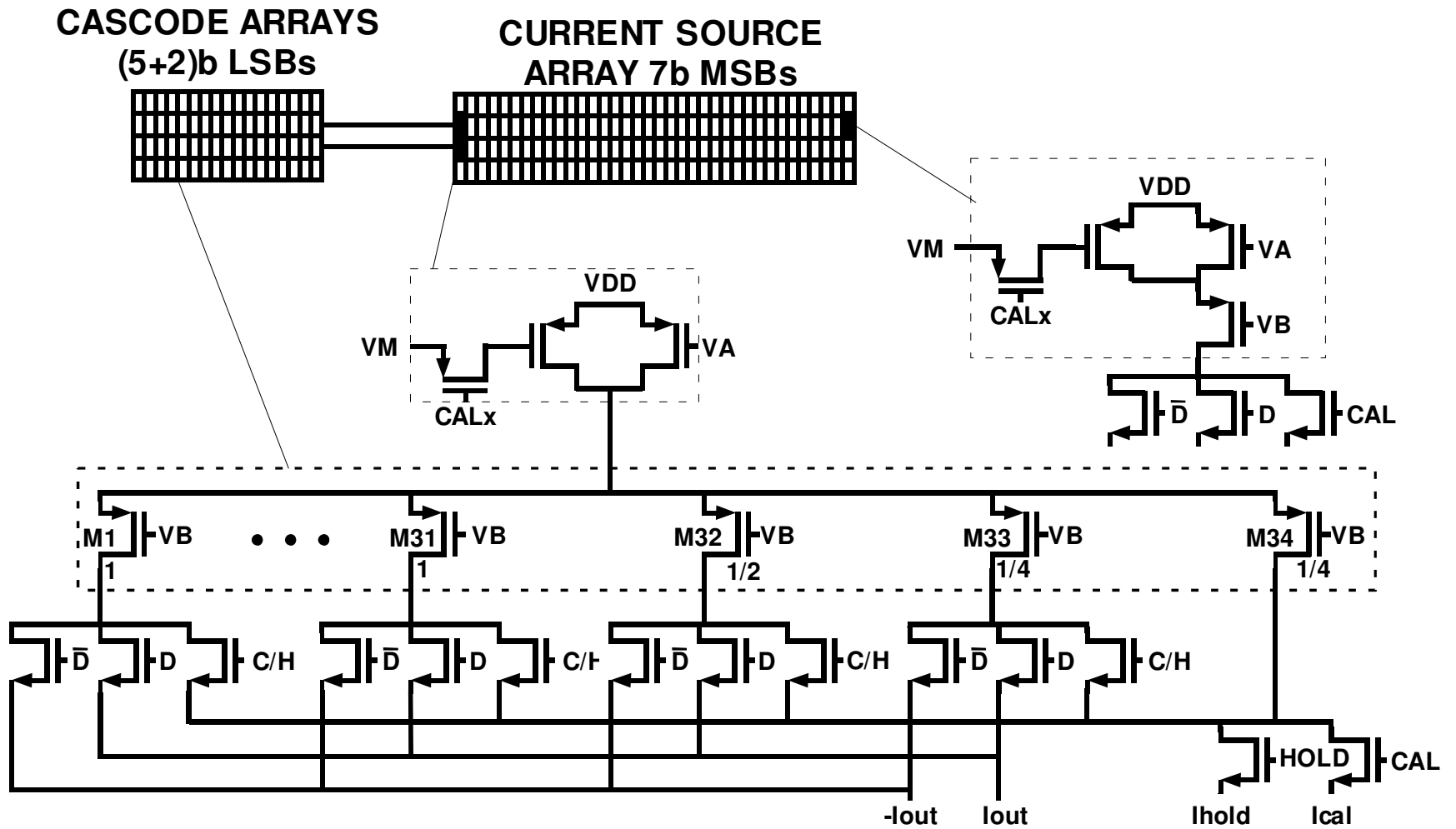


TRANSMITTER PATH

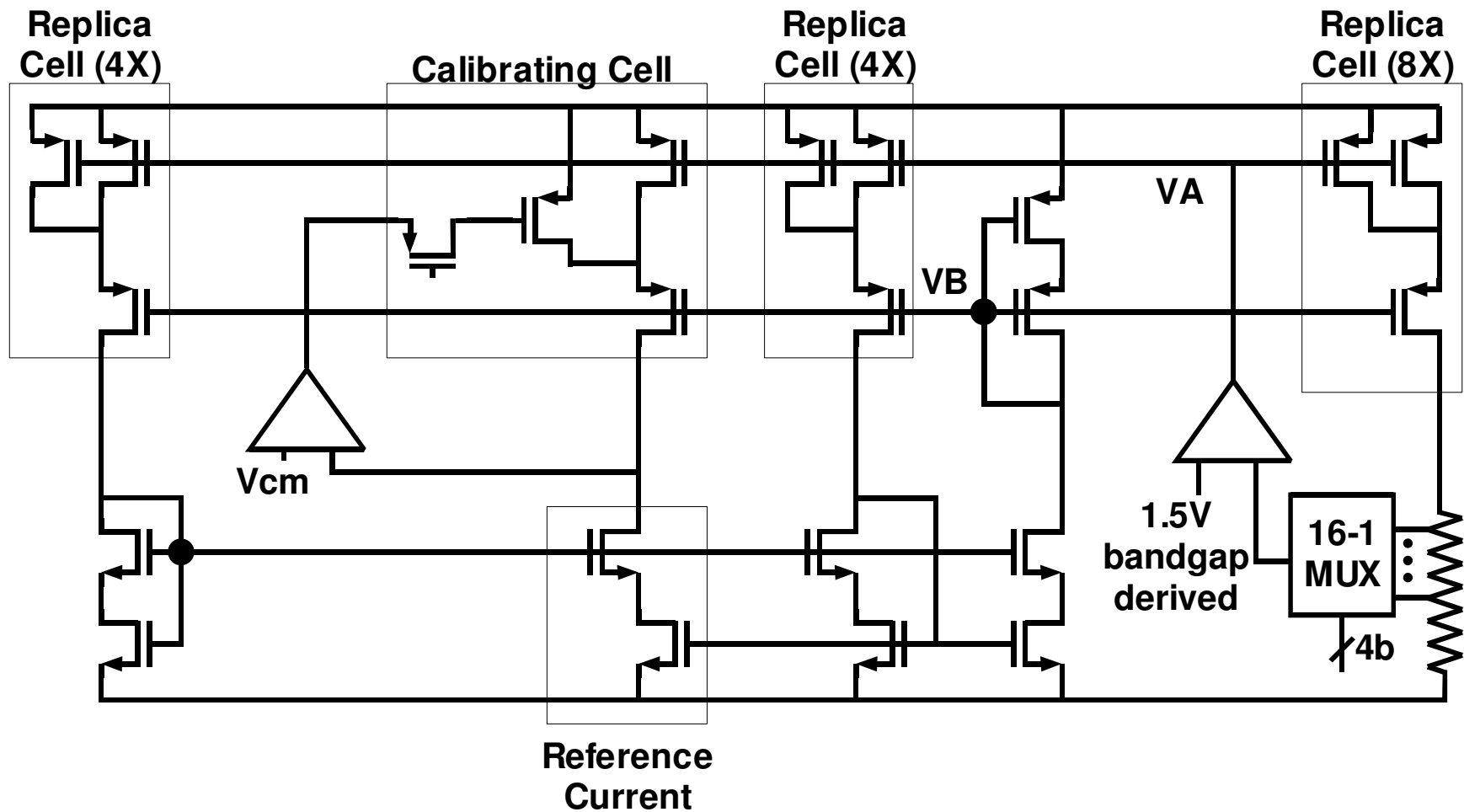


RECEIVER PATH

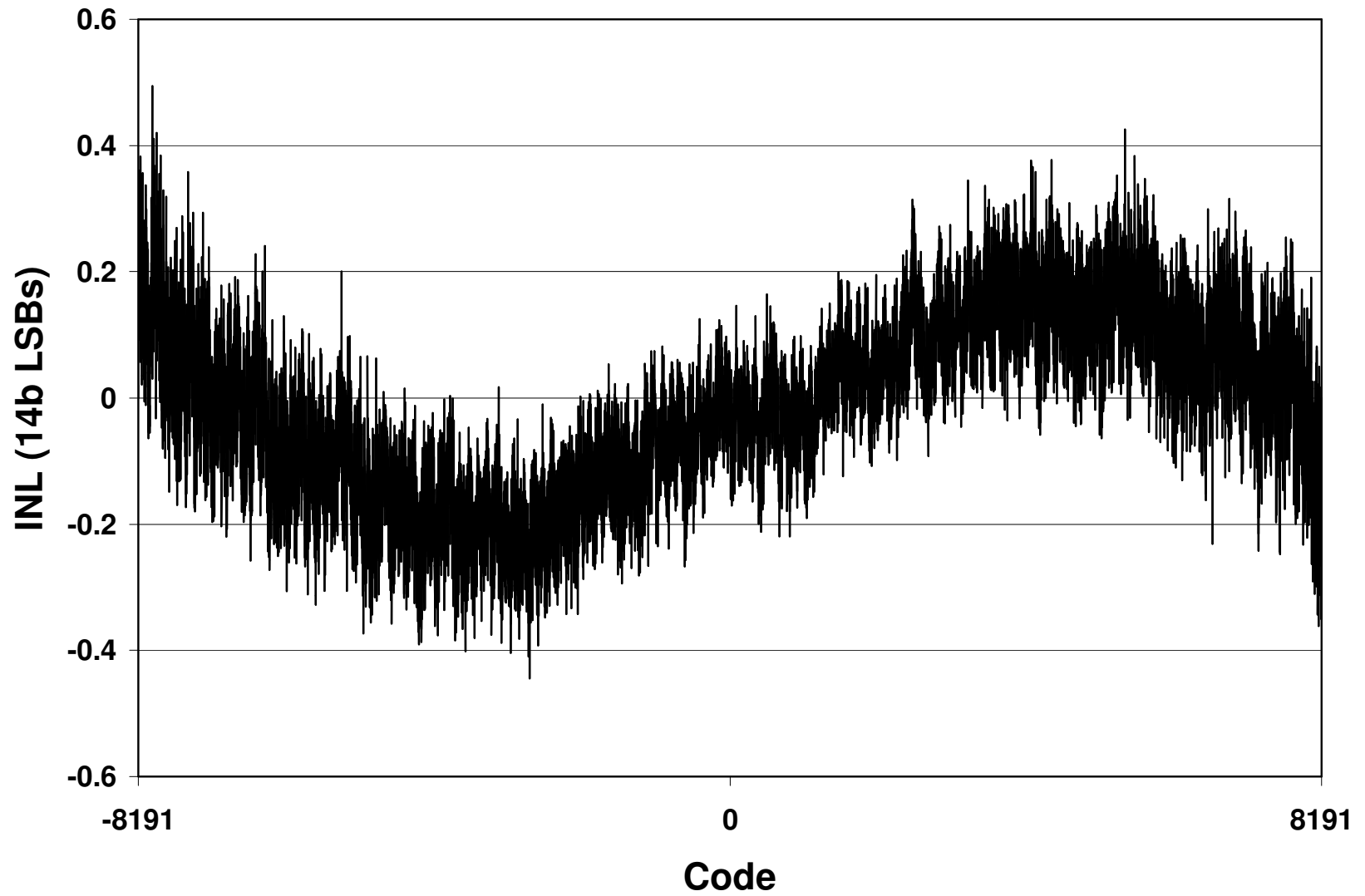
D/A Converter



Signal DAC Current Source Bias and Calibration

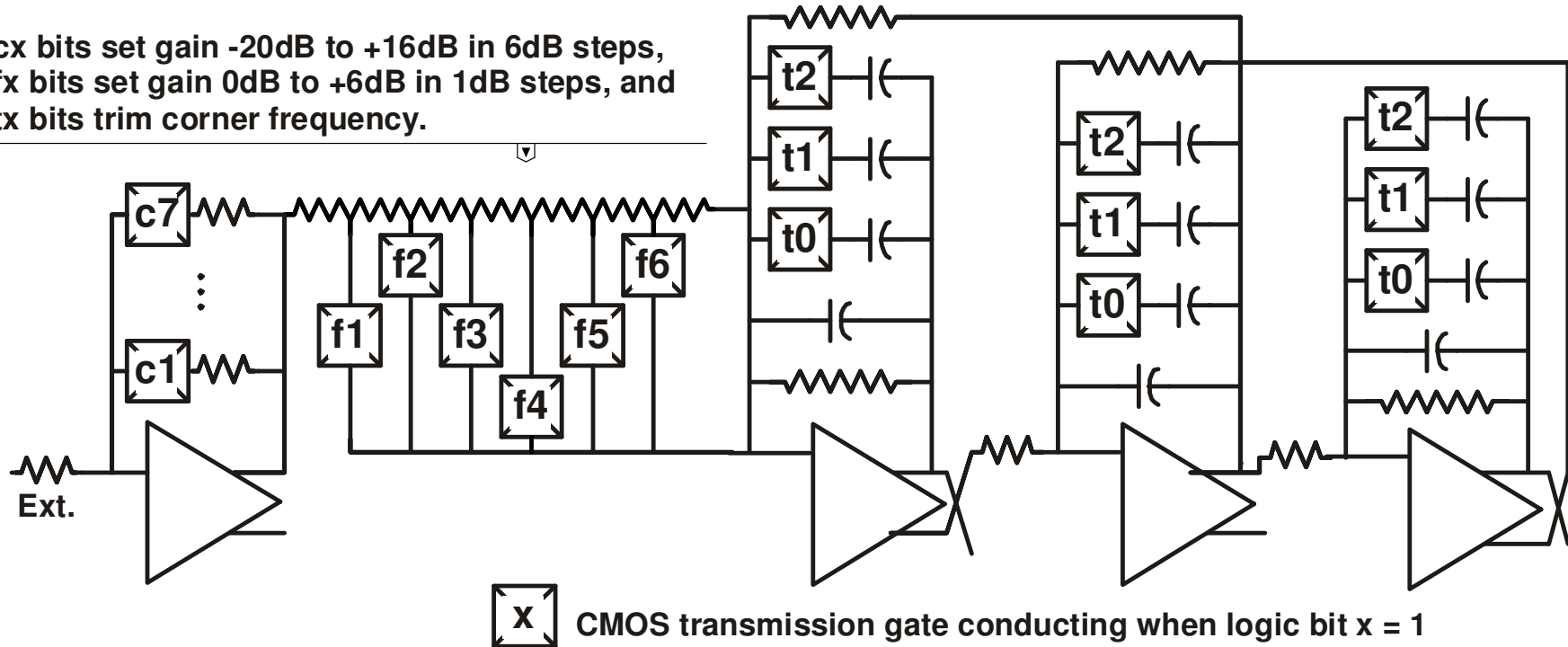


Transmitter Static Integral Non-Linearity (digital high-pass bypassed)

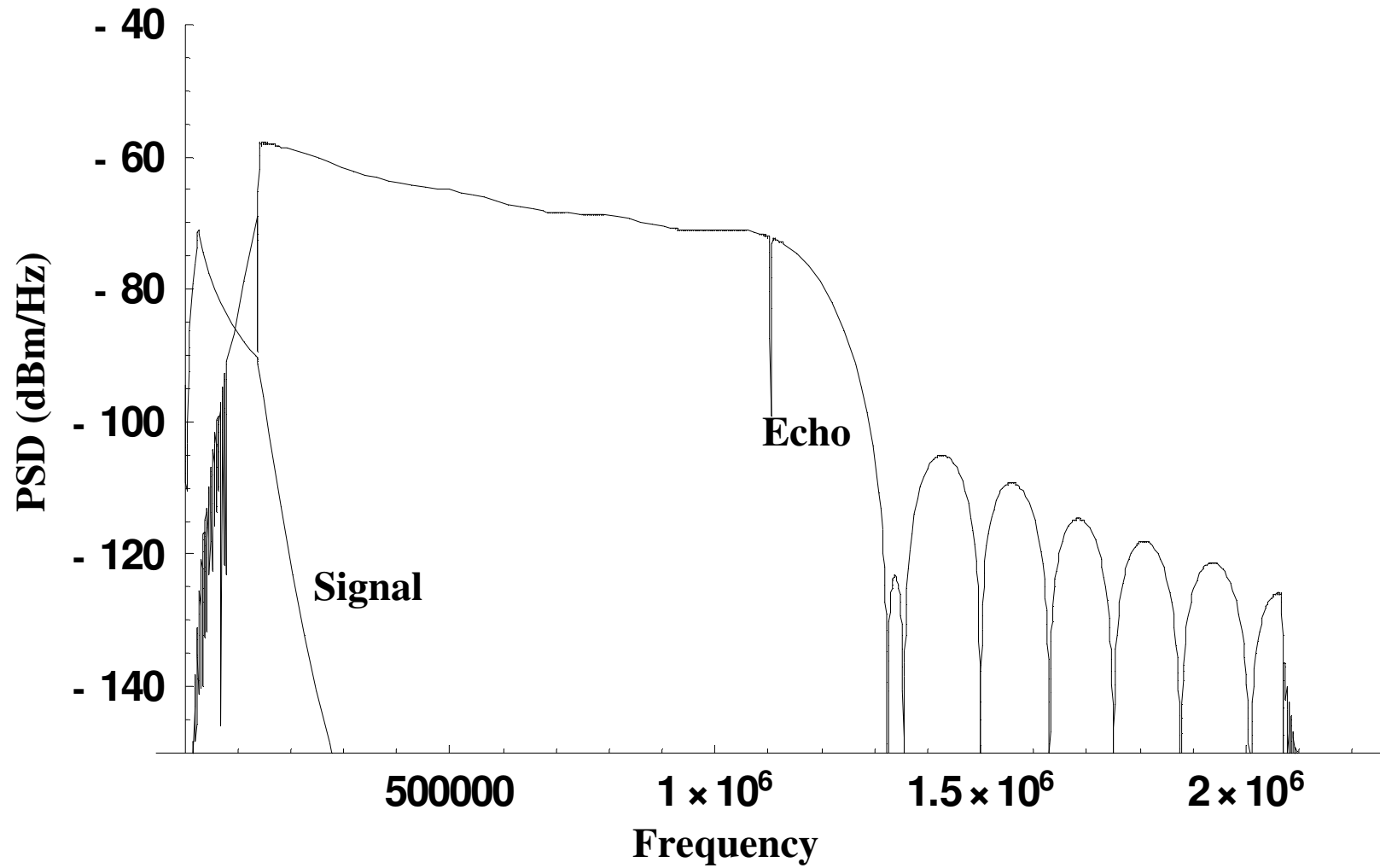


Receiver PGA/Low-Pass Combination

c_x bits set gain -20dB to +16dB in 6dB steps,
 f_x bits set gain 0dB to +6dB in 1dB steps, and
 t_x bits trim corner frequency.

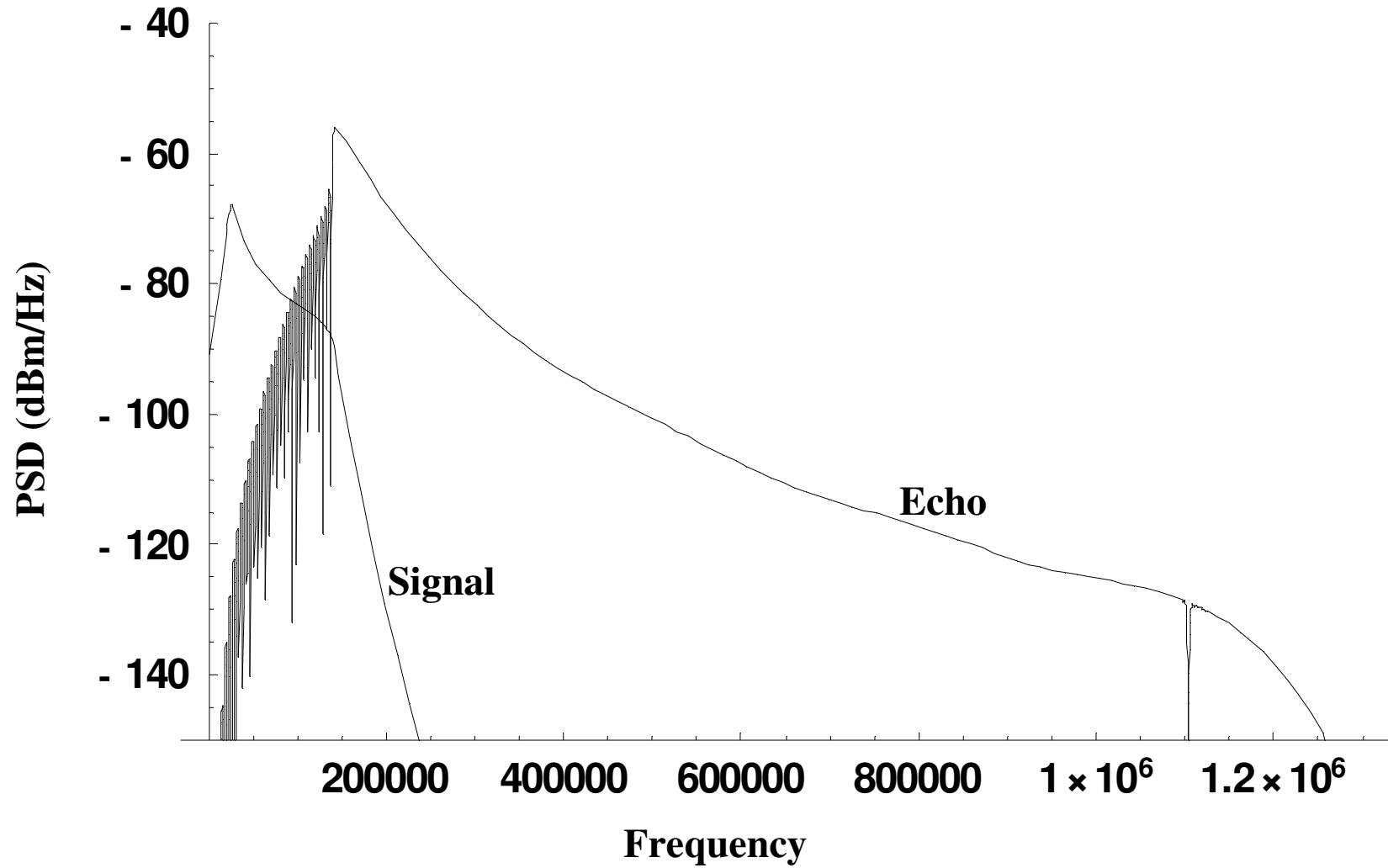


PSD at Input to Analog Low-Pass Filter (15kft, 26awg, $R_H=18\text{dB}$)



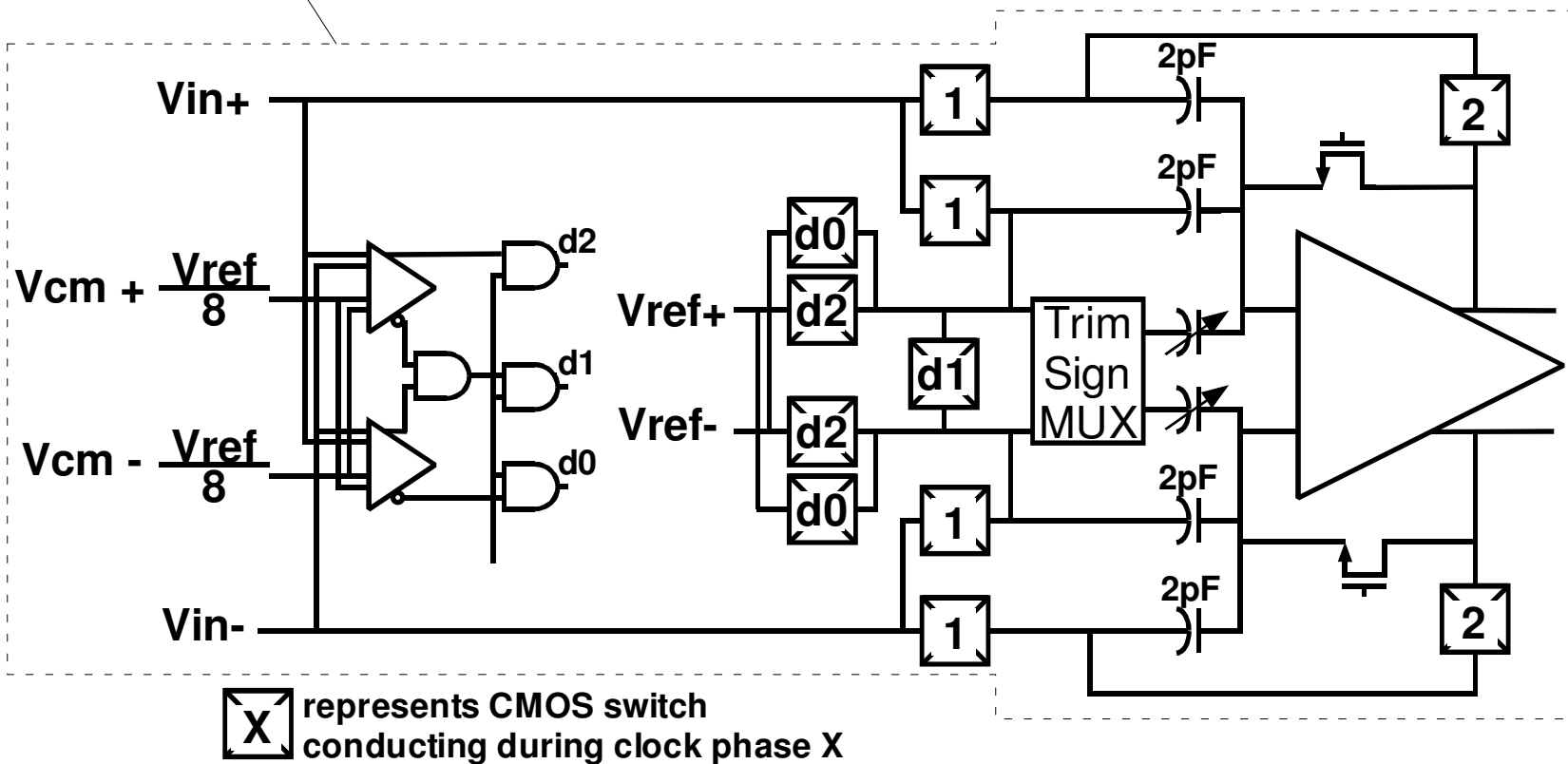
PSD at Input to ADC

(15kft, 26awg, $R_H=18\text{dB}$)

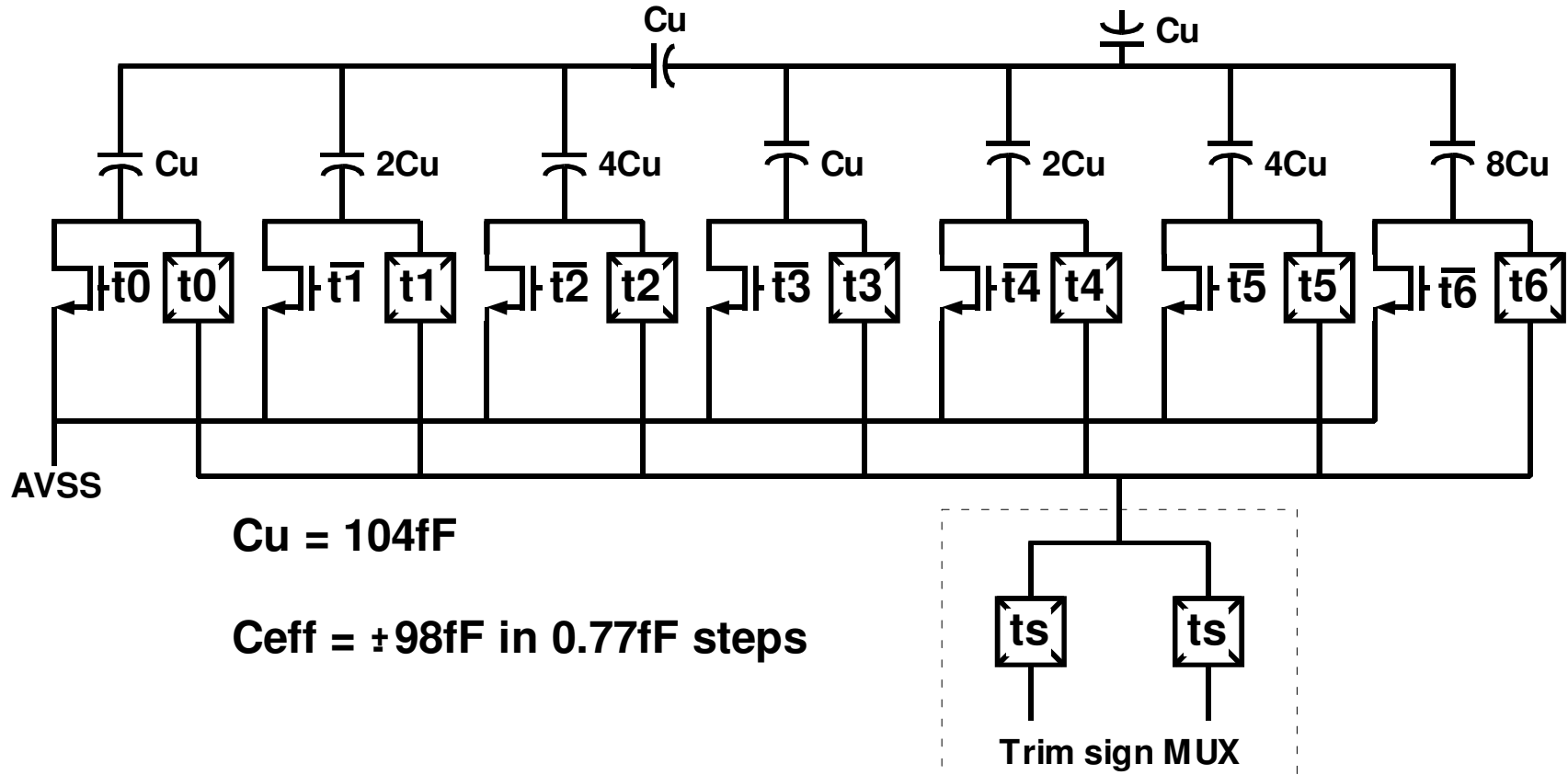


Pipelined Analog-to-Digital Converter

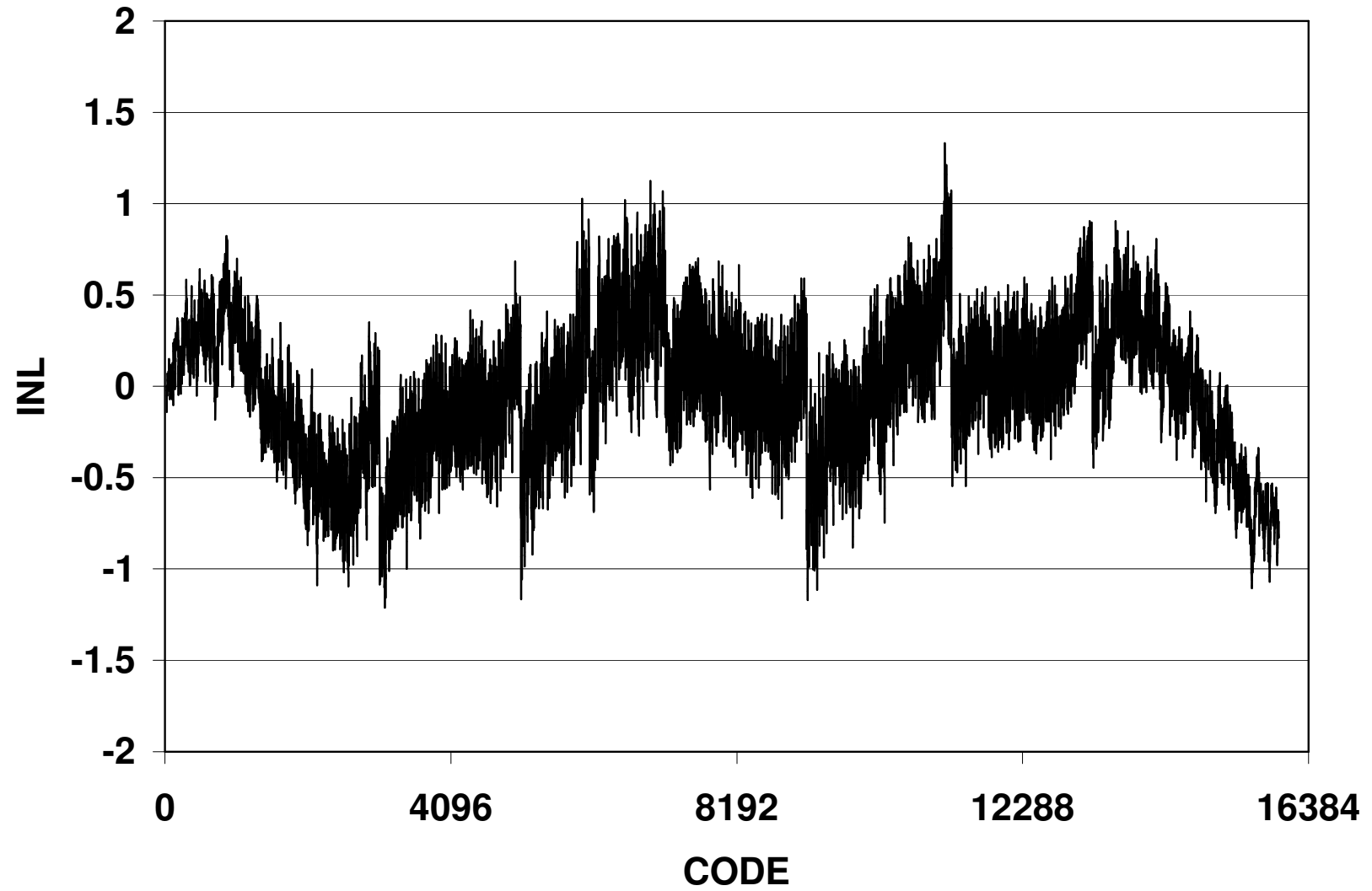
Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	...	Stage 12	2b flash
1.5b	1.5b	1.5b	1.5b	1.5b	1.5b		1.5b	
8b trim	8b trim	7b trim	7b trim	7b trim	no trim		no trim	



7-Bit Capacitor Trimming Array

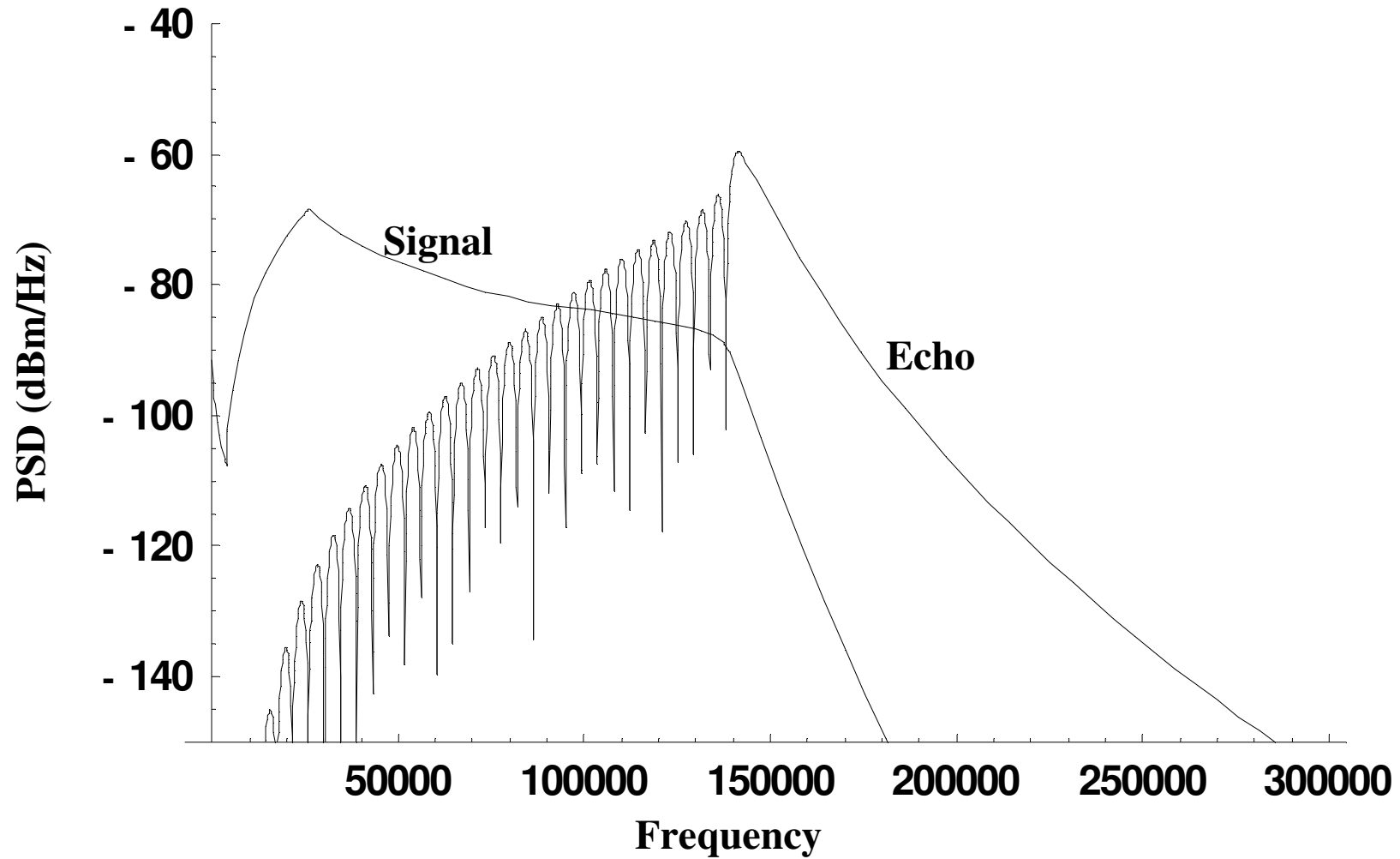


Receiver INL



PSD at Output of Digital Low-Pass Filter

(15kft, 26awg, $R_H=18\text{dB}$)



Summary

- The ADSL AFE requirements depend upon multiple system parameters such as
 - Duplexing method
 - Upstream and downstream frequency allocations
 - DSP transmit and receive sample rates
 - Receiver sensitivity
 - Hybrid rejection
- An AFE design example provides the optimum integrated solution for modems employing echo cancellation.