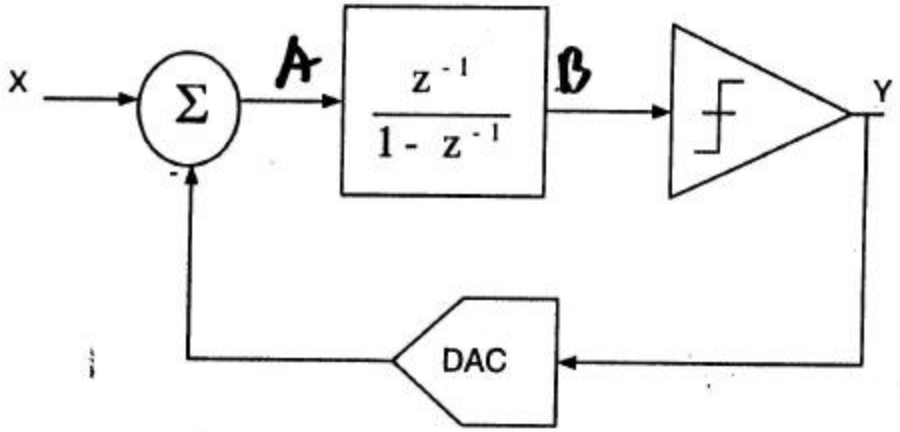
Overview

- Sigma-Delta Basics
  - Theory
  - General characteristics
  - Design methods
  - Recent activity
- Genetic Algorithm based analysis method

What is a Sigma-Delta

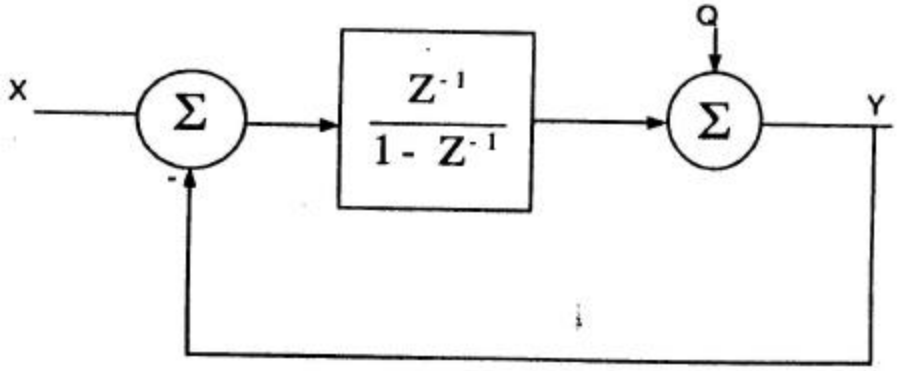
- ADC architecture that uses oversampling and shaping of the quantization noise out of the signal band to trade resolution for bandwidth
- Uses digital filtering of output to remove out of band quantization noise
- Applicable for effective sample rates in the KHz to low MHz ranges
- CMOS friendly

First-Order Sigma-delta



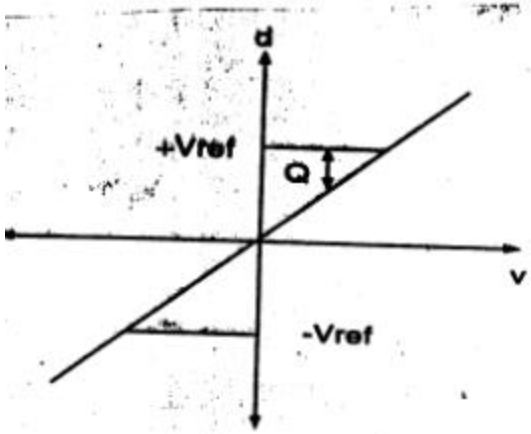
$$B = A\frac{z^{-1}}{1 - z^{-1}}$$

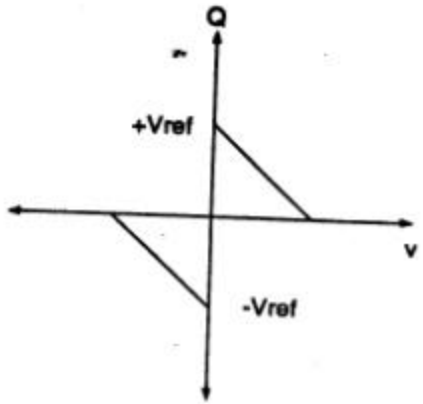
$$B = Az^{-1} + Bz^{-1}$$

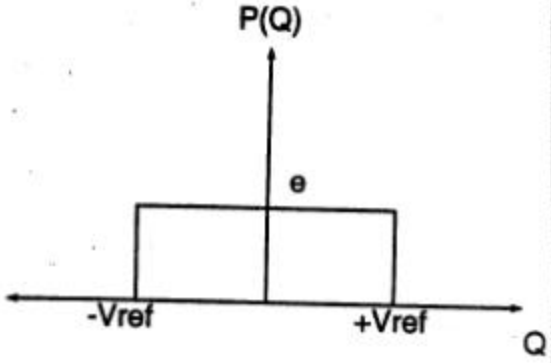


$$Y(z) = z^{-1}X(z) + E(1 - z^{-1})$$

Quantization Error Becomes Noise







$$Q^2_{rms} = \frac{1}{2Vref}\int_{-Vref}^{+Vref} e^2 de = \frac{1}{3}Vref^2$$

Noise power

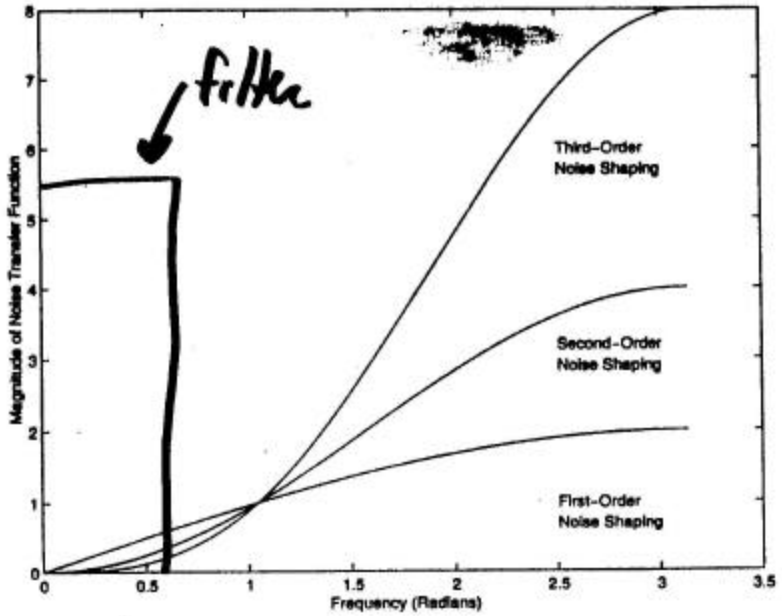
$$B(z) = Q_{rms}\sqrt{\frac{2}{f_s}} = \sqrt{\frac{2}{3}Vref^2 T_s} = Vref\sqrt{\frac{2T_s}{3}}$$

Spectral density

$$N(f) = E(1 - z^{-1}) = 2Vref\sqrt{\frac{2T_s}{3}}\sin(\pi f T_s)$$

Shaped by NTF

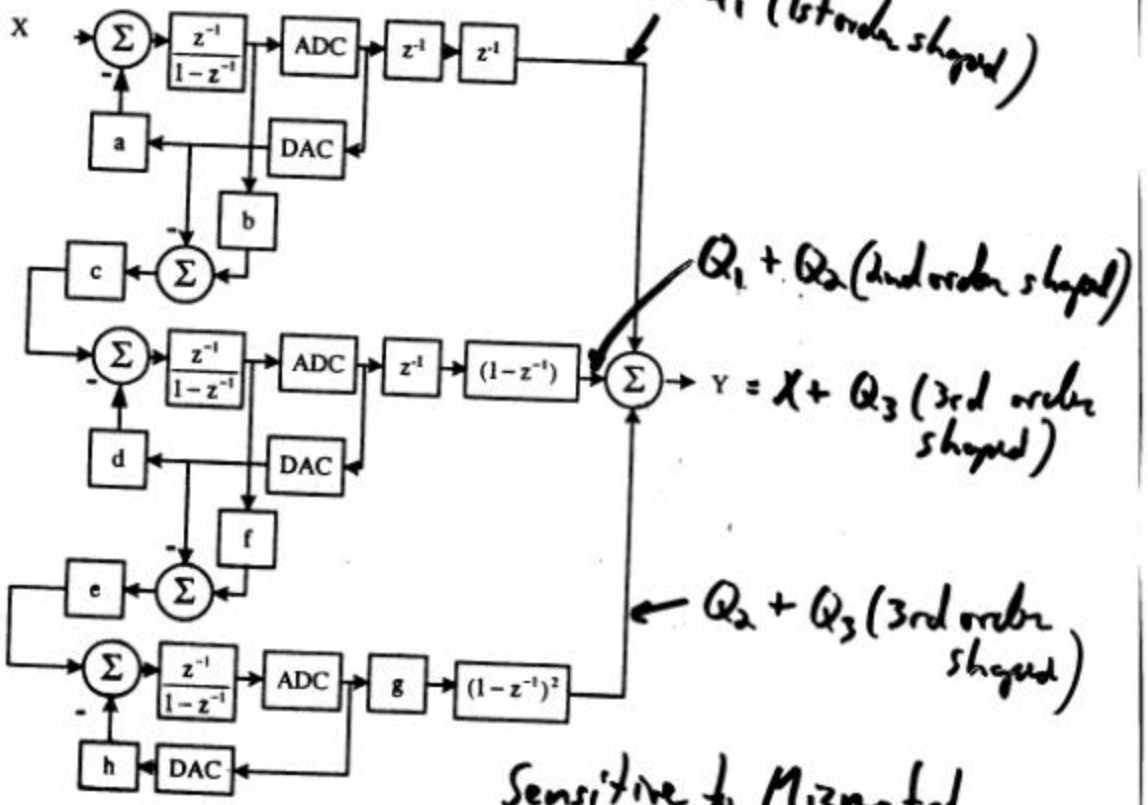
NTF for Higher Order Modulators



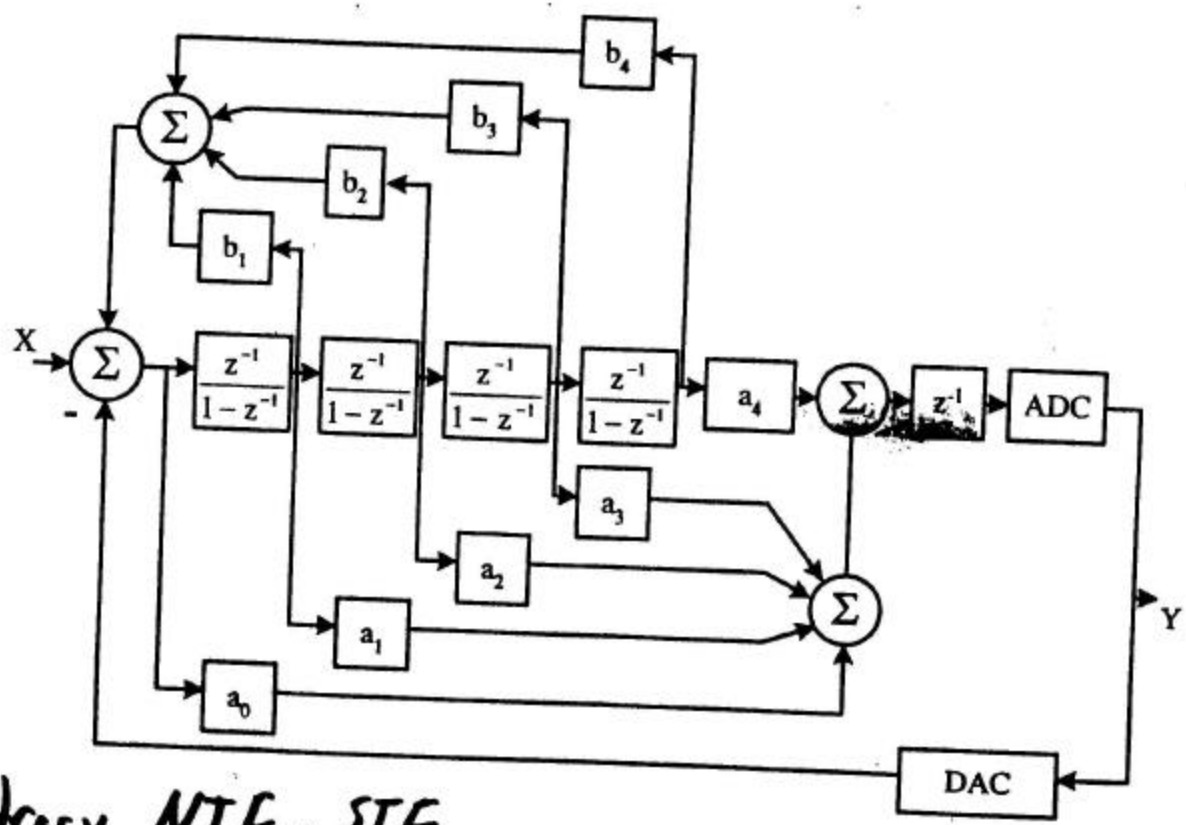
$$Y(z) = z^{-1}X(z) + E\,(1 - z^{-1})^{L}$$

$$\#\,\text{Bits} = (L + 0.5)\,\text{Log}_2\,\text{OSR} - \text{Log}_2\left[\frac{\Pi^{L}}{\sqrt{2L+1}}\right] + \text{Log}_2\,(2^{Q} - 1)$$

TFOC


X
ADC
DAC
a
b
c
d
e
f
g
h
$\frac{z^{-1}}{1-z^{-1}}$
z^{-1}
$(1-z^{-1})$
$(1-z^{-1})^2$
$X + Q_1$ (1st order shaped)
$Q_1 + Q_2$ (2nd order shaped)
$Y = X + Q_3$ (3rd order shaped)
$Q_2 + Q_3$ (3rd order shaped)
Sensitive to Mismatch

Single Loop



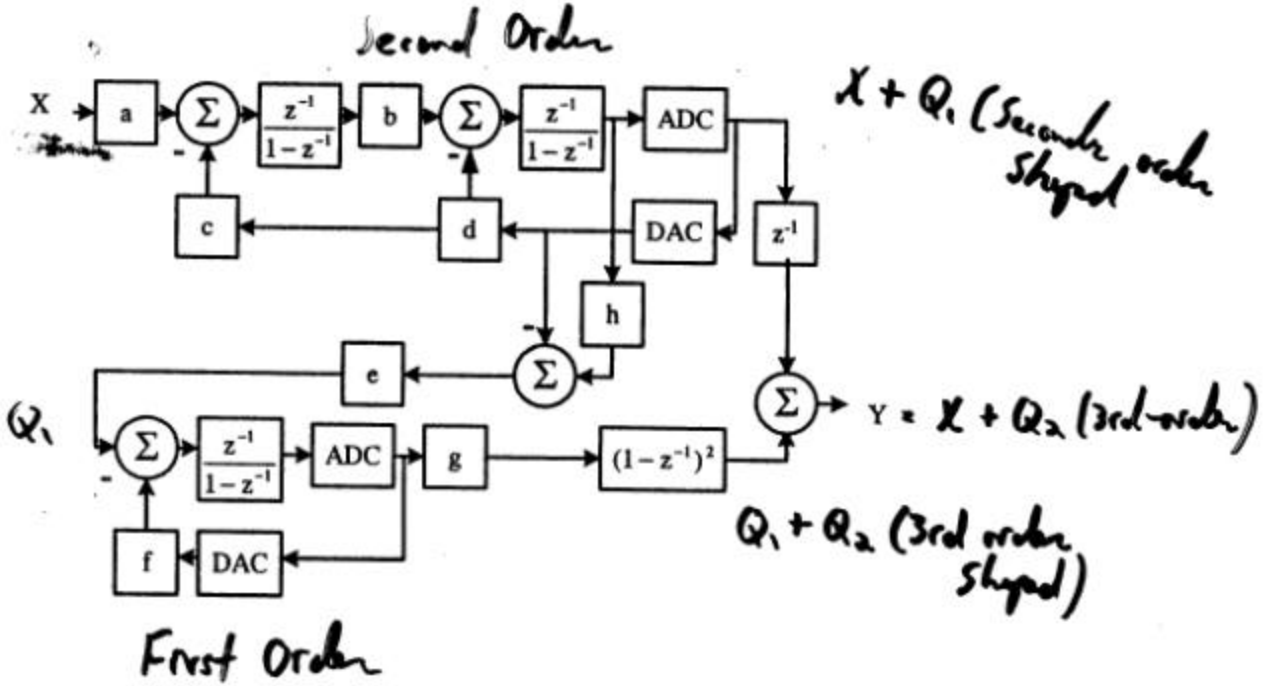
Arbitrary NTF, STF

Complex

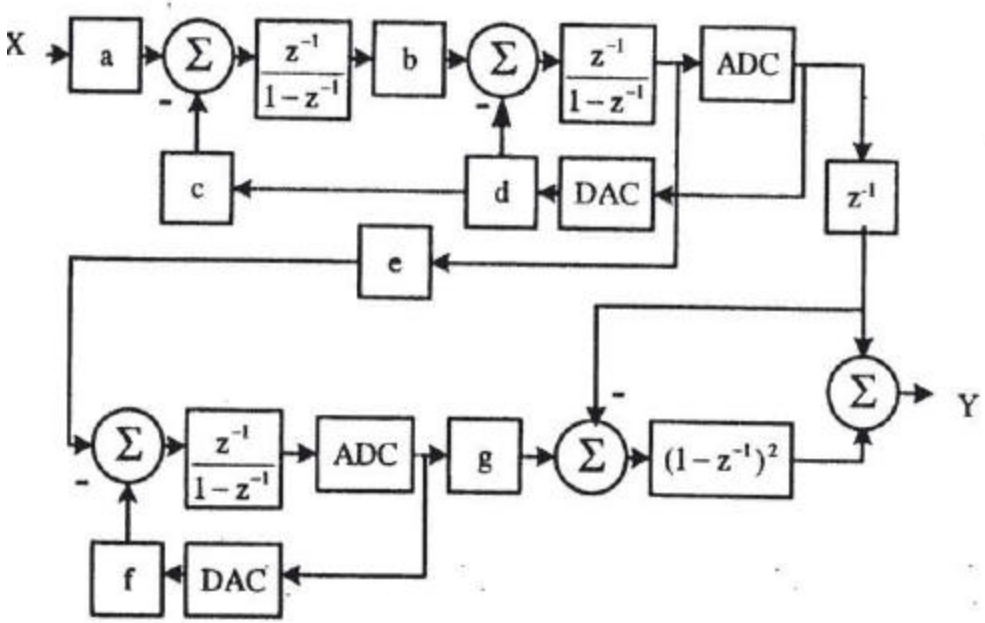
Large ratios

Conditionally Stable

SOFOC1


Second Order
X
a
b
ADC
c
d
DAC
h
e
Q1
f
DAC
First Order
X + Q1 (Second order shaped
Y = X + Q2 (3rd-order
Q1 + Q2 (3rd order shaped)

SOFOC2


X
a
Σ
-
$\frac{z^{-1}}{1-z^{-1}}$
b
Σ
-
$\frac{z^{-1}}{1-z^{-1}}$
ADC
c
d
DAC
z^{-1}
e
Σ
-
Y
Σ
-
$\frac{z^{-1}}{1-z^{-1}}$
ADC
g
Σ
$(1-z^{-1})^2$
f
DAC

General Characteristics

- Very high resolution – 24-bits not uncommon
- Use FETs and capacitors – 1% matching on caps
- No special anti-aliasing filters needed
- First integrator dominates performance
  - Noise (flicker and thermal)
  - Settling
  - Gain
  - offset
- Very tolerant to comparator characteristics
- Opamp gains on order of OSR
- No missing codes
- High linearity
- Inputs overload modulator (SNR/SDR plummet) as input approaches Vref – some architectures do not recover well
- Idle-channel tones are inherent – dithering eliminates

Design Methods

- Numerical simulation in C, Matlab, etc. to explore architecture and sensitivity to non-idealities
- Simulations of integrators
- Simulations of modulator and FFT output bit-stream – time consuming
- Integrator characteristic table based methods help

Recent Activity

- A 12mW ADC Delta-Sigma Modulator With 80dB of Dynamic Range Integrated in a Single Chip Bluetooth Transceiver
- A 1.8V Delta-Sigma Modulator Interface for an Electret Microphone With On-Chip Reference
- A 5mW Sigma-Delta Modulator With 84dB Dynamic Range for GSM/EDGE
- A Wideband CMOS Sigma-Delta With Incremental Data Weighted Averaging
- A 13.5mW 185Msps Delta-Sigma Modulator for UMTS/GSM Dual-Standard IF Reception
- A 2.5V Sigma-Delta Modulator for Broadband Communications Applications
- A Fourth-Order Bandpadd Delta-Sigma Modulator Using Second-Order Bandpass Noise-Shaping Dynamic Element Matching
- A 1V 10MHz Clock Rate 13-bit CMOS Delta-Sigma Modulator Using Unity Gain Reset Opamps
- A 113dB DSD Audio ADC Using a Density Modulated Dithering Scheme
- A 10-300MHz IF-Digitizing IC With 90-105dB Dynamic Range and 15-333KHz Bandwidth
- A 3.3mW Sigma-Delta Modulator for UMTS in 0.18um CMOS With 70dB Dynamic Range in 2MHz Bandwidth
- A 64MHz Clock Rate Sigma-Delta ADC with 88dB SNDR and –105dB IM3 Distortion at 1.5MHz Signal Frequency
- A 0.7V MOSFET-Only Swicthed Opamp Sigma-Delta Modulator in Standard Digital CMOS Technology
- Superconducting Bandpass Delta-Sigma Modulator With 2.23GHz Center Frequency and 42.6GHz Sampling Rate

Low-Power, Multi-bit with DEM, Non switched-cap are current areas of interest

Quiz

- Sigma-Delta are attractive because
  - It is a cool fraternity
  - It is used in telecommunications
  - It is easily integrable in CMOS
  - It requires no analog design

Quiz

- Sigma-Delta can be difficult to design because
  - Computers are not big enough or fast enough
  - They are non-linear circuits with no closed form solution
  - They use capacitors
  - No one really knows how they work

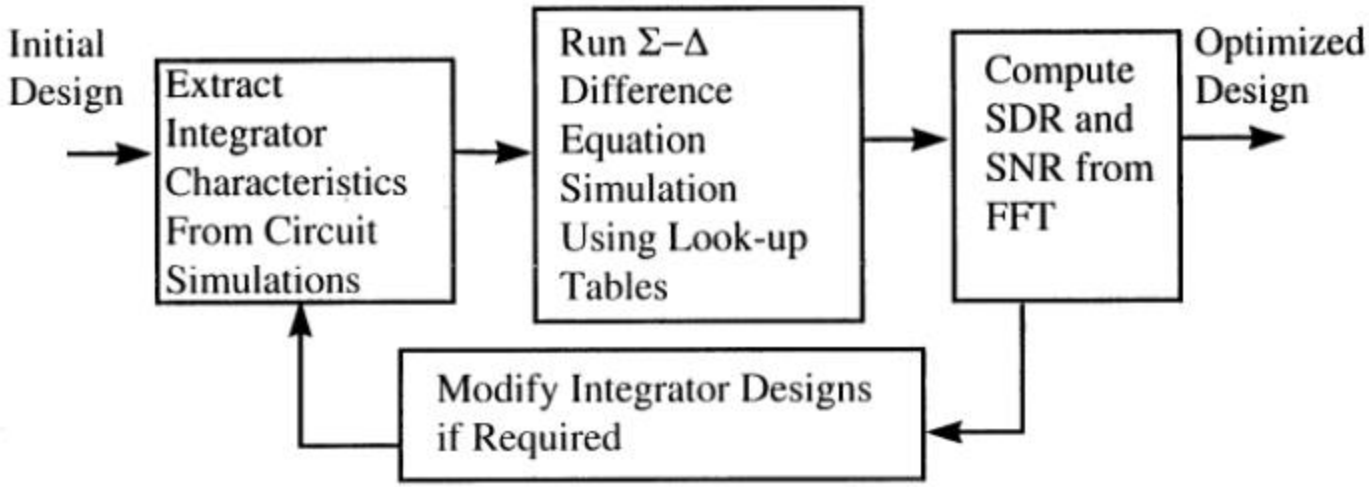
Quiz

- Which limits Sigma-Delta distortion most
  - Capacitor non-linearity
  - Integrator settling
  - Finite opamp gain
  - Comparator offset
  - noise

Research Objective

- Advance Σ–Δ Design and Test Methods
- Improve Design Methods for Automated Optimization of Σ–Δ
- Provide Insight into the Critical Integrator Non-Linearities which Degrade Σ–Δ Performance
- Develop Signal-to-Distortion Ratio (SDR) and Signal-to-Noise Ratio (SNR) Prediction Methods for Improved Σ–Δ Design and Test

Limitations of Current Methods for Σ–Δ Design Optimization



- Requires Σ–Δ Difference Equation Simulation and FFT for Many (64K) Clock Cycles
- Integrator Design Modification Guided by Performance Gradients Only
- Look-up Table Data Cannot Directly Guide Design Optimization

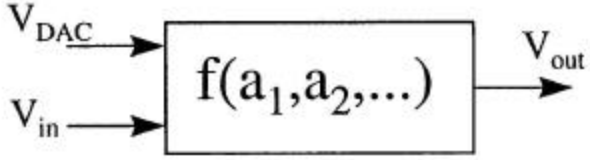
Techniques Employed

- Non-Linear Integrator Model
  - Models Realistic Integrator Non-Linearities
  - Accurately Represents Integrator Transfer Function Compared to SPICE Simulation
  - Captures Nature of Non-Linearities; Aids in Guiding Design Optimization
- Multi-Parameter Sampling Methods
  - Linear Search Sampling
  - Improved Linear Search Sampling
  - Gibbs Sampling
- Genetic Algorithm Surface Fit Optimizer
  - Determine Optimal Surface Equation Terms for Predicting SDR and SNR

Approach Overview

Σ–Δ "C" Program

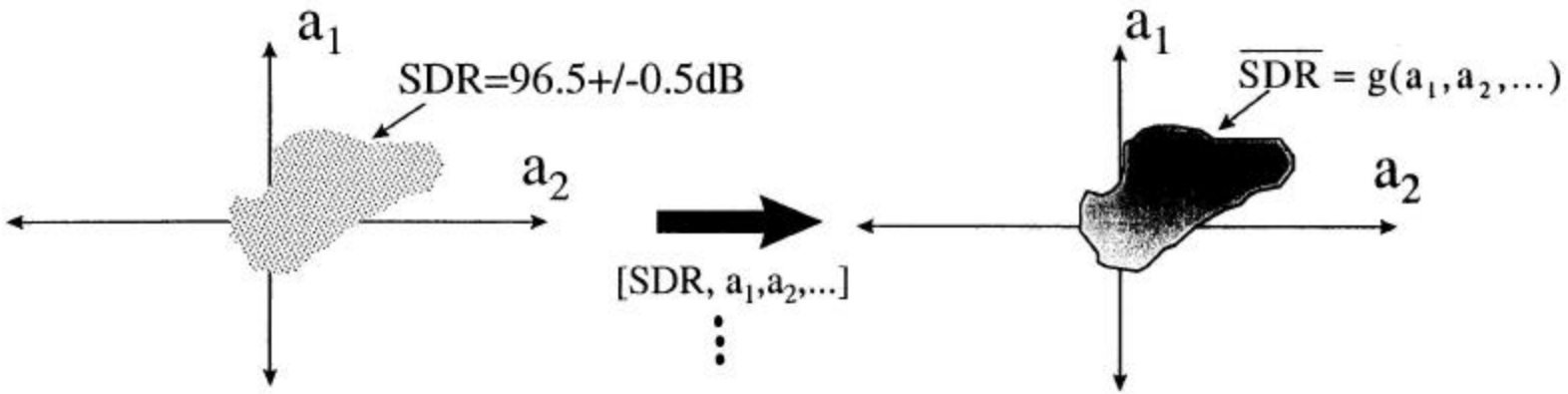
Non-Linear Integrator Model
Non-Linearity Described by $(a_1,a_2,...)$



Generates Samples on Equi-SDR Surface
In Integrator Non-Linearity Space

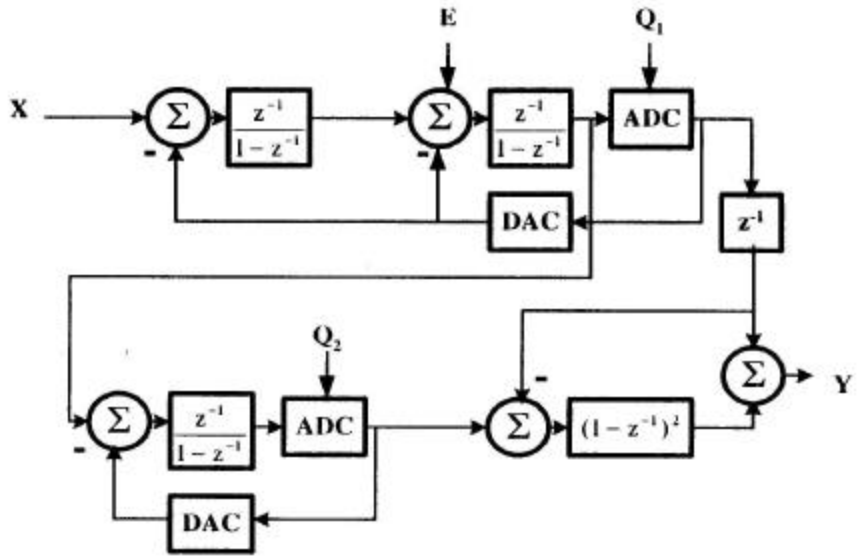
Genetic Algorithm Surface Fit Optimizer

Determines Optimal Polynomial Equation $g(a_1,a_2,...)$ for Predicting SDR Given Integrator Non-Linearity Parameters $a_1,a_2,...$



SDR Predicted Using $a_1,a_2,...$ Determined from Integrator SPICE Simulations

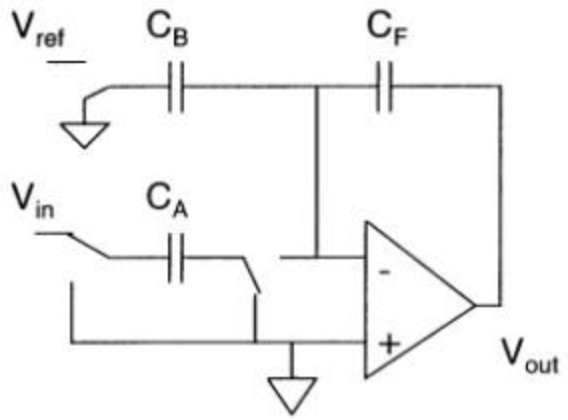
Effects of Integrator Non-Linearity



$$Y = z^{-3}X + Q_2(1-z^{-1})^3 + E(1-z^{-1})^2$$

- Errors Due to Integrator Non-Linearity Add Spectrally Shaped Noise
- Modulator Noise Transfer Function "Leaks" Lower Order Shaped Noise to Output
- Effects Difficult to Analyze Due to Non-Linearity of Quantizer
- Difference Equation Numerical Simulations Extensively Used to Determine SNR and SDR Performance

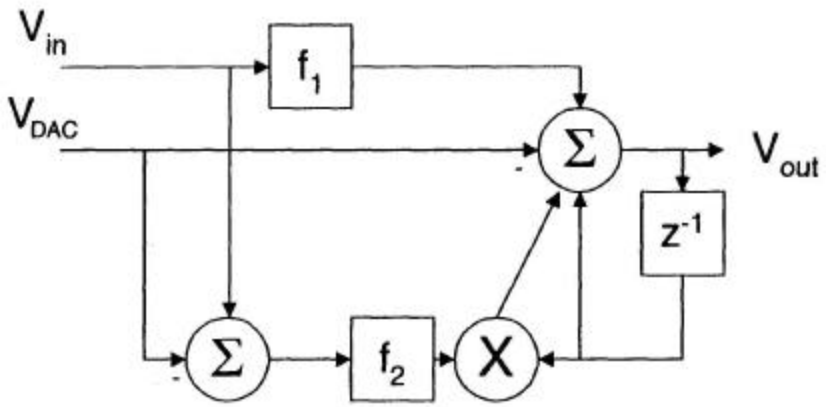
Switched Capacitor Integrator



$$V_{out} = \frac{C_A}{C_F} V_{in} - \frac{C_B}{C_F} V_{ref} + V_{out} z^{-1}$$

- Effects Such as Non-Linear Capacitors and Channel Charge Injection from Sampling Switches Contribute to Sampling Related Non-Linearity
- Incomplete Settling and Opamp Non-Linearity Contribute to Integration Related Non-Linearity
- These Non-Linearities Degrade SDR and SNR

New Integrator Model

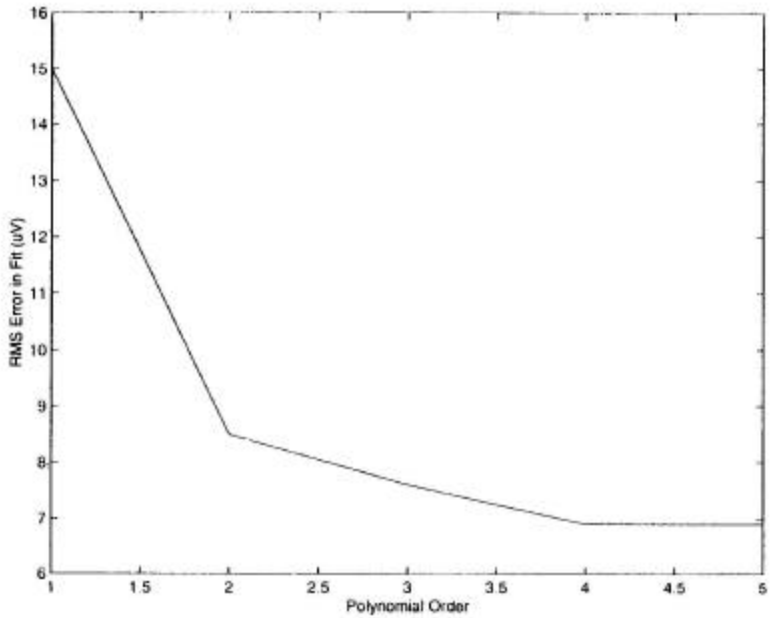


$f_1 = f(a_1, a_2, a_3)$

$f_2 = f(a_4, a_5, a_6, a_7)$

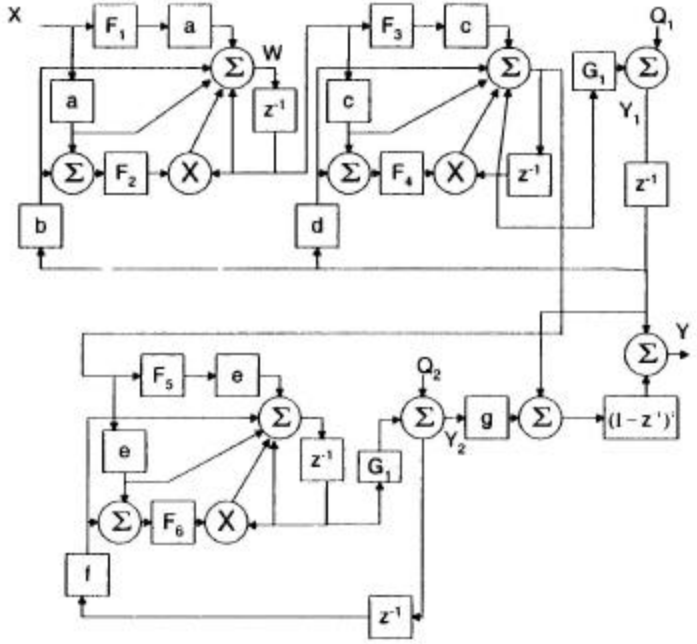
- Numerical Model for Use in "C" Program Difference Equation Σ–Δ Simulator
- Add Non-Linearity to Ideal Integrator
- Sampling Related Non-Linearity $f_1(V_{in})$
- Integration Related Non-Linearity $f_2(V_{in}-V_{DAC})$
- Parameters of f_1 and f_2 are $a_1, a_2, \ldots$

Model Testing



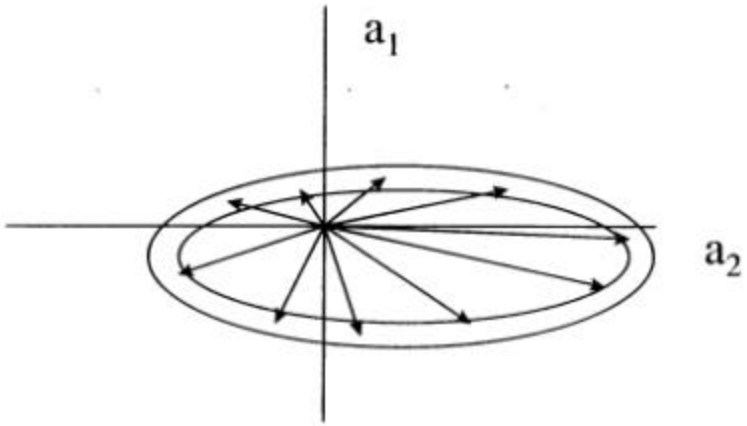
- Three Integrators Simulated to Obtain Model Coefficients for Eight Case Screening DOE (Seven Process and Environmental Factors)
- Aggregate Error of Less Than $10\mu V_{rms}$ in Fit to Simulation Data
- Coefficients of f_1 Substantially Larger for Single Ended Input Cases from DOE - Reflect Even Ordered Harmonics Due to Capacitor Non-Linearity
- Coefficients of f_2 Substantially Larger for Low Bias Current, High Capacitance, and High Temperature Case in DOE - Reflects Slow Settling

SOFOC2 With Non-Linear Integrators



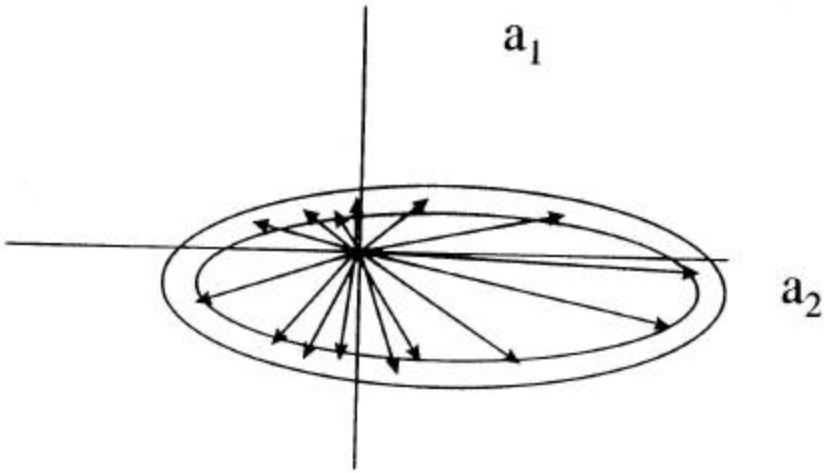
$$
\begin{aligned}
Y &= gQ_2(1-(1+F_6)z^{-1})(1-z^{-1})^2 \\
&\quad + Q_1 z^{-1}\left[(1-(1+F_4)z^{-1})(1-(1+F_2)z^{-1}) - (1-z^{-1})^2\right] \\
&\quad + Xz^{-3} + F_1 z^{-3} + G_1 F_3 z^{-1}(1-(1+F_2)z^{-1}) + G_2 e F_5 (1-z^{-1})^2
\end{aligned}
$$

Linear Search Sampling



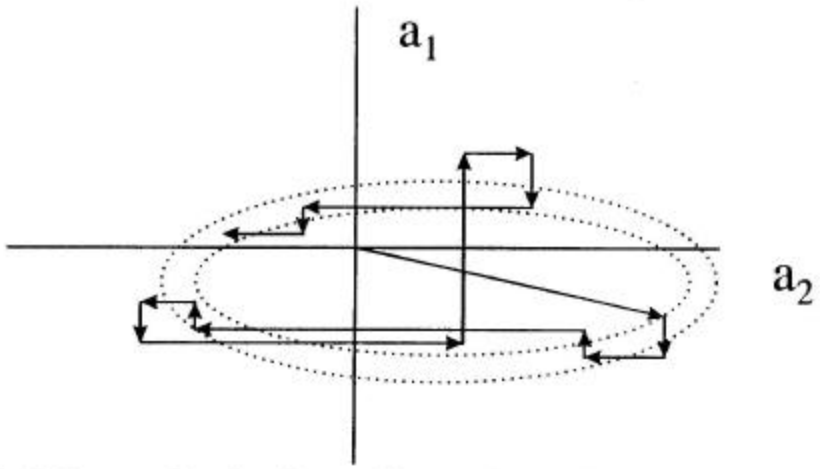
- Sample Space of Coefficients (a_1,a_2,...) of f_1 and f_2 for Integrators
- Monte Carlo Based Linear Search Sampling Method
- Random Vector Chosen in Coefficient Space of f_1 and f_2 for the Integrators in Difference Equation Σ–Δ Simulator
- Vector Extends or Contracts Until SDR/SNR Near Goal
- 2000 Modulator Instances - Integrator Non-Linearity Coefficients (a_1,a_2,...) and Resulting SDR/SNR

Improved Linear Search Sampling



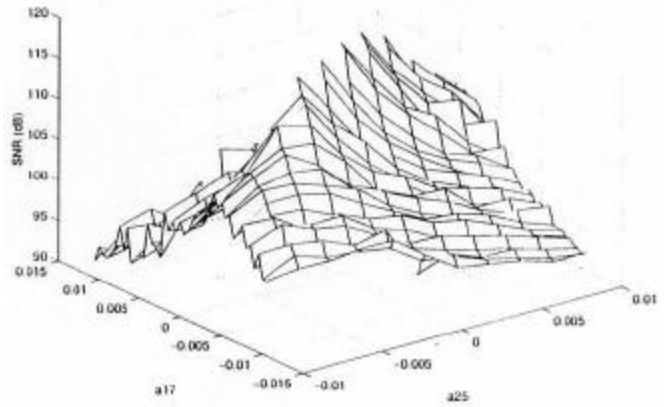
- Applies Random Weight to f_1 and f_2 Before Linear Search
- Increases Sampling Along Minor Axis
- Allows Less Sensitive Parameters to Impact SNR and SDR Improving Their Representation in the Sampled Data

Gibbs Sampling



- Markov Chain Monte Carlo Sampling Method
- Uses Prior Distributions and Desired SDR/SNR Distribution
- Uses Conditional PDFs of Generated Samples to Improve Likelihood that Drawn Samples are From Desired Distribution
- Converges to Desired Distribution (Metropolis and Hastings)
- Modified MCSIM (Bois and Maszle) Program to Call Difference Equation Σ–Δ Simulator
- Provides Better Control Over Range of Non-Linearity Coefficients (a_1,a_2,...) Sampled than Linear Search Methods

Effect of FFT Length



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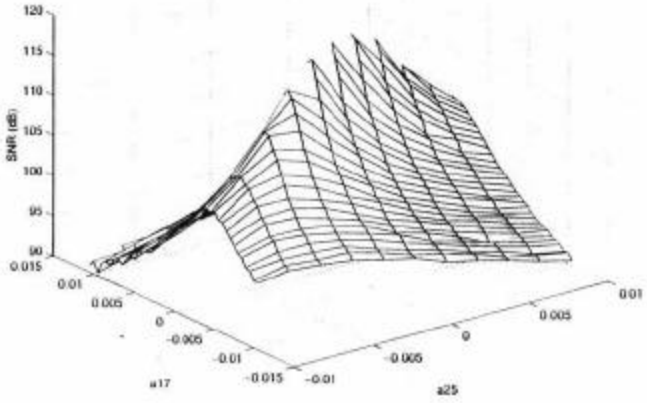


8192pts

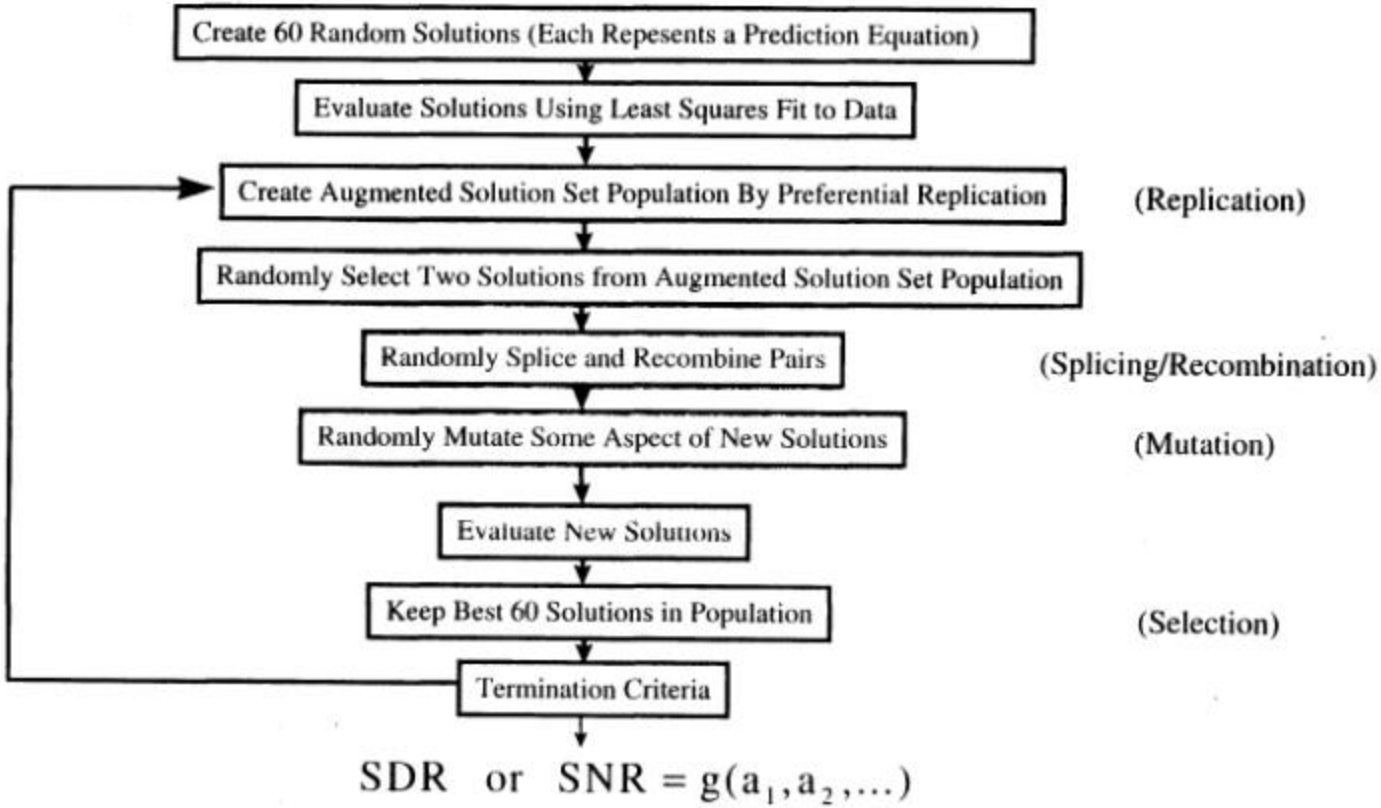
Surface Prediction Equation Fit

- Potentially Many Terms in Polynomial with Several Independent Variables

$$g(a_1, a_2, \ldots) = B_0 + B_1 a_1 + B_2 a_2 + B_3 a_1^2 + B_4 a_2^2 + \ldots$$

- Desire Minimum Number of Terms in Prediction Equation
- Genetic Algorithm Implemented to Determine Optimal Terms for Prediction Equation (Shen and Chen)

Genetic Algorithm Prediction Equation Fit



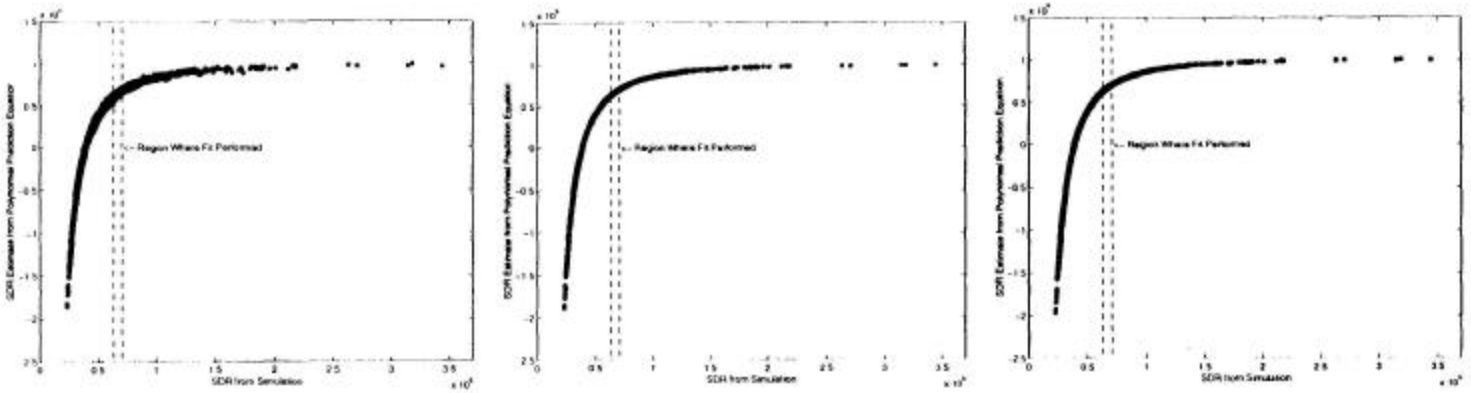
Each Solution Consists of a String of Ones and Zeros Representing the Set of All Possible Terms in Prediction Equation (1=Include, 0=Exclude)

SDR Prediction Equation Terms

Term	Coefficient
a_{11}	-0.029
a_{12}	-0.006
a_{13}	0.050
a_{15}	0.009
a_{17}	-0.004
a_{11}^2	7.300
a_{12}^2	5.758
a_{13}^2	9.972
a_{14}^2	0.004
a_{16}^2	0.002
a_{17}^2	0.001
$a_{11}a_{12}$	-0.003
$a_{11}a_{13}$	-12.701
$a_{11}a_{14}$	0.098
$a_{11}a_{16}$	-0.249
$a_{12}a_{15}$	-0.025
$a_{12}a_{17}$	0.110
$a_{13}a_{14}$	-0.091
$a_{13}a_{16}$	0.201
$a_{13}a_{17}$	0.001
$a_{14}a_{16}$	-0.002

a_{11}, a_{12}, a_{13}
Sampling related errors in 1st integrator

SDR Prediction Equation Accuracy



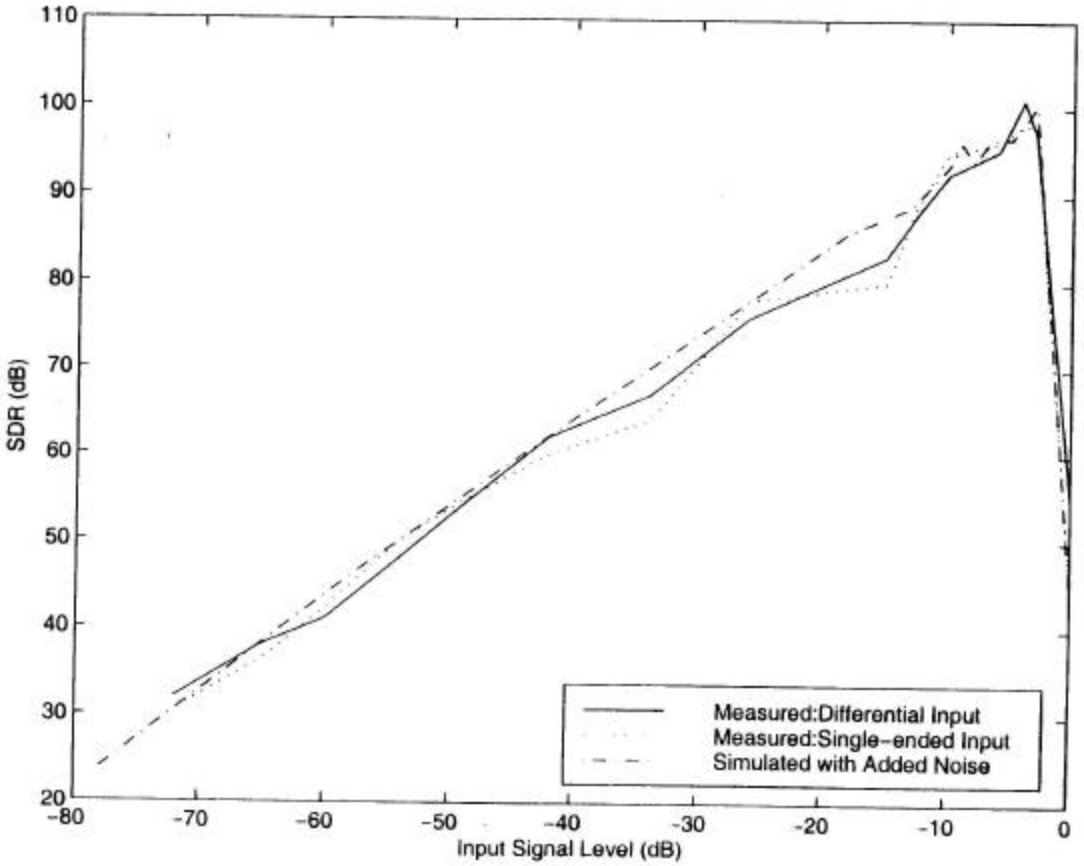
LSS ILSS Gibbs

- Tested with 2000 Modulators with Randomly Chosen f_1 and f_2 Coefficients (a_1,a_2,...) Generated Using "C" Program Difference Equation Simulator (Ranged 87dB to 111dB)
- Linear Search Sampling Makes Gross SDR Prediction Errors (10dB)
- Improved Linear Search Sampling and Gibbs Sampling Predict SDR with +/-0.5dB Accuracy When Non-Linear Relationship Compensated
- Optimal Prediction Equation is a Strong Function of Input Sampling Non-Linearity of First Integrator

SOFOC2 Σ–Δ Test Circuit

- SOFOC2 Third Order Σ–Δ Test Circuit Designed and Fabricated in AMI 0.6μm CMOS Process
- 16-Bit Designed Performance
  - 5MHz Clock Rate (40Ksps at OSR=128)
  - SDR > 96dB
  - SNR > 96dB
- Test Modes for Measuring SDR and SNR Response to Conditions which are Expected to Degrade SDR and SNR
  - Bias Current in First and Second Integrators
  - Common-Mode Output Voltages of First and Second Integrators

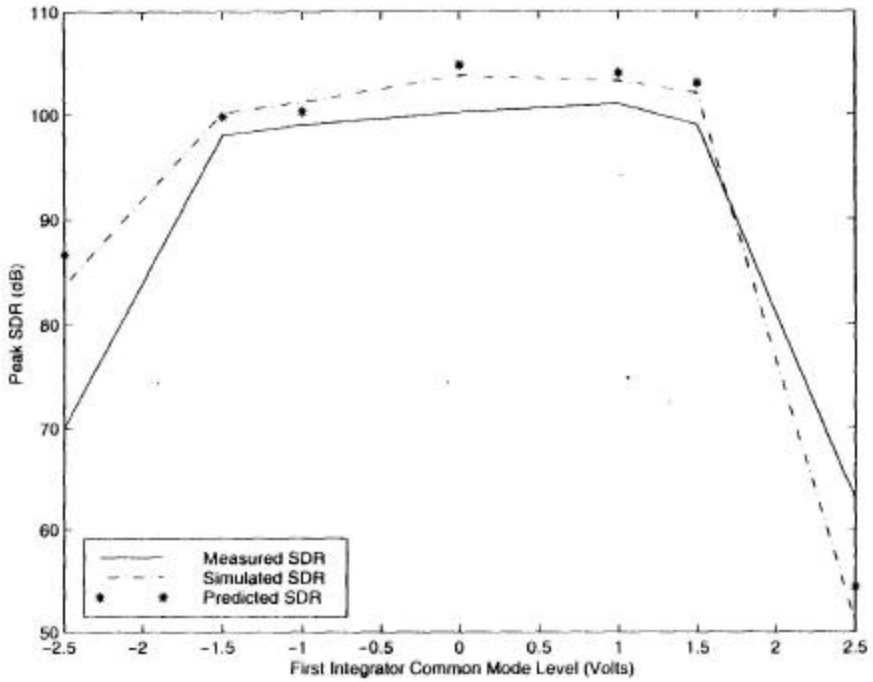
SDR Versus Input Level



Comparison of Measured, Simulated, and Predicted SDR/SDR

- Determined (a_1,a_2,...) from SPICE Simulation of Integrator Circuits Used in SOFOC2 Test Chip for Various Integrator Bias Currents and Common-Mode Output Voltage
- Determine Simulated SDR/SNR Using "C" Program Σ–Δ Simulator with (a_1,a_2,...) from SPICE Simulation
- Calculate Predicted SDR/SNR from Prediction Equations Using (a_1,a_2,...) from SPICE Simulation
- Measure Modulator SDR/SNR for Various Integrator Bias Currents and Common-Mode Output Voltages

SDR Response to First Integrator Common-Mode Output



- SDR Approximately 100dB Between +/-1.5 Volts
- Good Agreement Between Measured, Simulated, and Predicted SDR Versus First Integrator Common-Mode Output Voltage
- Difference at Extremes Due to Integrator Overload

Summary

- Overview of Sigma-Delta
- Method which uses
  - Multidimensional sampling
  - Genetic algorithms
- Showed first stage sampling is critical
- Demonstrated SDR prediction method is reasonably accurate with respect to simulation and measurements