Custom IC Blocks for Enabling Digital Control in Switching Power Converters

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Outline

- Motivations & CoPEC directions
- "Buffalo switcher"
  - Complete 1 MHz digital PWM controller IC
  - Hybrid digital PWM
  - Delay-line A/D
- CoPEC research highlights
- Education:
  - focus on power electronics & mixed-signal IC design

Power Electronics Applications

Portable devices

- On-chip power management /mW
- Power supplies for LCD-s / hundreds of mW
- Switching voltage regulators/ up to tens of Watts

Computers and Consumers Electronics

- Power supplies for components/ several watts
- Micro-processor supplies: Voltage Regulator Modules (VRMs)/ up to hundreds of Watts
- Off-line power supplies / up to kW

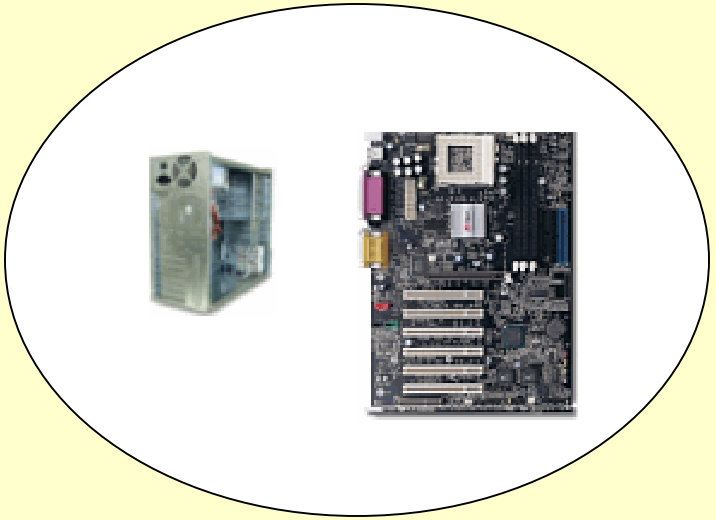
Telecomm. equipment

Industrial

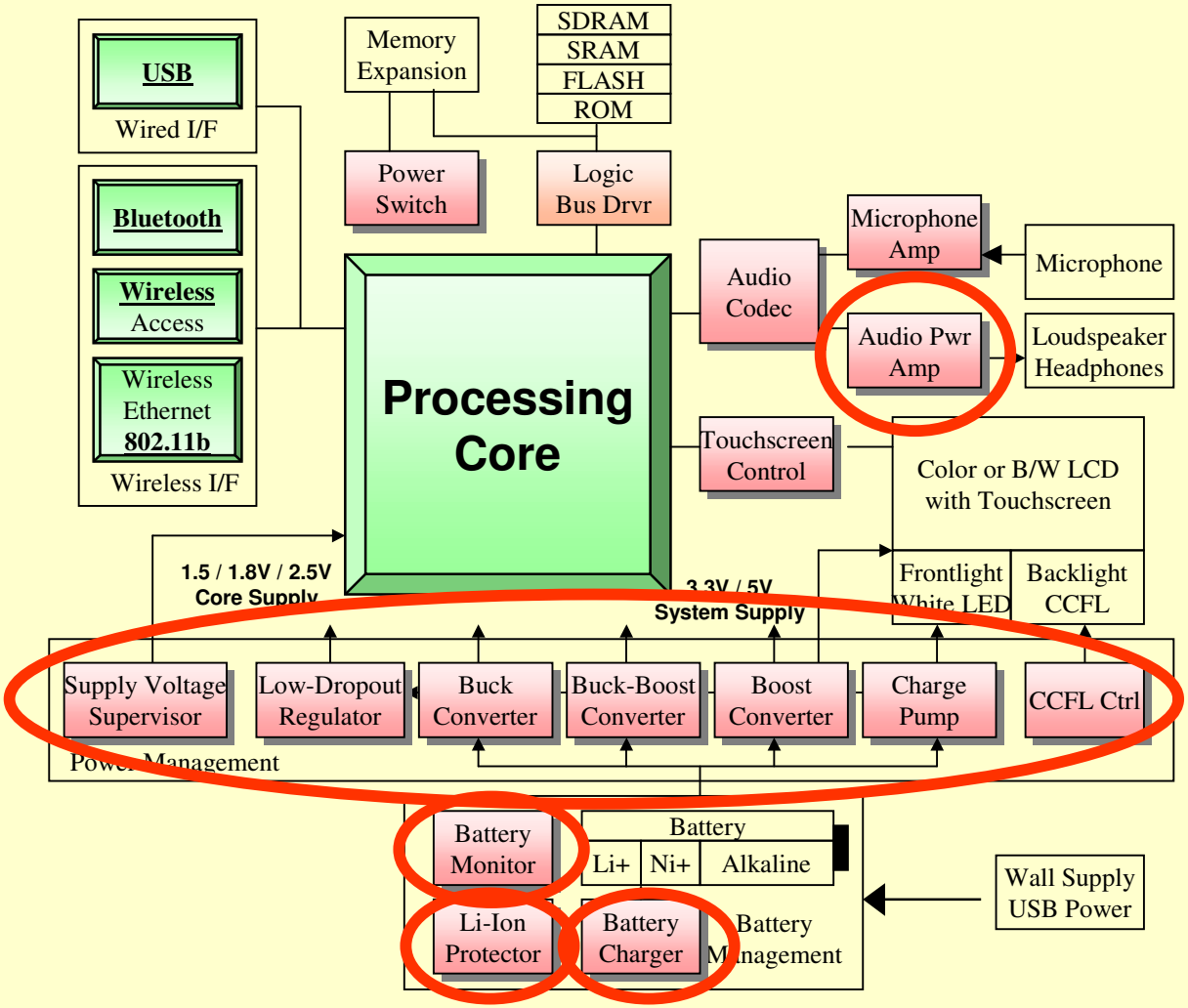
Automotive

Lighting (HID, fluorescent)

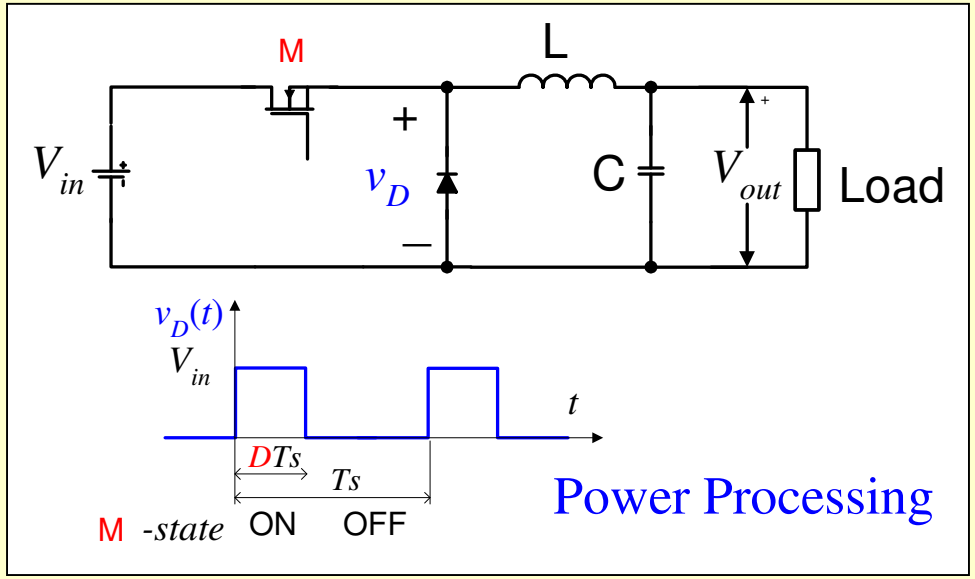
Aerospace

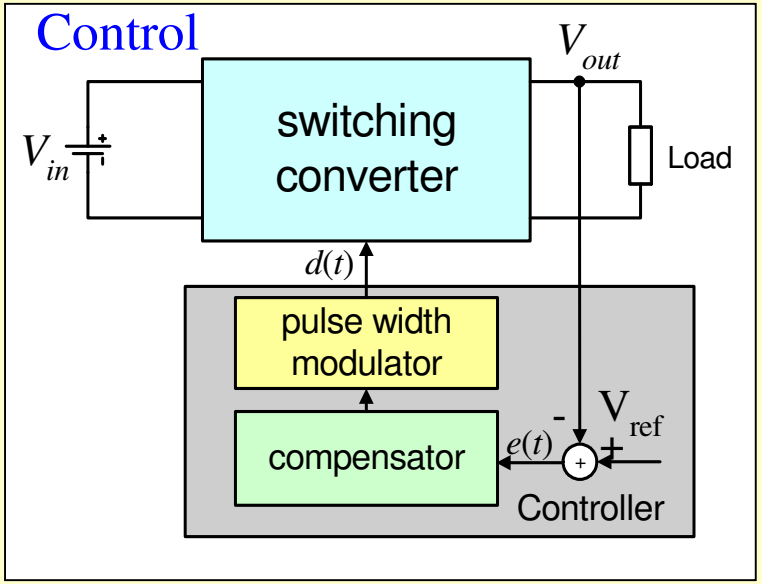


PDA Example: Power Management



Buck Switching Converter Example





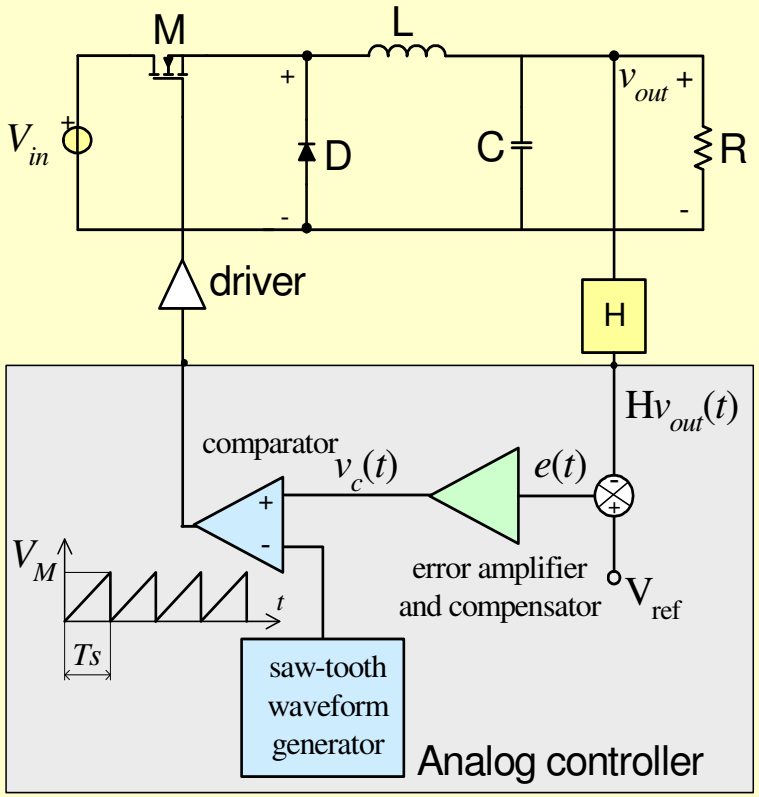
$$V_{out} = DV_{in}$$

Duty ratio

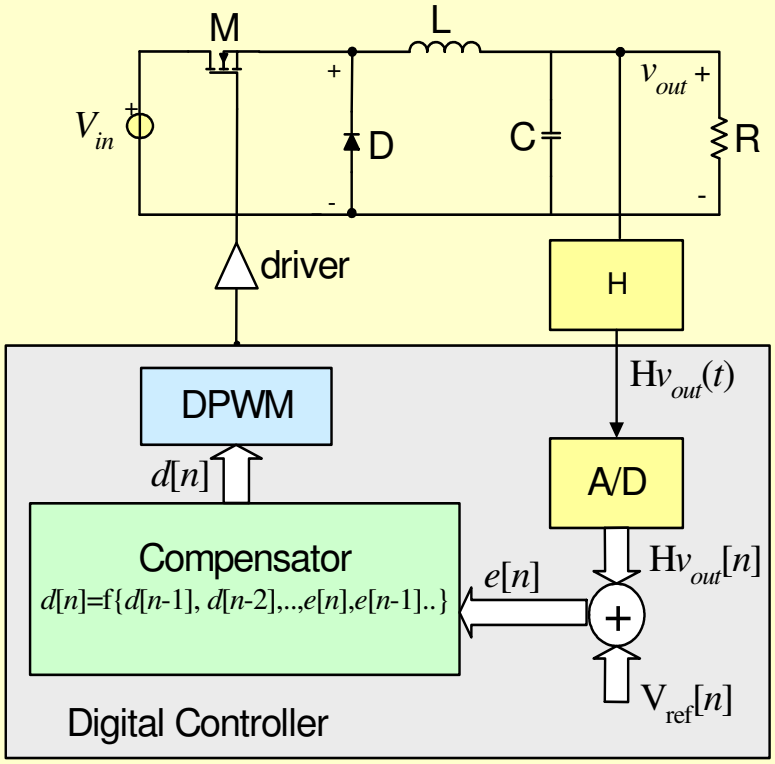
- Switching operation controls the average value of v_D
- LC low-pass filter reduces the voltage ripple in the dc output V_{out}
- High switching frequency (hundreds of kHz to MHz), small size
- Ideally lossless, very high efficiency in practice
- Tightly regulated V_{out} through a feedback loop

Controller Implementation: Analog vs. Digital

Analog Implementation



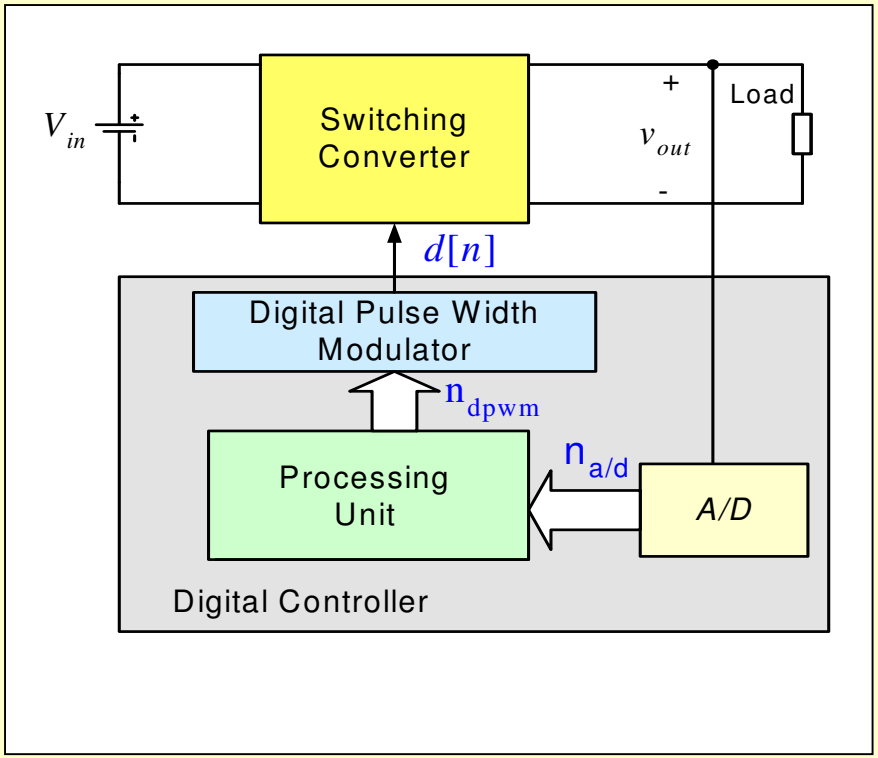
Digital Implementation



Research Motivation – Why Digital?

- Analog PWM controllers (30 year old technology)
  - Simple, low-cost
  - Well established design practices
- What can be accomplished with digital control in power electronics applications?
  - Programmability (e.g. one controller can serve a much wider range of applications)
  - Elimination or reduction of the number of passive components
  - System integration (e.g. dynamic voltage scaling), diagnostics, etc.
  - Static and dynamic performance (e.g. through adaptive control techniques)
  - Reduced sensitivity to tolerances, process and temperature variations
  - Reduced cost

Practical Limitations



- A/D –A complete analog controller could be simpler than a high-speed, high-resolution A/D
- Processing unit -Available microcontroller/DSP systems are still too slow, or too complex/costly
- DPWM – High-speed/ High-resolution (ns) digital pulse width modulators are needed

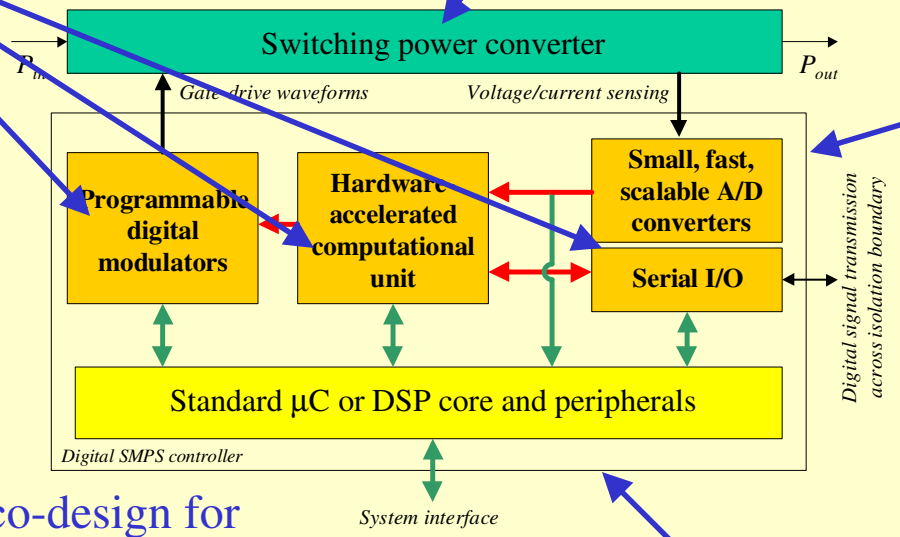
New design and implementation approaches for all functional blocks are needed

CoPEC Research Program

Power Electronics and Mixed-Signal IC Design

New SMPS-specific controller building blocks

New converter configurations tied to more sophisticated control techniques



New controller architectures for wide range of applications

Converter/controller co-design for significant gains in performance, size and/or cost:

- reduced size of passive components
- improved efficiency
- improved dynamic responses, etc.

New control algorithms

- parameter/state estimation
- adaptive control
- nonlinear control, etc.

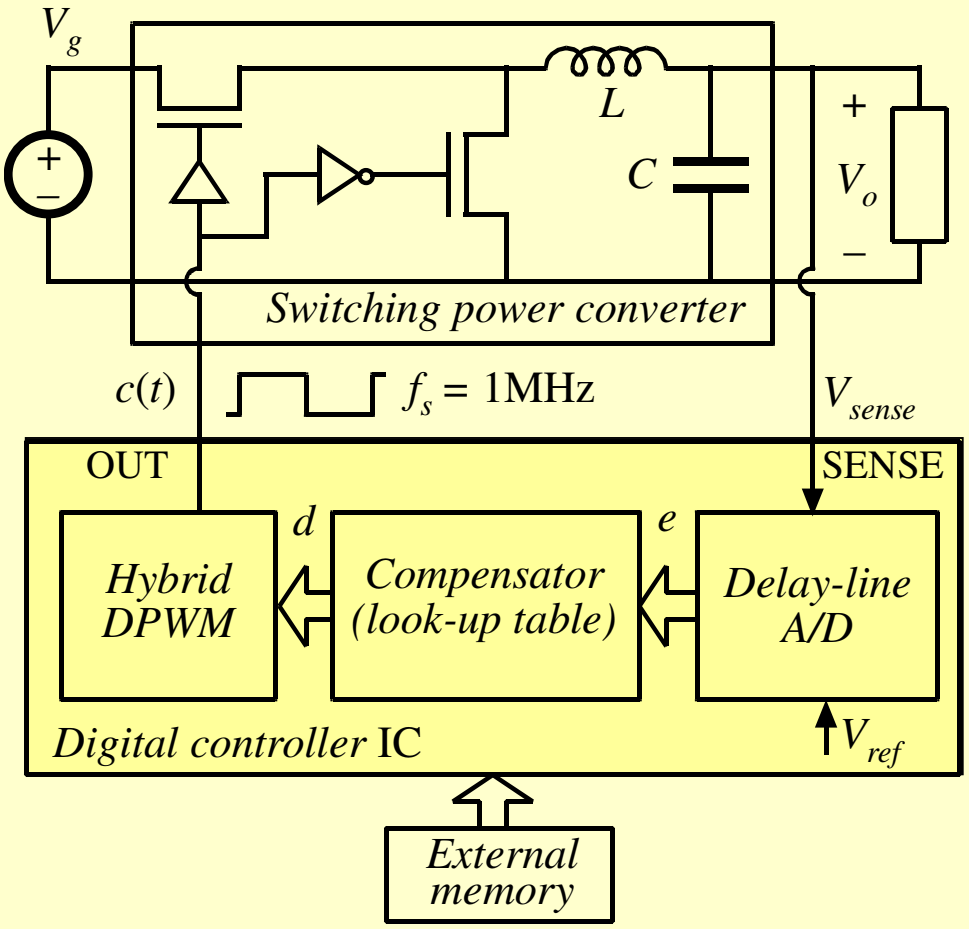
Modeling techniques

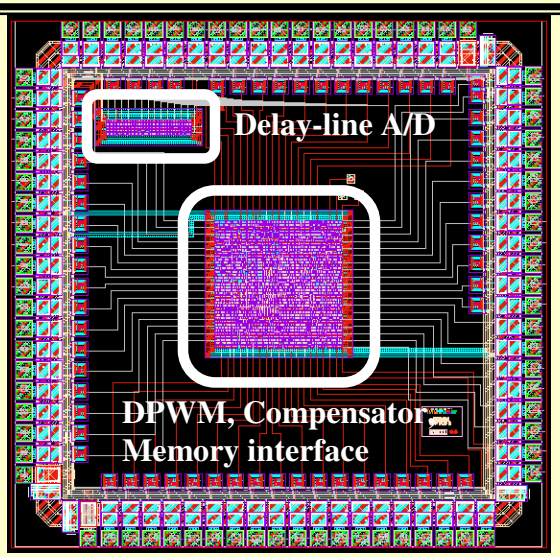
Examples of CoPEC Research Results

- **Complete 1 MHz digital PWM controller IC**
  - small size, programmable compensator, no discretes
- **Standard-cell based A/D converter ICs**
  - small size, fast sampling, scalable with digital technology
- **Digitally controlled 3.3 V, 20 A DC power supply**
  - chipset for isolated DC power supplies
- **Digital predictive current-mode control**
  - very fast response
  - applications to PFC and DC-DC converters
- **Digitally-controlled power-factor correction rectifiers**
  - order-of-magnitude improvement in dynamic response

Buffalo Switcher

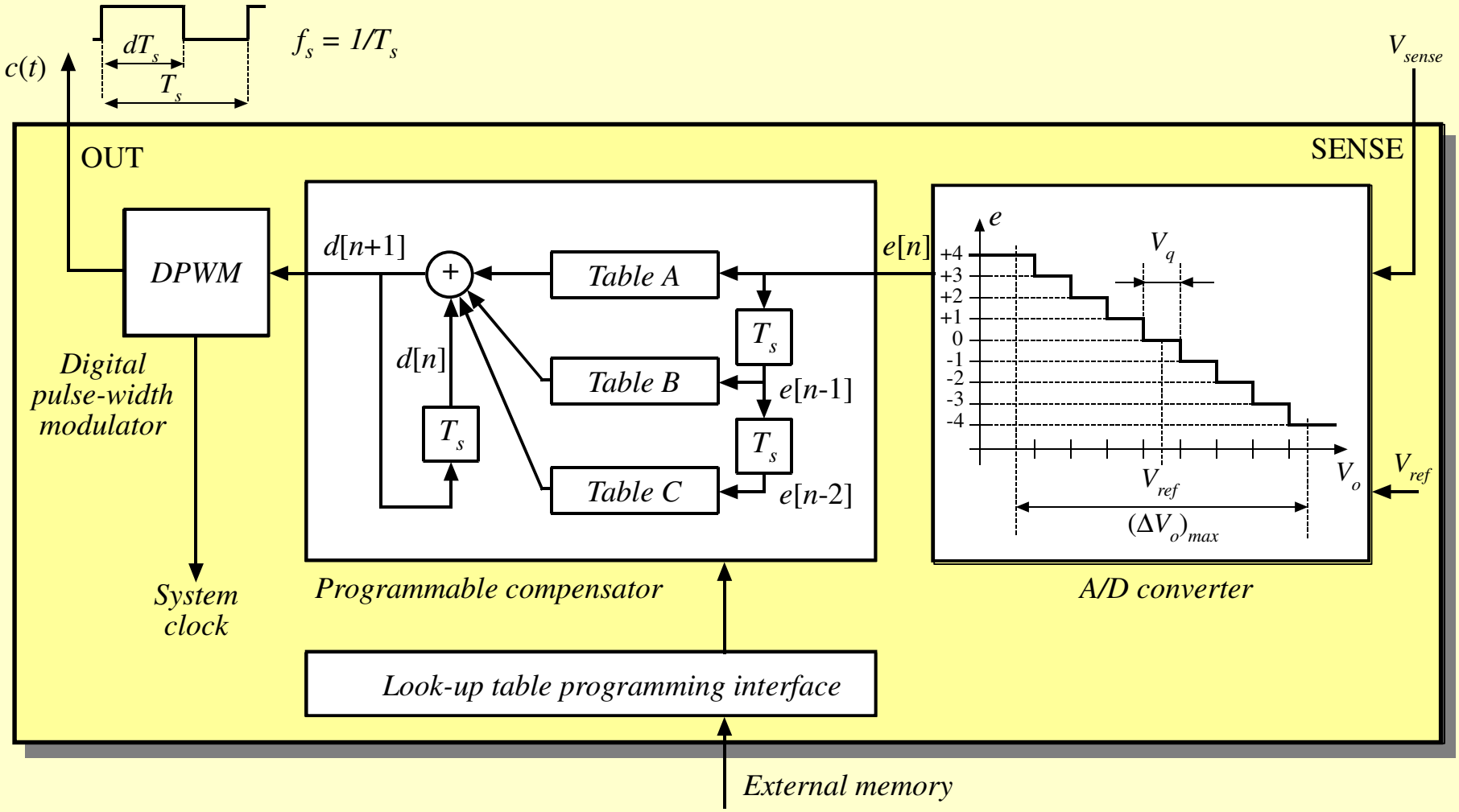
Complete High-Frequency Digital PWM Controller IC





- 1 MHz switching frequency
- Programmable compensator
- 0.5µ CMOS technology
- Chip area: 0.96 mm^2
- All-digital, HDL-based design
- Standard digital design flow:
  - HDL (Verilog) based design
  - Synthesis to standard-cell gates
  - Automated place & route

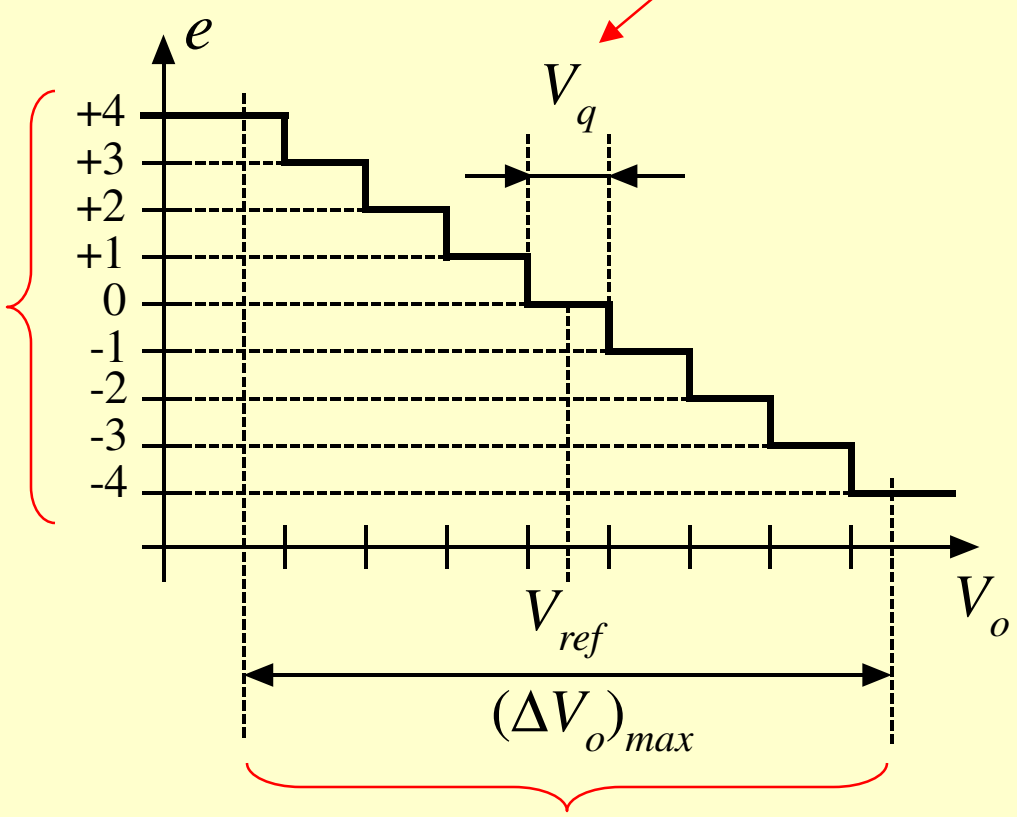
Chip architecture



A/D requirements

Static voltage regulation $\Rightarrow V_q \leq \Delta V_o$

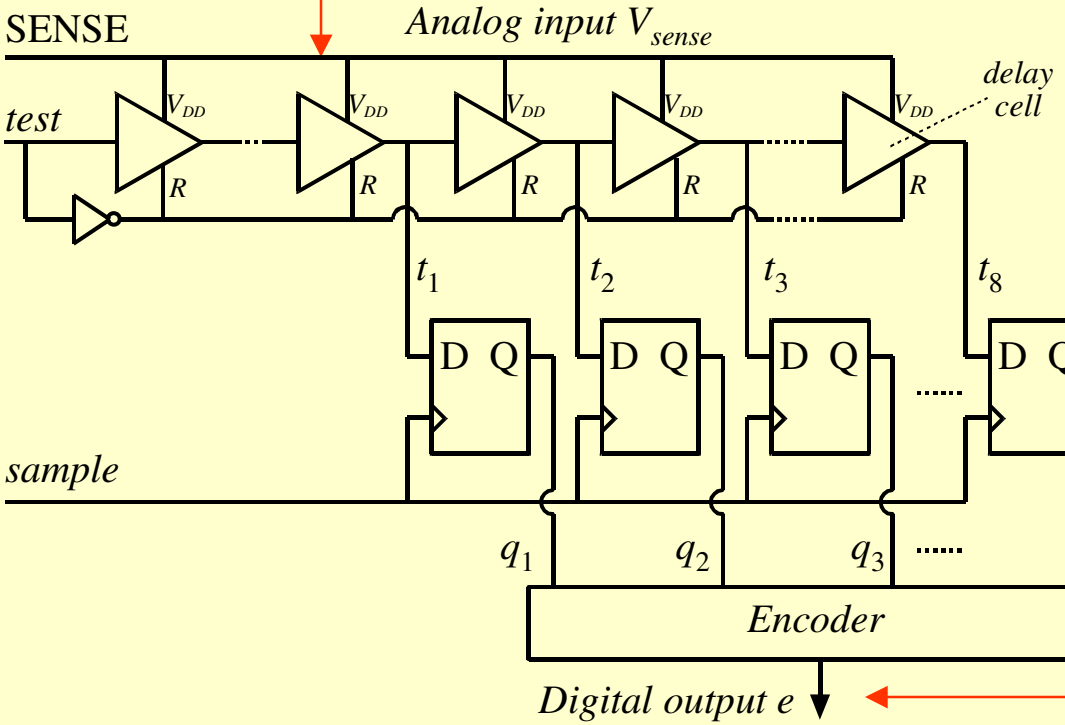
Only a few digital error outputs needed



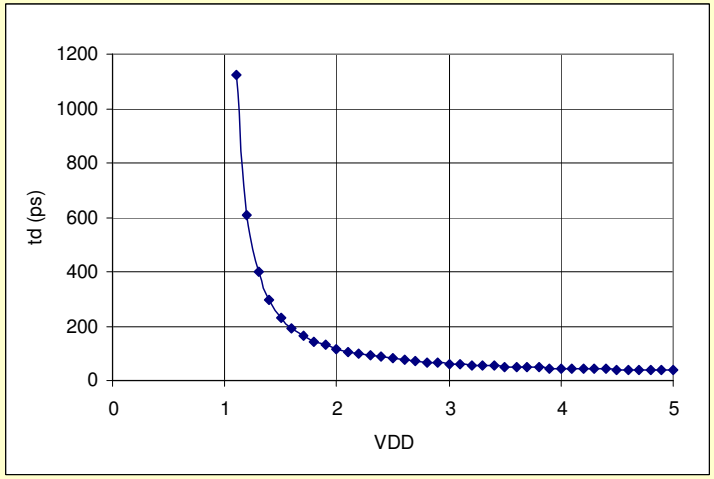
Dynamic voltage regulation $\Rightarrow$ small conversion range

Delay-line A/D

Analog input is the supply voltage VDD for a chain of logic gates



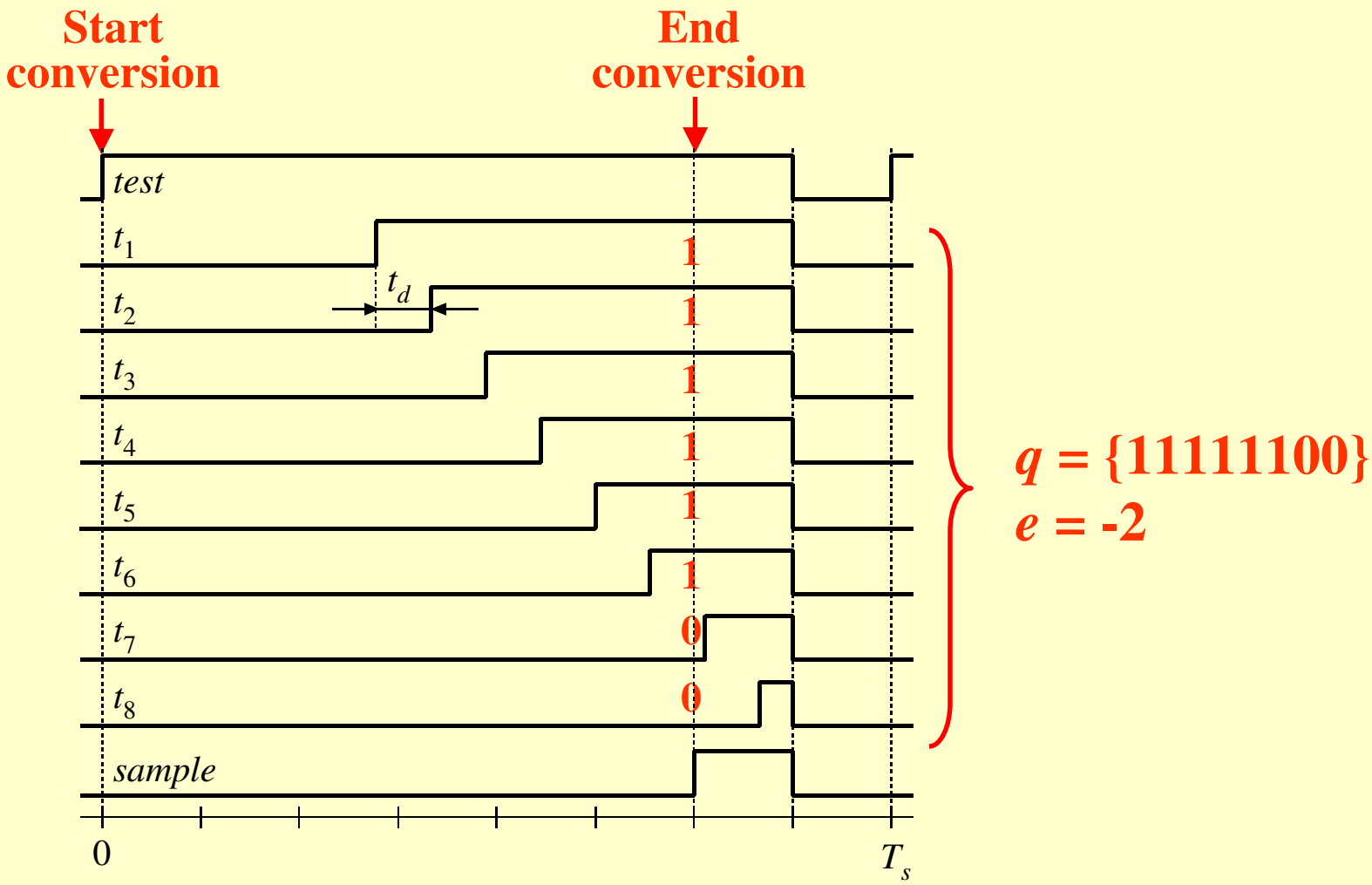
Delay t_d versus VDD



Digital output q (in "thermometer" code)

Digital output e

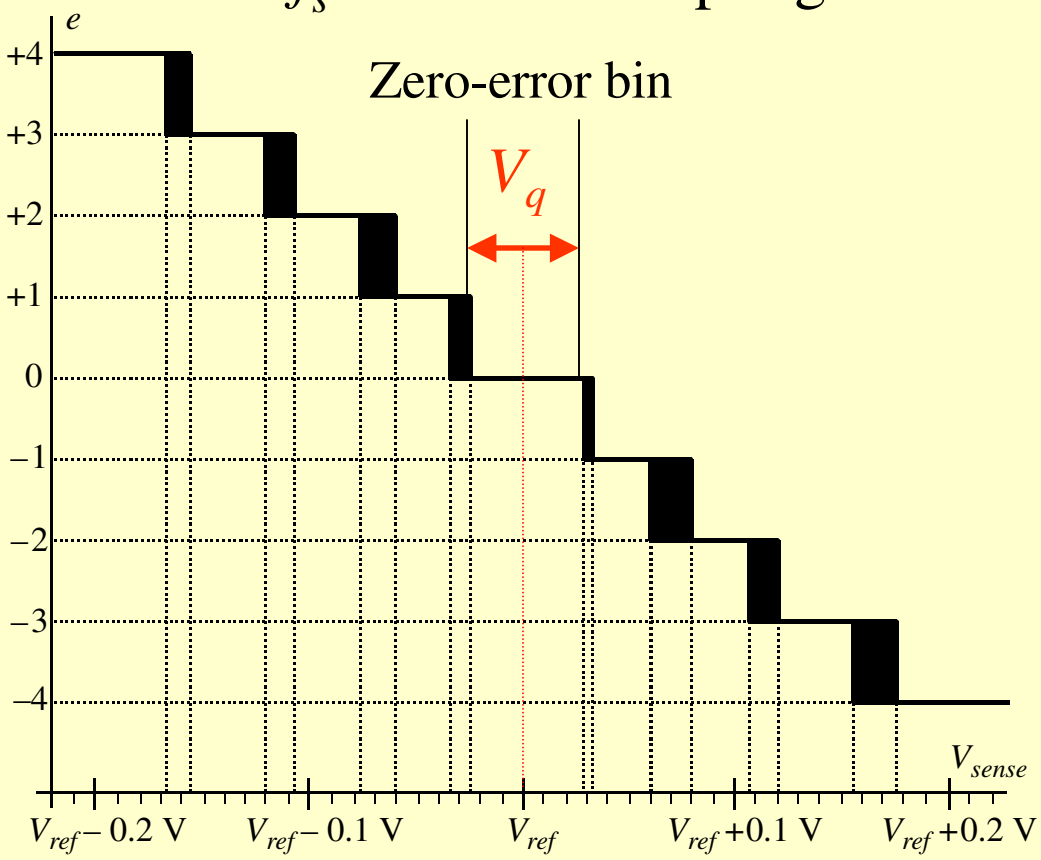
Delay-line A/D Operation



Delay-line A/D Experimental Results

V_q = 53mV, σ = 3.6mV
f_s = 1 MHz sampling

Error e



Sampled output voltage V_{sense}

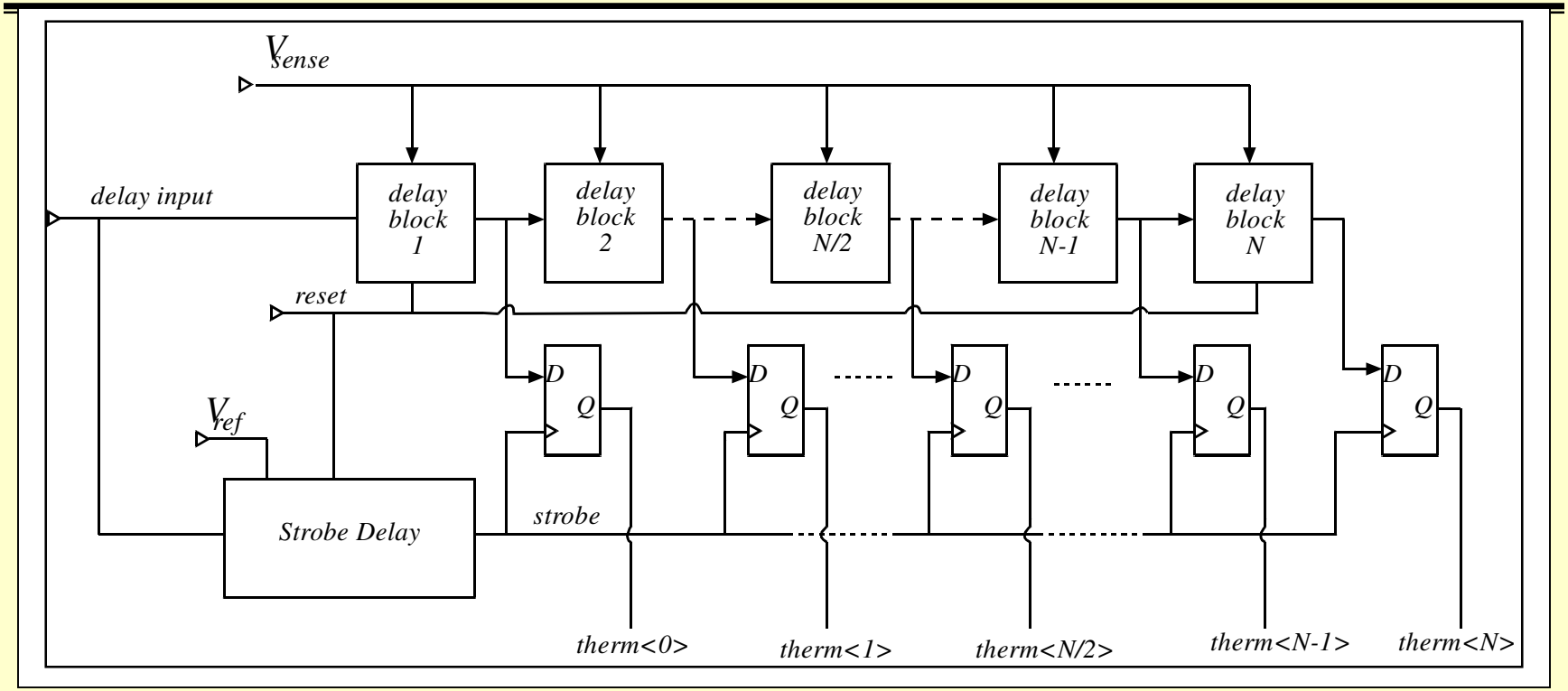
Advantages:

- Small area/low power
- Averaging over conversion time
- All digital implementation

Problem:

- Basic configuration is highly susceptible to process/temperature
- How to implement calibration to a reference voltage?

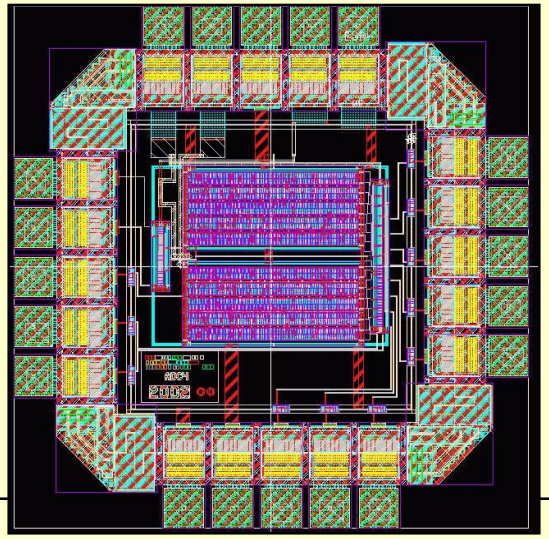
Strobe-Calibrated Delay-Line A/D

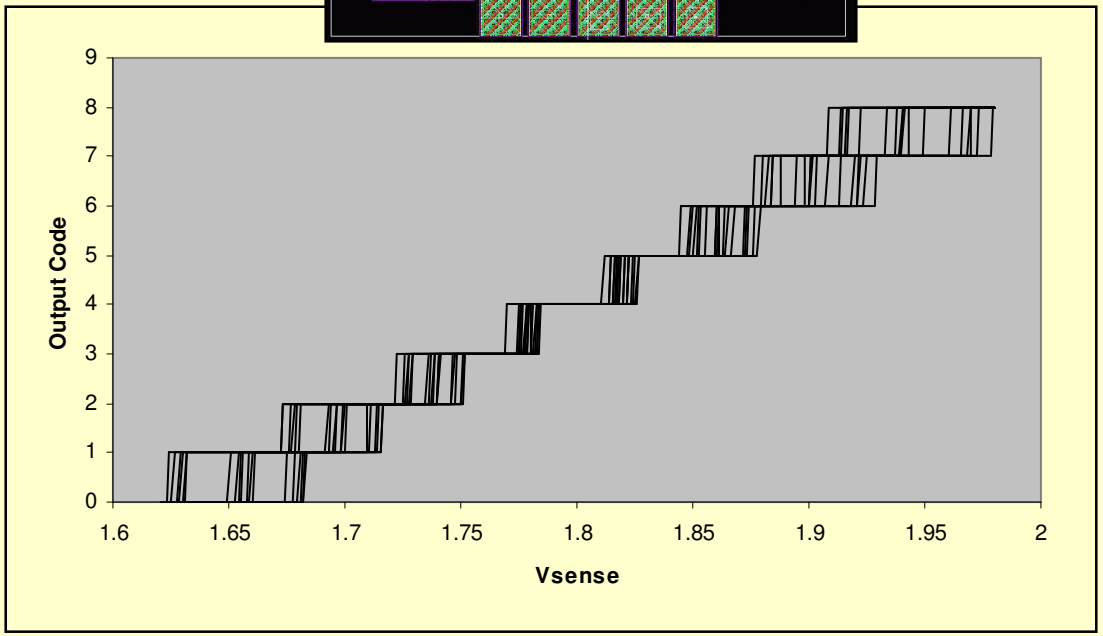


- Delay blocks constructed with standard cells
- Matched “strobe delay” added to provide self-calibrated reference point

Strobe-Calibrated Delay-Line A/D Exp Results

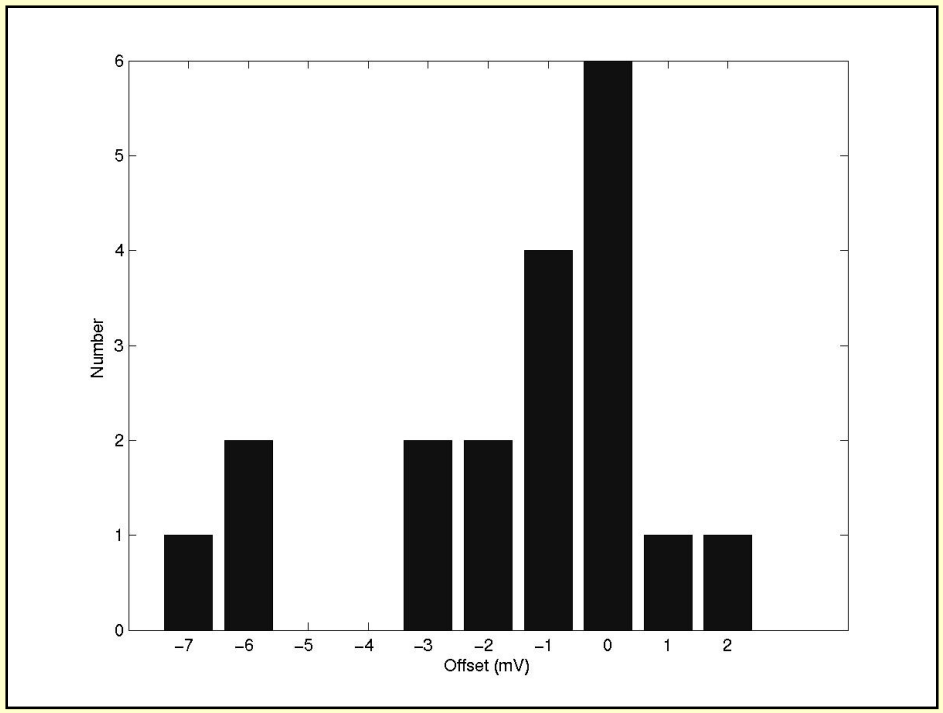
- 1.8 V reference
- 250ns typical conversion time (500ns worst case)
- Standard-cell HDL-based design, 0.5µ CMOS process
- Automated place-and-route of primary and matched delay lines
- Tested over the temperature range from -40ºC to 100ºC





Experimental characteristics over temperature

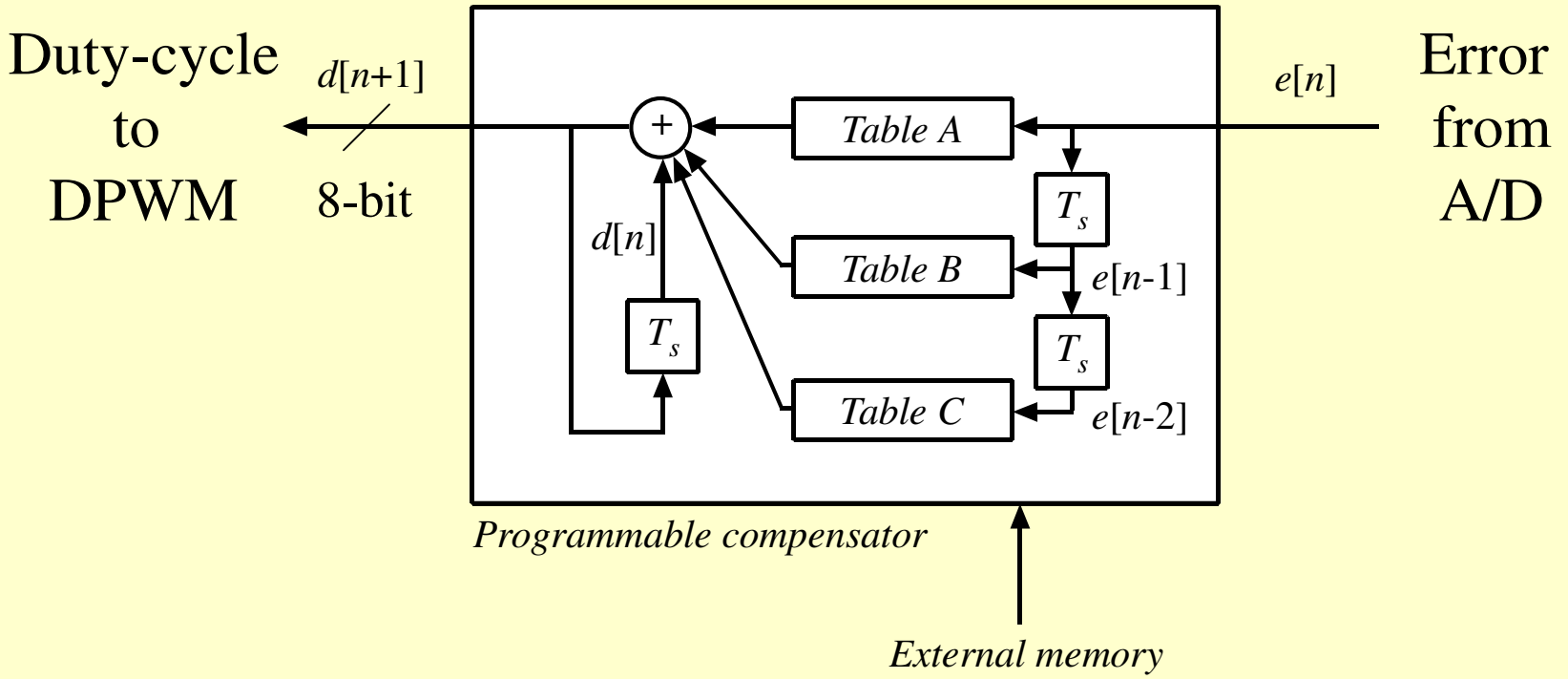
Strobe-Calibrated Delay-Line A/D Exp Results



Histogram of the measured offset over 18 prototype chips

- Average offset: 1.56mV (4% LSB)
- 11 of 18 chips < 2 mV offset
- Good performance holds over temperature
- The worst offset prototype chip of 18 samples at the worst temperature corner: -7.3 mV offset
- Total current consumption:
  - less than 100 µA

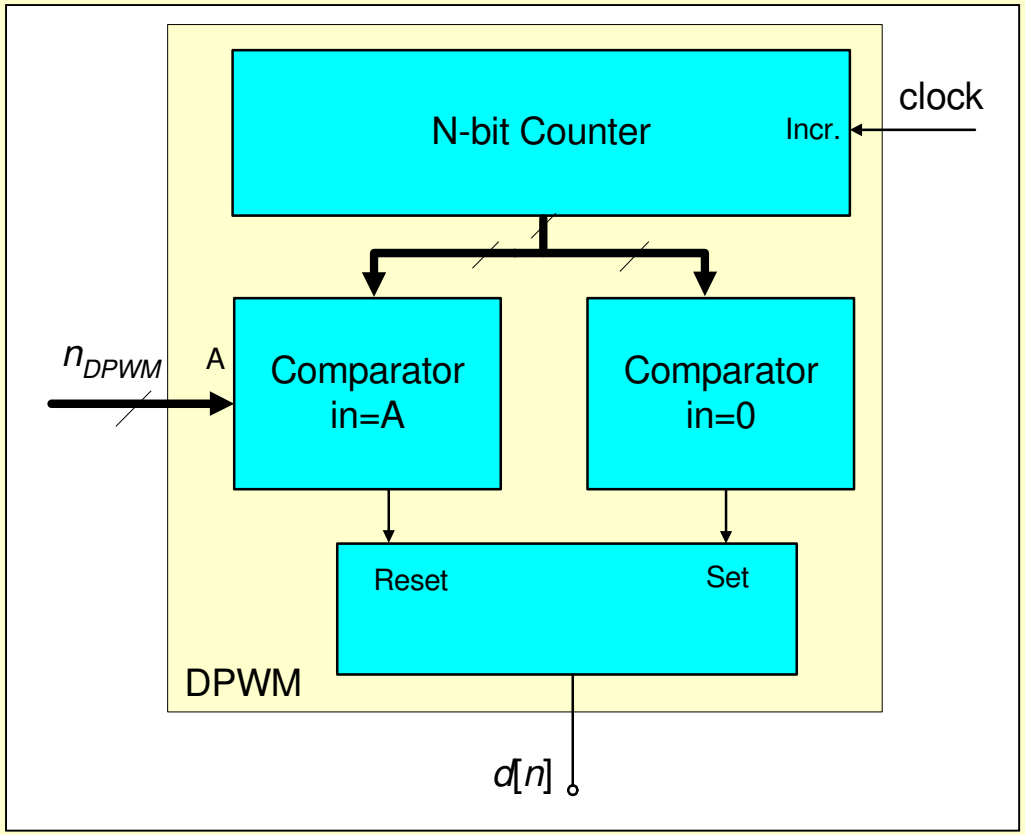
Look-up Table Based Programmable Compensator



PID compensator: $d[n+1] = d[n] + \underbrace{a\ e[n]}_{\text{Table A}} + \underbrace{b\ e[n\text{-}1]}_{\text{Table B}} + \underbrace{c\ e[n\text{-}1]}_{\text{Table C}}$

- "Zero" steady-state error
- Programmable response
- Very small area, very low power

Conventional Counter-based DPWM Design



$$f_{clk} \geq 2^{N_{DPWM}} \cdot f_s$$

f_{sw}: switching frequency
f_{clk}: processor clock frequency
n_{DPWM}: number of bits of DPWM

10-bit @ 1 MHz => 1 GHz clock signal!?

High-Resolution Hybrid DPWM

Combines a delay line (ring oscillator) with a counter to reduce the maximum clock speed

Conventional DPWM:

$$f_{clk} = 2^n \cdot f_s$$

Hybrid DPWM:

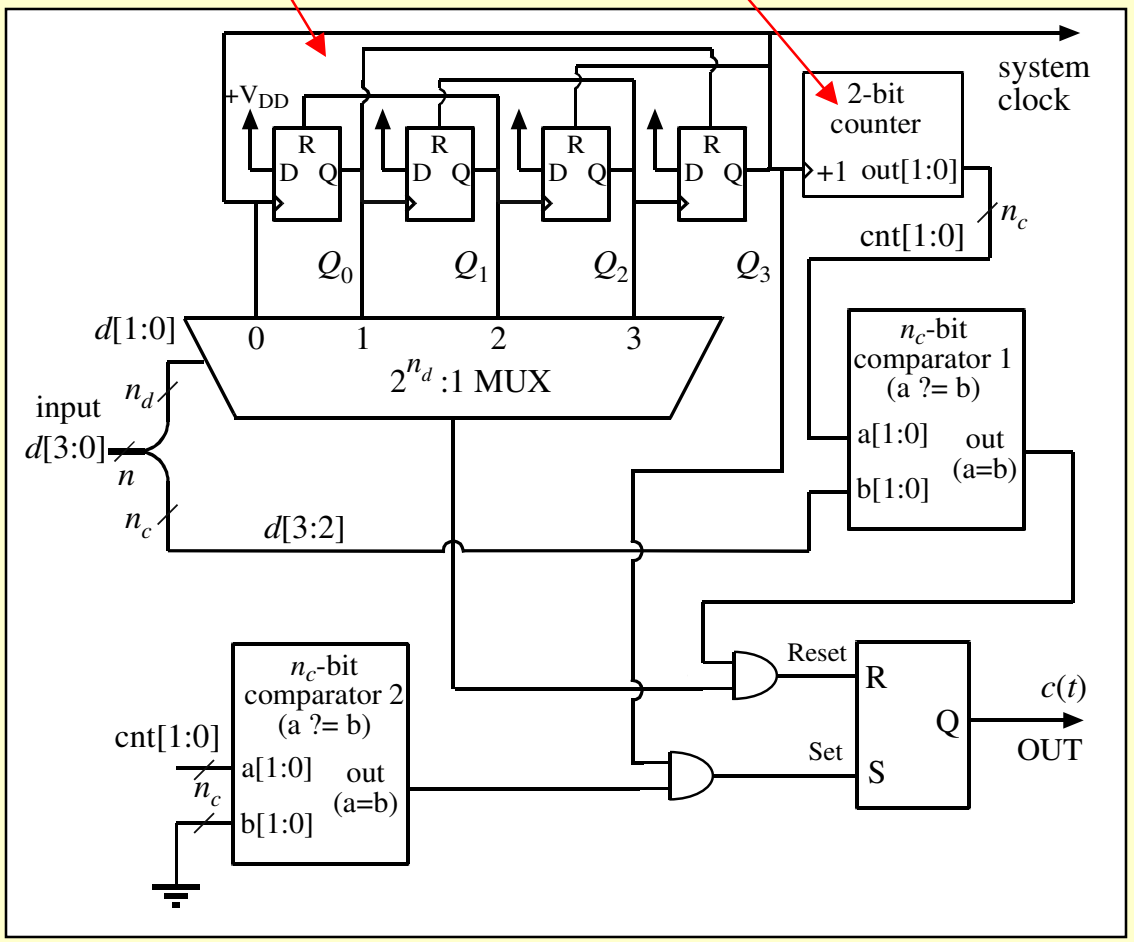
$$f_s \le f_{clk} \le 2^n \cdot f_s$$

Prototype:

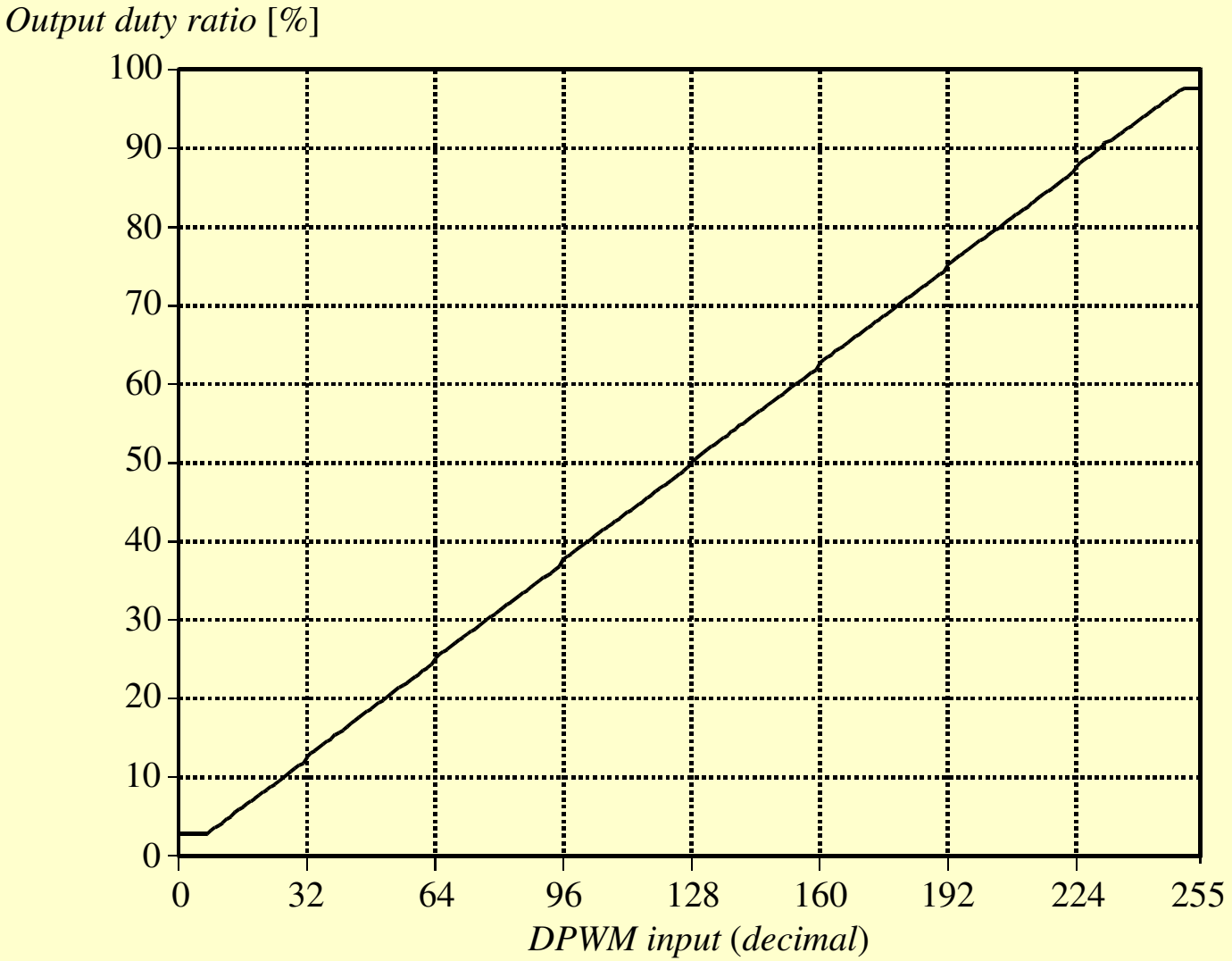
$n = 8$ bits

$f_s = 1$ MHz

$f_{clk} = 8$ MHz



DPWM Experimental Results



High-Resolution Hybrid DPWM

Hybrid DPWM combines a delay line (ring oscillator) with a counter to reduce the maximum clock speed

Conventional DPWM:

$f_{clk} = 2^n \cdot f_s$

$n = 8$ bits

$f_s = 1$ MHz

$f_{clk} = 256$ MHz

Hybrid DPWM:

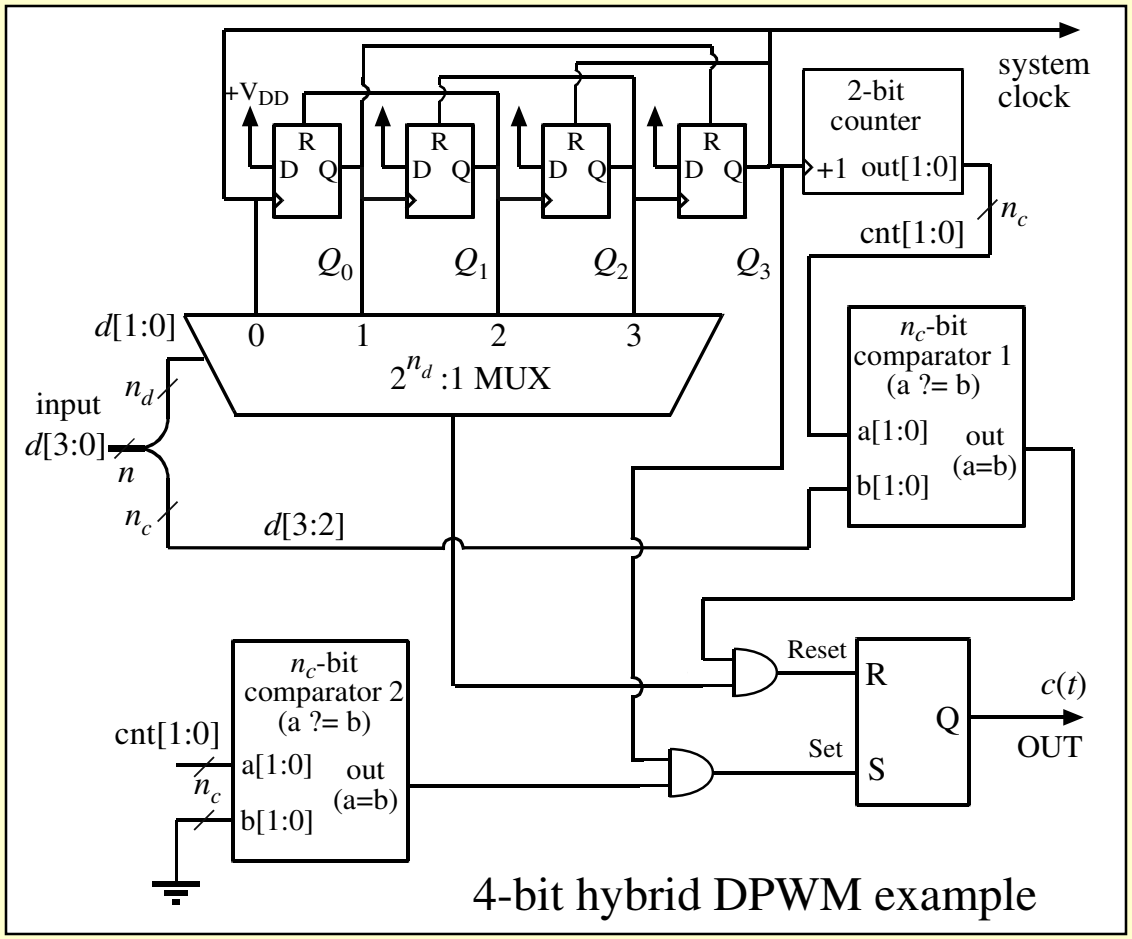
$f_s \le f_{clk} \le 2^n \cdot f_s$

Buffalo switcher hybrid DPWM prototype:

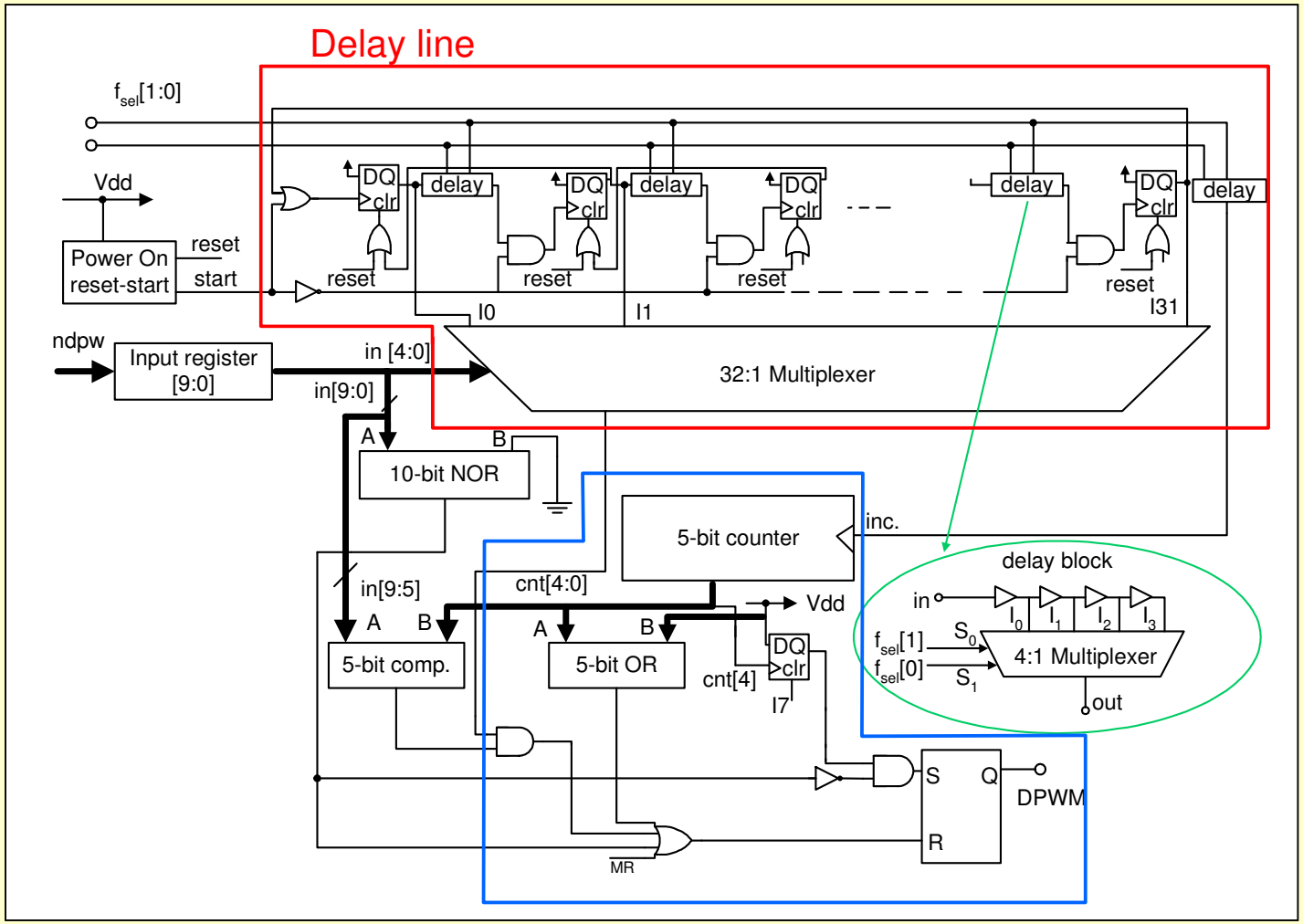
$n = 8$ bits

$f_s = 1$ MHz

$f_{clk} = 8$ MHz



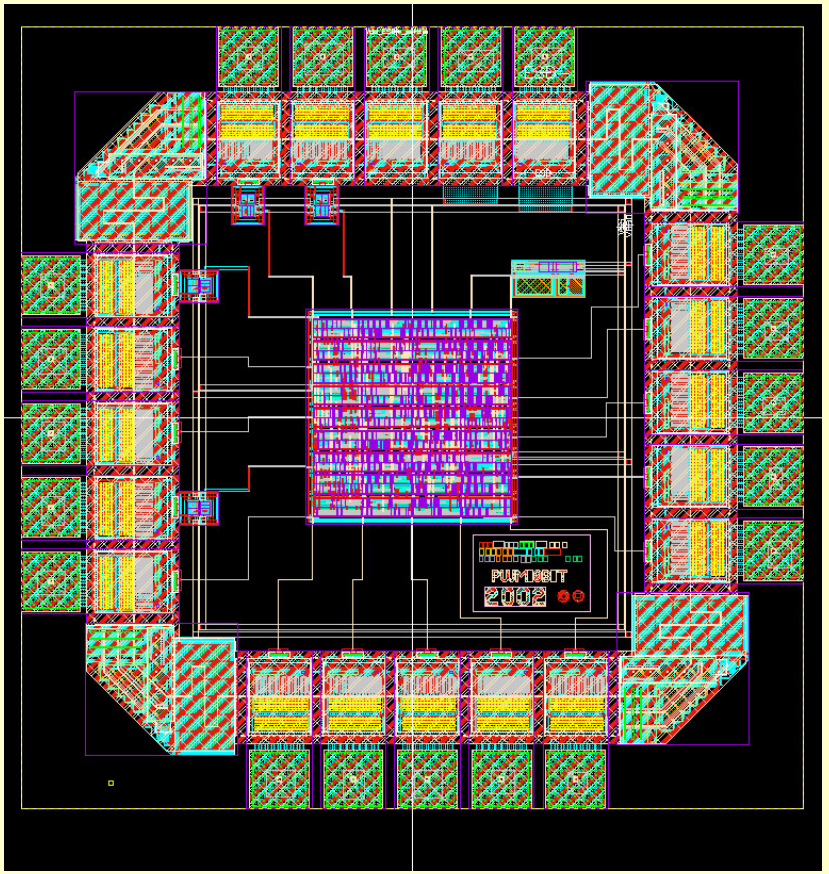
10-bit DPWM With Programmable Frequency



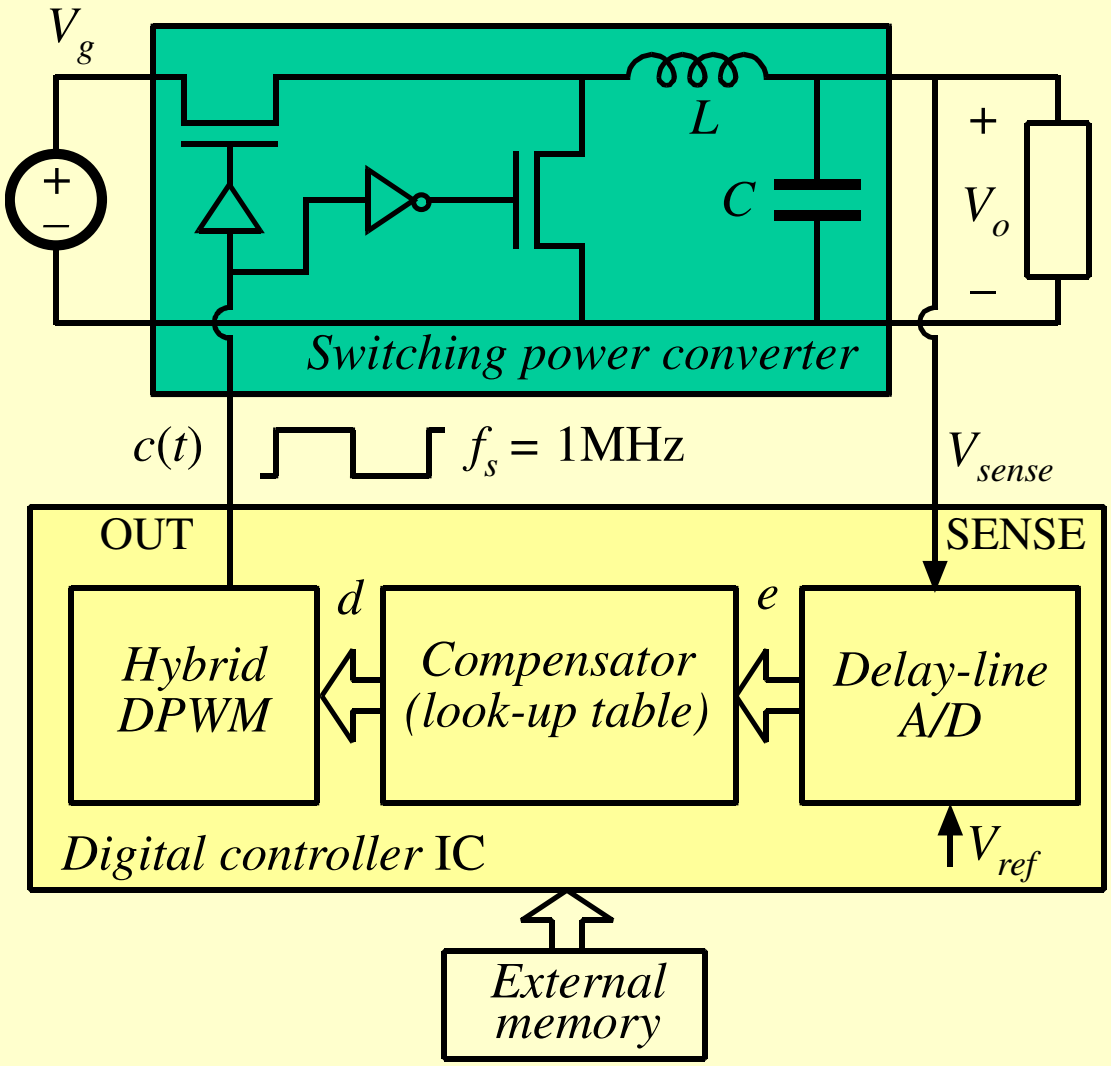
Delay- line/counter combination provides low power consumption, low on-chip area and high resolution at high frequencies

10-Bit Hybrid DPWM Implementation

- 10-bit resolution
- Programmable switching frequency: 750 kHz, 400 kHz, 200 kHz and 100 kHz/ 1.3 ns resolution
- 32 times higher clock frequency
- 0.5µ CMOS
- Active chip area: 0.16 mm^2
- Completely HDL coded



Experimental Digitally Controlled Power Supply



$L = 1\ \mu H,\ C = 22\ \mu F$

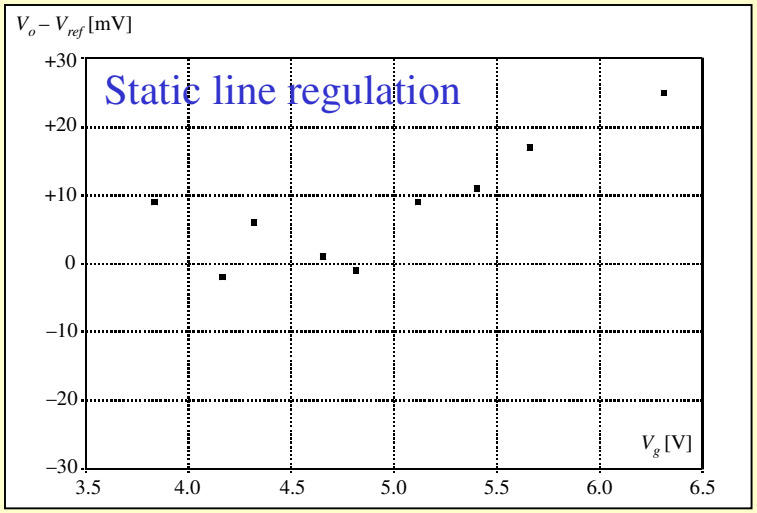
$4\ V < V_g < 6\ V$

$V_o = 2.7\ V$ +/- 25 mV

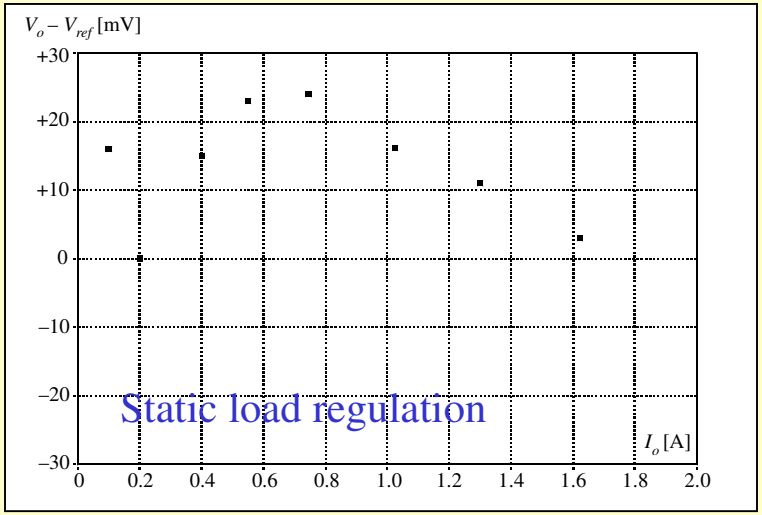
$0 < I_o < 1.5\ A$

$f_s = 1\ MHz$

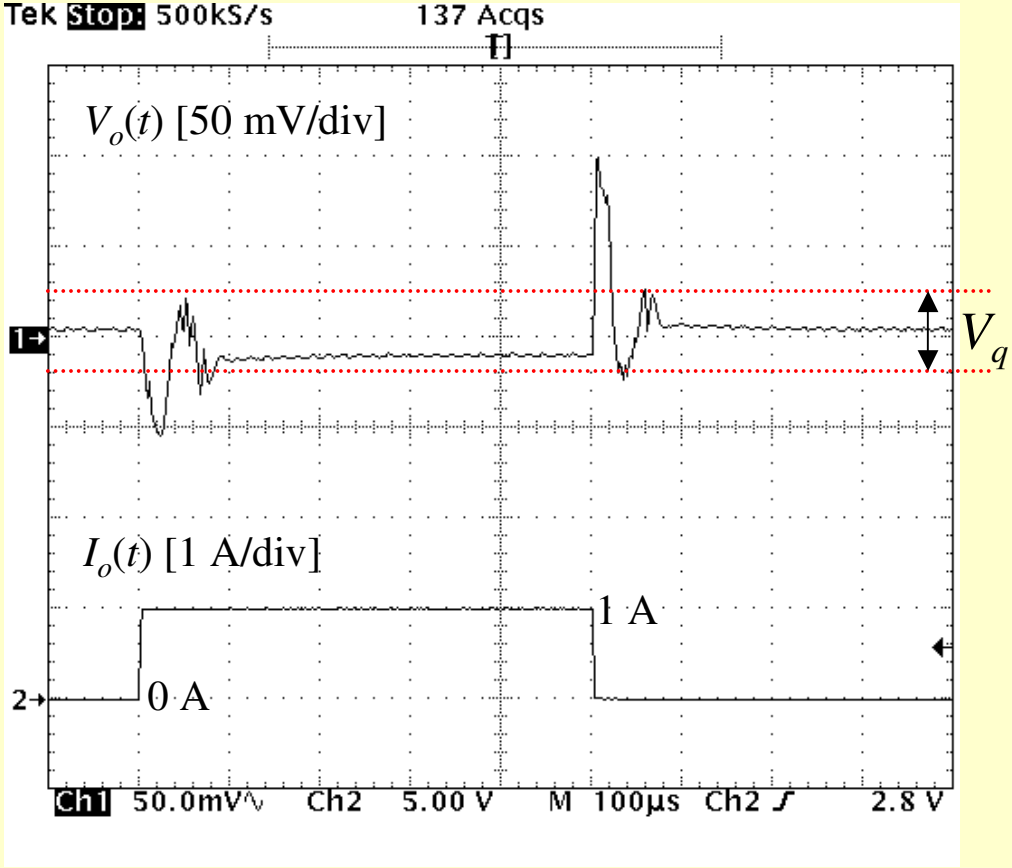
Experimental Results



Input voltage



Load current



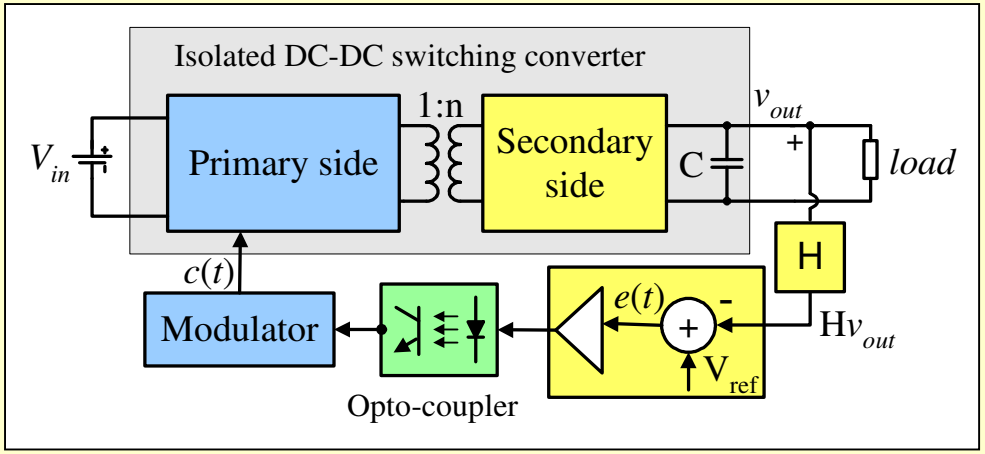
Load Transient Response

Conclusions

- Complete 1 MHz digital PWM controller IC
- New architecture and HDL-based design of the key building blocks:
  - Calibrated delay-line A/D
  - Programmable look-up table compensator
  - Hybrid DPWM
- Small area, low power, fast response
- Design scales with digital technology
- Open possibilities for a new generation of controller ICs (standard parts and ASICs) for power electronics

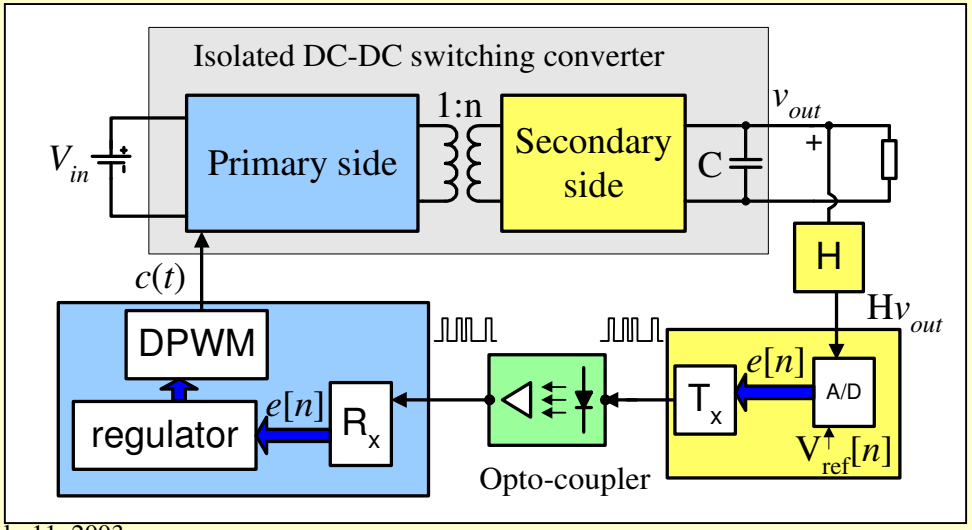
Extension: Digital Chipset for Isolated Power Supply

Analog implementation



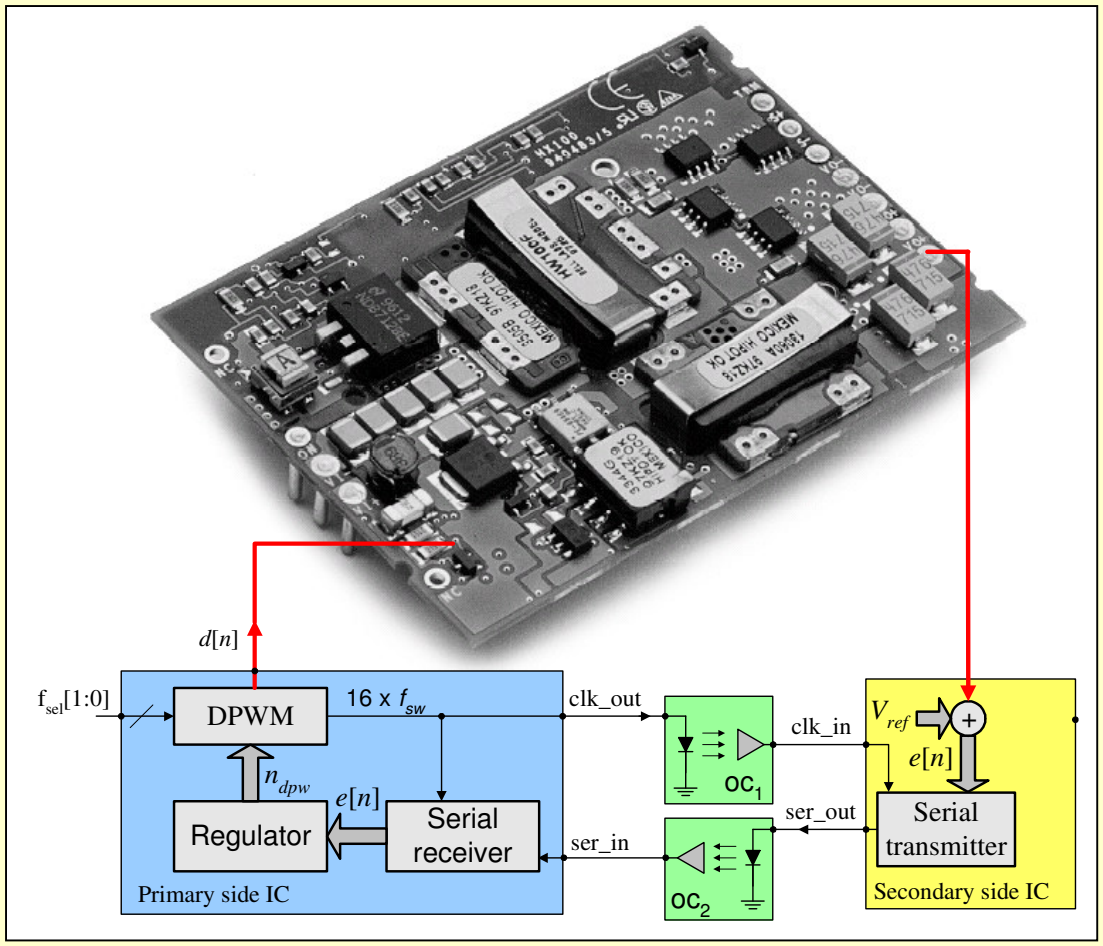
- Opto-coupler operates in linear mode

Digital solution based on serial communication



- Opto-coupler operates in digital mode (as a logic gate)
- Transfers just the error signal
- Potential for less conservative design of the feedback loop

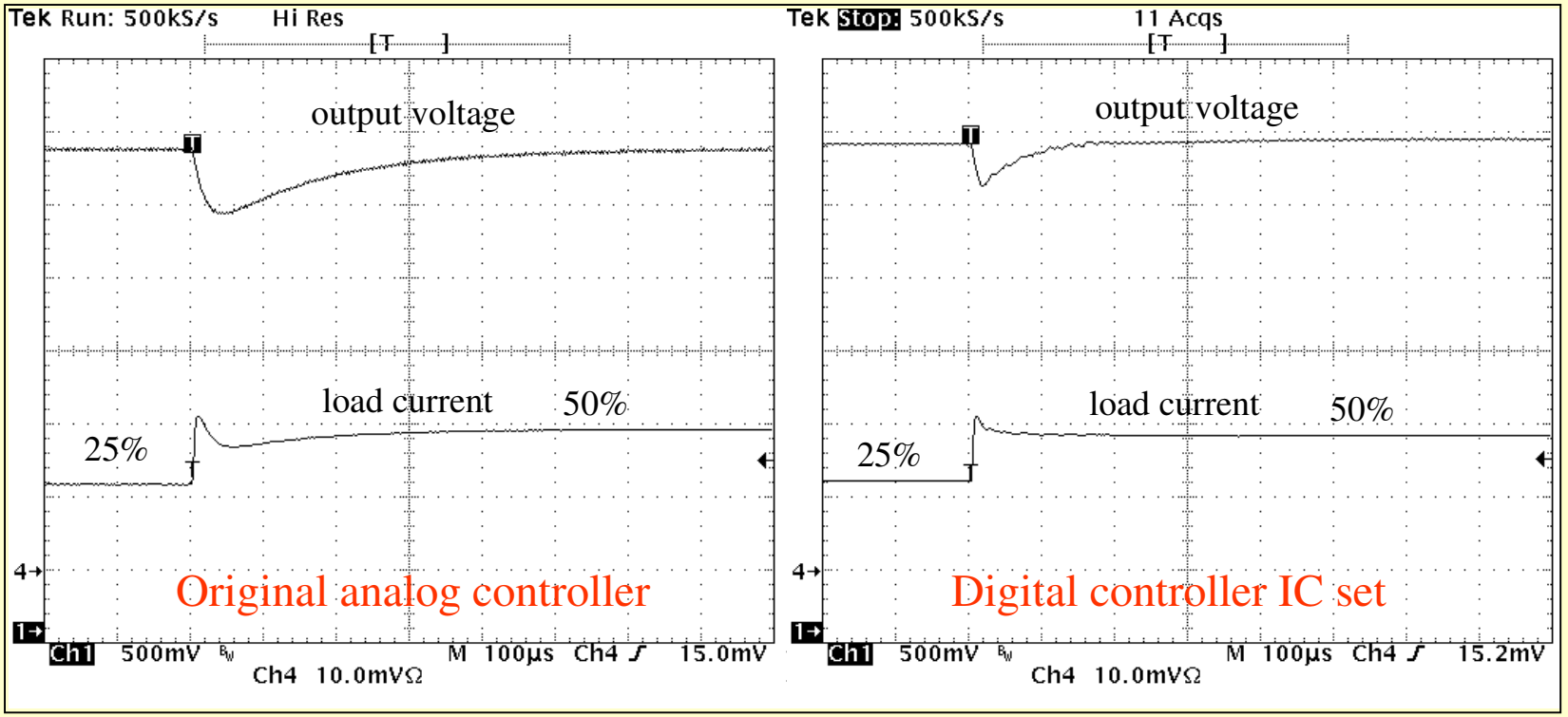
Isolated DC-DC: Test System



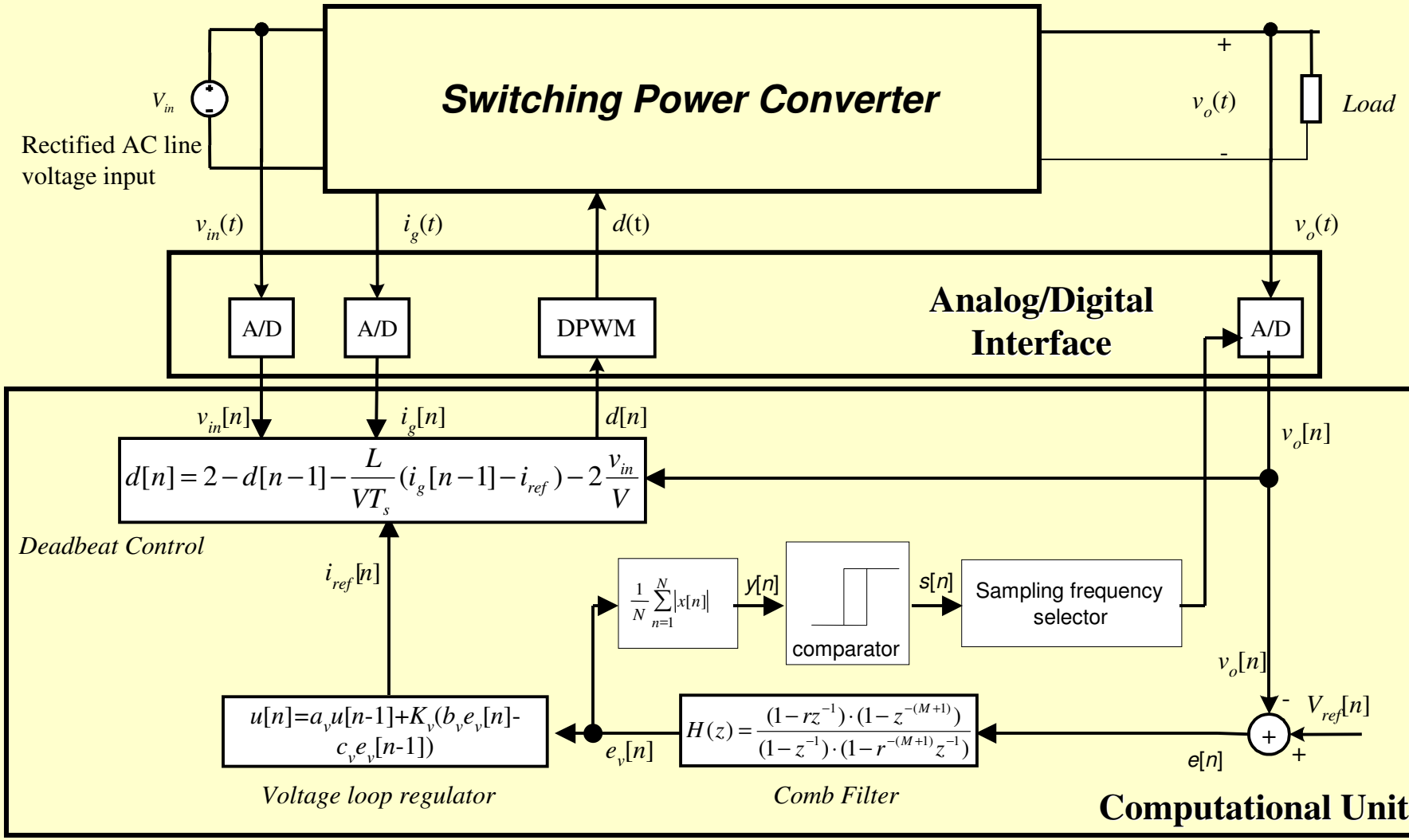
Tyco HW 100F

- Isolated converter
- 36 V ÷ 72 V to 3.3 V
- up to 20 Amps load
- 400 kHz switching frequency
- Replaced original analog current-mode controller on the board

Experimental Results

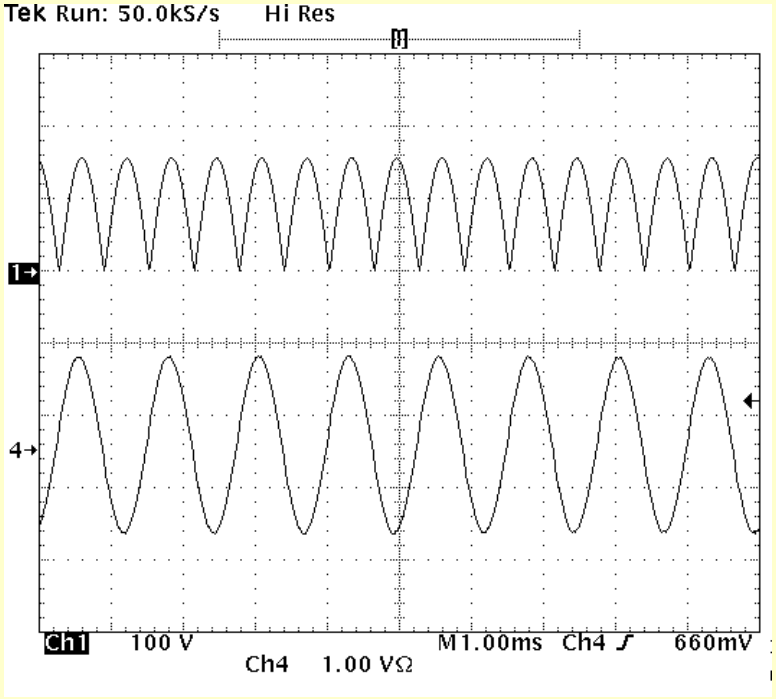


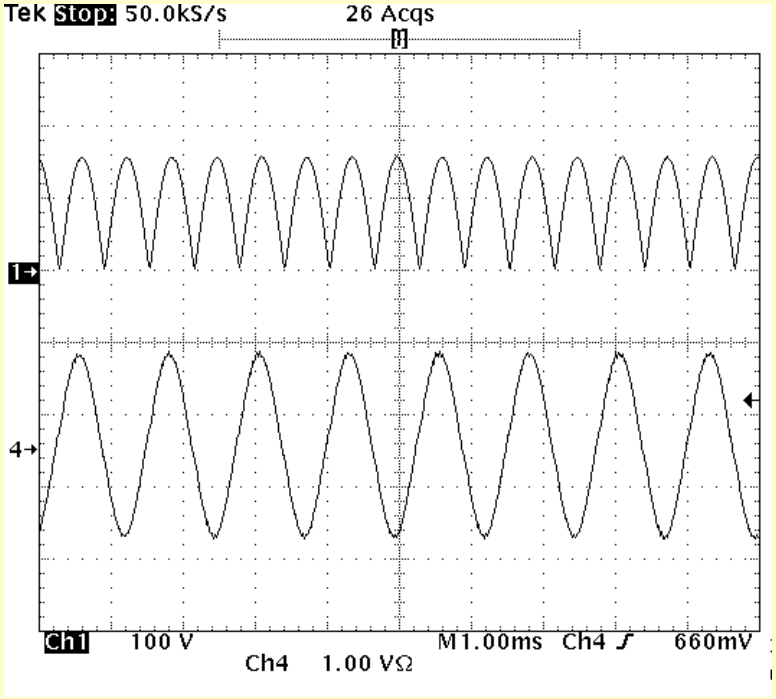
Digital Controller for AC/DC PFC



PFC Experimental Results (current loop)

Line frequency: 800Hz





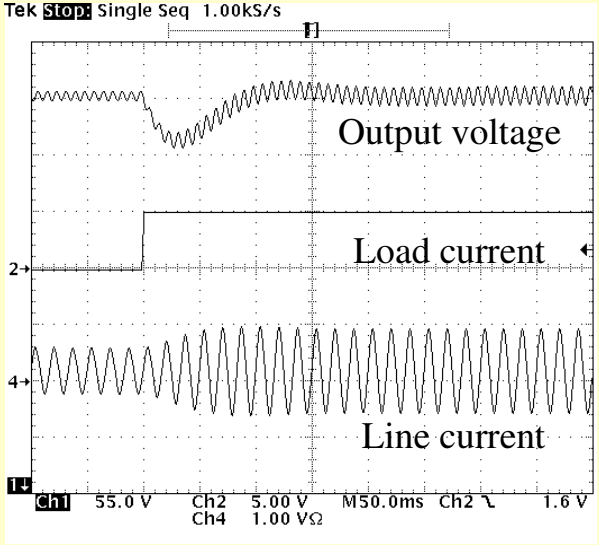
Switching frequency: 200KHz
THD: 2.2%

Switching frequency: 100KHz
THD: 2.4%

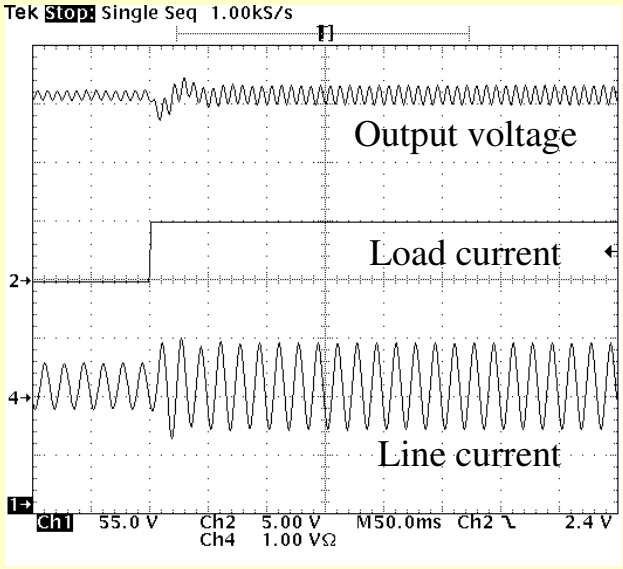
Dead-beat digital current mode control: near-perfect PFC even in demanding next-generation avionics applications (AC system with the line frequency up to 800 Hz)

PFC Experimental Results (voltage loop)

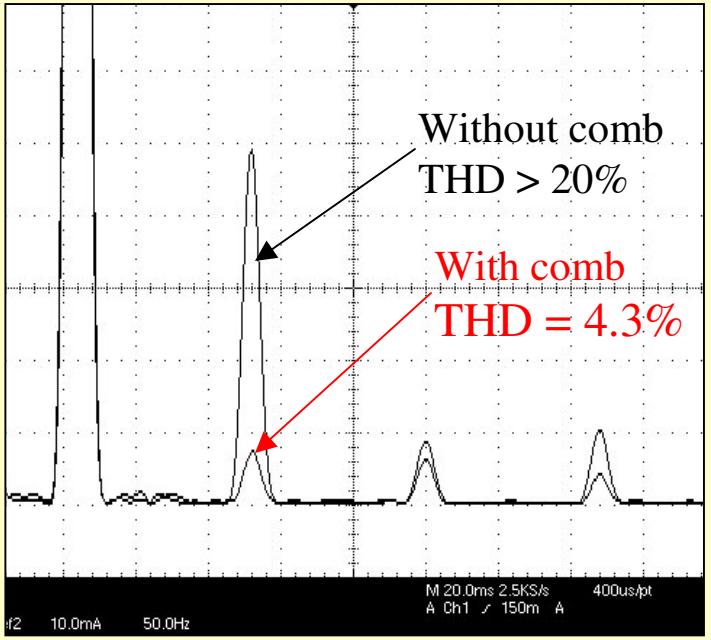
Conventional voltage loop



With STCF



High-bandwidth loop with and without a notch filter



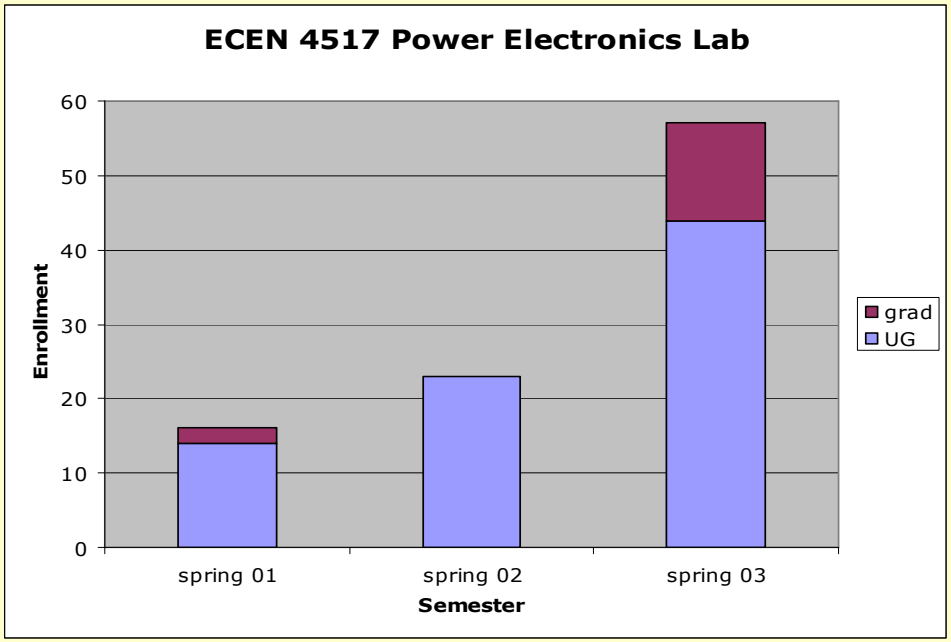
Other CoPEC Research Projects (2003)

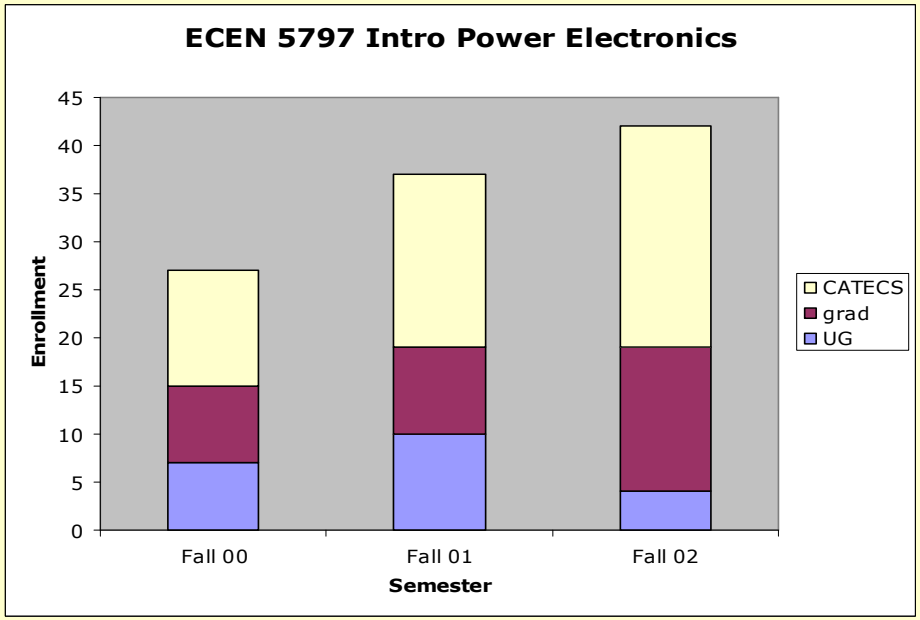
- **Advanced digital control of DC-DC converters**
  - High-performance predictive digital current-mode control for DC-DC converters (TI)
- **Power management for low-power electronics**
  - Digital DC-DC switcher for battery-powered systems (NSC)
  - Adaptive DC-DC converters for RF power amplifiers (DARPA)
  - Adaptive DC-DC converters and power management architecture for base-band µP/DSP (NSF, NSC)
  - Energy harvesting for wireless sensors and Implantable sensors for neuronal recording (Coleman Institute)
- **Microprocessor power supplies**
  - Multi-phase digital controller for microprocessor power supplies (Artesyn)
- **Off-line switching power supplies**
  - Modular mixed-signal control for electronic ballasts (GE)
  - Digital controllers for solar/utility power system (Philips)
  - Digitally controlled matrix converters for wind power system (NREL)

CoPEC Educational Program Objectives

- Strong undergraduate and graduate programs in power electronics and mixed-signal IC design
- Internship and job opportunities for students
- Continuing education
  - Courses available through CATECS
  - Certificate program in power electronics
- Technology transfer to CoPEC sponsors
  - Jointly defined and directed projects
  - Access to CoPEC IP

Growth of Program: Enrollment

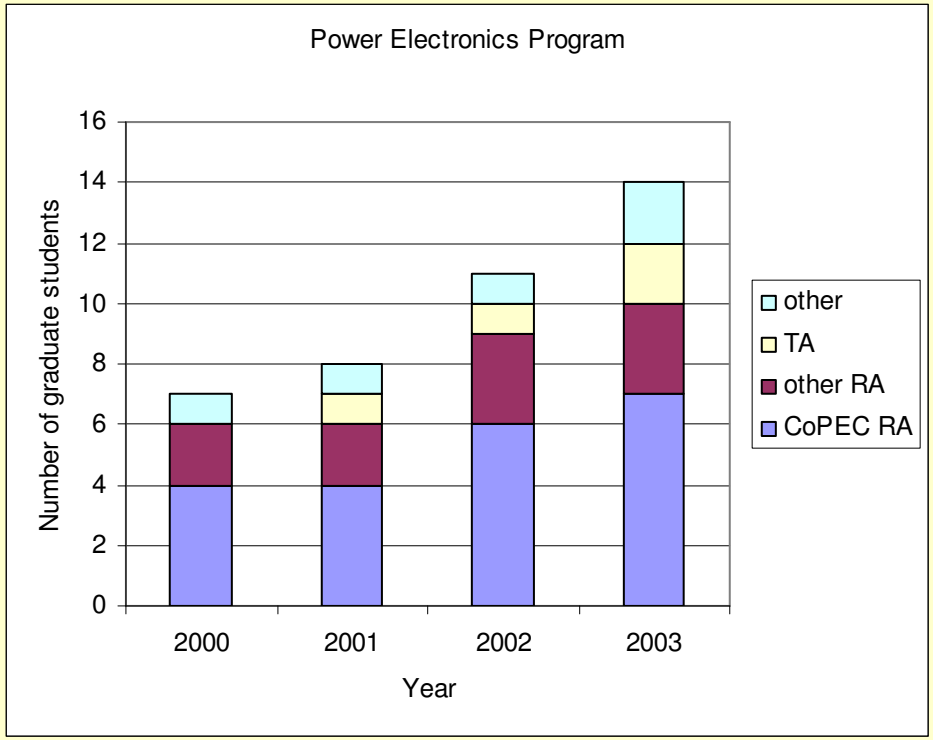




Enrollment for Analog IC Design, Spring 2002: **31**, Spring 2003: **66**
Enrollment for Mixed-Signal IC Design, Fall 2002: **15**

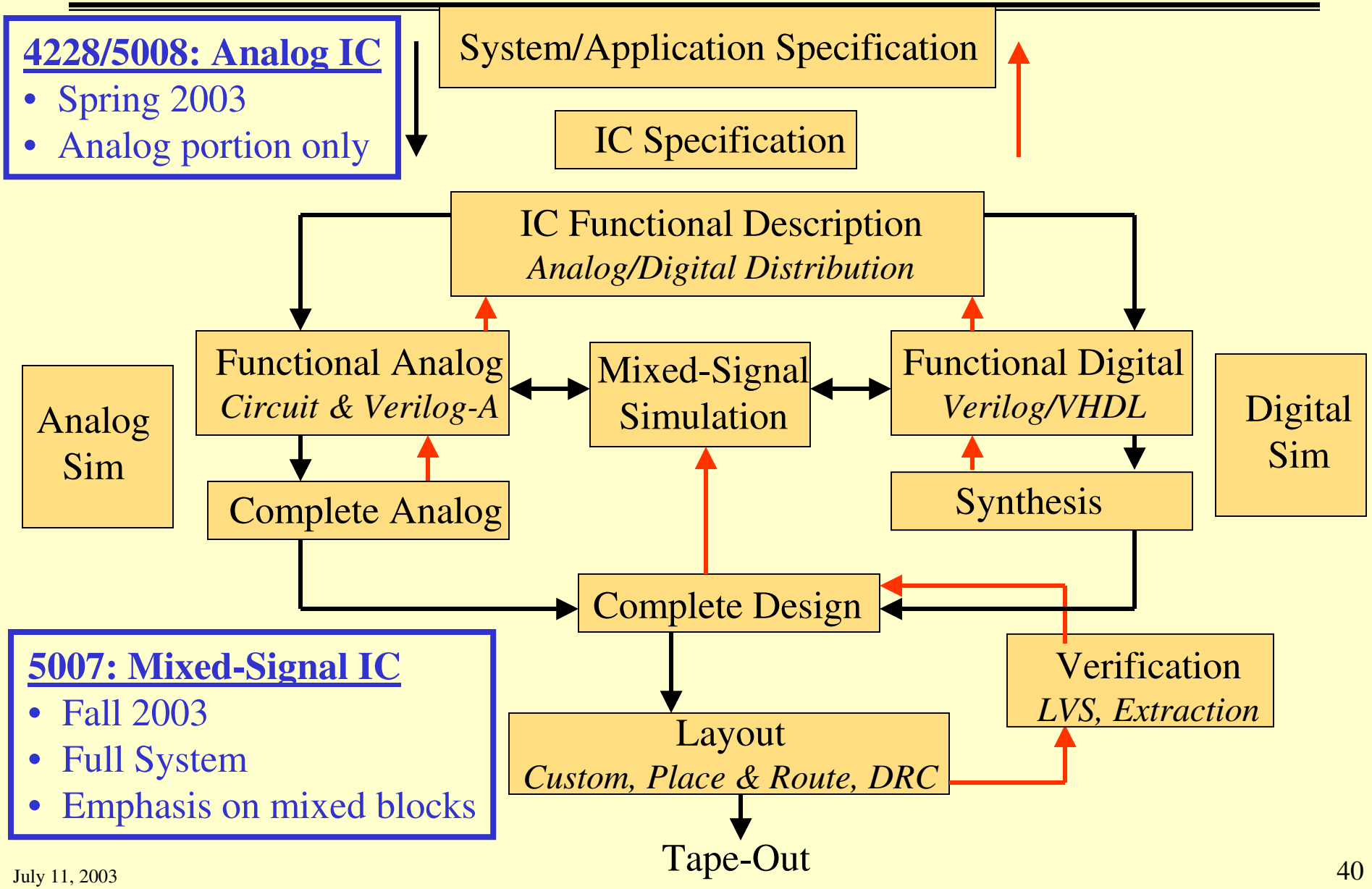
Our visibility is increasing, and we are attracting more students to the power electronics and micro-electronics areas

Growth of Program: Graduate Students



With increased visibility and availability of projects, we are able to attract better students into our program

Mixed-Signal IC Design Flow



Analog IC Course Outline

- *Week 1:* **Review circuits I-II**
  - Text Ch. 1, Appendix A & C; Supplementary notes
- *Week 2:* **Review CMOS technology and device models**
  - Text Ch. 2-3
- *Weeks 3-4:* **Analog CMOS sub-circuits**
  - Text Ch. 4
- *Weeks 5-7:* **CMOS amplifiers**
  - Text Ch. 5
- *Weeks 8-10:* **CMOS operational amplifiers**
  - Text Ch. 6
- *Weeks 11-13:* **High-performance CMOS op-amps**
  - Text Ch. 7
- *Weeks 14-15:* **Comparators and select advanced topics**
  - Text Ch. 8, Supplementary notes

Text used: Allen/Holberg, Gray/Meyer, Johns/Martin

Mixed-Signal IC Lecture Topics

Comparators
- 2-stage amp, hysteresis, latched, high-speed

Sample & Hold Circuits

Discrete-Time Signals (Fundamentals)

Sampled-Data Circuit Techniques
- SC & SI Circuits: Filter Design, Amplifiers, Applications
- Non-idealities: clock-feedthrough, matching

Data Converters
- Fundamentals
- Nyquist Rate D/A, A/D
- Oversampling Converters

System Level IC Design
- System Description & Specification
- IC Functional Specification
- Top Down & Bottom Up Methodologies
- System Planning: fabrication options, foundry selection, silicon area estimation, packaging options, prototype and production cost & time estimation
- Design for Testability
- Reviews: data sheet preparation, design reviews, risk analysis

System Simulation
- Software Preparation: technology files, model files, standard cell libraries, software setup
- Functional Simulation: Verilog-A and Verilog HDL languages, hierarchical designs with multiple cell-views
- Mixed-Signal Simulation: co-simulation of analog & digital, functional and circuit level blocks in the Cadence tools
- Ballast Controller & PLL Case Studies

Physical Layer (time & setup permitting)
- Floorplanning & Layout: custom and semi-custom layout in Cadence
- Practical Considerations: matching, digital/analog isolation, latch-up, ESD and pad design, power distribution, noise coupling
- Verification: LVS, DRC, extracted simulation
- Fabrication: GDSII extraction to foundry

Mixed-Signal IC Final Project

- Select a mixed-signal project that targets a specific application
- Work in teams of 1 to 4
- Deliverables include:
  - ***Proposal:*** Create a final project website with an overview of the target application, pr
of the digital &
  - ***Functional De***
date, which mu
functional bloc
include at leas
circuit level bl
your project w
  - ***Final Design Review:*** Final in-class presentation on your project. The complete "front-end" design of the projects must be complete, ready for transition to a layout engineer. Time permitting, various phases of layout and verification may be required as well.

Local Industry Involvement (?)

- Suggest relevant project/research topics
- Be involved with design and/or final reviews
- Fund fabrication of best designs → hold competition?