Introduction to Copper / Low-*K* Interconnects & Electromigration Fundamentals

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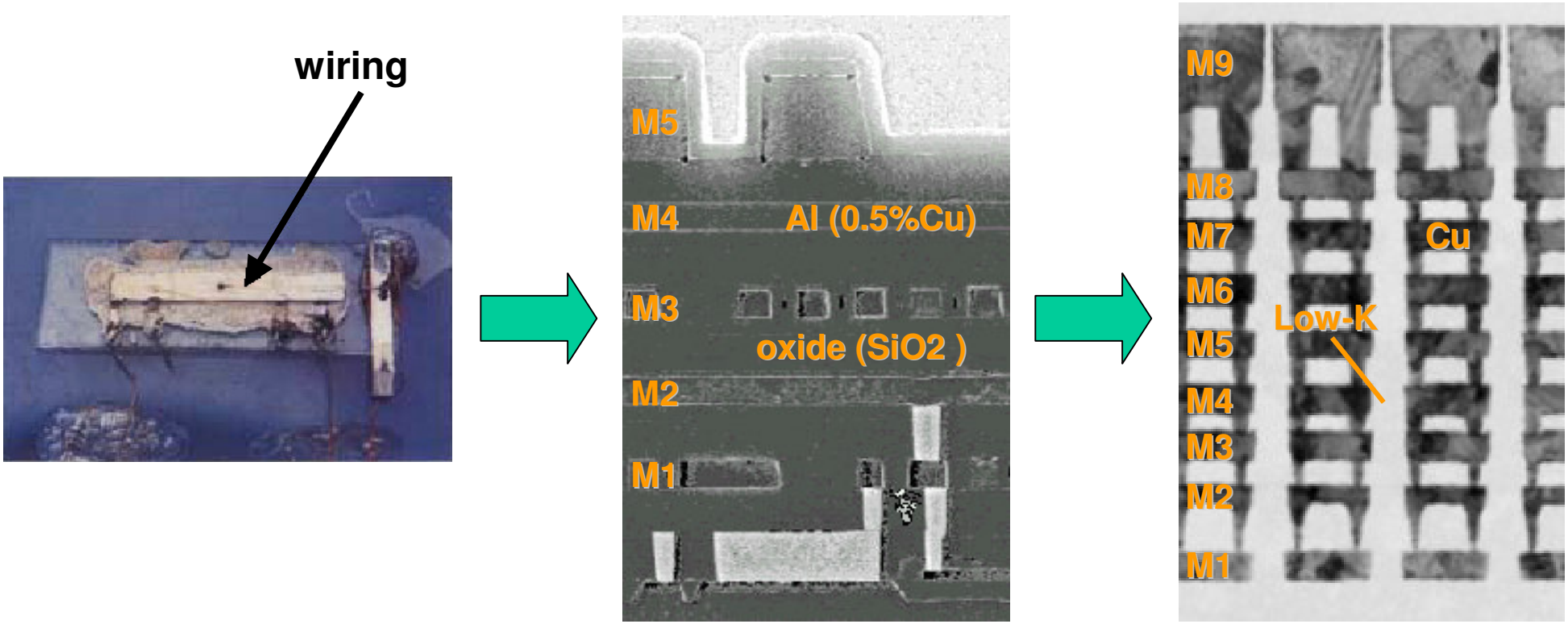
Outline

- Conventional Interconnect Technology
- Copper / Low-K Interconnects
  - Fundamental Motivations
  - Technology Challenges
  - Integration
  - Manufacturing Issues
  - Summary
- Electromigration Fundamentals
- Summary / Future Trends

Evolution of Interconnect Technologies

Where is the transistor?



1st Fabricated IC
(Texas Instruments, 1958)

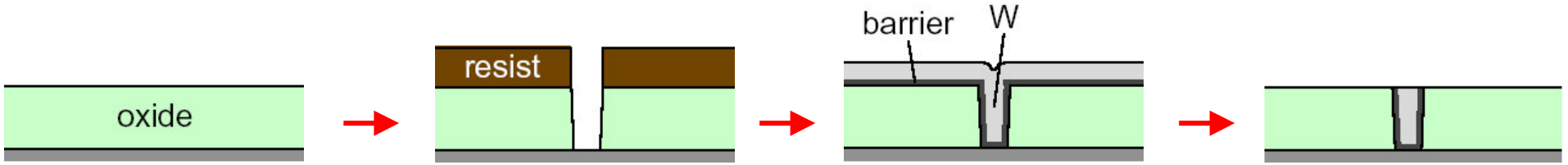
0.25µm Technology
(Motorola, 1996)

90nm Technology
(TSMC, 2002)

Scaling & interconnect density / number of metal layers

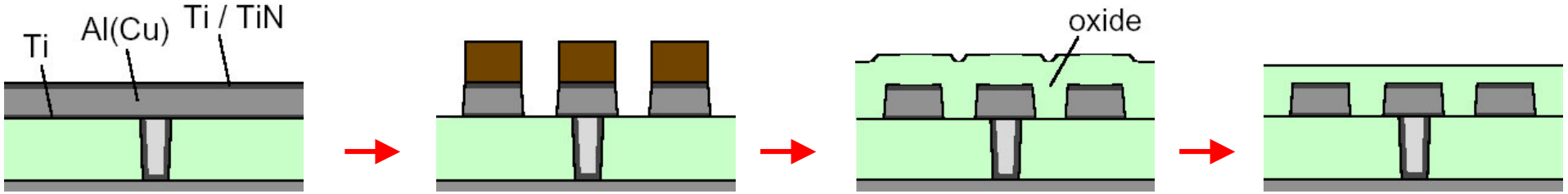
Aluminum Alloy Technology

Via Fabrication



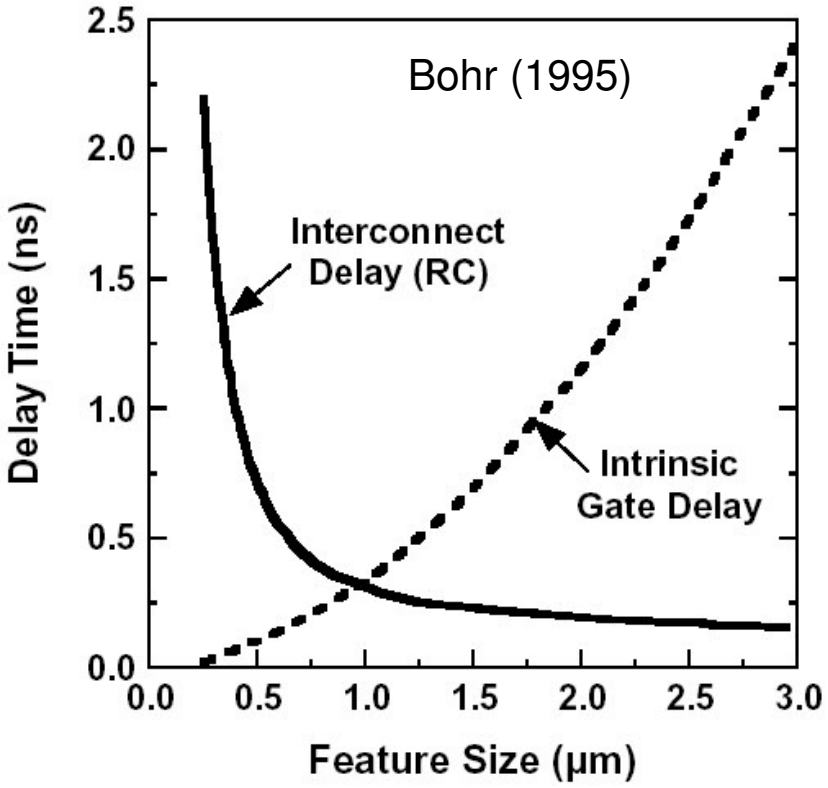
1. Oxide deposition
2. Via etch
3. Barrier & W fill
4. W & barrier CMP

Metal Fabrication



5. Metal stack deposition
6. Metal stack etch
7. Oxide gapfill deposition
8. Oxide CMP (chemical-mechanical polishing)

Interconnect Scaling – Performance Limiter



Limitations with Al/SiO_2 Technology

- wire (RC) delay
- reliability
  - electromigration
  - stress migration
- power dissipation
- crosstalk noise
- cost

Materials Solutions

- copper
  → R ↓, reliability ↑
- low-*K* dielectric
  → C ↓, power dissipation ↓, crosstalk ↓

Copper Processing Challenges

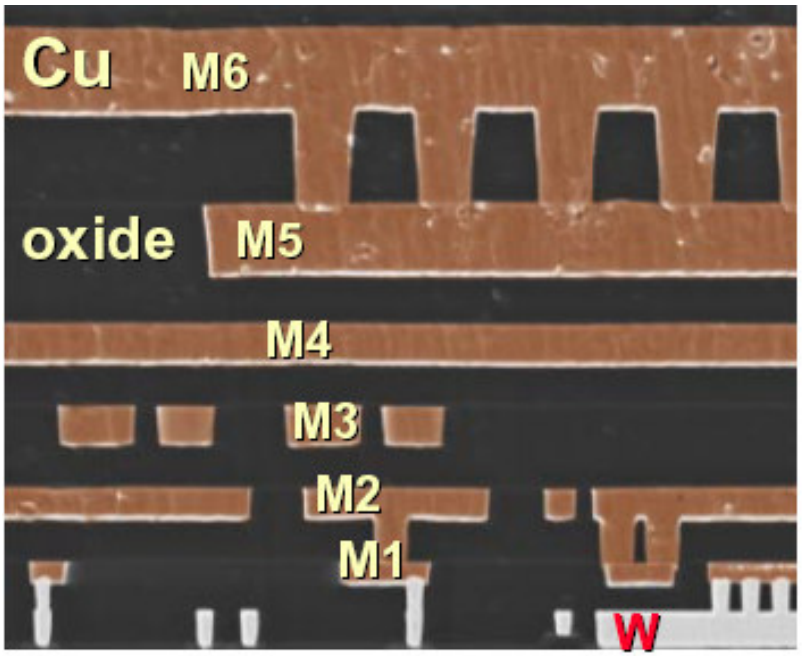
Issues

- copper is difficult to dry-etch
- copper diffuses quickly in Si and SiO_2
  $\rightarrow$ junction & dielectric leakage $\uparrow$, carrier lifetime $\downarrow$

Solutions

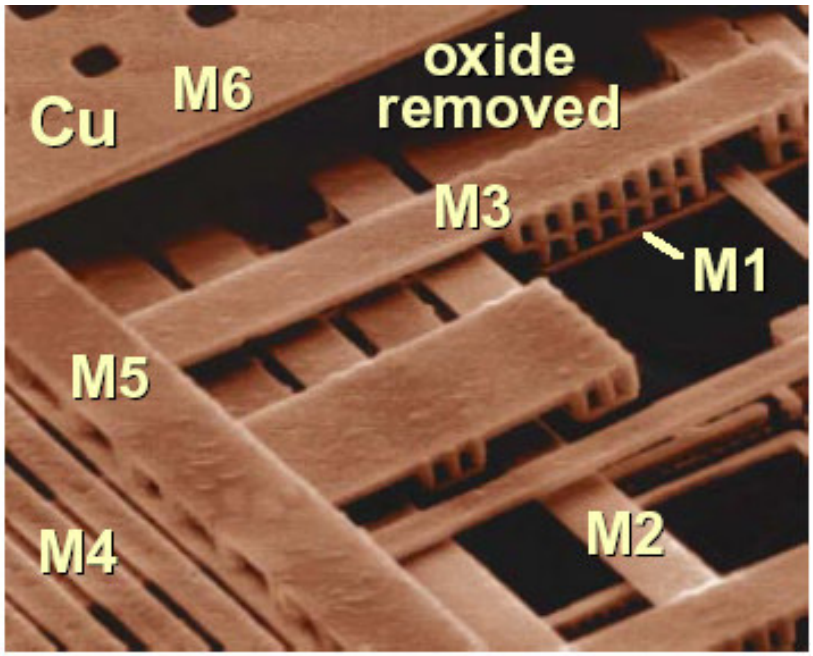
- pattern using Damascene (inlaid) scheme
- encapsulate copper wires/vias with diffusion barriers

First Declarations of *Manufacturable* Copper Process Technology



IBM

(Sept. 1997)

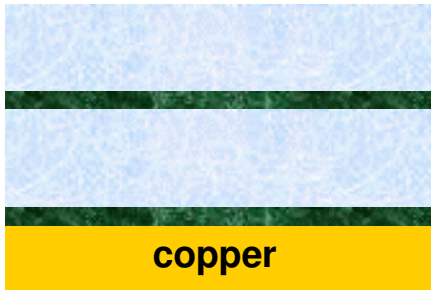


MOTOROLA

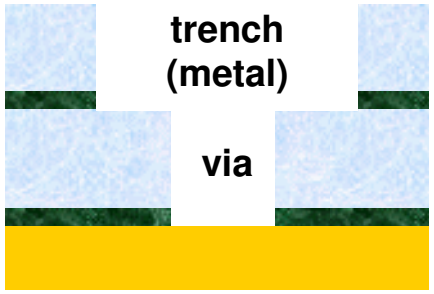
(Oct. 1997)

- Announcements accelerated industry-wide commitment to switch to copper interconnects
- First incorporate copper with oxide, then introduce low-*K* dielectrics

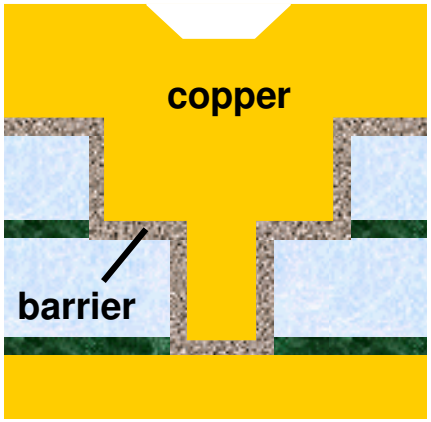
Dual Damascene Technology



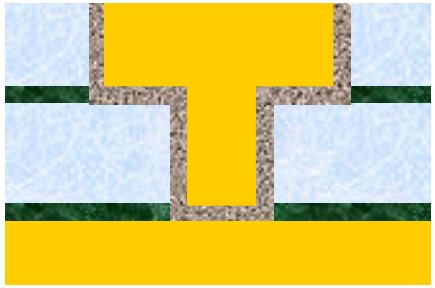
1. Dielectric deposition



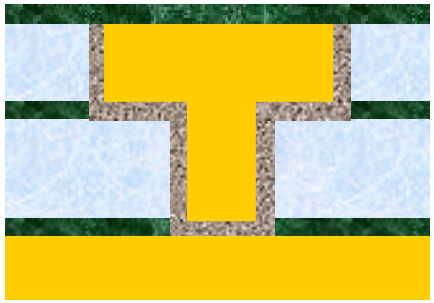
2. Trench/via patterning
   - buried-etchstop
   - trench-first
   - full-via-first



3. Metal barrier deposition,
   Cu seed deposition &
   Cu electroplate fill

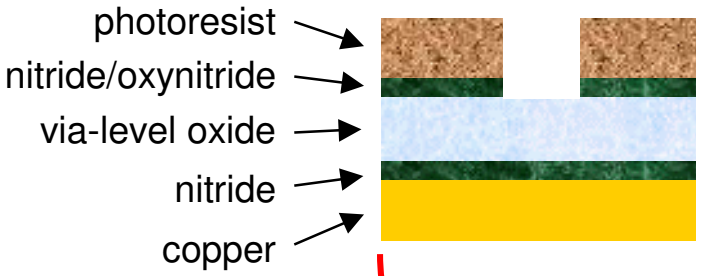


4. Cu & barrier CMP
   (chemical-mechanical
   polishing)



5. Nitride barrier
   passivation

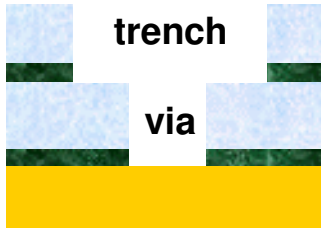
Buried-Etchstop Approach



1) Dielectric stack deposition
2) Via photo
3) buried etchstop etch

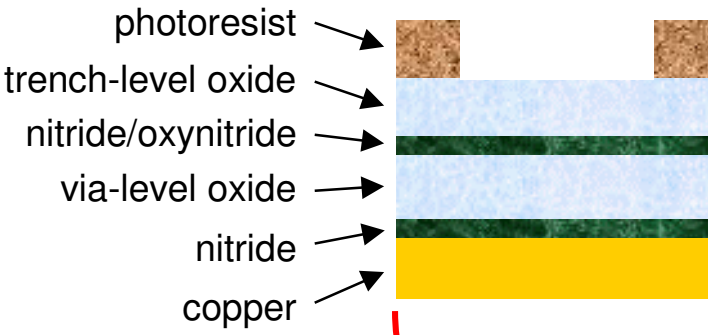
- Via resist strip
- Trench-level oxide deposition

- Trench photo



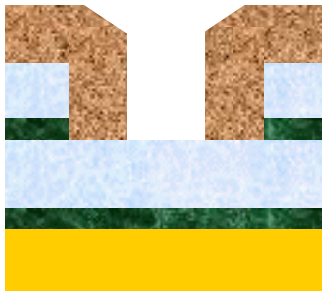
- One-step trench/via etch (stop on nitride)
- Trench resist strip
- Nitride etch

Trench-First Approach

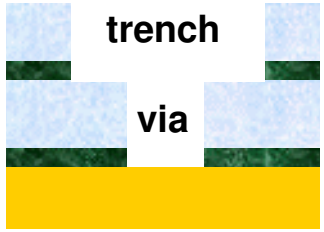


1) Dielectric stack deposition
2) Trench photo

- Trench etch
- Trench resist strip

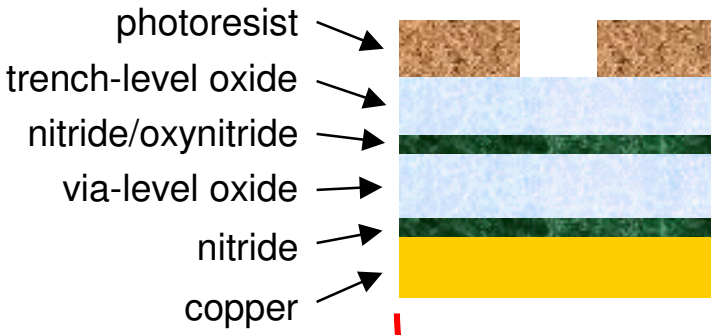


- Via photo



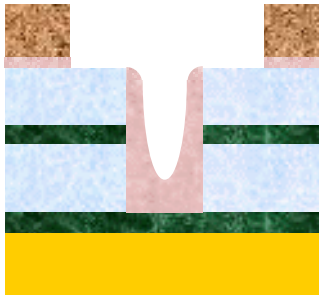
- Via etch (stop on nitride)
- Via resist strip
- Nitride etch

Full-Via-First Approach

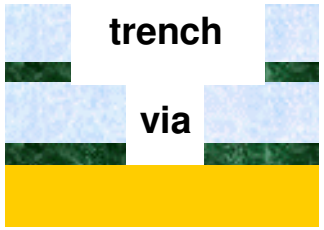


1) Dielectric stack deposition
2) Via photo

- Via etch (stop on etchstop layer)
- Via resist strip



- BARC deposition
- Trench photo
- BARC etch

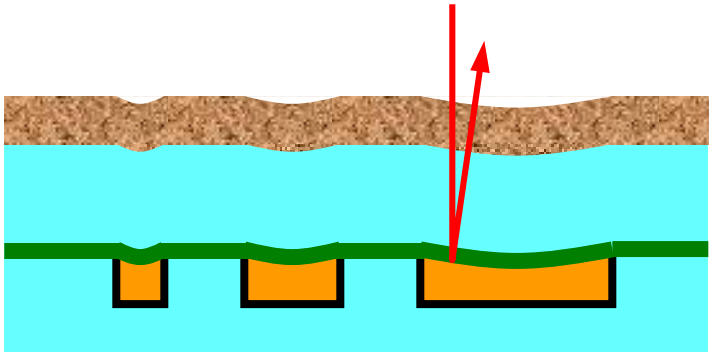


- Trench etch
- Trench resist/BARC strip
- Nitride etch

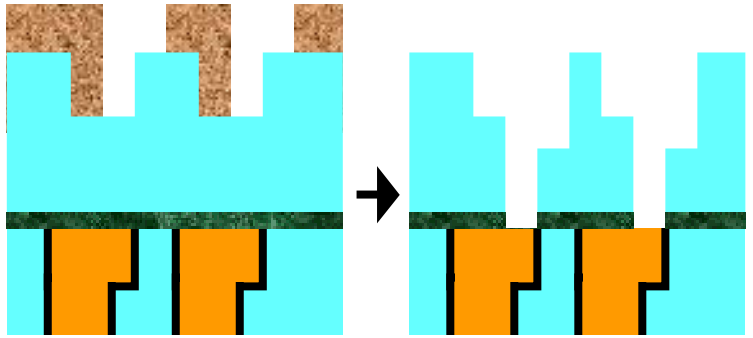
Lithography Issues

- wafer planarity for maximum depth of focus
  - resist thickness variation → poor CD control
  - limits extendibility of via photo in trench-first approach

- reflective notching for CD control
  - need anti-reflective films in dielectric stack or spin-on organic BARC
  - less effective if underlying topography is present

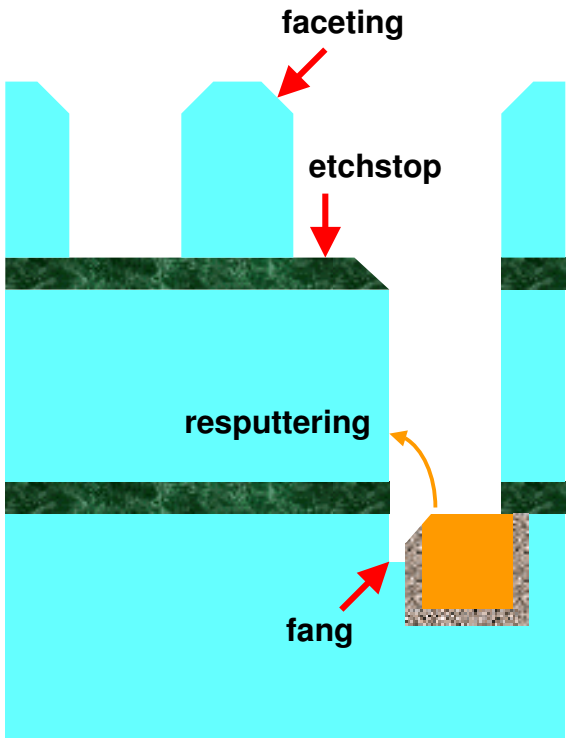


- overlay error between trench & via masks
  - big issue in buried-etchstop & trench-first
    - misalignment decreases size of via landing as well as intervia and/or intrametal spacing
  - least severe in full-via-first
    - only intrametal spacing misaffected
  - may ultimately limit scalability of dual damascene



Dielectric Etch Issues

- trench etch selectivity to stop layer
  - need to control microloading & trench bottom profile
  - big issue in buried-etchstop
- resist stripping
  - need to remove before exposing copper since resist is difficult to strip without oxidizing copper
- BARC stripping
  - difficult to remove fence residues in full-via-first
- excessive faceting from unmasked nitride etch
  - some desired for easier barrier & copper seed fill
  - over-faceting reduces intrametal spacing → leakage
- copper resputtering onto via sidewall
  - must avoid copper trapped outside barrier which could diffuse into dielectric
- unlanded via fangs from unselective nitride etch
  - poor barrier/seed coverage → poor reliability



Barrier & Copper Seed Deposition

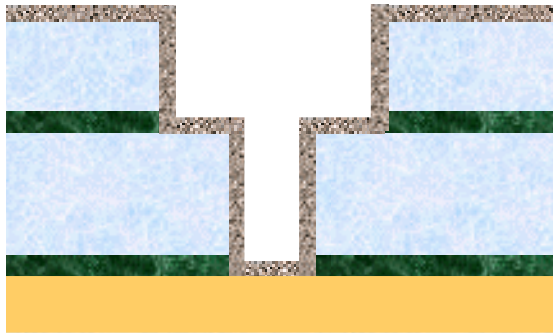
Step 1: Barrier Deposition (Ta, TaN, TiN)

- prevent diffusion of copper from trench/via into Si or SiO_2
- adhesion layer for copper to dielectric
- must be thin to preserve conductivity advantage of copper
- CVD or directional PVD (e.g., ionized metal plasma (IMP))

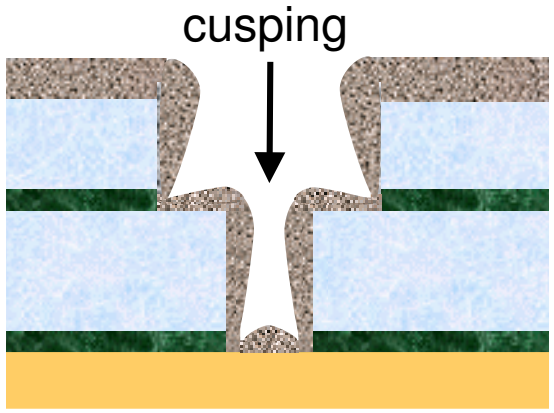
Step 2: Copper Seed Layer Deposition

- conductive layer for copper e-plate fill → better within wafer uniformity
- control of plated copper film grain size & texture → better reliability
- CVD or directional PVD (e.g., ionized metal plasma (IMP))

Important to have conformal barrier & seed layer to ensure good fill.

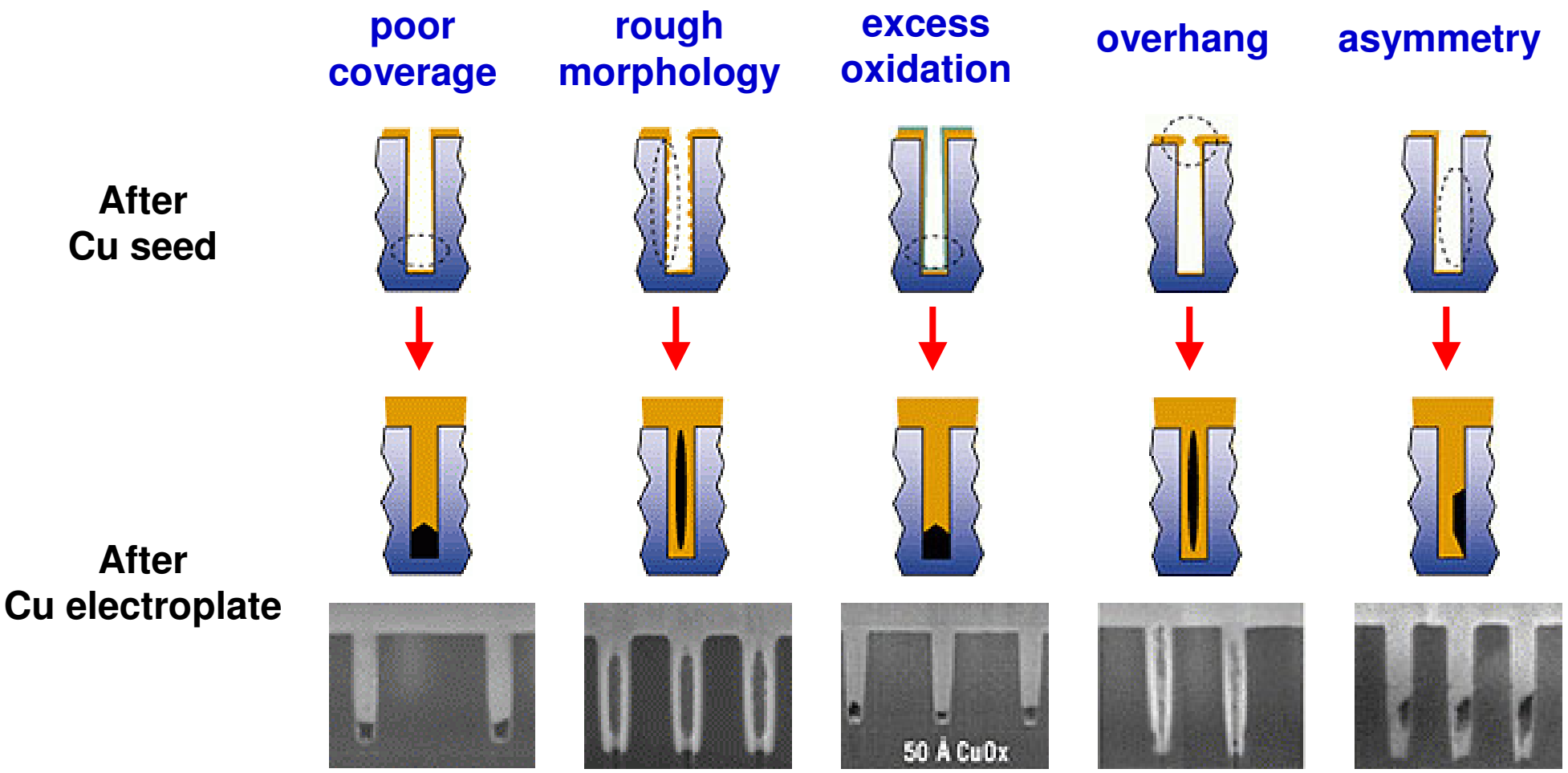


ideal step coverage



typical step coverage

Barrier & Copper Seed Deposition Issues



Courtesy of Solid State Technology

Copper Electroplating Fundamentals

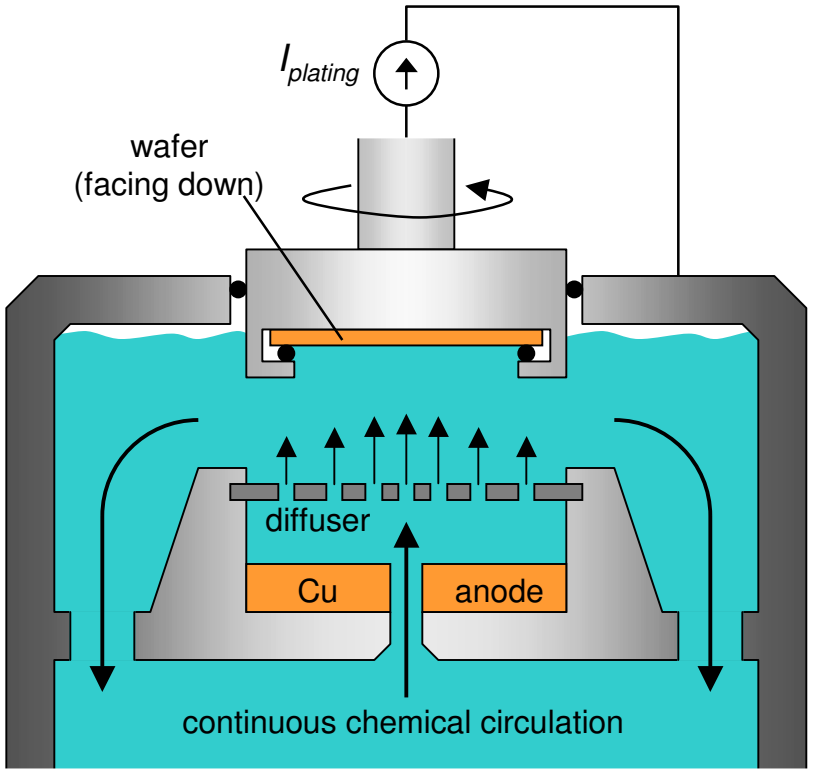
Basic Principle

- immerse wafer into solution of copper ions
- cathode clamped to wafer edge
- apply potential between cathode & anode to plate copper on wafer

$$Cu^{2+} + 2e^{-} \rightarrow Cu^{0}$$

Copper Plating for IC Application

- most popular method for copper fill
- cheap
- optimized tool, plating bath & current for good gapfill & deposition uniformity
  e.g., careful diffuser design to compensate for intrinsic edge-fast deposition
- post-plating anneal required to accelerate room-temperature self-annealing of plated copper
  → better grain size control for CMP



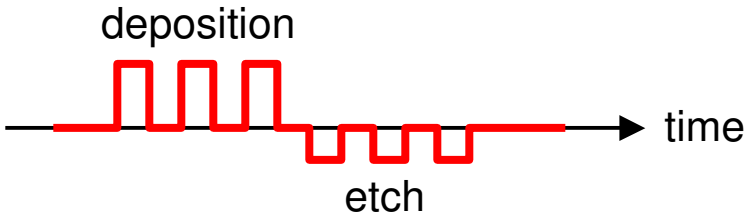
Copper electroplating for IC's pioneered by IBM

Techniques for Good Plating Gapfill

Want *superfilling* (bottom-up deposition)

1. Pulsed Plating Current Waveform

- simultaneous deposition-etch
- improve diffusion of copper ions into via



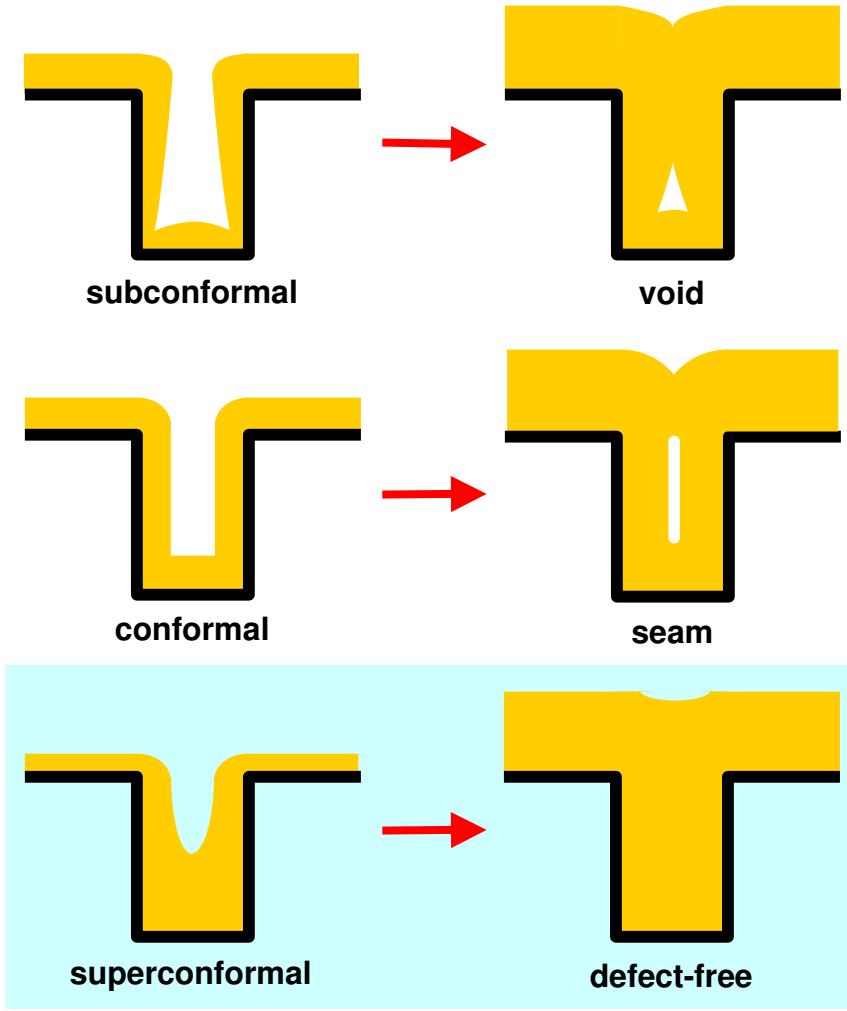
2. Organic Additives in Plating Bath

brightener

- enhance deposition rate in via & trench
- small organic molecules

leveler

- retard deposition rate at open field corners
- large organic macromolecules



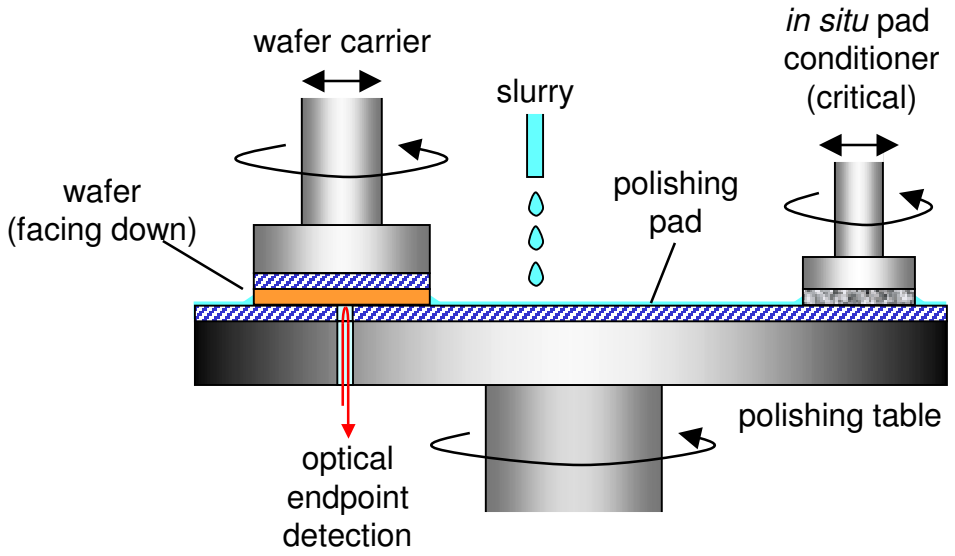
Copper CMP Fundamentals

Basic Principles

- planarize wafer surface
- remove excess copper & metal barrier from wafer field to form inlaid copper
- removal rate depends on pad pressure, pad velocity, selectivity of slurry chemistry & mechanical abrasion

Basic Process

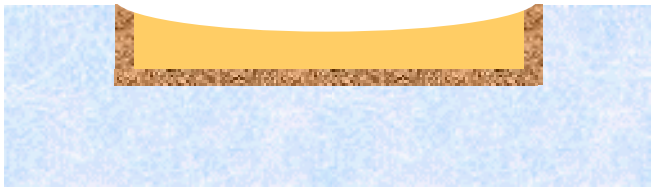
1. bulk copper removal
   - stop on barrier
2. barrier removal
3. oxide buff
   - reduce defects
   - apply corrosion inhibitor
4. post-CMP scrub
   - remove slurry residues
   - clean surface
   - dark ambient to suppress galvanic copper deposition



CMP technology pioneered by IBM

Copper CMP Issues

copper dishing in wide metal lines



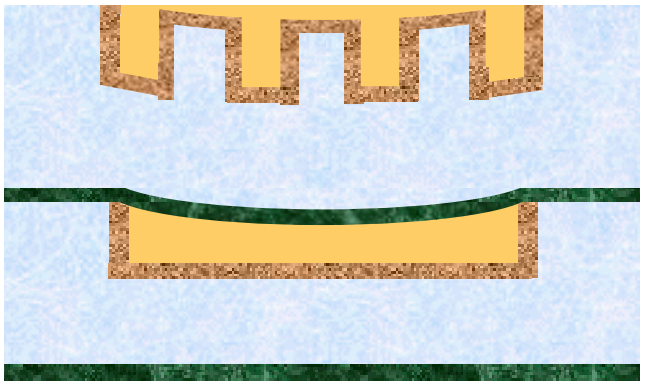
oxide erosion in dense metal lines

Good planarity is very critical for multilevel integration!!!

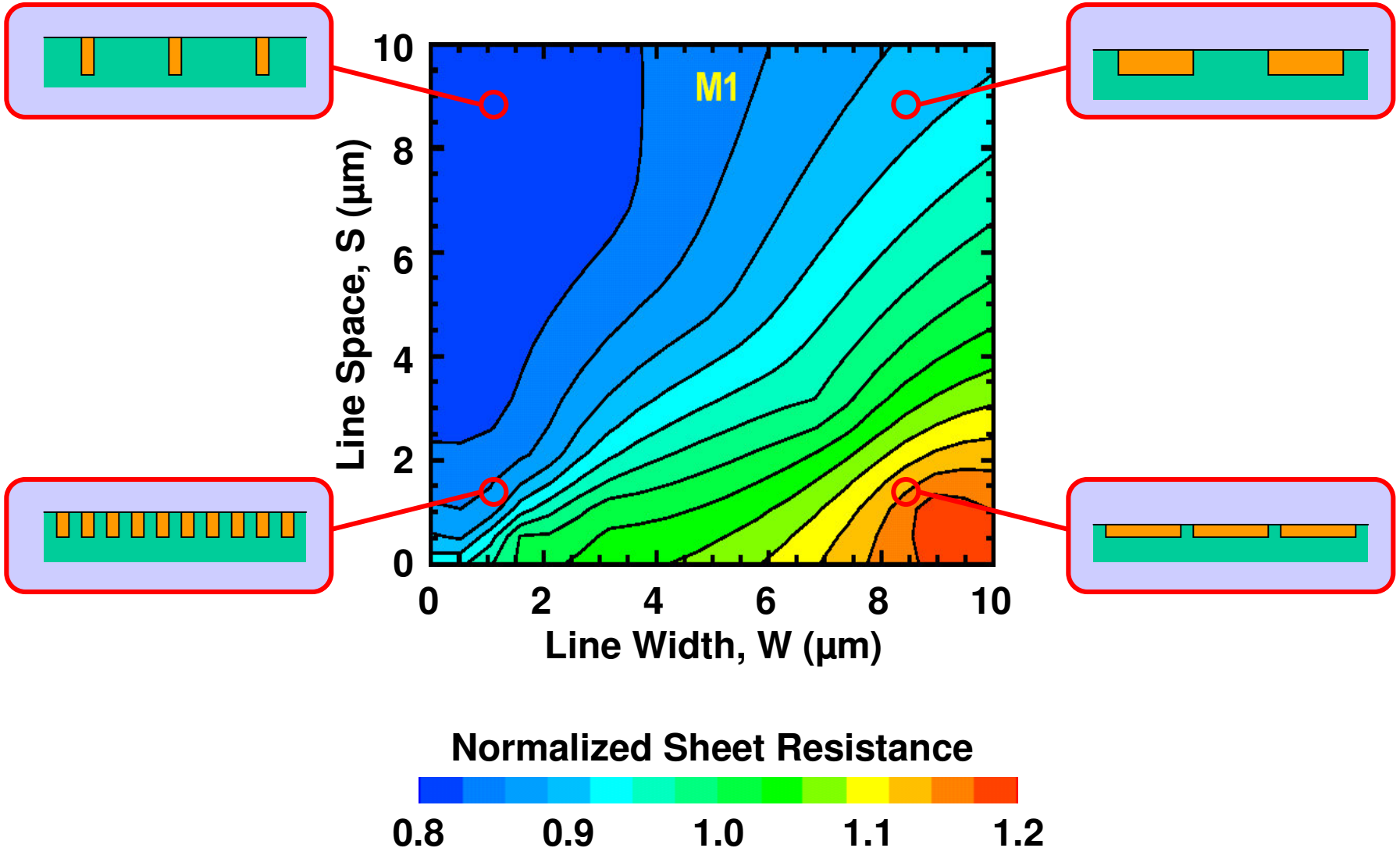
- minimize metal residues at higher metal levels
- essential to optimize process conditions, polishing pad & slurry chemistry while maintaining practical removal rates

post-CMP topography

metal residue!!!

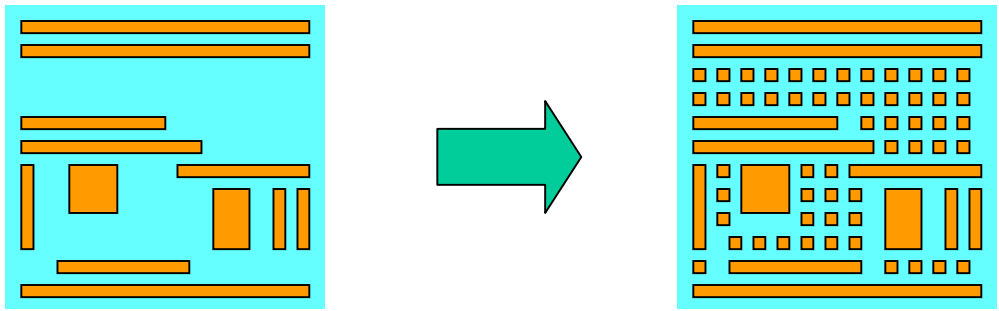


CMP Layout/Pattern Density Effects

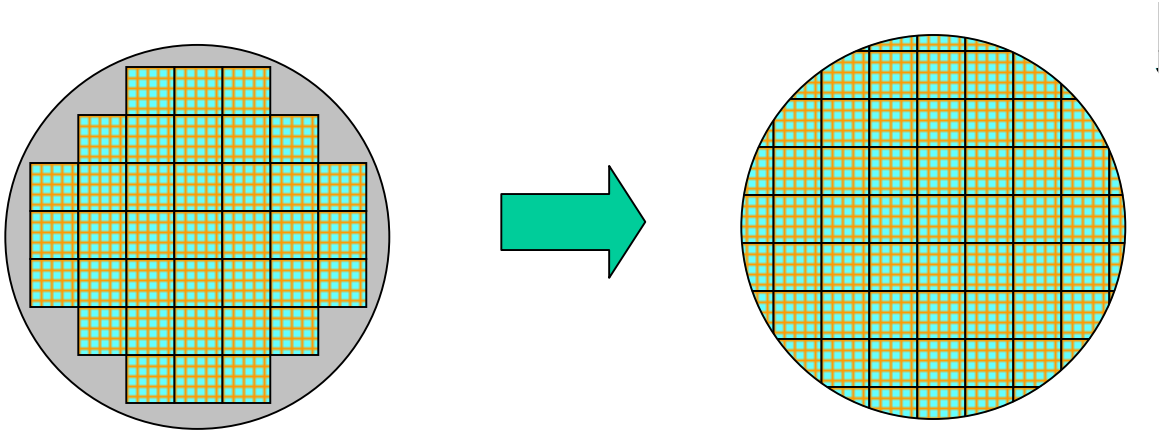


Interconnect *Dummification*

- Add dummy patterns to open spaces to minimize layout density variations
  - → Minimize R_S variation
  - → Minimize surface topography (depth of focus, metal residues)
  - → Added design complexity to check layout density & insert dummy patterns



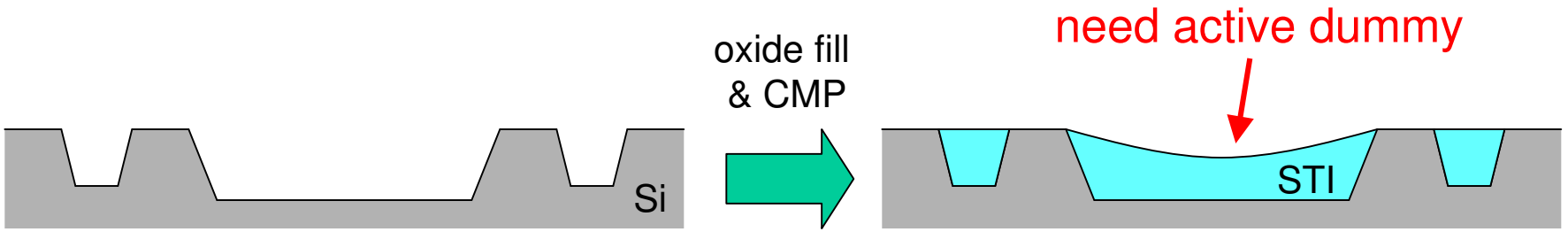
- Also critical to step dummy dies along wafer circumference



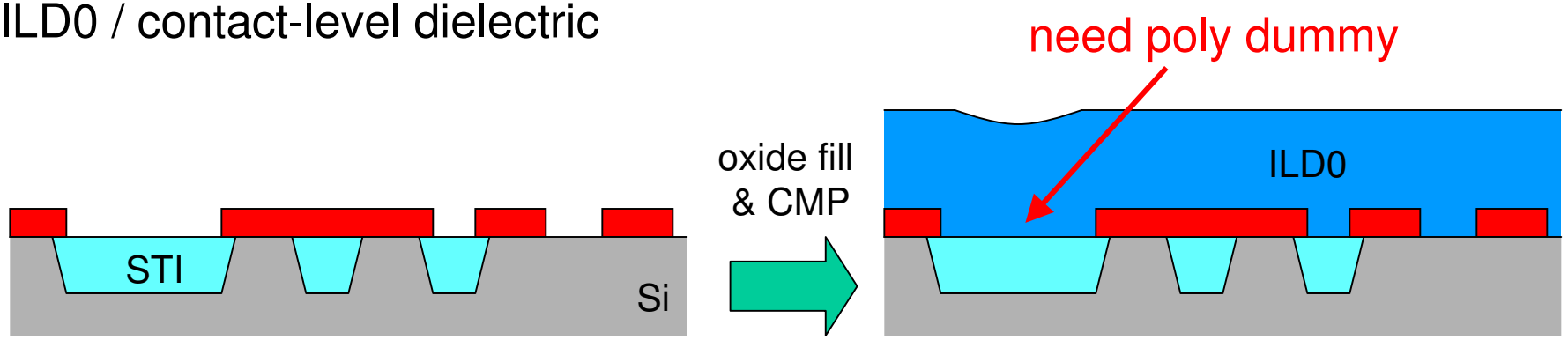
Dielectric CMP

- Original motivation for CMP development at IBM
- Dummification also required for active & poly layers
  - Planarity important since metal layers build on top of polished dielectrics

- STI (shallow trench isolation)



- ILD0 / contact-level dielectric

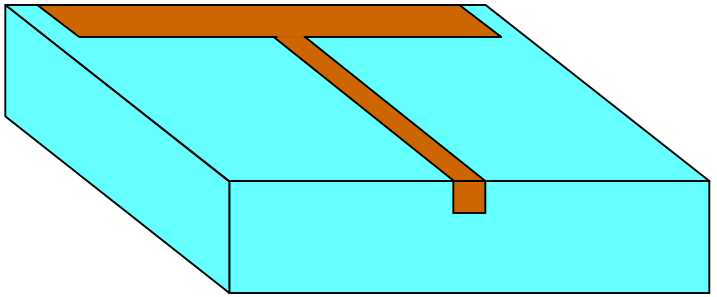


Electrical Monitoring of CMP Performance

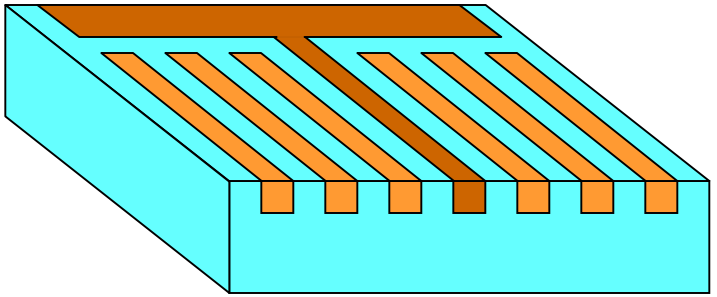
Compare resistances of lines with various adjacent patterns.

Motorola (1998)

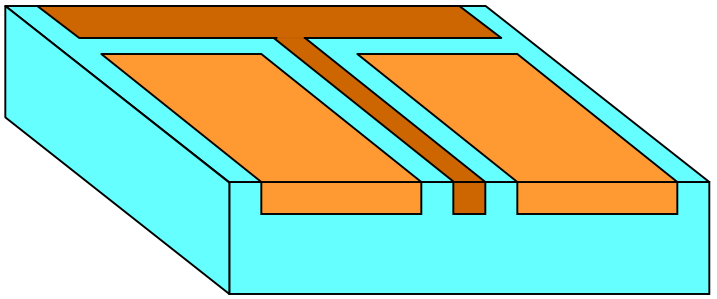
- no adjacent lines, i.e., isolated
  - worst-case low pattern density
  - lots of Cu in field area to remove



- minimum-pitch adjacent lines
  - prone to dielectric erosion



- wide adjacent lines, e.g., bus
  - wide lines very prone to dishing
  - erosion of dielectric supporting tested line



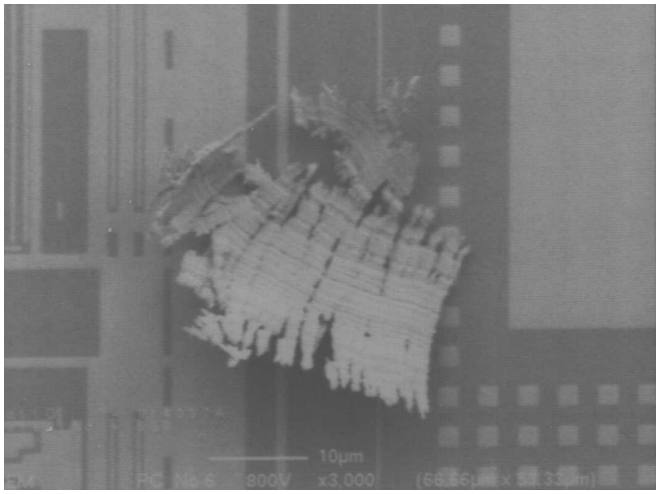
Post-CMP Inline Electrical Testing

Motivations

- measuring metal leakage after each copper CMP step can identify wafers with copper or barrier residues that need CMP rework
- monitoring of dishing & erosion with various test structures

Limitations

- contact on copper bondpads not reliable
- increased contact overdrive of probetips creates copper debris
- essential to minimize overdrive & maintain probecard with clean / planar tips
- test structure is very dependent on surrounding pattern density
- throughput

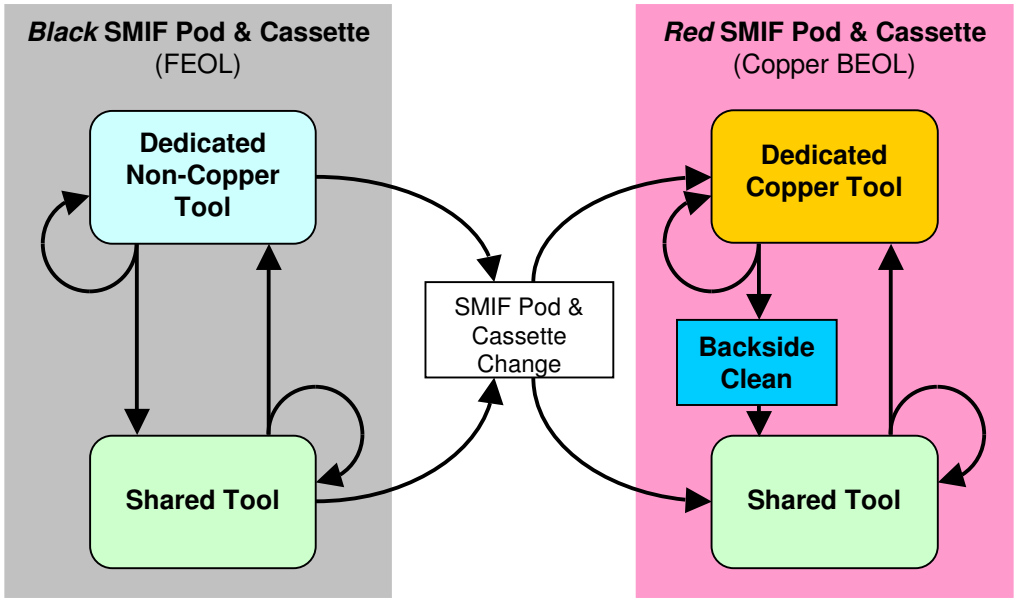


Recent Development

- sensitive optical detection of metal residues (contactless)

Potential Fab Contamination Concern

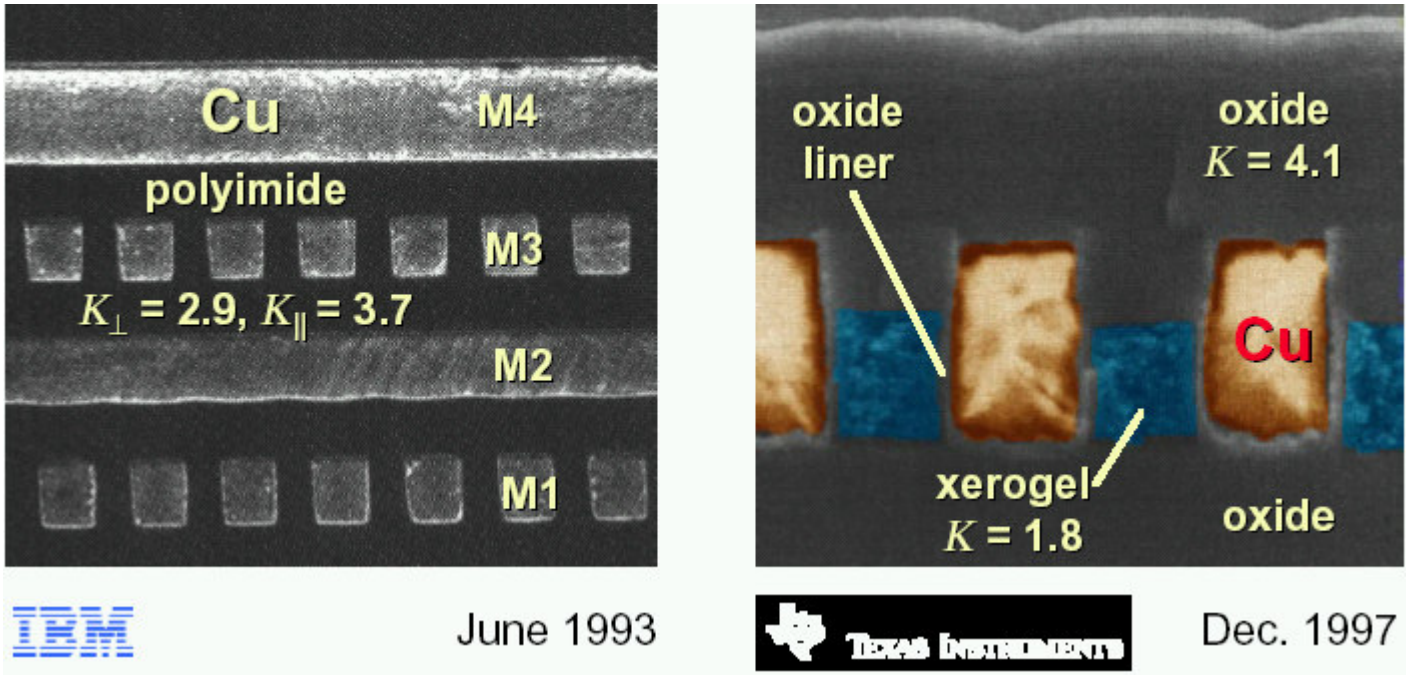
- high tool costs require some tool sharing between copper & non-copper processes, e.g., lithography, metrology
- wafer handling by copper tools adds Cu to wafer backside
- shared tools can cross-contaminate frontend tools through common wafer handling of copper & non-copper wafers



SMIF pod

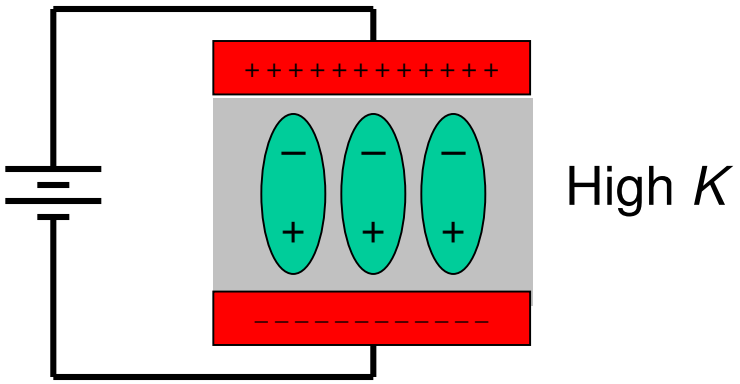
Moving to Low-*K* Dielectrics

- Damascene Cu integration with lower *K* dielectrics for reduced capacitance
- Migration to FSG only an incremental improvement
- Plenty of new integration & reliability issues beyond FSG due to fundamental differences in materials properties
- Plenty of early demonstrations in 1990's, but not manufacturable until recently

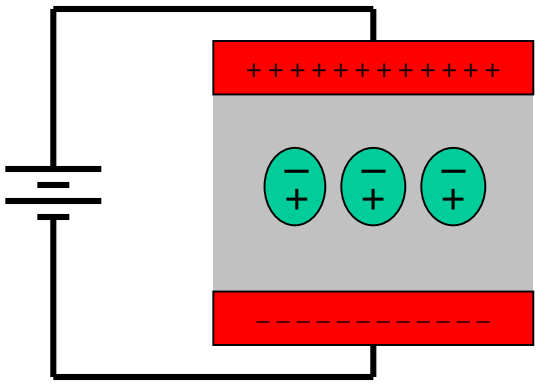


What Makes *K* Low?

- *K* = dielectric constant = relative permittivity = $\varepsilon / \varepsilon_o$
- *K* measures an insulator's polarizability when exposed to an electric field
- Low *K* → weak polarization (difficult to induce dipoles)



High *K*

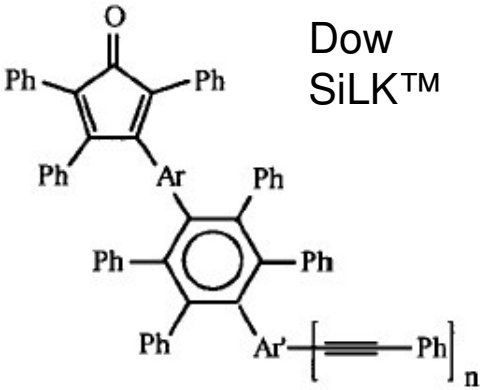


Low *K*

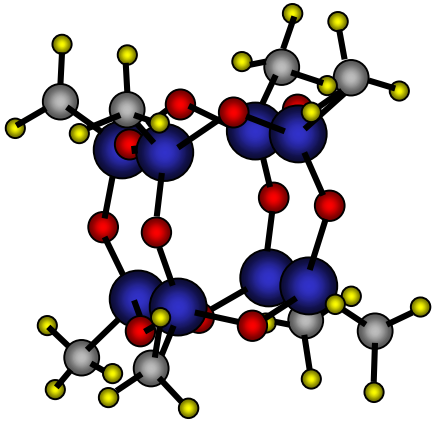
- Materials with low *K* have:
  - Weakly polar chemical constituents
  - High porosity (K_{AIR} = 1)
  - Minimal / no moisture content (K_{WATER} = 80)
  - High degree of structural symmetry for dipole cancellation

Low-*K* Materials Choices

- FSG / F-TEOS (*K*=3.2-3.9) – first generation low-*K*, just incremental
  - Fluorine reduces polarity of bridging oxygens in glass – undoped TEOS (*K*=4.0-4.2)
  - Moisture uptake if % F is too high, *K* > 3.5 for stable film
  - Weaker adhesion to metals & dielectrics, potential corrosion
- Nonporous organic polymers / open-structure glasses – spin-on vs. CVD
- Porous materials (*K*<2.5)
  - Porous MSQ (methyl silsesquioxane) most extensively developed so far
  - e.g., AMAT Black Diamond, Novellus Coral® (contains Si, O, C, H)
- Conservative industry favoring CVD of porous silicate-based material although some companies invested heavily in spin-on pure organics



Dow
SiLK™



MSQ

H
C
O
Si

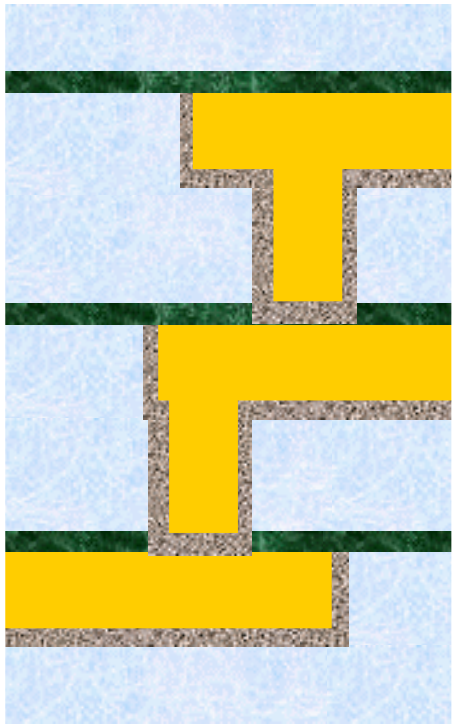
Low-*K* Materials Limitations

- Introduces significant integration complexity

- Mechanically weak (low Young's modulus)
- Softness → CMP compatibility
- Thermal stability → limited process options
- Thermal conductivity → reliability
- Adhesion (intrinsic to low *K*)→ delamination, interface leakage
- Porosity → moisture uptake
- Wet chemical clean compatibility → surface treatments
- Dry etch / ashing compatibility → hard masks, plasma damage

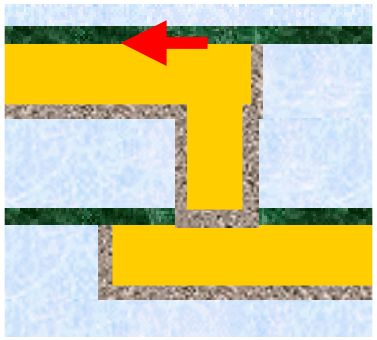
Why is Low-*K* Integration So Tough?

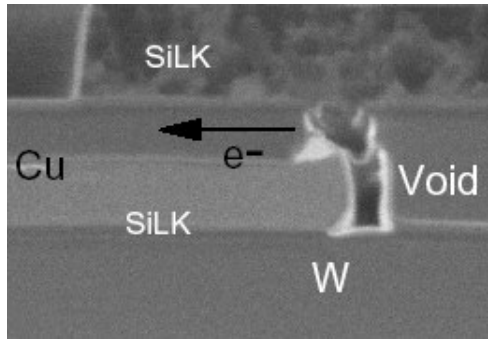
- Not just a simple matter of replacing oxide/FSG with low-*K* dielectric
- Lots of integration issues
  - Lithography (resist poisoning, multilevel planarity)
  - Damage-free etch & resist ashing (dielectric hard masks & etch stops)
  - Void-free & low-stress Cu plating
  - Scaling higher-ρ barrier & higher-*K* dielectric liner thicknesses (atomic layer deposition)
  - CMP compatibility (low down-force with minimal dishing, polish stops)
  - Impact on Transistors (high-*K* gate integration, NBTI)
  - Packaging (mechanical integrity, delamination, thermal budget)
  - …



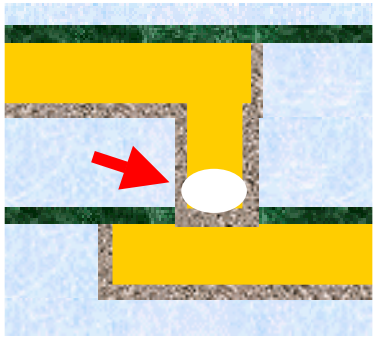
Reliability Even Tougher…

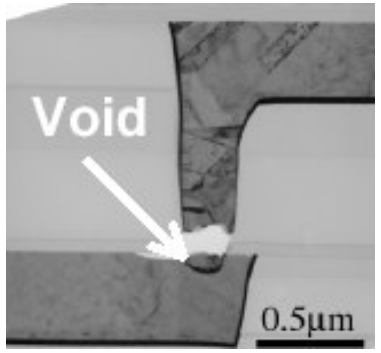
- Electromigration along weak interfaces
  - need surface/interface treatments



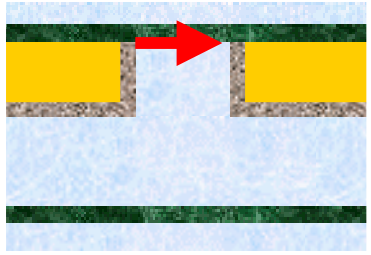


- Via stress migration voiding
  - HUGE PROBLEM
  - backend/package heat cycles
  - barrier delamination, metal stresses





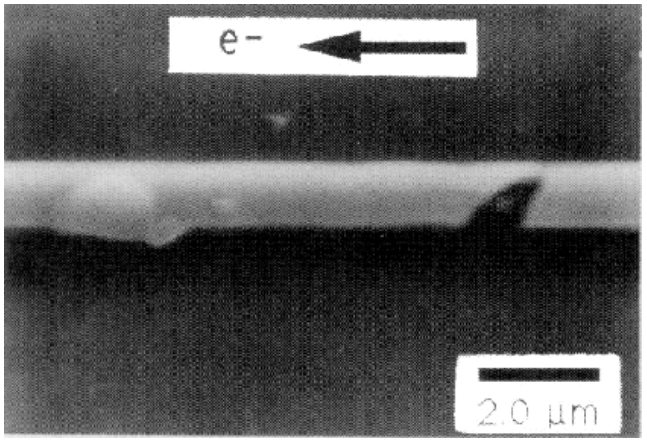
- TDDB
  - time-dependent dielectric breakdown
  - leakage from dielectric wearout



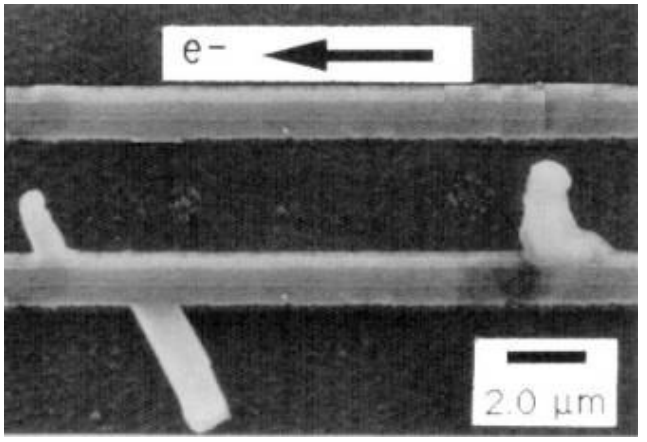
- Interface control is key!!!

What is Electromigration?

- Major wearout failure mode for IC interconnects → reliability issue



Metal void → open circuit



Metal hillock → short circuit

Nix *et al.* (1992)

- Mass transport in electrical conductor due to momentum exchange between large flux of conducting electrons and diffusing metal atoms
- Fundamentally a materials problem
- Phenomenon discovered by Gerardin (1863) in liquid metal alloys

Why Does Electromigration Happen?

- At high current densities, “electron wind” imparts momentum onto metal atoms during scattering events or collisions
- Mass transport or self-diffusion of metal atoms
  - $\rightarrow$ atomic densities (ρ) deviate from equilibrium (ρ_0)
  - $\rightarrow$ regions of tensile & compressive stress in metal
  - $\rightarrow$ atomic bonds experience tensile & compressive strain
- Void forms when tensile stress in metal is so high that it is thermodynamically more favorable to form void instead of sustaining build-up of tension in metal
- Hillock forms when compressive stress in metal is so high that surrounding dielectric/barrier encapsulation can no longer resist further build-up of compression in metal
- Understanding mechanical stresses is key to designing EM-resistant interconnects

Some Mass Transport Physics

- Driving Forces for mass transport

$$F = \nabla\mu = F_{EM} + F_{TM} + F_{\sigma} + F_{S}$$

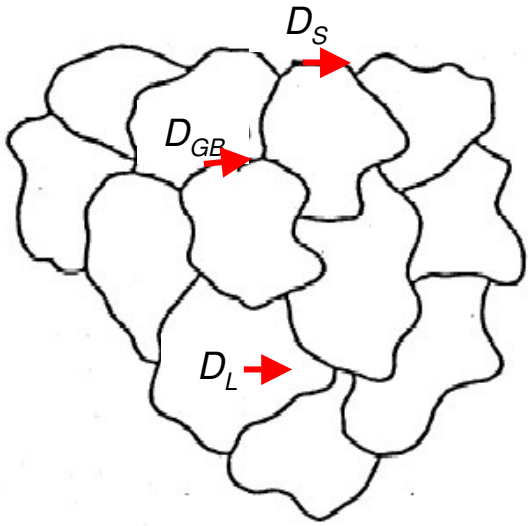
- F_{EM} = migration due to electron wind (electromigration)
- F_{TM} = migration due to temperature gradient (Soret effect)
- F_{σ} = migration due to stress gradient (creep or stress migration)
- F_{S} = migration due to entropy (atomic concentration)

Diffusion Paths

- Metal self-diffusion is a thermally activated process

$$D = D_0 \exp(-E_A / k_B T)$$

- Generally, $D \downarrow$ as $E_A \uparrow$
- E_A depends on diffusion path
  - Lattice / bulk diffusion ~ 20 $k_B T_{MELT}$
  - Grain boundary diffusion ~ 10 $k_B T_{MELT}$
  - Surface / interface diffusion ~ 7 $k_B T_{MELT}$



- Electromigration slowest when bulk diffusion dominates
  - High T_{MELT} metals → copper, refractory metals (W, Ta)
  - Large grains (bamboo structure) → cut off grain boundaries paths
  - Passivate surfaces/interfaces → cut off rapid diffusion paths

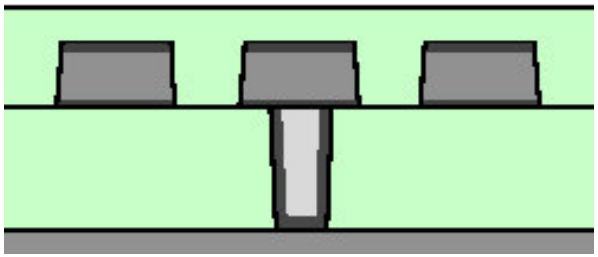
Black's Equation

$$t_{50} = (A / j^{n}) \exp (E_A / k_B T)$$

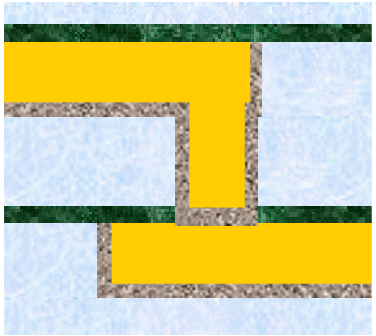
- t_{50} = median TTF (time-to-failure)
- A = constant (depends on microstructure)
- j = current density
- n = current density exponential (n =1-2 typical) → growth / nucleation
- E_A = activation energy → diffusion path
- k_B = Boltzmann's constant
- T = absolute temperature

Reliability Engineering

- Al / oxide
  - 0.5% Cu doping in Al typical to plug up grain boundaries
    - Incubation period in EM failures
  - Large grains with (111) orientation
    - Minimize *flux divergence* / scattering
    - Special seed layer requirements
  - Encapsulation by compressive dielectric



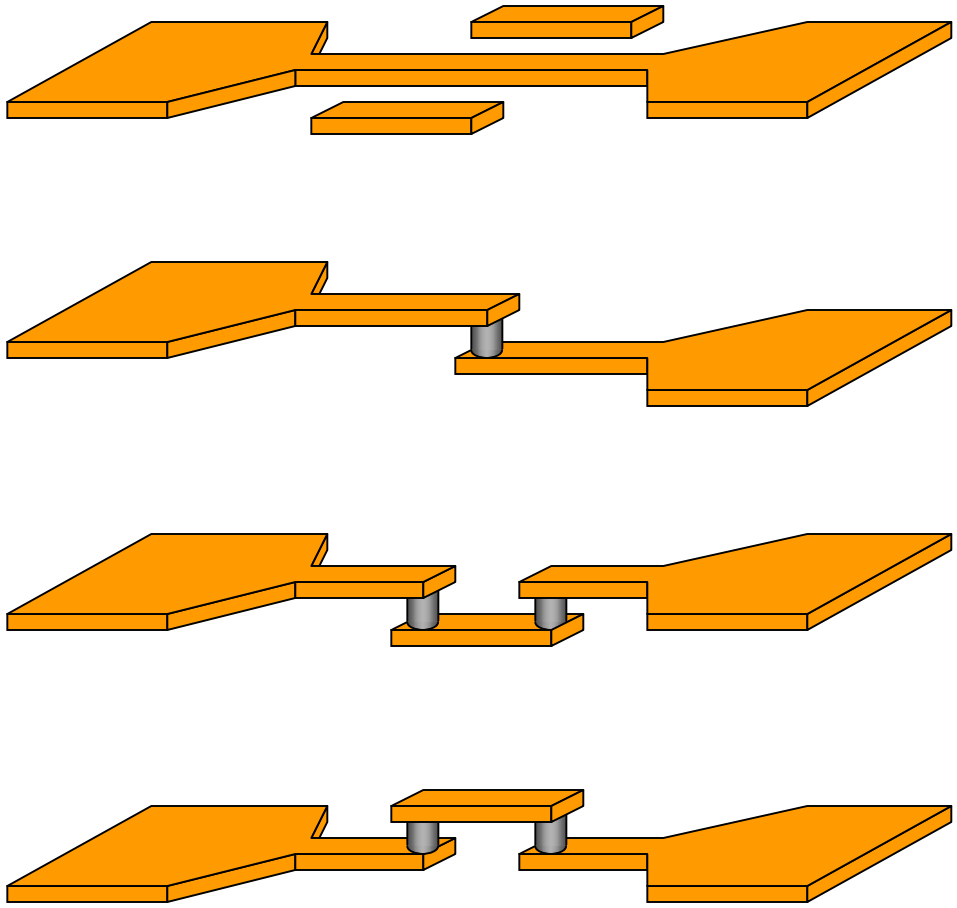
- Damascene Cu / oxide & Cu / low-*K*
  - Stress reduction in plated films
  - Interface sealing with surface treatments
  - Conformal Barrier coverage
  - Large grains with (111) orientation
    - Minimize flux divergence / scattering
    - Special seed layer requirements
  - Mechanical rigidity



Electromigration Testing

- Accelerated testing of many lines at higher temperatures & current densities
  - Record line time-to-failure (*TTF*), e.g., defined as time for line resistance to increase by some % due to voiding
  - Extrapolate some conservative TTF (e.g., 0.1 percentile) to nominal IC operating conditions using Black's equation
- Very statistical in nature → want high *TTF* **AND** small σ_{TTF}
- Compare different types of test structures to exercise different weak spots in interconnect structure
  - Via EM very significant (current crowding, weak interfaces)

EM Test Structure Examples



How Do These New Interconnect Technologies Impact Designers?

- More to worry about… like there isn't enough in design alone
- Design must account for process limitations
  - Greater process variations (in addition to voltage & temperature)
  - CMP constraints
  - Yield considerations
  - Reliability considerations (electromigration)
- Design rule complexities
  - Layout density checks / dummification
  - More conservative rules, e.g, redundant vias
  - Metal slot / maximum line width rules
  - Mechanical integrity, e.g., sea of vias to support large bondpads

Summary / Future Trends

- Limitations with aluminum interconnect scaling has forced industry-wide migration to on-chip copper metallization.
- Dual-damascene copper interconnect processes with FSG now in mass production.
- Leading IC manufacturers on track to successfully integrate true (non-FSG) low-*K* dielectrics, some migrating to single damascene copper.
- *K* scaling has not kept pace with forecasted IC roadmaps due to materials integration challenges.
  - Pressure to recover performance from higher performance transistors (e.g., with strained Si, high-*K* dielectrics, SOI)
- Interconnect reliability much more challenging but performance bar is much higher than before.
- Industry trend is to integrate more porous low-*K* with copper in 300mm.

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