Monolithic Instruments

(New opportunities for wafer fabs)

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Outline

- Trend in Manufacturing and Instrumentation
- Definition of Monolithic Instruments
- Examples
  - Elevated Photodiode Arrays
  - OLED Microdisplays
  - Digital Micromirrors
- Manufacturing/Integration Challenges
- Future Opportunities
Product Trends

- **Instrumentation**
  - Reduced system size.
  - Increased computational power.
  - Increased operational speed.
  - Improved levels of process control.
  - Improved reliability of manufacturing systems.
  - Reduced system cost.

- **Integrated Circuits**
  - Reduced system size.
  - Increased computational power.
  - Increased operational speed.
  - Reduced transducer size.
  - Novel solid-state transducers/actuators.
  - Reduced system cost.

Largely Enabled by Integrated Circuits!
Semiconductor Manufacturing

- **Current Manufacturing Tolerances**
  - Wafer flatness: < 100nm across a 300 mm wafer.
  - Metal impurity concentration: < 1 x 10\(^{10}\) cm\(^{-3}\).
  - Stacking fault density: < 1/cm\(^2\).
  - Layer-to-layer alignment tolerance: < 25 nm.
  - Linewidth control: 3 nm 3\(\sigma\).
  - Minimum feature half-pitch: 100 nm.
  - Film thickness control: < 4% 3\(\sigma\) over 300 mm.

- **Current typical high-volume CMOS device specs.**
  - Transistor Density: ~9 x 10\(^7\) transistors/cm\(^2\).
  - Operating Frequency: ~1.7 GHz.
  - Manufacturing Cost: ~ $32/cm\(^2\).
    - $3.6x10^{-7}$/FET
## Value of a Semiconductor Mfg. Platform

<table>
<thead>
<tr>
<th></th>
<th>Semiconductor Mfg</th>
<th>Machining Mfg</th>
<th>Mach./Semi.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Minimum Feature Size</strong></td>
<td>0.25 µm</td>
<td>100 µm</td>
<td>400:1</td>
</tr>
<tr>
<td><strong>Alignment Tolerance</strong></td>
<td>&lt; 25 nm</td>
<td>~ 10 µm</td>
<td>40,000:1</td>
</tr>
<tr>
<td><strong>Manufacturing Cost</strong></td>
<td>$1 \times 10^{-6}$ FET</td>
<td>~$2 \times 10^{-1}$ /switch</td>
<td>200,000:1</td>
</tr>
</tbody>
</table>

For the number of devices made, a semiconductor fab is the most precise and least expensive manufacturing environment.
Definition of Monolithic Instruments

Monolithic instruments are miniaturized systems, combining conventional integrated circuits with novel solid-state components, that interact with their physical environment.

Concept- Incorporate several instrumentation system functions onto a single die.

- Transducer/actuator
- Driver (analog function)
- Analog/Digital interface
- Signal processing
- Data analysis
- I/O
Classes of Monolithic Instruments

- Pre-integrated circuit.
- During integrated circuit fabrication.
- Post-integrated circuit fabrication.

Monolithic Instrument Examples

- Some types of monolithic instruments that have been fabricated include:
  - a-Si:H photodiode arrays.
  - Organic LED micro-arrays.
  - Digital Micromirror Devices.
  - Liquid-crystal microdisplays.
  - Bio-assay array systems.
  - Inter-cellular communications.

- Components proposed for future monolithic instruments include:
  - Thin-film bulk acoustic resonators.
  - Photonic crystals.
  - Planar light-guide systems
  - Group IV-based LEDs.
  - SQUID magnetometers
Fabricated Monolithic Instruments

- Inkjet heads (Hewlett-Packard, Loveland and Corvallis).
- Digital micromirror displays (Texas Instruments).
- DNA microarray detectors (Infineon).
- Direct neuron communicators (Infineon).
- a-Si:H photodiode arrays (Agilent).
Advantages of Monolithic Instruments

- Better performance.
  - Improved signal integrity.
  - Access to novel transducer technology.
- Smaller.
- Cheaper.

What we have come to expect from improvements in integrated circuit technology can be applied to instrumentation systems.
Monolithic Instrument Technologies

- Elevated Photodiode Arrays.
- OLED Microdisplays.
- Digital Micromirror Arrays.
a-Si:H Elevated Photodiodes

- Hydrogenated amorphous silicon is a deposited semiconductor.
  - Bandgap ~1.8 eV.

- Advantages
  - Higher QE.
  - Tunable spectral response.
  - Lower thermal effects.
  - Higher fill factor.
  - Cheaper imager.

- Disadvantage
  - Subject to metastabilities that can affect performance (Staebler-Wronski Effect).
Dielectric Isolation Interconnect

- Two extra masking levels.
- Requires a dry etch with high selectivity between two conductive materials.
TFT-Based Monolithic Interconnections

**Fig. 4.12.** Cross-sectional view of a pixel showing the a-Si:H TFT and p-i-n photodiode sensor


**Fig. 4.19.** Example of the design of a high fill factor sensor array using a continuous a-Si:H photodiode layer with a patterned n-type doped contact
Local-via Monolithic Interconnect Structure

Transparent Conductor
p a-Si:H

Top Conductor Contact

i a-Si:H

Bottom Contact

n a-Si:H

IC Passivation

US Patent 6018187
Elevated a-Si:H Photodiodes - Pixel Size Reduction

**c-Si 3T Pixel**

**a-Si:H 3T Pixel**
Integrated a-Si:H Photodiode/CMOS Stack

- 0.35 μm 4LM CMOS process.
- 5.9 μm square pixel, on a 7 μm pitch.
- Interpixel isolation created by etching of the n-layer a-Si:H.
- Planarized passivation layer.
a-Si:H Material Properties

- Integrated DOS $\sim 2.5 - 4 \times 10^{15}$ cm$^{-3}$.
- Mid-gap peak $\sim 0.88$ eV from the conduction band edge.
  - A second peak at $\sim 0.83$ eV.
- 1.85 eV band-gap.
- $E_a \sim 0.9$ eV.
- $E_U \sim 56$ meV.
- Deposition Rate $> 30\text{Å/s}$.

J. Theil, D. Lefforge, G. Kooi, M. Cao, G. Ray,
Effect of p-layer thickness on quantum efficiency

![Graph showing the effect of p-layer thickness on quantum efficiency. The graph illustrates the quantum efficiency (el/ph) as a function of wavelength (nm) for two different p-layer thicknesses: 200A and 100A. The graph indicates that thicker p-layers generally result in higher quantum efficiencies at certain wavelengths.](image-url)
Effect of layer doping on quantum efficiency

AA008 Spectral Response
(Effect of B Doping)

Quantum Efficiency (el/ph)

Wavelength (nm)

LD p Layer (08)
Control (09)
LDp LDn (12)
No n-layer (20)
Dark Current Components

- Two components of dark current:
  - Junction leakage.
  - Array edge leakage.

- Guard ring prevents edge current from reaching the array.

- Sweep guard ring and area diode together.
  - Assume: $I_x = 0$.
  - $I_E = I_A \frac{A_{\text{ring}}}{A_{\text{area diode}}}$.
Dark Current Density vs Electric Field

![Graph showing the relationship between Dark Current Density and Electric Field](image)

- Current Density (A/cm²) vs Electric Field (V/cm)
- Logarithmic scale for Current Density
- Lines for different currents (9000A, 7500A, 5500A, 4000A, 3000A)
Structures and Junction Parameters

- n-layer thickness: 500Å. ([P] 2 x 10²⁰ cm⁻³)
- i-layer thickness: 3000 to 9000Å. (5500Å default value)
- p-layer thickness: 200Å. ([B] 7 x 10¹⁹ cm⁻³)
Effect of Pixel Edge Length on Reverse Bias Current (3000Å I-layer)

Voltage (V)

<table>
<thead>
<tr>
<th>Current Density (A/cm²)</th>
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<tbody>
<tr>
<td>1.23E+06 microns</td>
</tr>
<tr>
<td>5.77E+05 microns</td>
</tr>
<tr>
<td>1.94E+05 microns</td>
</tr>
<tr>
<td>5.95E+04 microns</td>
</tr>
<tr>
<td>2.11E+04 microns</td>
</tr>
<tr>
<td>3.84E+03 microns</td>
</tr>
</tbody>
</table>
Stacked Elevated Photodiode Concept
Optical Response of Stacked Diode Elements

![Graph showing the optical response of stacked diode elements.](image)

- Blue line: 800A i
- Green line: 2000A i
- Red line: 9000A i
- Black line: 9000A i with filter

Quantum Efficiency (e-/ph) vs. Wavelength (nm)
a-Si:H Color Sensor Image
(640x480 4.9 x 4.9 µm pixel, 1900 lux)
OLED Microdisplays

- **Organic Light-Emitting Devices (OLEDs)**
  - Charge transport mechanism: localized state-based hopping.
  - Use for large area emissive displays, fabricated using evaporation or printing.
  - Just gaining acceptance.
  - Has lifetime issues.

- **Applications**
  - Eyepiece imagers (digital cameras).
  - Eyeglass displays.
    - Computers
    - Instrumentation

- **Advantages over LCD microdisplays**
  - Smaller
  - Brighter (more power efficient).
  - Less expensive (fewer components required).

Thanks to Howard Abraham for driving the Ft.Collins Development
Microdisplay Systems

LCD/LED-based Microdisplays

Value Proposition:
Simpler, Cheaper, Brighter

Microdisplay Based on Light Emitting Polymers

LEP
CMOS Silicon APIX

Viewing eye
Lens

Agilent Technologies
Monolithic Instruments- Jeremy Theil
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Organic LED Materials

Organic LED’s: Materials and Devices

OLEDs rely on organic materials (polymers and small molecules) that give off light when tweaked with an electrical current.

Small Molecules (vacuum evaporated)
- HTL: metal-phthalocyanines, arylamines (CuPc, NPD)
- ETL, EML: metal chelates, distyrylbenzenes

Polymers (spin cast)
- HTL: conducting polymers (PDOT, PANI)
- ETL, EML: polyphenylenevinylene, fluorenes

Eastman Kodak, Pioneer, Idemitsu Kosan, Sanyo, FED Corp., TDK
CDT, Philips, Uniax, Dow Chemical, DuPont

NPD (HTL)  Alq3 (ETL, EML)  R-PPV (EML)  Polyfluorene (EML)

Operating voltage ~10V  Operating voltage ~5V

Agilent Technologies
Organic Electroluminescence

Organic electroluminescence by charge injection

- Hole injection from high work function transparent anode (ITO) and transport through HTL
- Electron injection from low work function cathode (Ca, Mg, LiF/Al, CsF/Al) and transport through ETL
- Since \( I_P < E_A \) electrons are blocked by HTL and holes tunnel to ETL
- Formation of excitons and light emission from ETL
  - Diode-like I-V (no light on reverse bias)
  - Low turn-on voltage (\( \sim 2 \) V)
  - Operating voltage >> turn-on voltage
    - Charge Injection limitations
    - Charge Transport limitations
- Efficiency
  - 1-5% ph/el
  - 1-22 lm/W

Charge Injection limitations
Charge Transport limitations
OLED Diode Construction

Process Overview for APIX/LEP Microdisplay

Device Layout:

- **Seal Layer (Transparent)**
- **Cathode (Semitransparent)**
- **Light Emitting Polymer (Diode)**
- **APIX Active Matrix Circuit on Silicon**

Emitted Light

Light Emitting Polymer (Diode)

Electrical Schematic
OLED Challenges

- Environmental sensitivity.
- Device lifetime.
**OLED Diode Structure**

**Process Overview for APIX/LEP Microdisplay**

**Device Layout:**

```
| Transparent Passivation Layer 2 |
| Transparent Passivation Layer 1 |
| Semitransparent Cathode Layer 1 |
| Semitransparent Cathode Layer 2 |
| Polymer Layer (ETL, EML)         |
| PEDOT Layer (HTL)               |
| ANODE | ANODE | ANODE |
```

**Specific Fabrication Steps (sequence is bottom up):**

- Functional test, Mount chips to daughter board, Wire bond pads to board, Final test
- Encapsulate cathode with seal process steps. N2 atmosphere.
- Thermally evaporate semitransparent cathode using die-sized shadow mask. N2 atmosphere.
- Spin Electron Transport Layer (also the Emission Layer) light emitting polymer. N2 atmosphere.
- Bake PEDOT (180°C, 1 hr).
- Spin Hole Transport Layer (PEDOT).
- Surface clean (IPA/O2 Plasma).

Process APIX on 6” or 8” silicon wafers.
OLED Microdisplay Driver Circuits

Pulse-width modulation pixel driver circuit.
OLED Microdisplay Operation
Digital Micromirrors

- Invented at Texas Instruments in 1987 (by Larry Hornbeck).
- Build hinged mirrors from BEOL metallization over SRAM pixels.
- Operates by electrostatic attraction between mirror and pixel electrodes.
Digital Micromirror- Construction

DMD array (progressive cutaway)

© Texas Instruments
Digital Micromirror- Schematic

DMD Pixel Electrical Schematic

- $V_b$: Bias Voltage
- $V_a$: Address Voltage
- $\bar{V}_a$: Address Voltage Complement

Regions of Electrostatic Attraction

Memory Cell (CMOS SRAM)

© Texas Instruments
Digital Micromirror - Mechanics

Potential Energy of a Mirror as a Function of Angle and Bias (address voltage = 0)

© Texas Instruments
Digital Micromirror- Applications

- Projections Displays
- Digital Movie Projectors
- Digital Printing and Photofinishing
- 3D Non-holographic displays
- Maskless photolithography
  - DNA sequencing
- Broadband switching
- Holographic storage
- ... Anywhere LCD can be used, with higher contrast.

Integration Challenges

● Known Issues
  ● Material compatibility with the “nominal” process flow.
    ● Adverse effects of the standard structures.
    ● Adverse effects of the new structures.
  ● Manufacturability of new unit modules.
  ● Materials optimization.
    ● Material performance considerations.
    ● Integration compatibility considerations.

● Unknown Issues
  ● There will be plenty of them.
  ● We encountered 8 major issues in one project.
    ● Example: The 9 causes of adhesion failure.

Expect the unknown!
The Future

- Integrated circuit manufacturing platforms can be extended to make monolithic instruments.
- Many classes of monolithic instruments can be created.
- The attributes of monolithic instruments enable hundreds of new applications.
  - Low cost
  - Small size

- There are plenty of opportunities out there.
- Who is going to take advantage of them?