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A BASIC PROPERTY OF MOS TRANSISTORS AND ITS CIRCUIT IMPLICATIONS

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INTRODUCTION

- Goals of transistor modeling:
  - simulation by quantitative calculation on computer
  - highlighting properties to facilitate
    - understanding circuits
    - synthesis of robust circuits

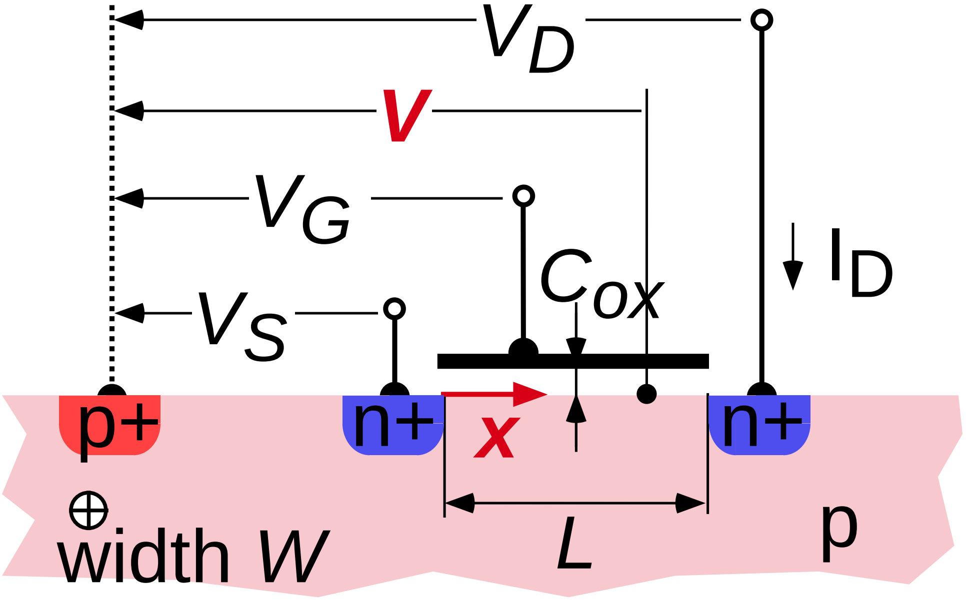
- Best models: combine both goals by hierarchical structure

  example: EKV model [1].

- EKV approach will be used to explicit a basic property.

DEFINITIONS

for EKV model



- Substrate referred-voltages

  V_S, V_D, V_G

- Local "channel voltage" V

  splitting of quasi-Fermi levels due non-0 V_S and/or V_D

  $V = V_S$ at source

  $V = V_D$ at drain

  n-channel: holes at equilibrium

  thus V = electron quasi-Fermi level + constant.

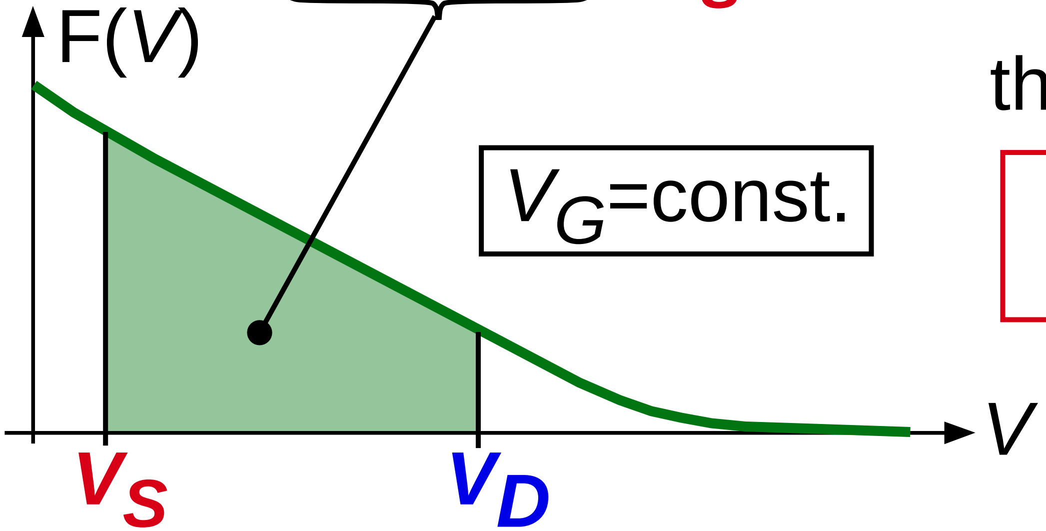
BASIC PROPERTY (1)

- For a long and wide channel:

$$I_D = \mu W(-Q_i)\frac{dV}{dx} \underset{\uparrow}{=} \frac{F(V,V_G)dV}{G(x,V_G)dx}$$

- Condition: separable in V and x

$$\text{then: } \underbrace{I_D\int_0^L G\,dx}_{} = \int_{V_S}^{V_D} F\,dV \equiv \int_{V_S}^{\infty} F\,dV - \int_{V_D}^{\infty} F\,dV$$



$\boxed{V_G\text{=const.}}$

thus:

$$\boxed{I_D = I(V_S,V_G) - I(V_D,V_G)}$$

BASIC PROPERTY (2)

$$\boxed{I_D = \mathrm{I}(V_S, V_G) - \mathrm{I}(V_D, V_G)} \quad \text{with: } \mathrm{I}(V, V_G) = \frac{\int_V^\infty \mathrm{F}\,\mathrm{d}V}{\int_0^L \mathrm{G}\,\mathrm{d}x}$$

- The drain current is the superposition of independent and symmetrical effects of source and drain voltages.

- Definitions:
  - **Forward** current $I_F = \mathrm{I}(V_S, V_G)$, independent of V_D
  - **Reverse** current $I_R = \mathrm{I}(V_D, V_G)$, independent of V_S

$$\boxed{\text{then } I_D = I_F - I_R}$$

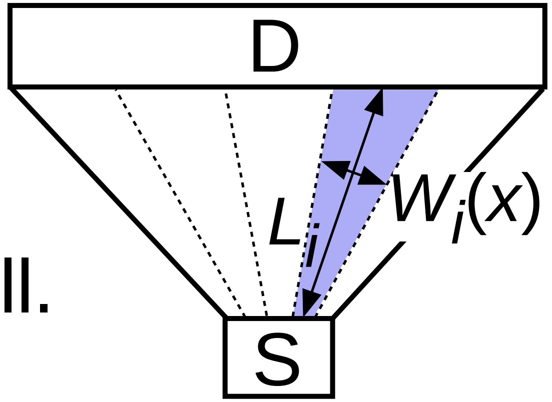
- Saturation: forward: $I_R \ll I_F$; reverse: $I_F \ll I_R$

DOMAIN OF VALIDITY (1)

- Condition:

$$\boxed{\mu W(-Q_i) = \frac{F(V,V_G)}{G(x,V_G)}}$$

- W is independent of V; thus:
  - is part of G, and may thus depend on x
- Whatever its shape, a transistor can be split into several parallel transistors i of variable W_i and differents L_i.
  - as long as each element i fulfils



$$I_{Di} = I_i(\mathbf{V_S},V_G) - I_i(\mathbf{V_D},V_G)$$

then the sum I_D of I_{Di} fulfils it as well.

- The property independent of shape.

EFFECT OF NARROW CHANNEL

- Increased importance of side effects.
- Equivalent to parallel connection of several transistors with different characteristics.
  - if each transistor *i* fulfils

$$I_{Di} = \mathrm{I}_i(\boldsymbol{V_S}, V_G) - \mathrm{I}_i(\boldsymbol{V_D}, V_G)$$

  - then the sum I_D of I_{Di} fulfils it as well.
- The property is not degraded.

DOMAIN OF VALIDITY (2)

- Condition: $$\boxed{\mu W(-Q_i) = \frac{F(V,V_G)}{G(x,V_G)}}$$

with: $$-Q_i = \underbrace{C_{ox}(V_G - V_{FB} - \Psi_s)}_{\text{total charge}} - \underbrace{\sqrt{2qN_b\varepsilon_{si}\Psi_s}}_{\text{depletion charge } Q_b}$$

- Mobile charge Q_i depends on surface potential Ψ_s, and $\Psi_s = f(V)$, thus Q_i should not be a (direct) function of x to be part of F. Therefore:
  - $V_G - V_{FB}$
  - C_{ox}
  - N_b

- must be independent of position x along the channel : homogeneous channel.
- but may depend on Ψ_s or V.

(*e.g.*: $C_{ox}(\Psi_s)$: polydepletion)

DOMAIN OF VALIDITY (3)

- Condition:

$$\boxed{\mu W(-Q_i) = \frac{F(V,V_G)}{G(x,V_G)}}$$

- Mobility μ depends on vertical field thus on V_G-Ψ_S, but not on x (for homogeneous channel) thus
    - included in F, property not degraded at large V_G.
- But μ must be independent of drain current I_D
    - otherwise could not be included in F or G
    - Large L to limit longitudinal field.
- Furthermore, the effective value of L along which G(x,V_G) is integrated must be independent of I_D, V_S and V_D.

DOMAIN OF VALIDITY (SUMMARY)

The basic property is available

- For long and homogeneous channel
- Independently of channel shape
- Even if the channel is very narrow
- Even for large gate voltages reducing the mobility.

CAUSES OF DEGRADATION (1)

- Non homogeneous channel: Q_i direct function of x.

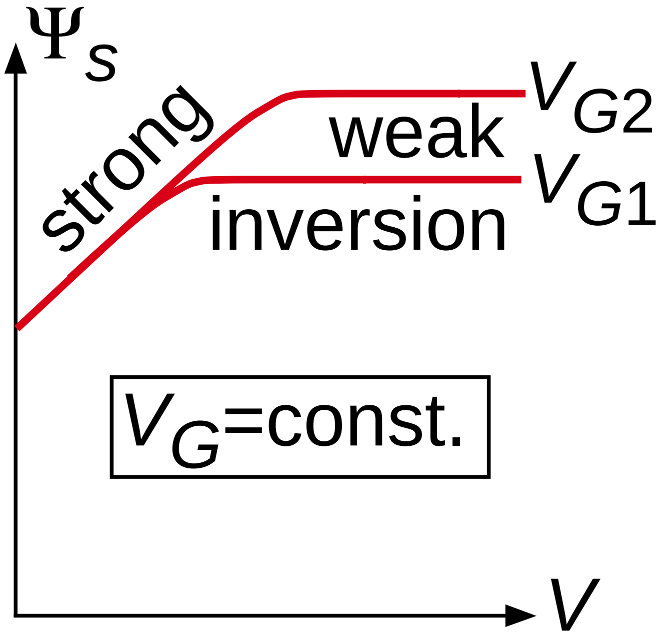
$$Q_i = -C_{ox}(V_G - V_{FB} - \Psi_s) + \sqrt{2q\, N_b\, \varepsilon_{si} \Psi_s}$$

There may be variations with position x in the channel of:

- substrate doping N_b, which can be
  - intentional (e.g.: LDD)
  - artifact of process (gradient or piling-up) (always present at very ends of channel)
- flat-band voltage V_{FB} , caused by
  - variation of N_b
  - variation of charge in oxide
- effective C_{ox}, always present at very ends of channel.

SPECIAL CASE OF WEAK INVERSION

- Weak inversion characterized by $Q_i \ll Q_b$, therefore:
  - Q_i has negligible effect on potential and field
- Can be expressed as $-Q_i = \mathrm{G_q}(\Psi_s)\mathrm{e}^{-V/U_T}$
  - with Ψ_s independent of V , thus:
  - $\mathrm{G_q}$ can be any function of x and is included in G, therefore:



- The property is valid even if the channel is not homogeneous.
- Mobility μ independent of V, thus part of G,
  - F is reduced to $\mathrm{F} = \mathrm{e}^{-V/U_T}$: independent of V_G.

CAUSES OF DEGRADATION (2)

- Channel long ⇒ non-long ⇒ short
  - property progressively degraded by...
  - several independent mechanisms:

a. Voltage effects:

- channel length modulation
  - I_F or I_R becomes function of both V_D and V_S
  - effect proportional to $1/L$
- barrier lowering and 2-D effects: further degradation.

b. Current effects:

- if I_D is increased by reducing L, then
  ⇒ carrier velocity increases towards saturation
  ⇒ mobility reduced, thus function of I_D

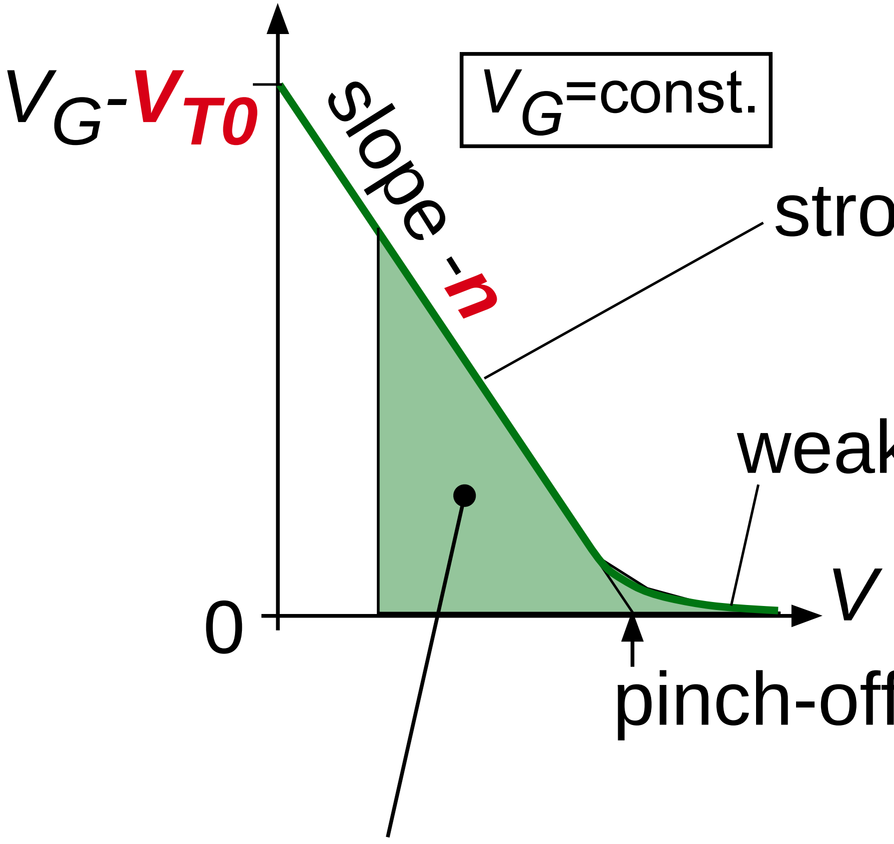
c. Non-homogeneous channel (except in weak inversion):

- importance of end-effects proportional to $1/\boldsymbol{L}$.

EXPLICIT I(V,V_G) IN FIRST ORDER EKV MODEL (1)

[1]

$F = -Q_i / C_{ox}$ and $G = \dfrac{1}{\mu W C_{ox}}$



V_G=const.

strong inversion: $n(V_P - V)$

weak inversion: $2nU_T \exp \dfrac{V_P - V}{U_T}$

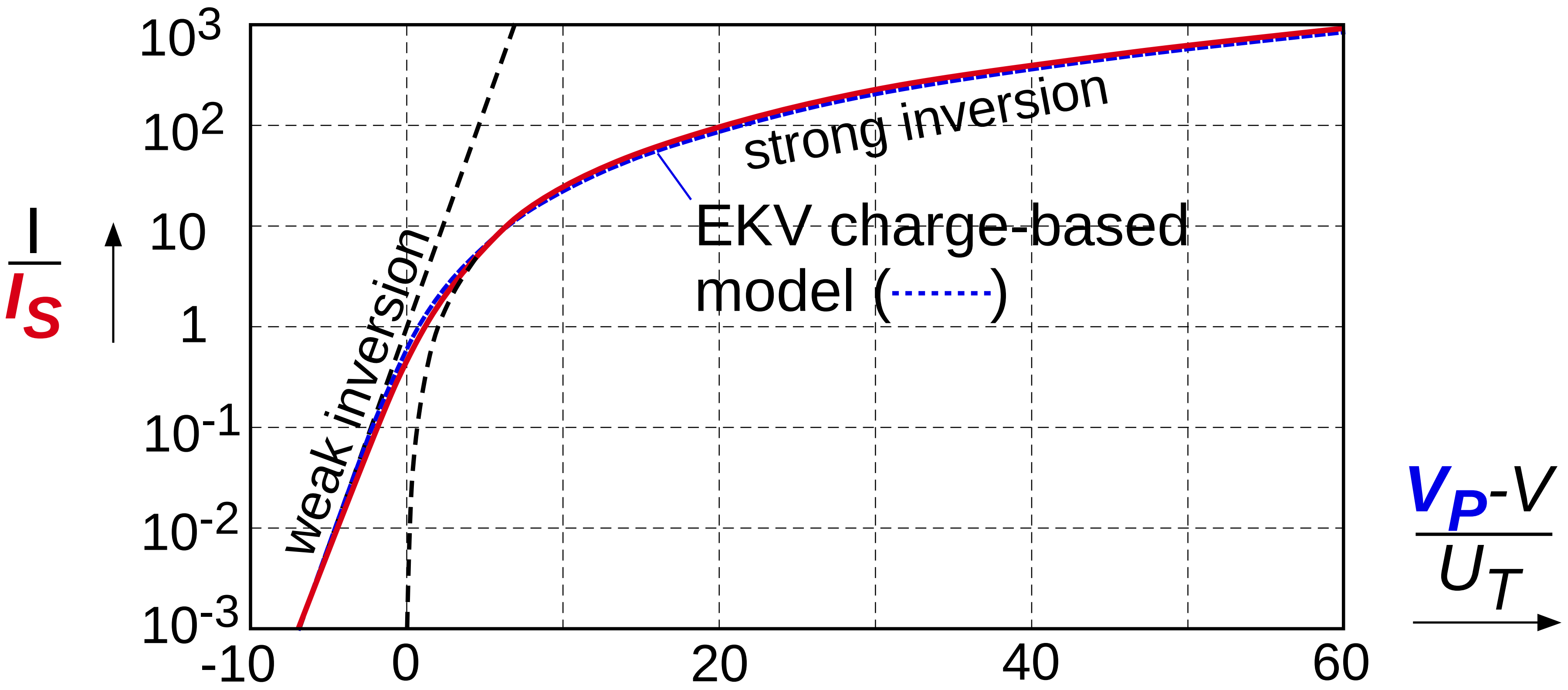
$$V_P = \frac{V_G - V_{T0}}{n}$$

$$\int_V^\infty F \mathrm{d}V = \frac{I(V, V_G)}{\beta}$$

with $\beta = \mu C_{ox} \dfrac{W}{L}$

EXPLICIT I(V,V_G) IN SIMPLIFIED EKV MODEL (2)

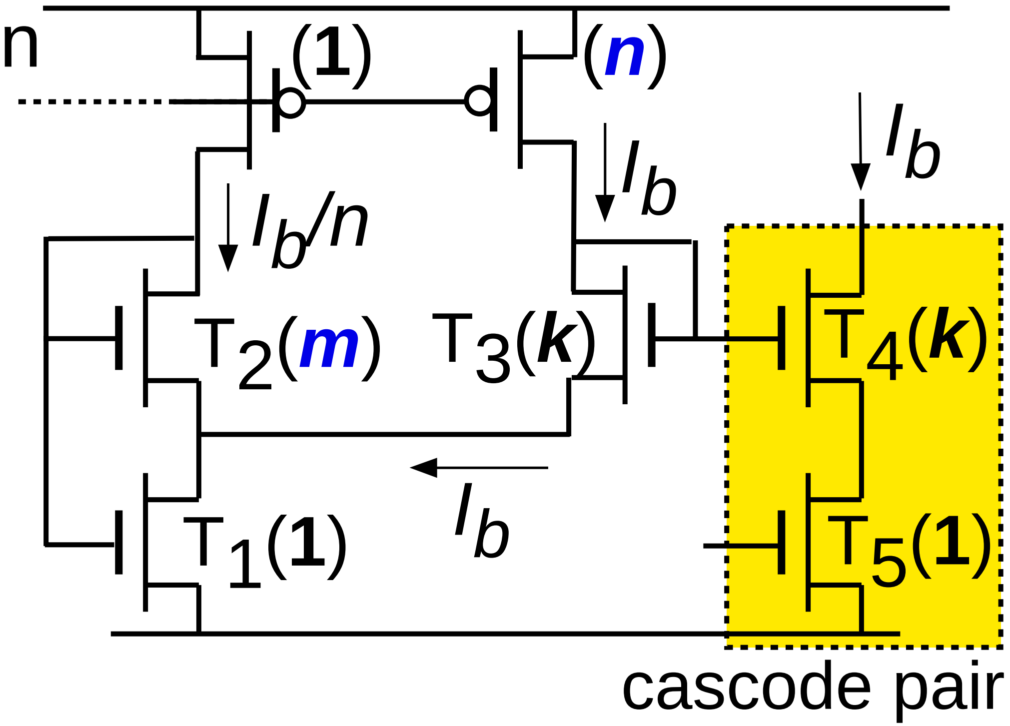
$$I(V,V_G)=\underbrace{2n\beta U_T^2}_{\text{specific current } I_S}\ \ln^2\left(1+\exp\frac{V_P-V}{2U_T}\right)=\begin{cases}\dfrac{\beta n}{2}(V_P-V)^2 & \text{for } I \gg I_S\\[2ex] I_S\exp\dfrac{V_P-V}{U_T} & \text{for } I \ll I_S\end{cases}$$



CIRCUIT EXAMPLE: LOW-VOLTAGE CASCODE

[2]

- Goal: V_{D5} min. for saturation
- Means: control $\frac{I_{R5}}{I_{F5}} \ll 1$:
  - $\boldsymbol{m}$ and $\boldsymbol{n} \gg 1$, hence:
  - $I_{D5} \cong I_{D1}$ with $V_{D5}=V_{D1}$
  - thus $I_{R5}/I_{F5} \cong I_{R1}/I_{F1}$



$$\left.\begin{array}{l} \bullet\ I_{F2} = I_b/\boldsymbol{n} = \boldsymbol{m}\, I_{R1} \\ \bullet\ I_{F1} \cong I_b \end{array}\right\} \Rightarrow \frac{I_{F1}}{I_{R1}} \cong \boxed{\boldsymbol{mn} \cong \frac{I_{F5}}{I_{R5}}}$$

- Large enough to ensure saturation
- Independent of I_b.

CONCEPT OF PSEUDO-RESISTOR [3,4]

- We have shown that: $I_D = \dfrac{1}{\int_0^L G\mathrm{d}x}\left[\int_{V_S}^{\infty} F\mathrm{d}V - \int_{V_D}^{\infty} F\mathrm{d}V\right]$

- Definitions:
  - pseudo-voltage: $\boxed{V^* = -K_0 \int_V^{\infty} F(V, V_G)\mathrm{d}V}$
  - pseudo-resistor: $\boxed{R^* = K_0 \int_0^L G\,(x, V_G)\mathrm{d}x}$

(where K_0: any positive constant)

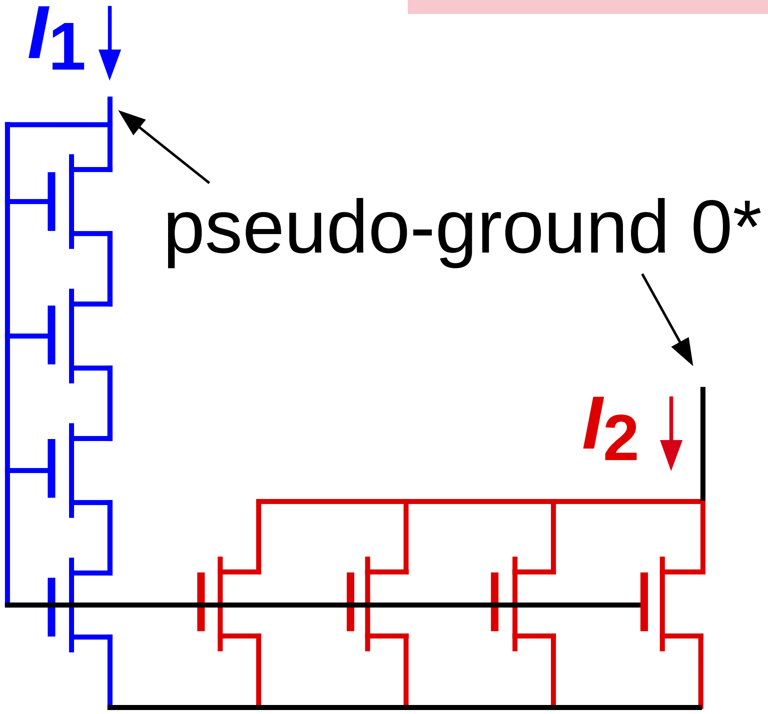
- Results in pseudo Ohm's Law: $\boxed{I_D = (V_D^* - V_S^*)/R^*}$

LINEAR CURRENT-MODE CIRCUITS [3,4,5,6]

- Implications of pseudo Ohm's law $I_D = (V_D^* - V_S^*)/R^*$
  - Any network interconnecting transistors with same F(V,V_G) and same V_G is linear with respect to currents.
  - Any circuit of linear resistors can be implemented by transistors only, provided only currents are considered.
  - A resistor connected to ground (V=0) in the resistive prototype corresponds to a saturated transistor that provides a pseudo-ground (V^*=0).
- In weak inversion:
  - F indep. of V_G, but V_G included in function G, hence:
  - Different V_G possible for each transistor
  - Each R^* can be separately adjusted by its V_G.

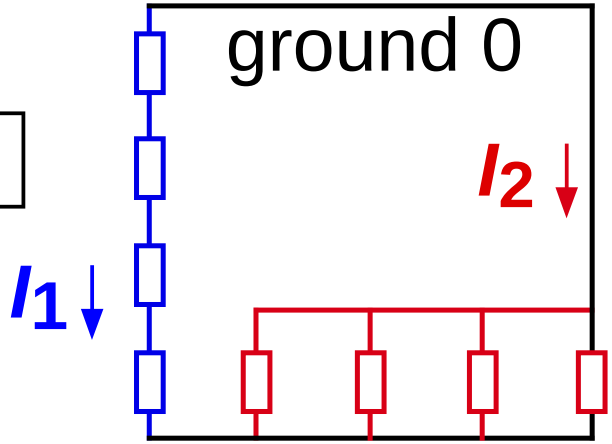
Example of application of pseudo-R:

LARGE-RATIO MIRROR



$I_2/I_1 = 16$

- pseudo-resistor prototype:

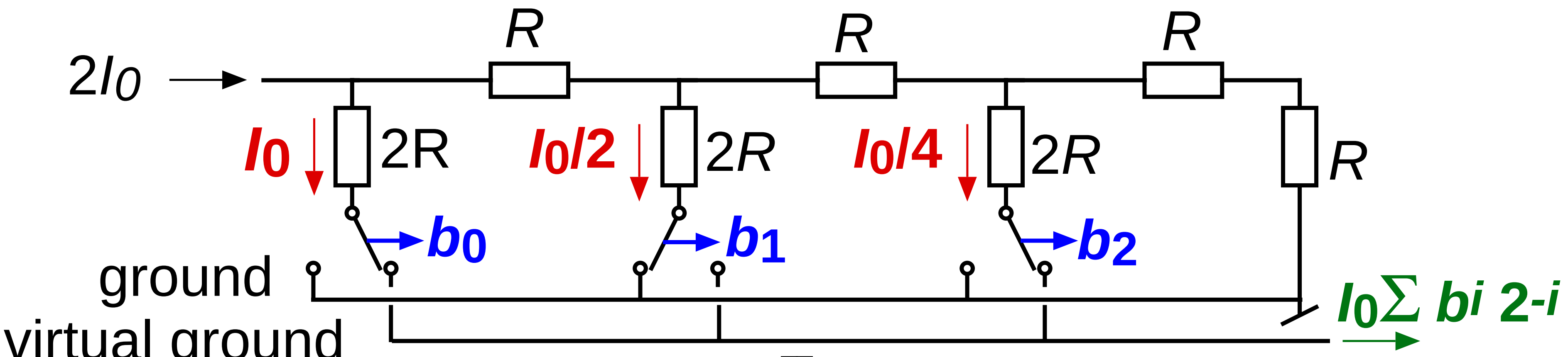


- identical transistors, all in same substrate
- much more precise than different *L* for input and output
- less precise than parallel trans. only (limits of property).

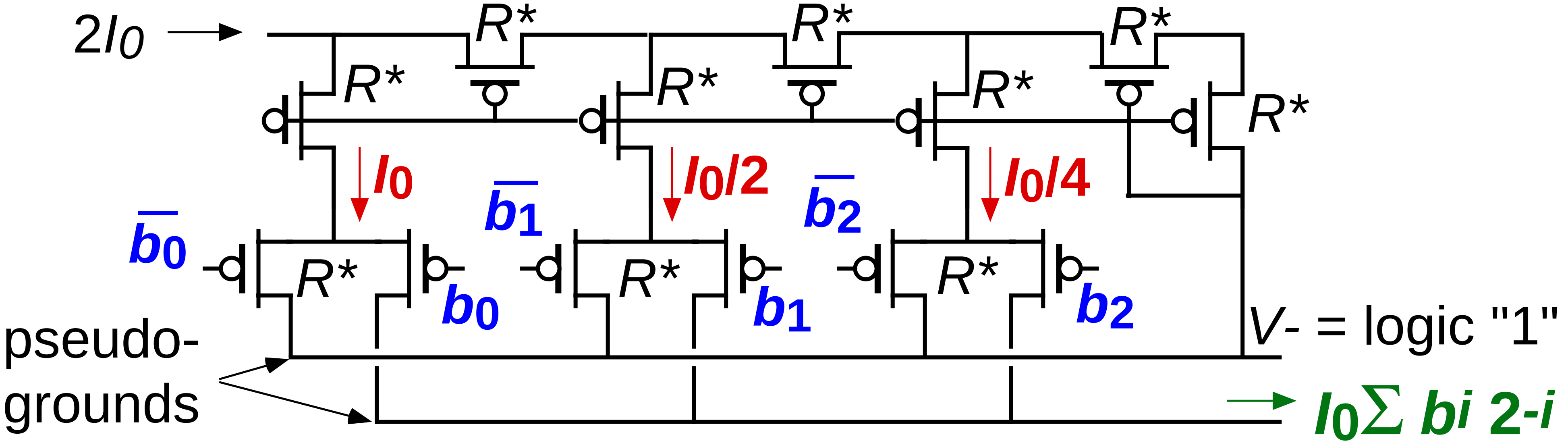
Example of application of pseudo-R:

R-2R D/A CONVERTER [7,8]

- Standard resistive circuit (example for 3-bit):

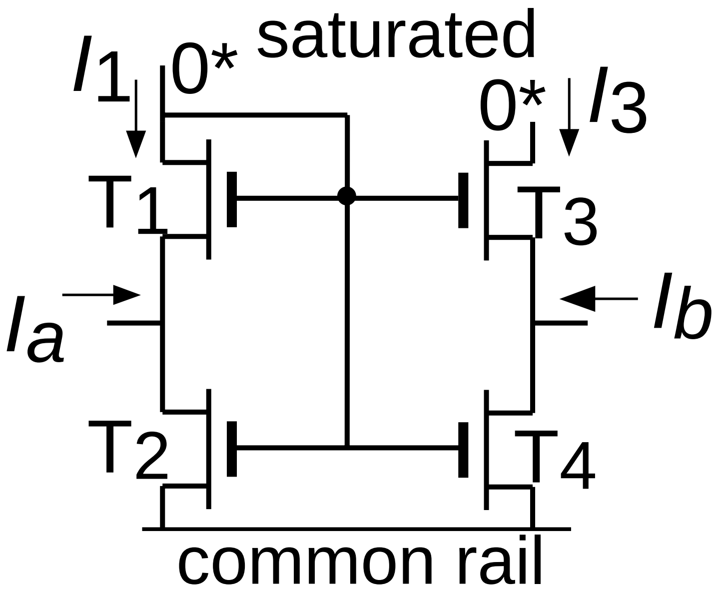


- Pseudo-resistive implementation:

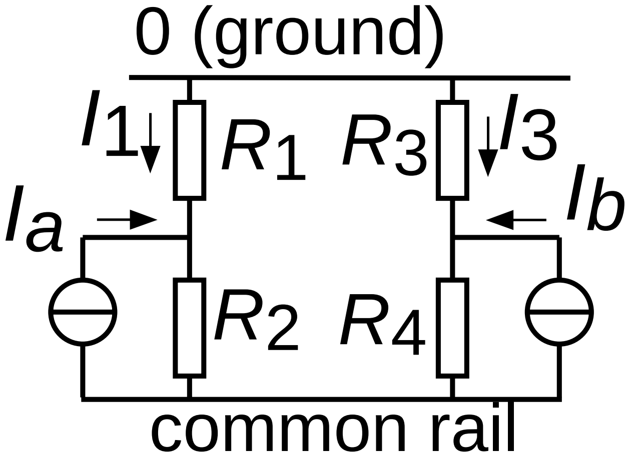


Example of application of pseudo-R:

EXTENDED CURRENT MIRROR



$R_i \sim L_i / W_i$



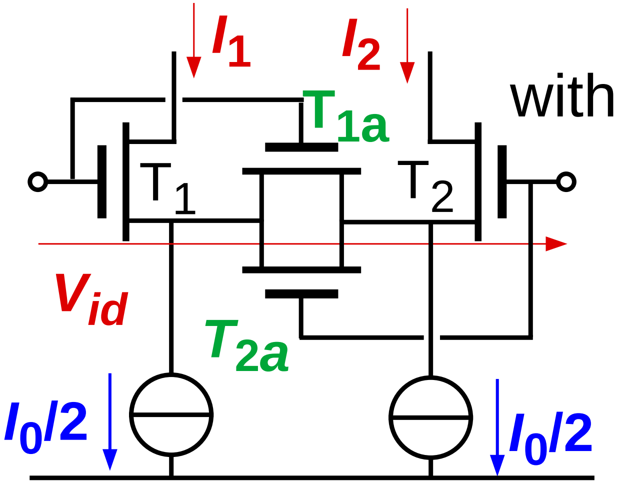
$$(R_3+R_4)I_3+R_4I_b = (R_1+R_2)I_1+R_2I_a$$

thus: $$\boxed{I_3 = k_1I_1 + k_aI_a - k_bI_b}$$

- Output I_3 is the weighted sum of I_1, I_a and $-I_b$.
- I_a and I_b are low-voltage inputs (T_2 , T_4 not saturated)

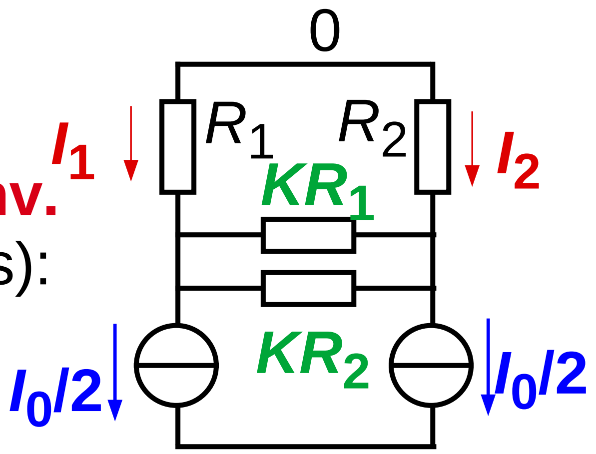
example of pseudo-R in weak inversion:

LINEARIZATION OF DIFFERENTIAL PAIR [9]



with $\frac{\beta_1}{\beta_{1a}} = \frac{\beta_2}{\beta_{2a}} = K$

Equivalent circuit in **weak inv.** (concept of pseudo-resistors):

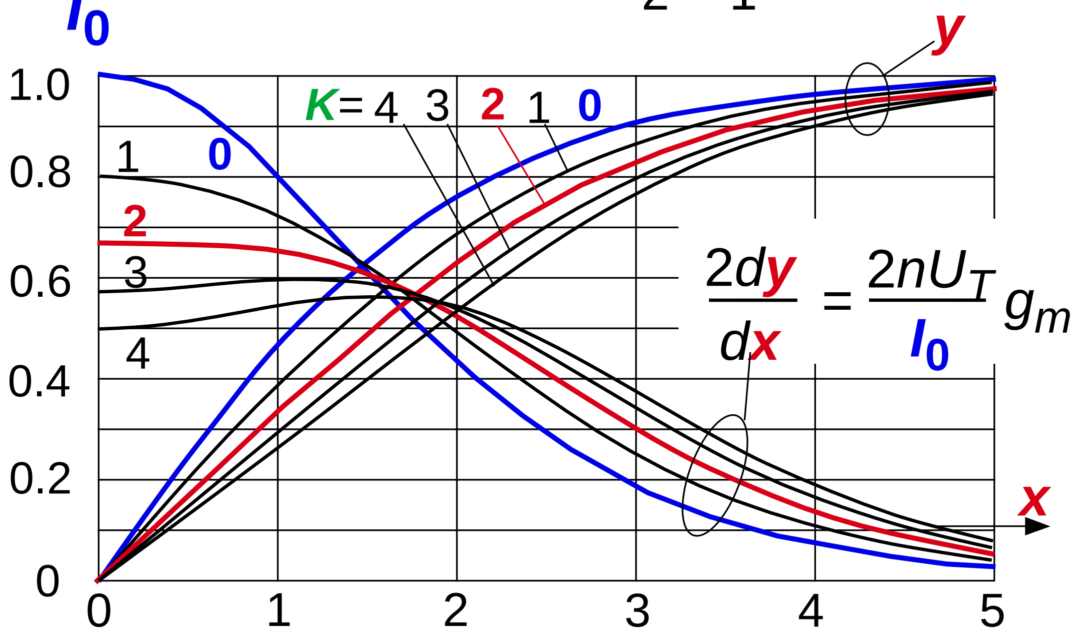


definitions: $x = \frac{V_{id}}{nU_T}$ and $y = \frac{I_1 - I_2}{I_0}$

then: $R_2/R_1 = e^x$

- Results in:

$$\boxed{y = \frac{e^x - 1}{e^x + 1 + K\frac{e^x}{e^x + 1}}}$$

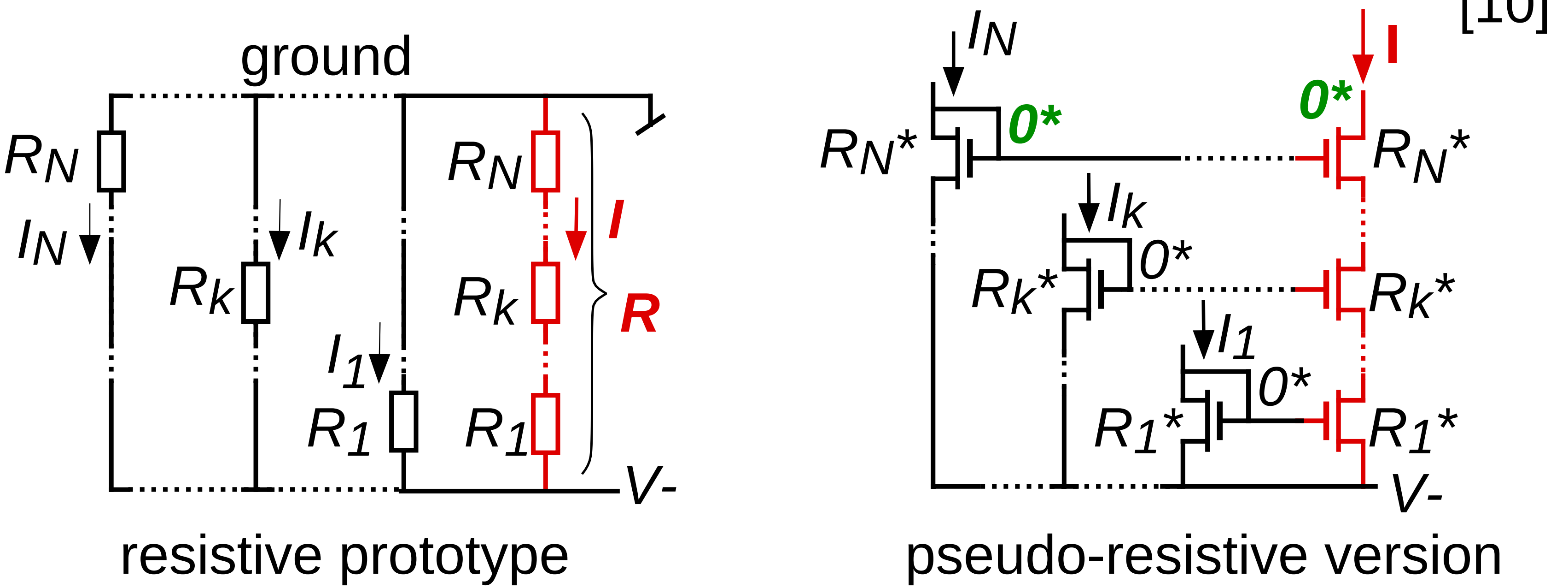


$$\frac{2dy}{dx} = \frac{2nU_T}{I_0} g_m$$

example pseudo-R in weak inversion

HARMONIC MEAN AND FUZZY AND GATE

[10]



resistive prototype

pseudo-resistive version (**0***=pseudo-ground)

- Series combination of R_i: $\mathbf{R} = \sum R_i$
- Same voltage across **R** and R_i, thus $I = \dfrac{1}{\sum 1/I_i} = \dfrac{I_{hm}}{N}$

harmonic mean

- Can be used as a fuzzy logic AND gate.[19,20]

FURTHER APPLICATIONS OF PSEUDO-RESISTORS

- Linear attenuators [5] (electrical control in weak inversion)
- Spatial information processing:
  - n^{th} oder moment computation [11,12,13]
  - diffusion networks (isotropic or not) [14,15]
  - 2-D emulation of physical media [16]
  - path finding [17].
- In weak inversion: exploitation of current distribution in voltage- (or current-) dependent linear networks:
  - local normalisation in vision processing [18]
  - generation of nonlinear functions [19]
  - fuzzy logic processor [20]
  - ...

CONCLUSION

- Basic MOS property for long and homogeneous channels:

$$I_D = \mathrm{I}(V_S, V_G) - \mathrm{I}(V_D, V_G) = I_F - I_R$$

  - superposition of independent and symmetrical effects of S and D voltages.
  - forward and reverse components.
- Underlies first-order EKV transistor model.
- Property progressively degraded when channel shortened.
- Underlies the concept of pseudoresistor:
  - linear current mode circuits
  - transistor implementation of arrays of resistors.
  - simpler analysis of transistor circuits.

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