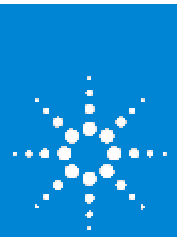
Minh Quach.

Signal Integrity Consideration and Analysis

4/30/2004

Frequency & Time Domain Measurements / Analysis



Agilent Technologies

Outline

- **Three Measurement Methodologies**
  - **Direct**
  - **TDR (Time Domain Reflectometry)**
  - **VNA (Vector Network Analyzer)**

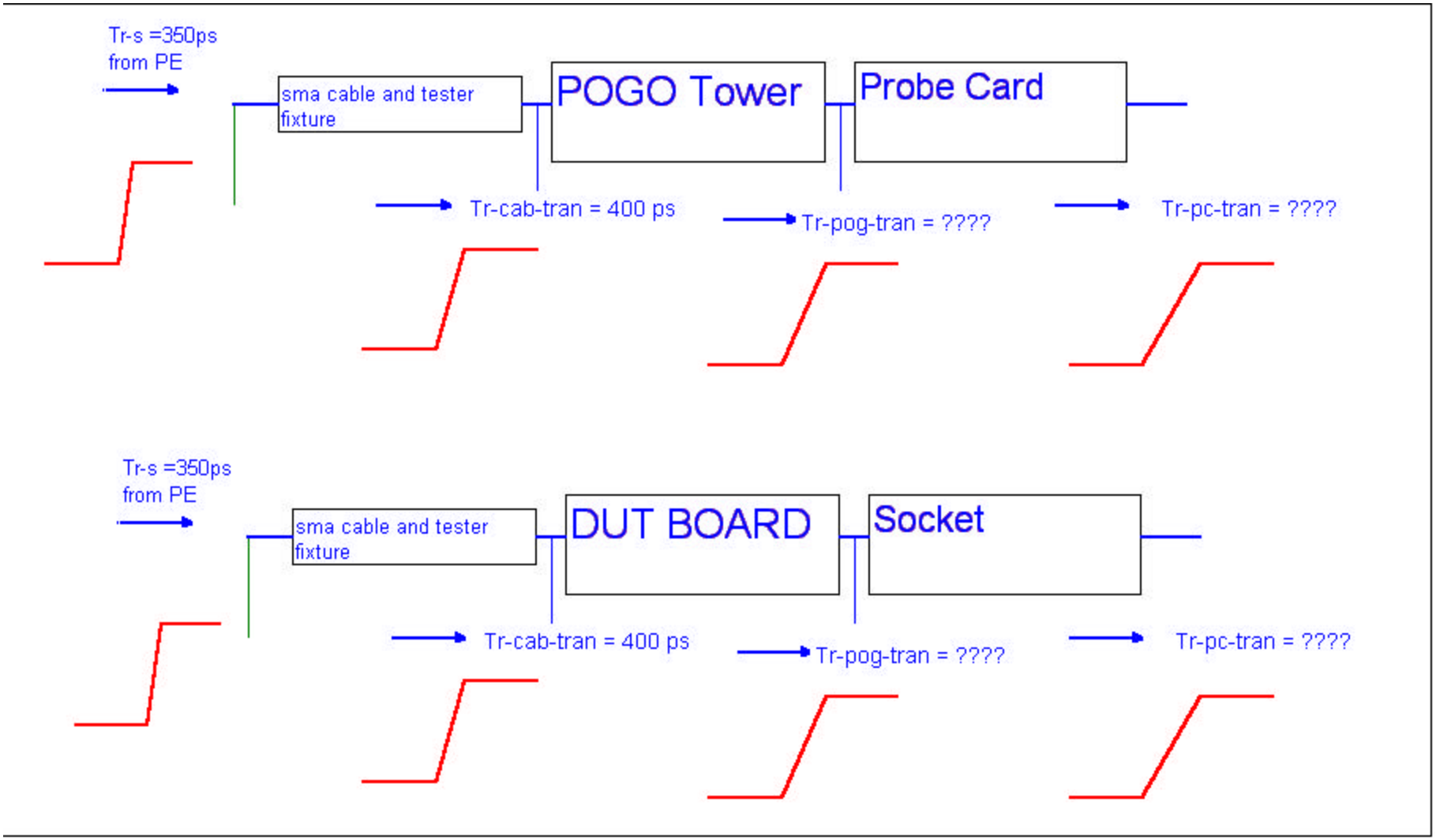
- **Fundamental Transmission line & TDR Theory**
  - **Lossless and lossy line**
  - **Filter Rise Time calculation**
  - **Bandwidth Interpretation**

Outline (Cont)

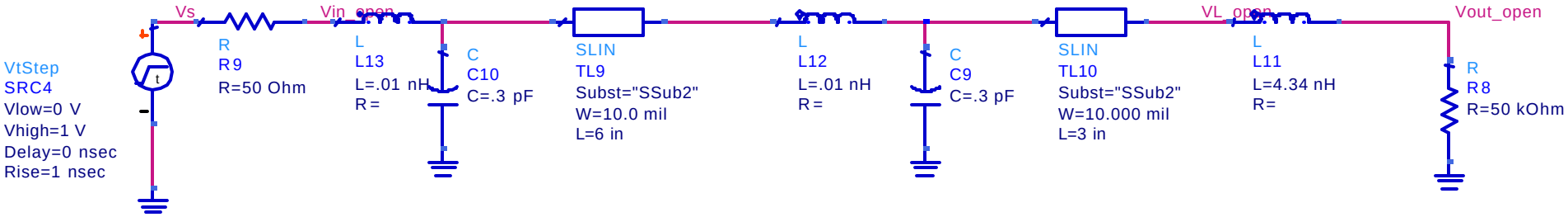
- **Signal Integrity**
  - Ground Bounce
  - Inadequate power bus decoupling
  - Dispersion
  - AC loss (skin effect and dielectric loss)
  - Cross Talk

- **Differential Pair**
  - Common & Differential Mode
  - Even & Odd Mode

Test Environment Hardware



Interconnect



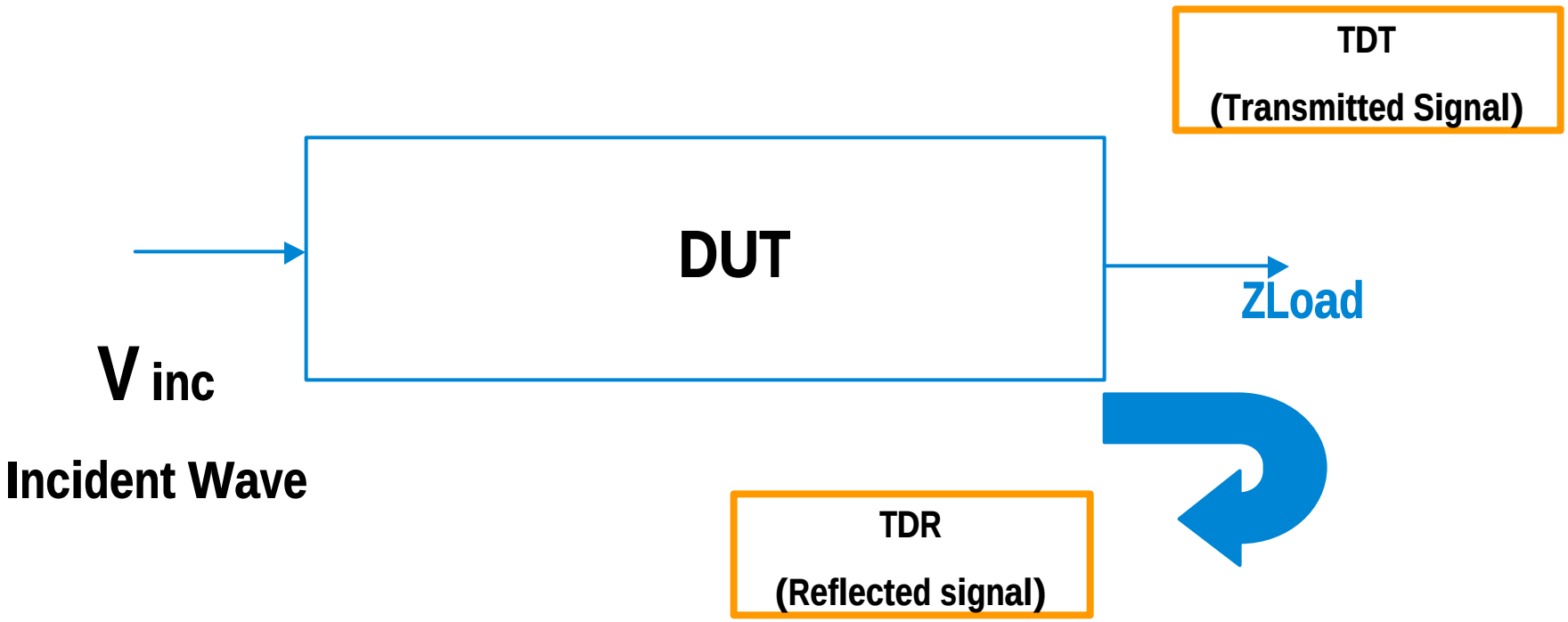
Measurement Methods

- **Direct Measurement**

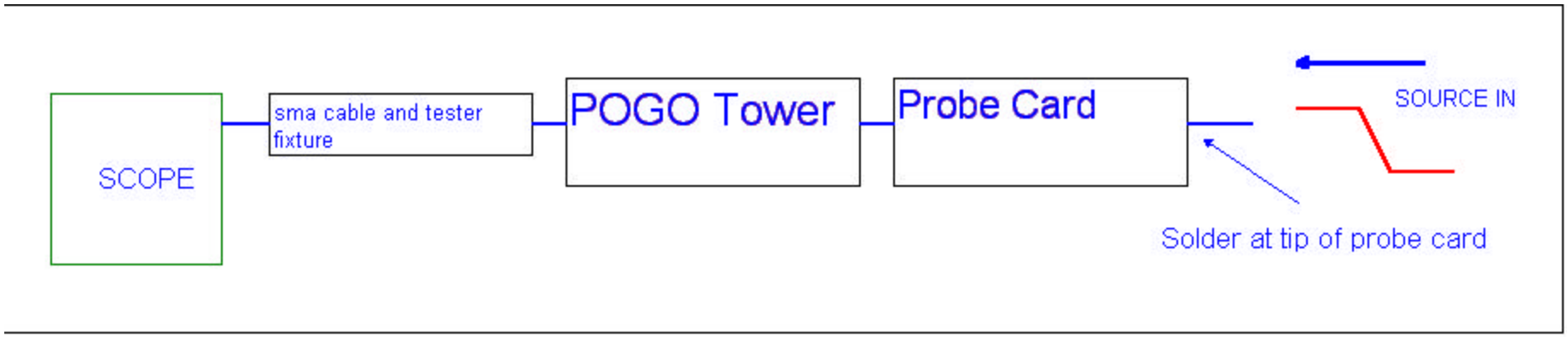
- **TDR (Time Domain Reflectometry, Time Domain)**

- **VNA (Vector Network Analyzer, Frequency Domain)**

Measurement Method



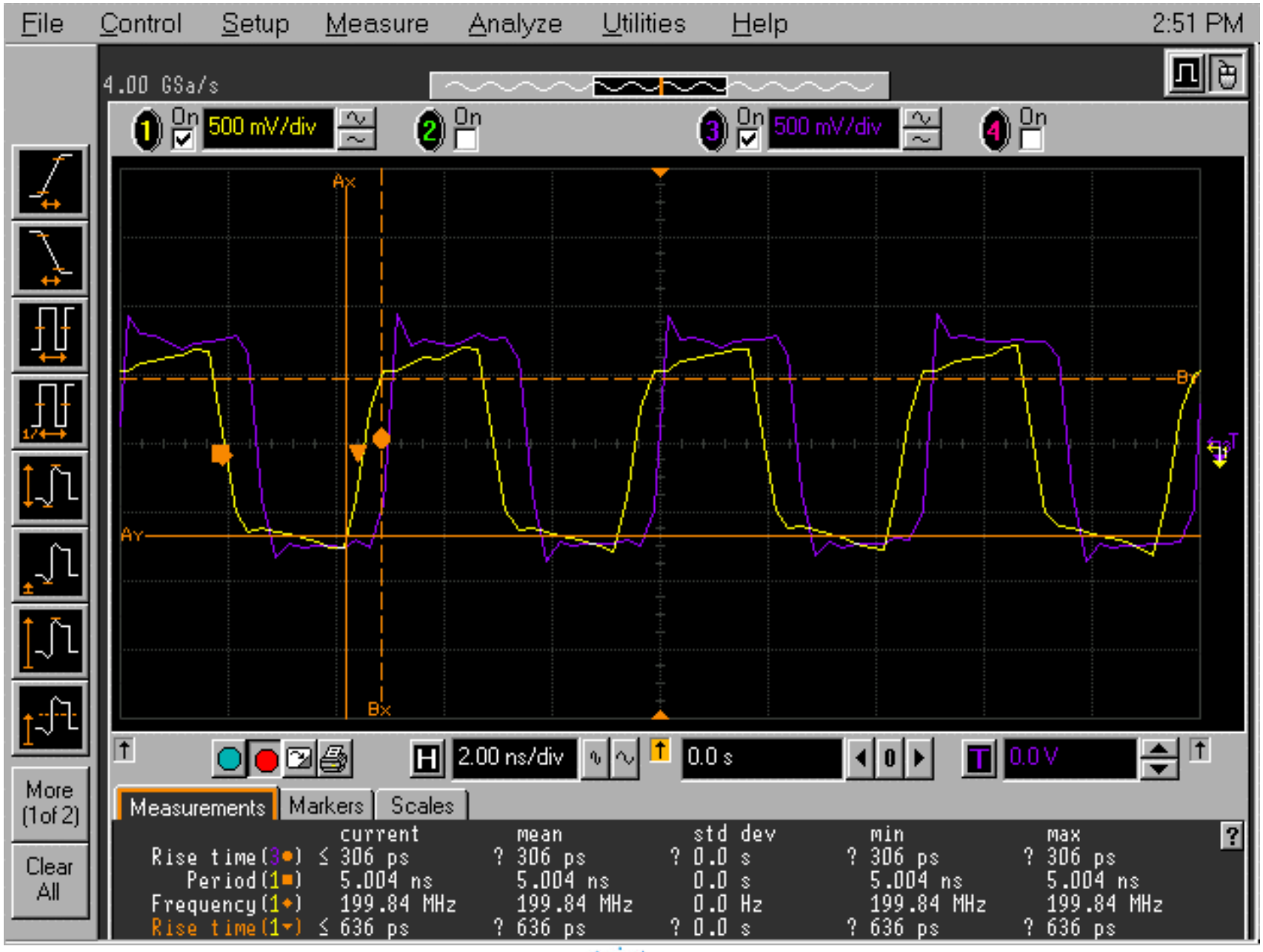
Direct Measurements



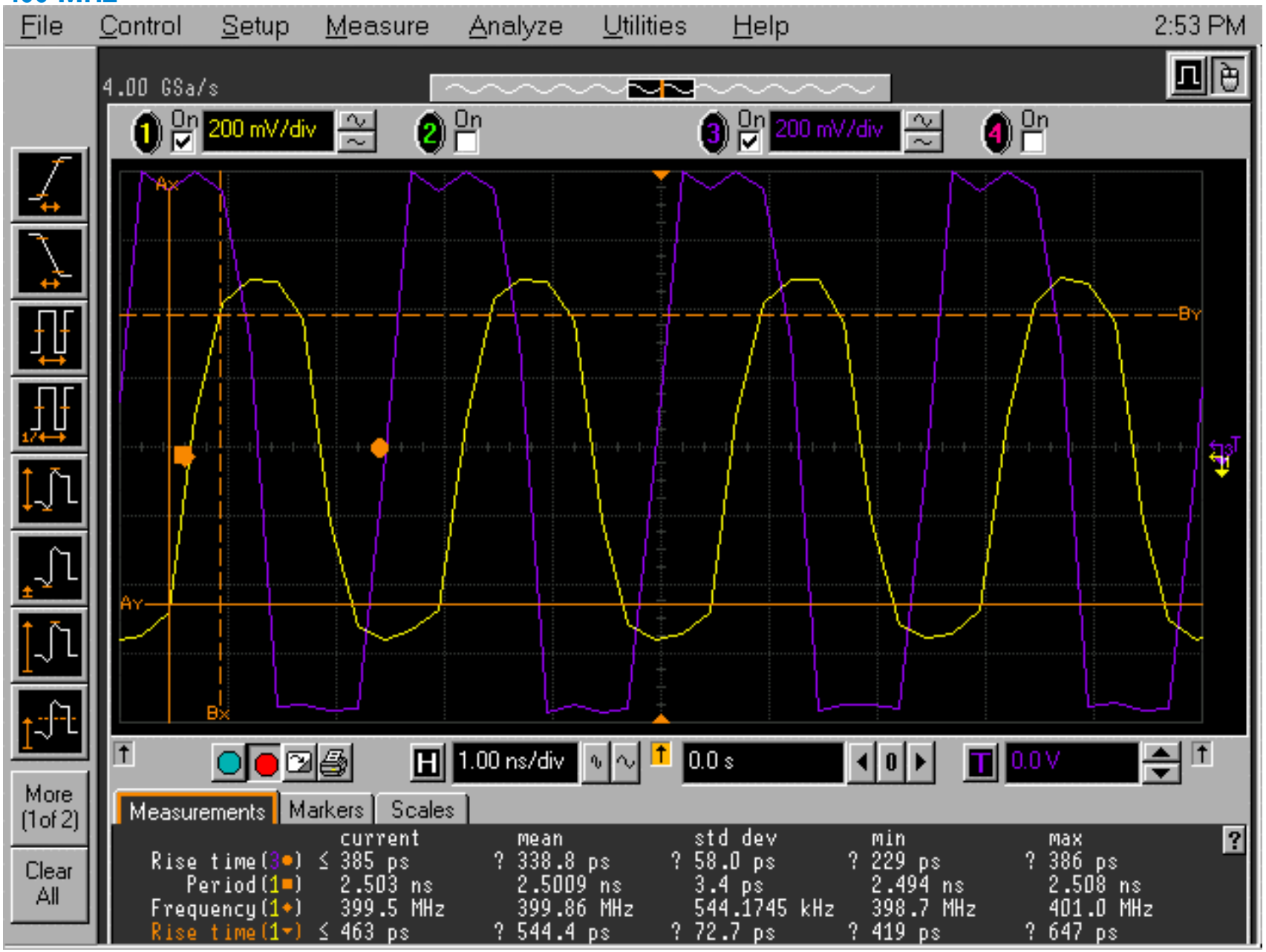
Freq = 100MHZ


File Control Setup Measure Analyze Utilities Help 2:50 PM
4.00 GSa/s
1 On 500 mV/div
2 On
3 On 500 mV/div
4 On
Ax
Bx
Ay
By
2.00 ns/div
0.0 s
0.0 V
More (1 of 2)
Clear All
Measurements
Markers
Scales
current mean std dev min max
Rise time(3) ≤ 372 ps ? 374 ps ? 2 ps ? 372 ps ? 375 ps
Period(1) 9.986 ns 9.986 ns 0.0 s 9.986 ns 9.986 ns
Frequency(1) 100.14 MHz 100.14 MHz 0.0 Hz 100.14 MHz 100.14 MHz
Rise time(1) 1.308 ns 1.308 ns 0.0 s 1.308 ns 1.308 ns

Freq = 200MHZ


File Control Setup Measure Analyze Utilities Help 2:51 PM
4.00 GSa/s
1 On 500 mV/div
2 On
3 On 500 mV/div
4 On
Ax
Ay
Bx
By
2.00 ns/div
0.0 s
0.0 V
More (1 of 2)
Clear All
Measurements
Markers
Scales
current mean std dev min max
Rise time(3) ≤ 306 ps ? 306 ps ? 0.0 s ? 306 ps ? 306 ps
Period(1) 5.004 ns 5.004 ns 0.0 s 5.004 ns 5.004 ns
Frequency(1) 199.84 MHz 199.84 MHz 0.0 Hz 199.84 MHz 199.84 MHz
Rise time(1) ≤ 636 ps ? 636 ps ? 0.0 s ? 636 ps ? 636 ps

Freq =400 MHZ


File Control Setup Measure Analyze Utilities Help 2:53 PM
4.00 GSa/s
1 On 200 mV/div
2 On
3 On 200 mV/div
4 On
Ax
Ay
Bx
By
1.00 ns/div
0.0 s
0.0 V
More (1 of 2)
Clear All
Measurements
Markers
Scales
current mean std dev min max
Rise time(3) ≤ 385 ps ? 338.8 ps ? 58.0 ps ? 229 ps ? 386 ps
Period(1) 2.503 ns 2.5009 ns 3.4 ps 2.494 ns 2.508 ns
Frequency(1) 399.5 MHz 399.86 MHz 544.1745 kHz 398.7 MHz 401.0 MHz
Rise time(1) ≤ 463 ps ? 544.4 ps ? 72.7 ps ? 419 ps ? 647 ps

Fundamental Differences Between Analog and Digital in Interconnect Applications

Analog

-- Impedance Matching
for max power transfer

-- Frequency Domain

-- VNA

-- Amplitude loss

-- Frequency

Digital

-- Impedance Matching
to minimize signal distortion

-- Time Domain

-- TDR

-- Edge timing degradation

-- Edge rate and frequency

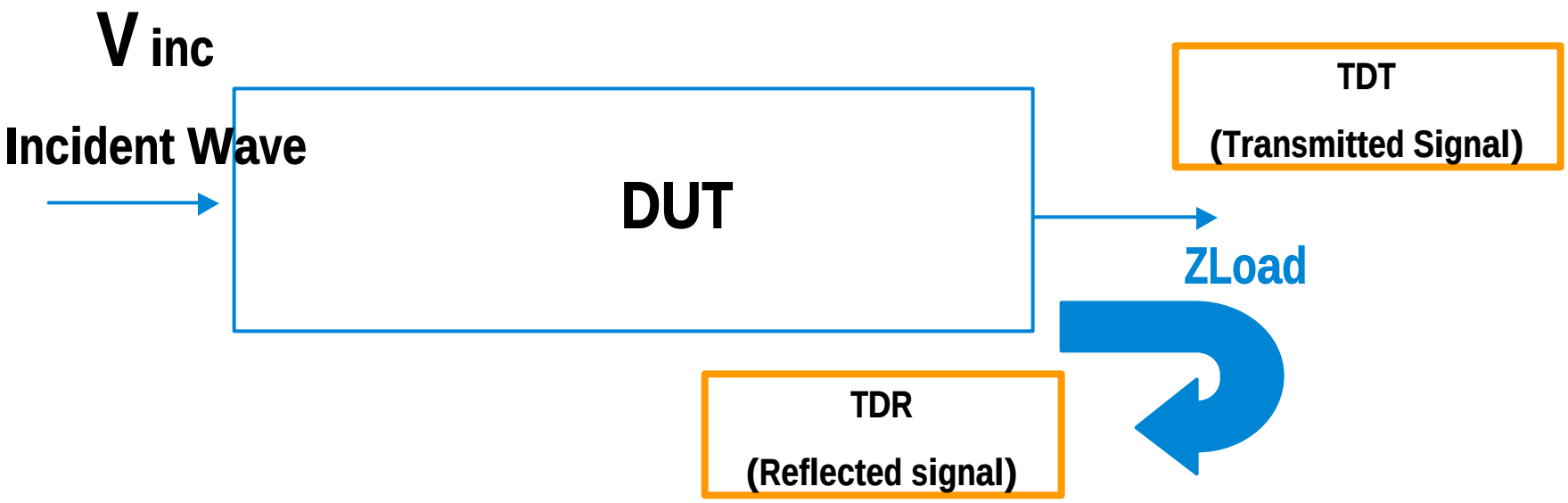
Using the Reflected Waveform to Construct the Spice Model

- **Direct Measurement**

- **TDR (Time Domain Reflectometry, Time Domain) Using the Reflected Waveform to construct the spice model**
  - **Using ADS (Advanced Design Software)**
    - **Transmission Line Theory**

- **VNA (Vector Network Analyzer, Frequency Domain)**

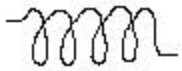
Lump or Distributed



LUMPED

C — A CAPACITOR? - SOMETIMES

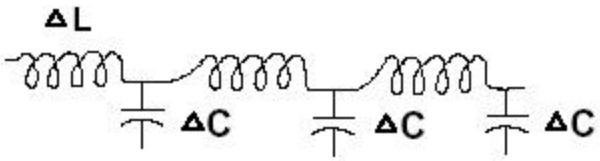
L — AN INDUCTOR? - SOMETIMES



V, I RELATIONSHIPS:

$$V = L\frac{\Delta i}{\Delta t} \qquad i = C\frac{\Delta v}{\Delta t}$$

DISTRIBUTED

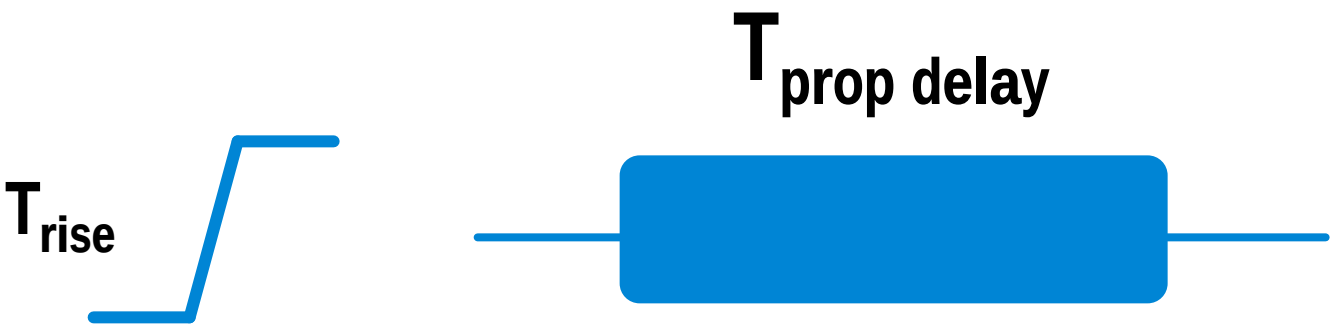


V, I RELATIONSHIPS:

$$\frac{V_I}{I_I} = \sqrt{\frac{\Delta L}{\Delta C}} = Z_O$$

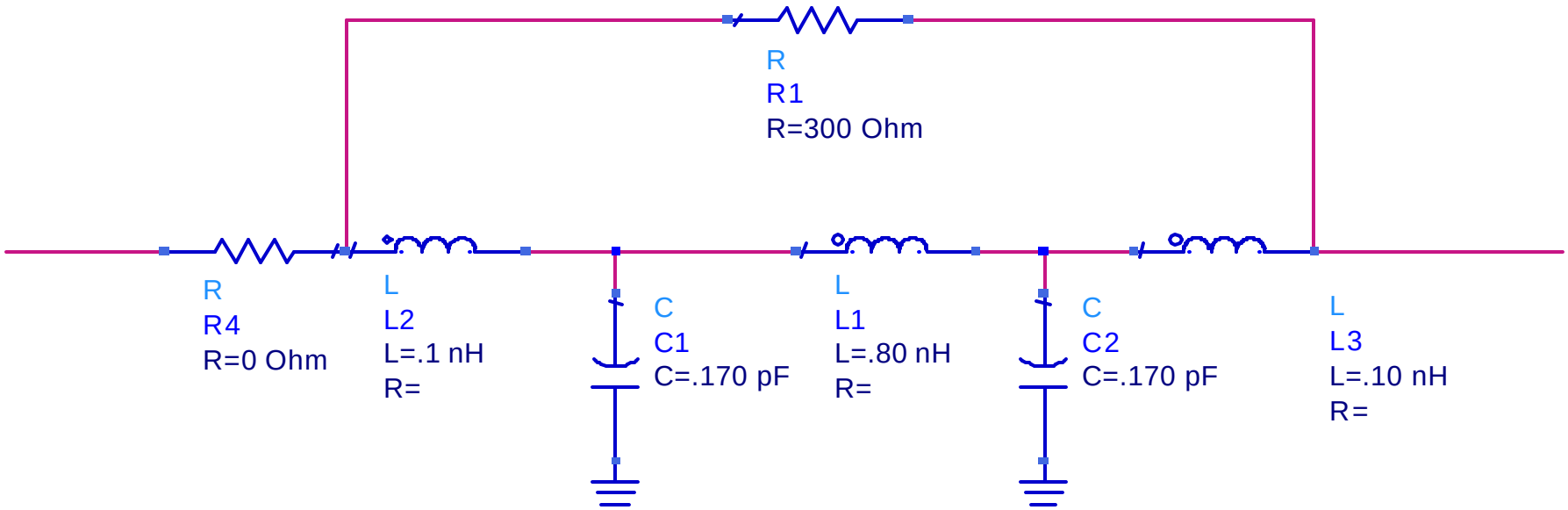
$$V_{TOTAL} = V_I + \sum (V_{RR} + V_{RI})$$

Lump or Distributed



Lump Parameter if: $T_{rise} > T_{prop\ delay} * 6$

High Frequency Socket Model in Lump Parameters Valid up to 7GHz



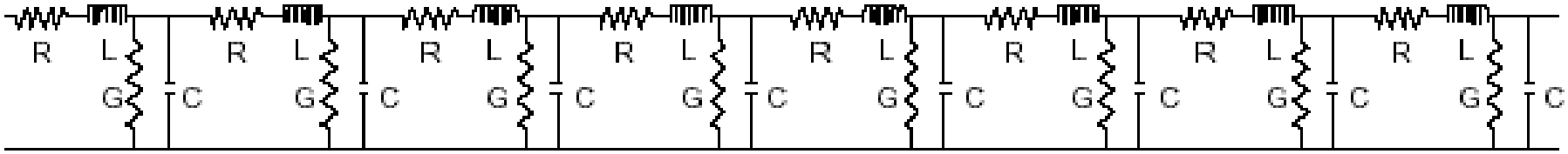
What is a transmission line

- A transmission line is any pair of conductor that are used to move electromagnetic energy from one place to another.
- In printed circuit boards, this is typically a trace and one or more power planes.
- Power lines are transmission lines.
- Coaxial cable is a transmission lines.
- Twisted pairs are transmission lines.

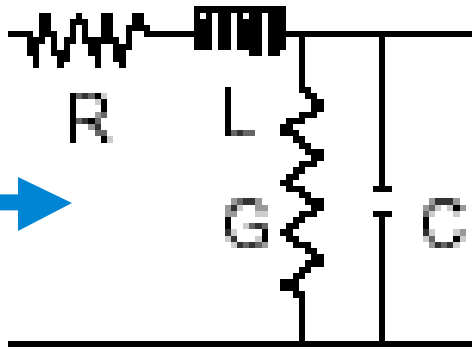
- Electromagnetic waves are moving in a transmission line not electron

Characteristic Impedance Zo

Zo → Transmission line



Zo →



V = (R+jWL)I ✍ Short circuit

I = (G+jWC)V ✍ Open circuit

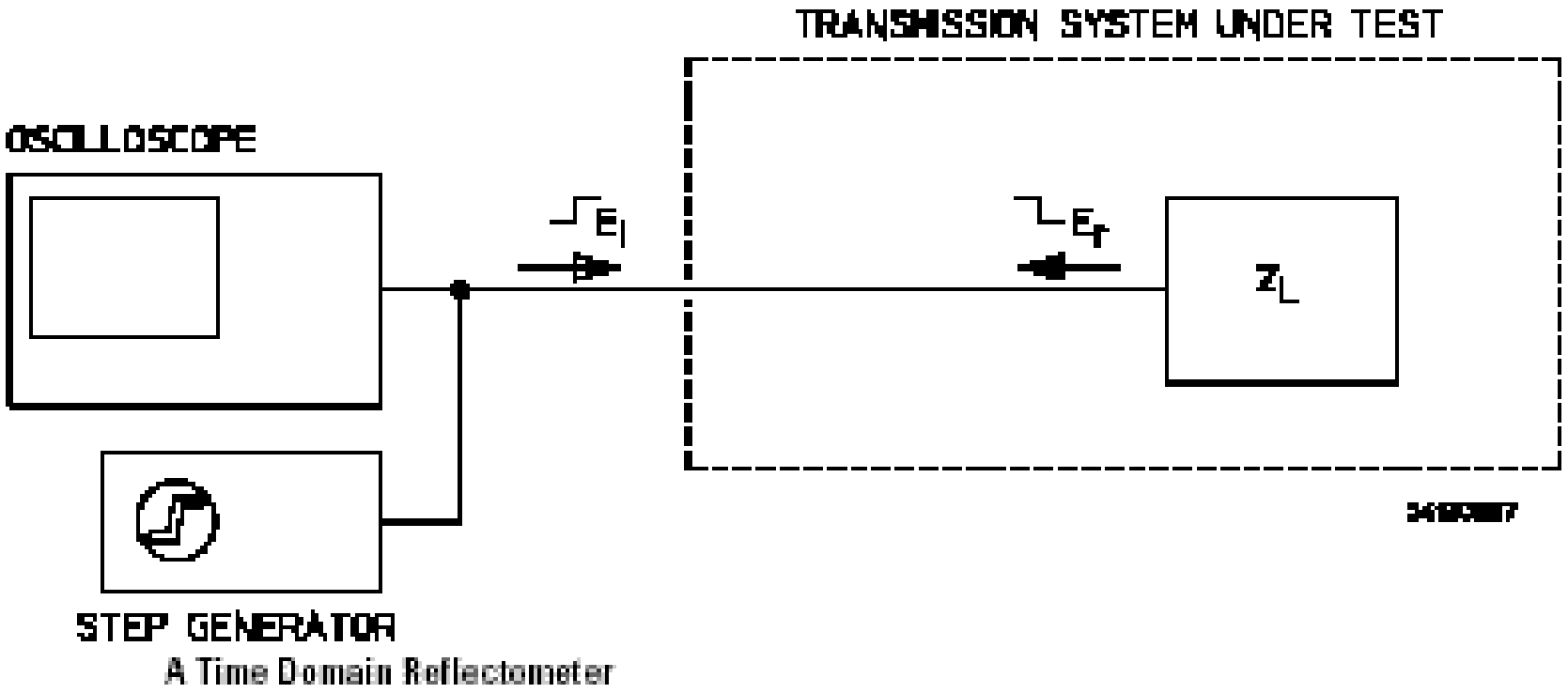
$$Zo = \sqrt{\frac{(R+jWL)}{(G+jWC)}}$$

For Low Loss →

$$\sqrt{\frac{L}{C}}$$

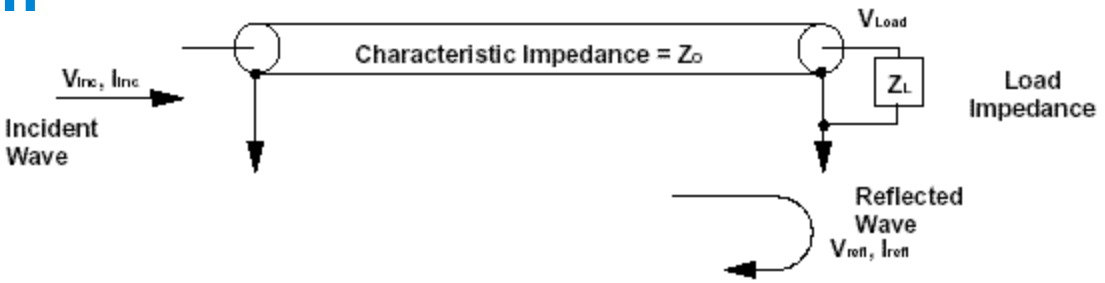
Transmission Line Fundamental Software

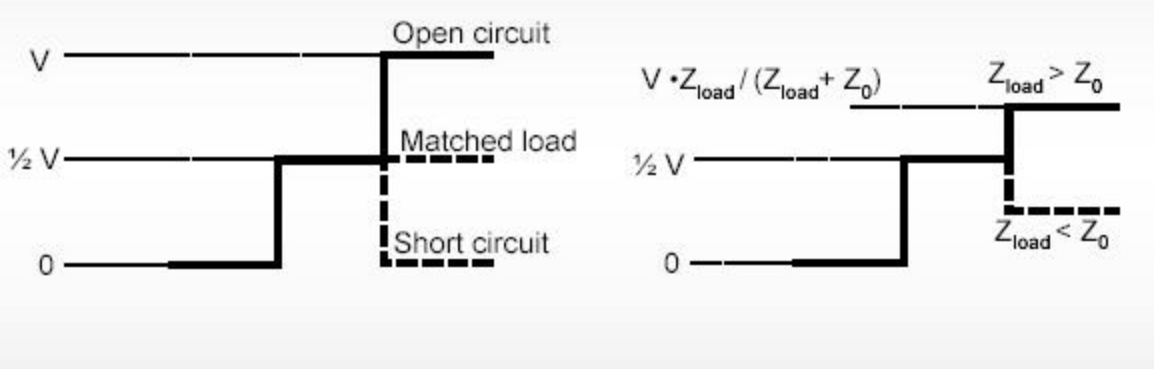
Time Domain Reflectometry (TDR)



A Time Domain Reflectometer

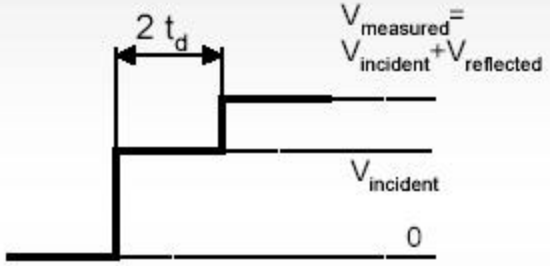
Transmission Line Basic





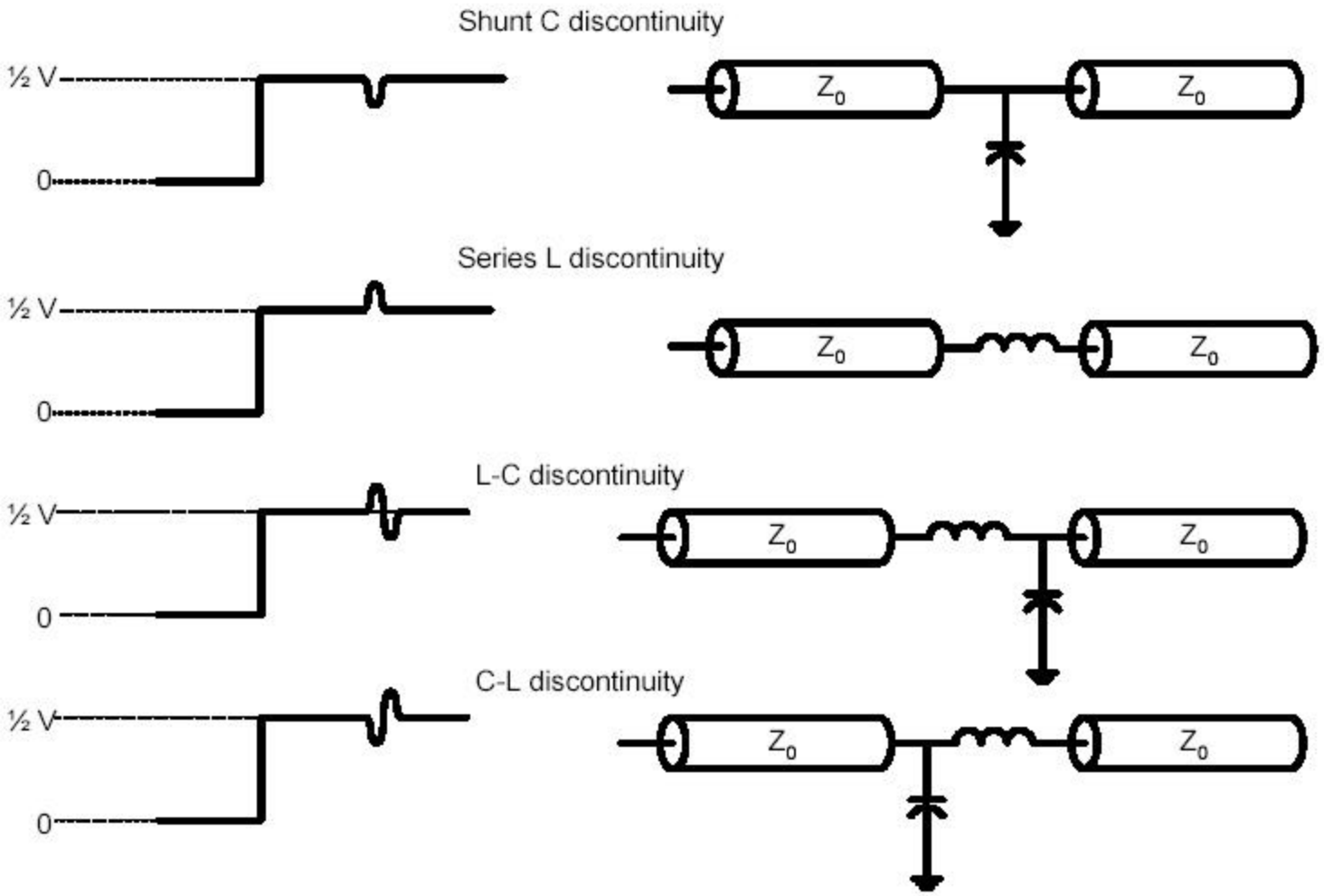
$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{load} - Z_0}{Z_{load} + Z_0}$$

$$V_{reflected} = V_{incident} * \rho$$

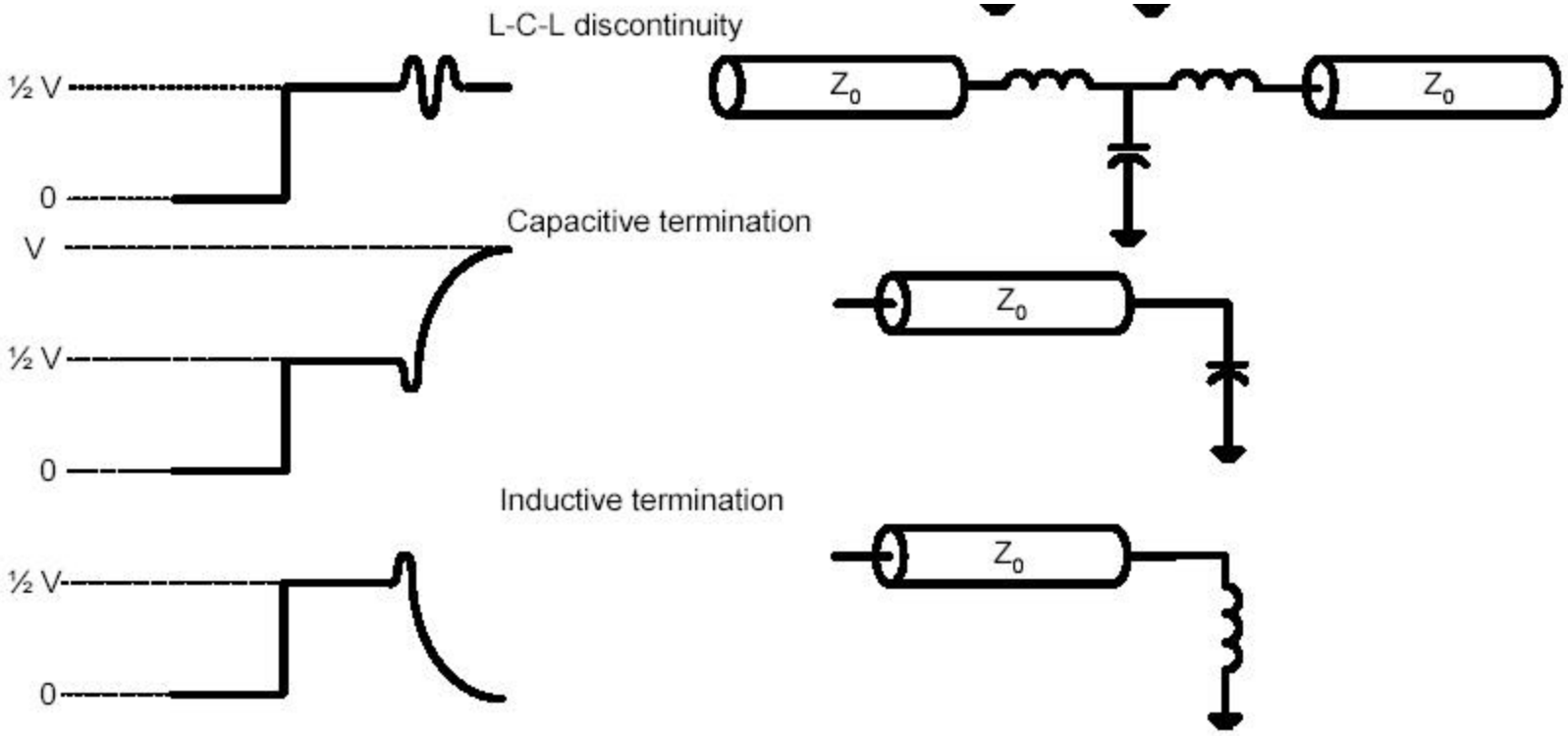


$$Z_{DUT} = Z_0 \cdot \frac{1+\rho}{1-\rho} = Z_0 \cdot \frac{V_{incident} + V_{reflected}}{V_{incident} - V_{reflected}} = Z_0 \cdot \frac{V_{measured}}{2 \cdot V_{incident} - V_{measured}}$$

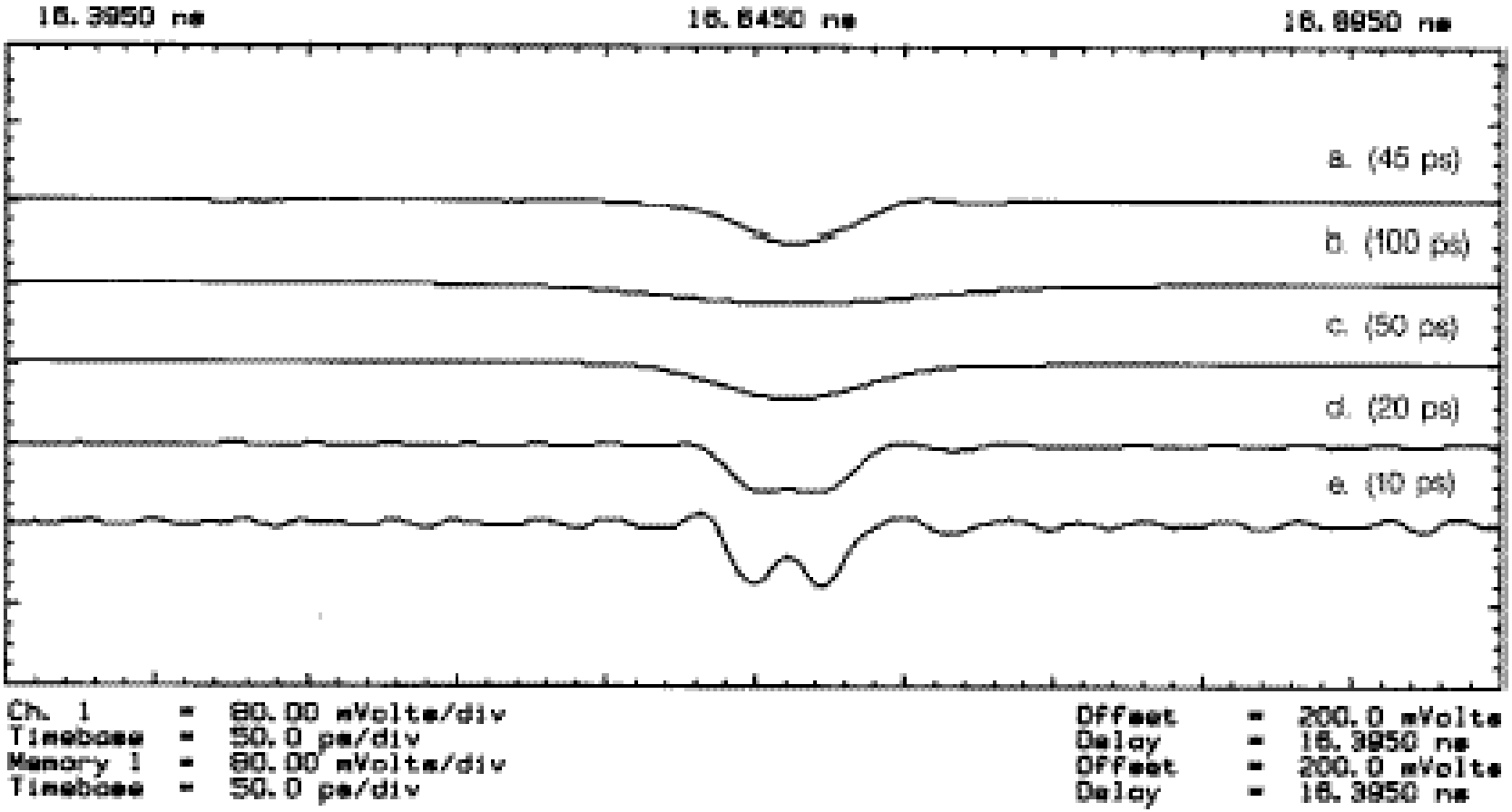
Discontinuity Examples



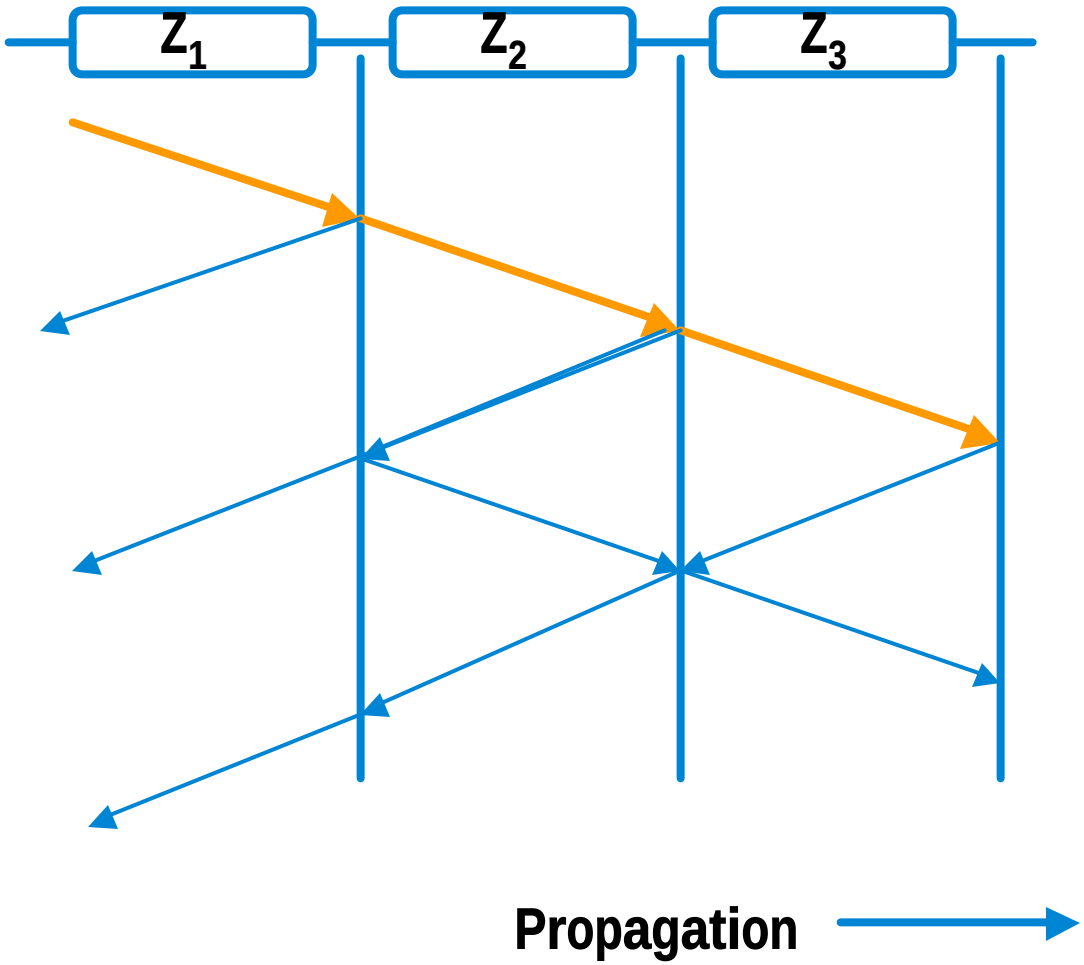
Discontinuity Examples



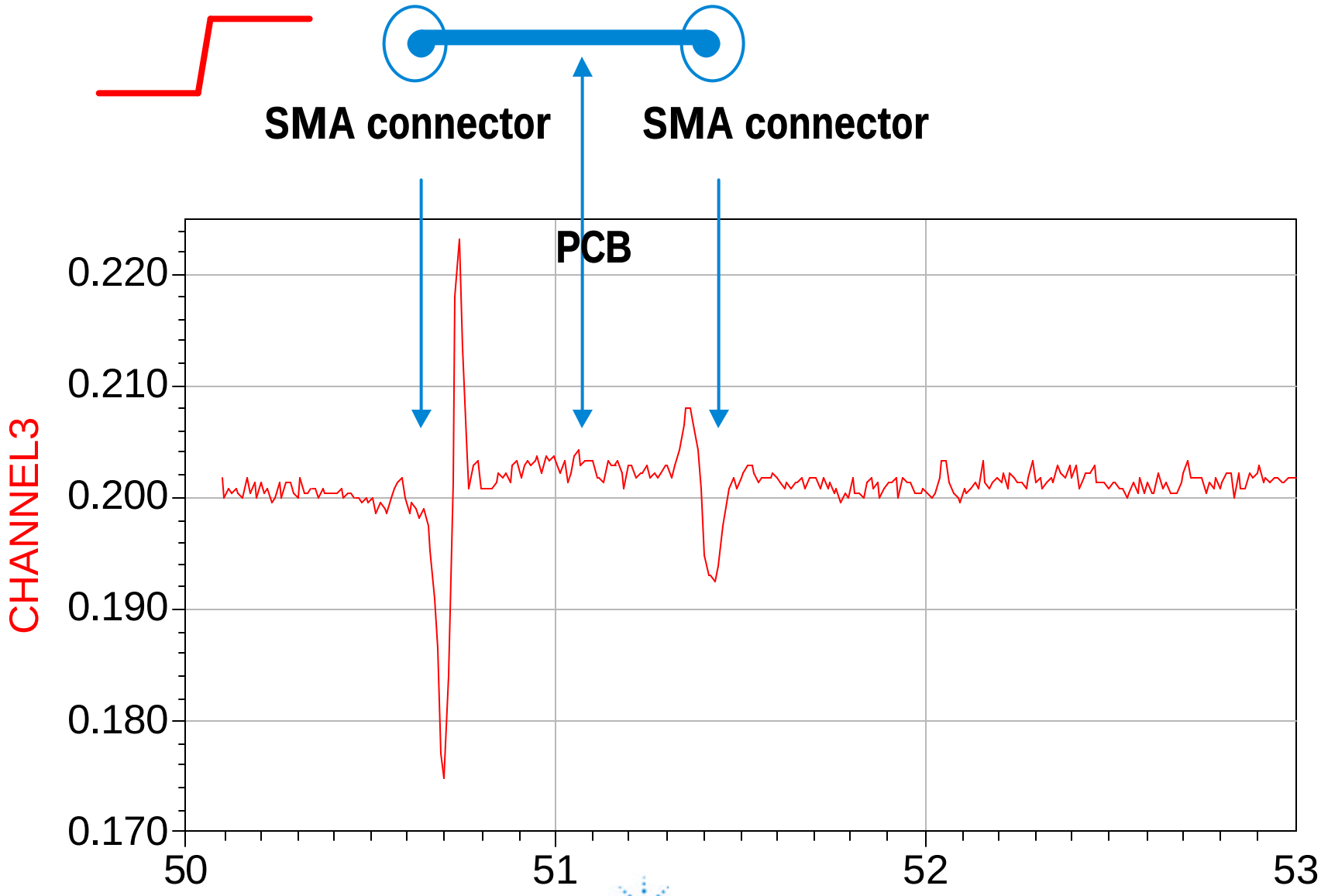
Reflection Response is a function of System Rise Time



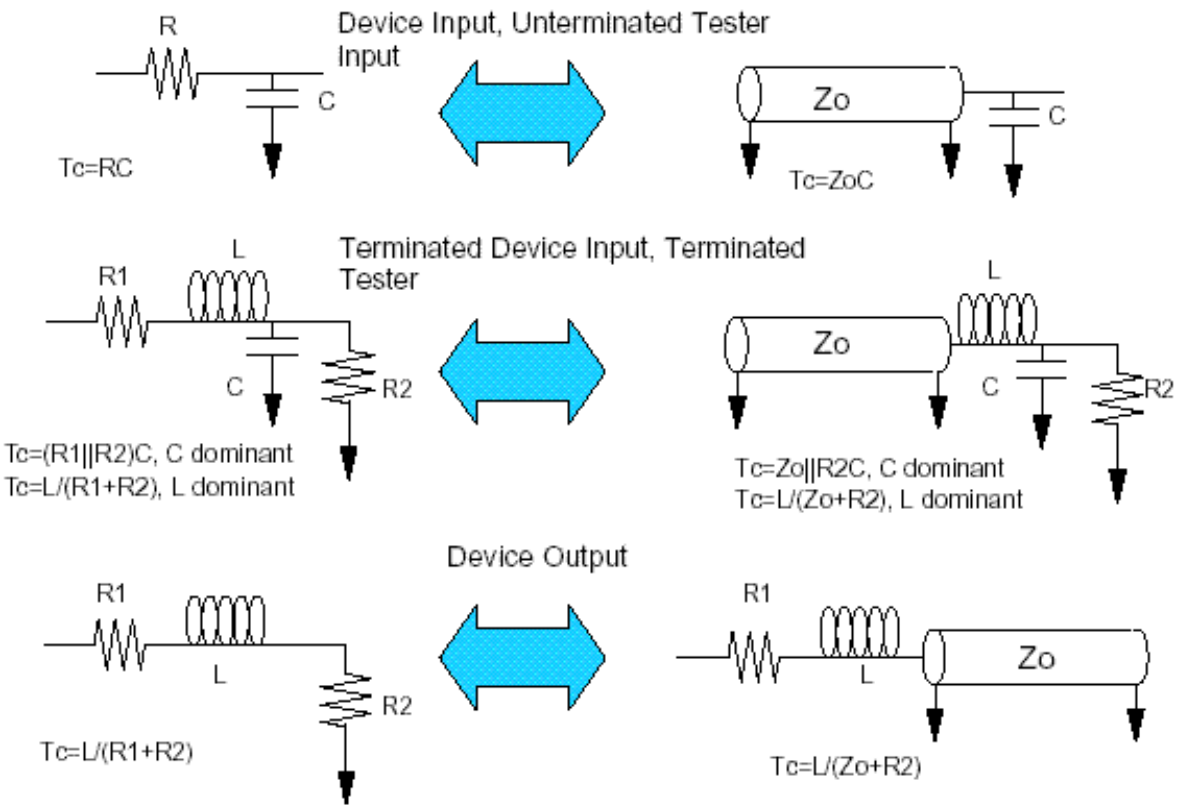
Impedance Profile



TDR responses different due to lossy line



Filter Rise Time Calculation



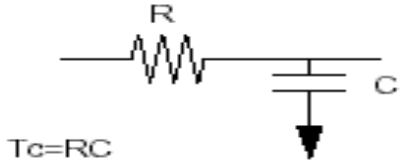
$T_{risetime} = 2.2\ Tc = 2.2\ RC$ **Rise time of RC filter**

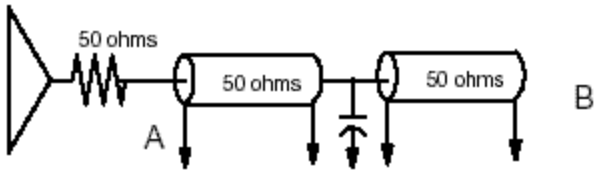
$T_{risetime} = 2.2\ Tc = 2.2\ L/R$ **Rise time of RL filter**

$T_{risetime} = 3.4(LC)^{\wedge 1/2}$ **Rise time of LC filter**

Filter Rise Time Calculation (cont)

C = 0.5pF R=50





Tr in = 400ps

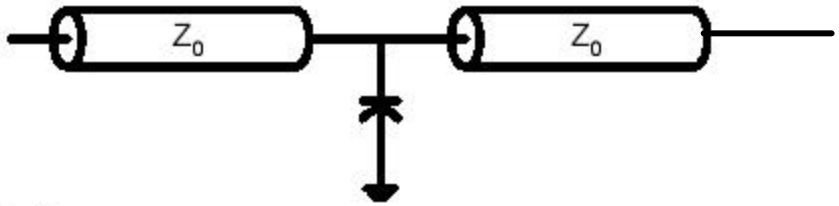
Tr filter =2.2 X 50 X .5 pf = 55pS

Tr filter =2.2 X 25 X .5 pf = 27.5pS

$$T_{rise\ composite} = (Tr_{in}^{\wedge 2} + Tr_{filter}^{\wedge 2})^{\wedge 1/2}$$

$$T_{rise\ composite} = 403.8\ pS$$

$$T_{rise\ composite} = 400.9pS$$



$T_{risetime} = 2.2\ Tc = 2.2\ RC$

$R = Zo / 2$

$T_{risetime} = 2.2\ Tc = 2.2\ L / R$

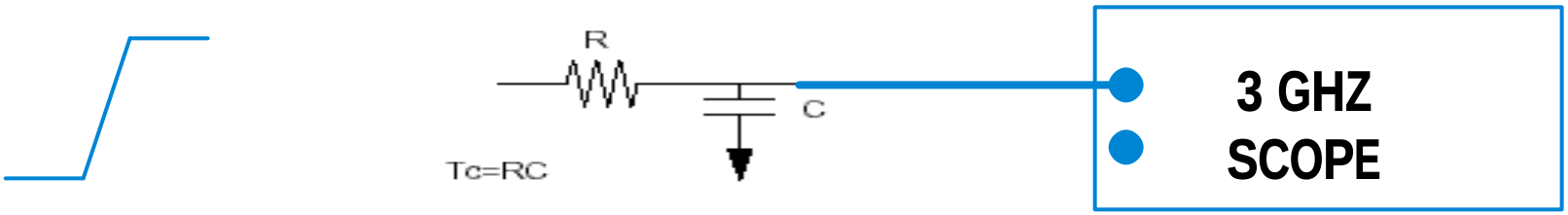
$R = 2 * Zo$

Filter Rise Time Calculation (cont)

Note:Tr=k/BW3db

Where: K from 0.338 to 0.35 for gaussian pulse and single pole exponential decay respectively

C = 0.5pF R=50



Tr in = 400ps

Tr filter =2.2 X 50 X .5 pf = 55pS

Tr scope = 0.361/Frms
= 120ps

$T_{rise\ composite} = (Tr_{in}^{\wedge 2} + Tr_{filter}^{\wedge 2})^{\wedge 1/2}$

$T_{rise\ composite}$ = 403.8 pS ✍ Output of filter

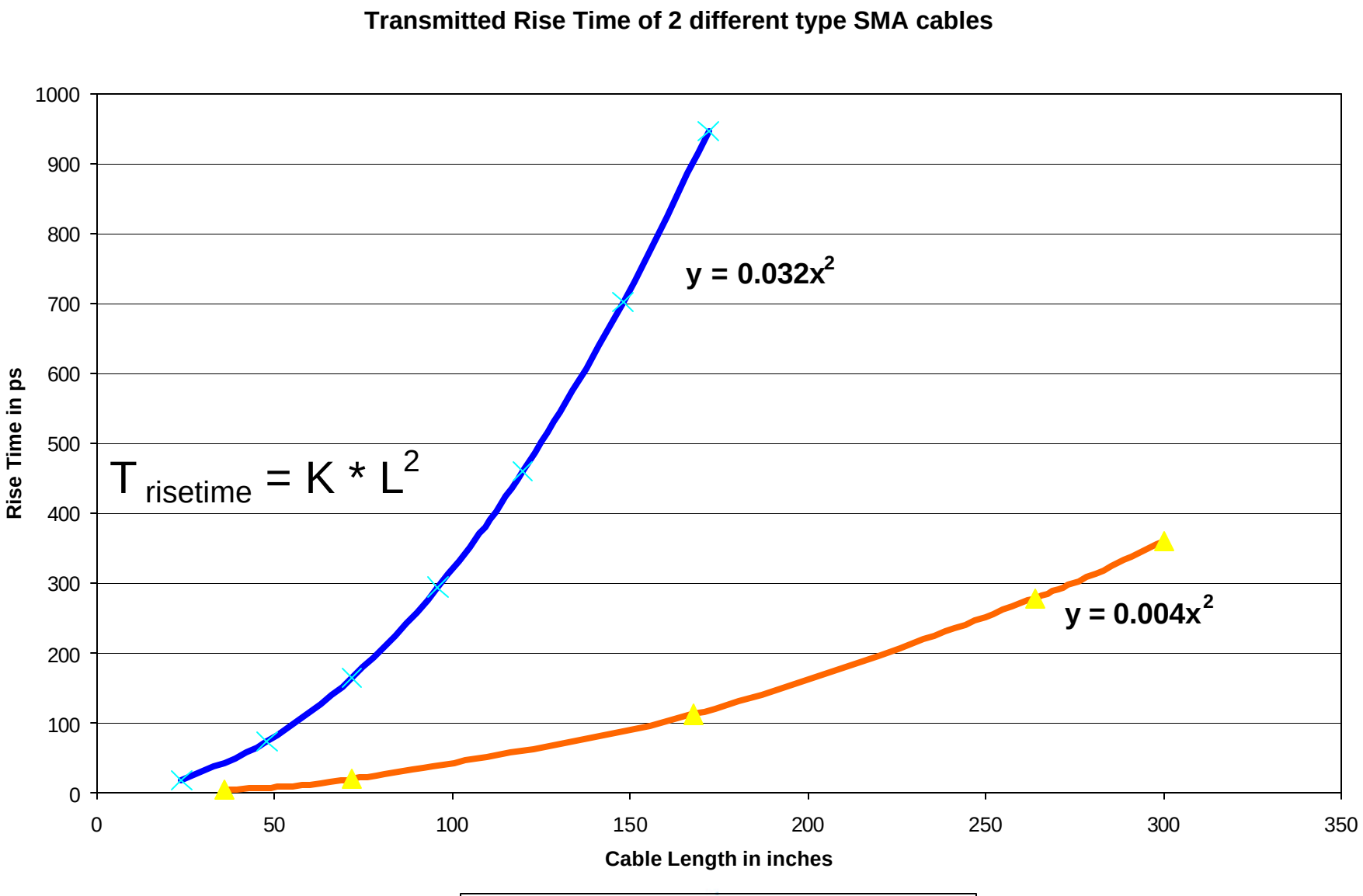
Note:Tr=k/BWrms

Where: K from 0.36 to 0.549 for gaussian pulse and single pole exponential decay respectively

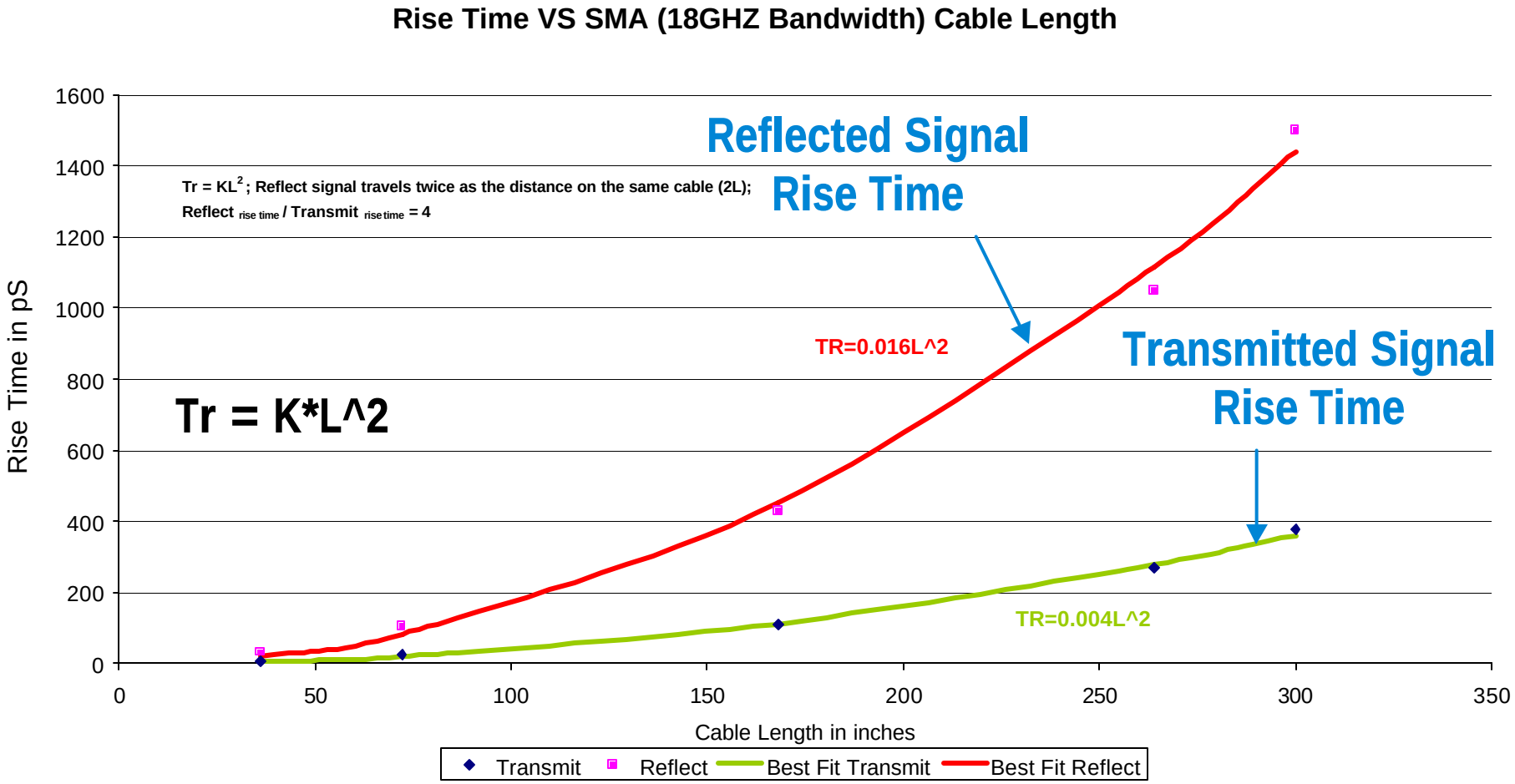
$T_{rise\ composite} = (Tr_{in}^{\wedge 2} + Tr_{filter}^{\wedge 2} + Tr_{scope}^{\wedge 2})^{\wedge 1/2}$

$T_{rise\ composite}$ = 421 pS ✍ Scope Display

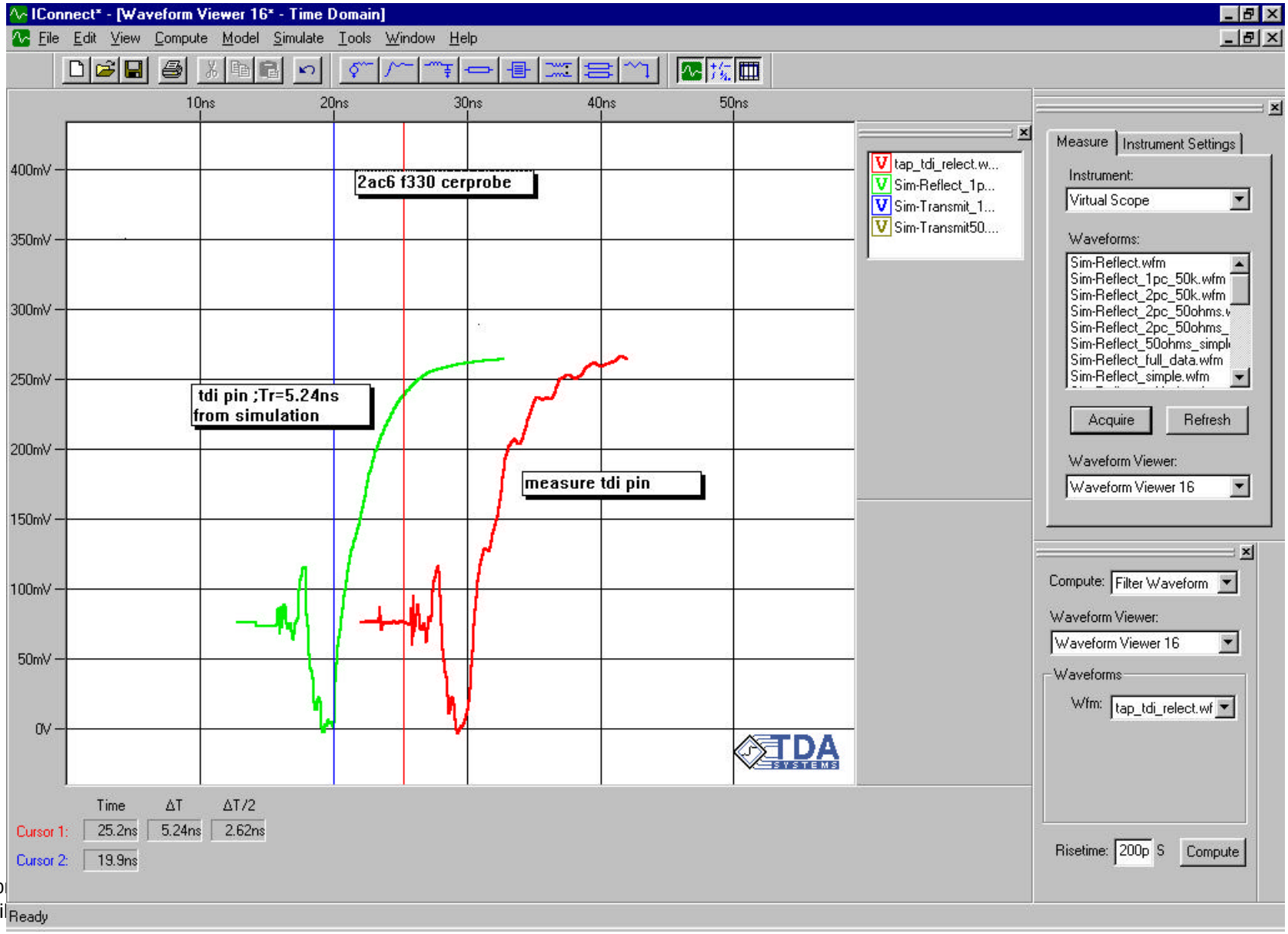
Transmitted Rise Time of 2 different type of SMA cables



Cable Length VS Rise Time of high BW sma cable. Using Reflected Signal to Predict Transmitted Signal



TDR indicates a large Capacitor presents at the load causing rise time to degrade to 5ns



Q / A

When Speed or Wire/Net length are important

- The edge rate (rise or fall time) of a signal is fast enough that the signal can change from one logic state to the other less time than it takes the signal to travel the length of the wire/net.

- Example: Rise time = 1ns, pcb trace length = 6 inch.

  v = 6 inch/ns.

- Overshoot and undershoot begins to show at ¼ of this length

  (1.5 inch).

When should impedance be controlled

- When the length of the transmission line exceeds ¼ of the transition electrical length (TEL = Tr X Velocity)
- Tr= 1ns, Velocity = 6 inch / ns; TEL = 6 “

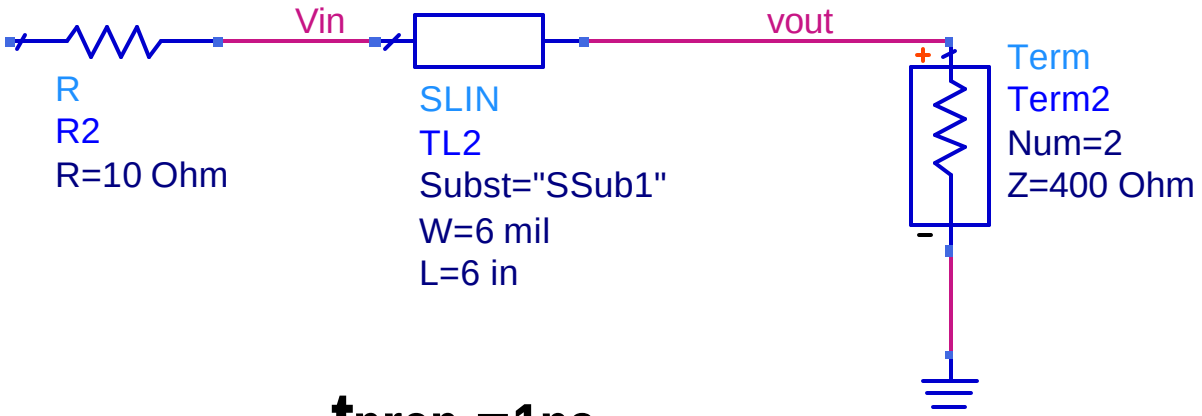
And

- When reflections may cause malfunction from:
  - Overshoot or undershoot and
  - The logic technology support termination

Reflection causes by un-proper termination with fast rise time

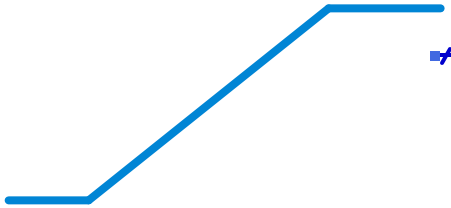
Rise time=0.5ns

Period=10ns



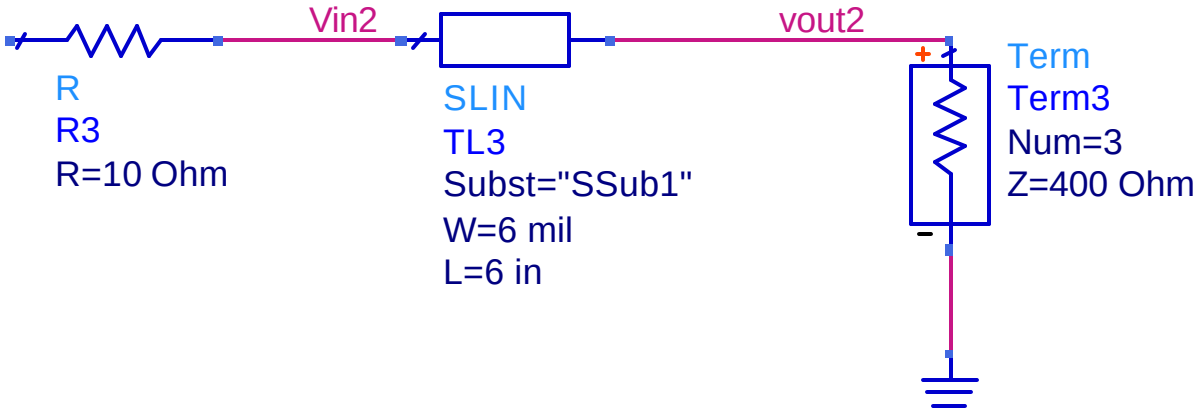
tprop =1ns

(6” FR4 PCB)

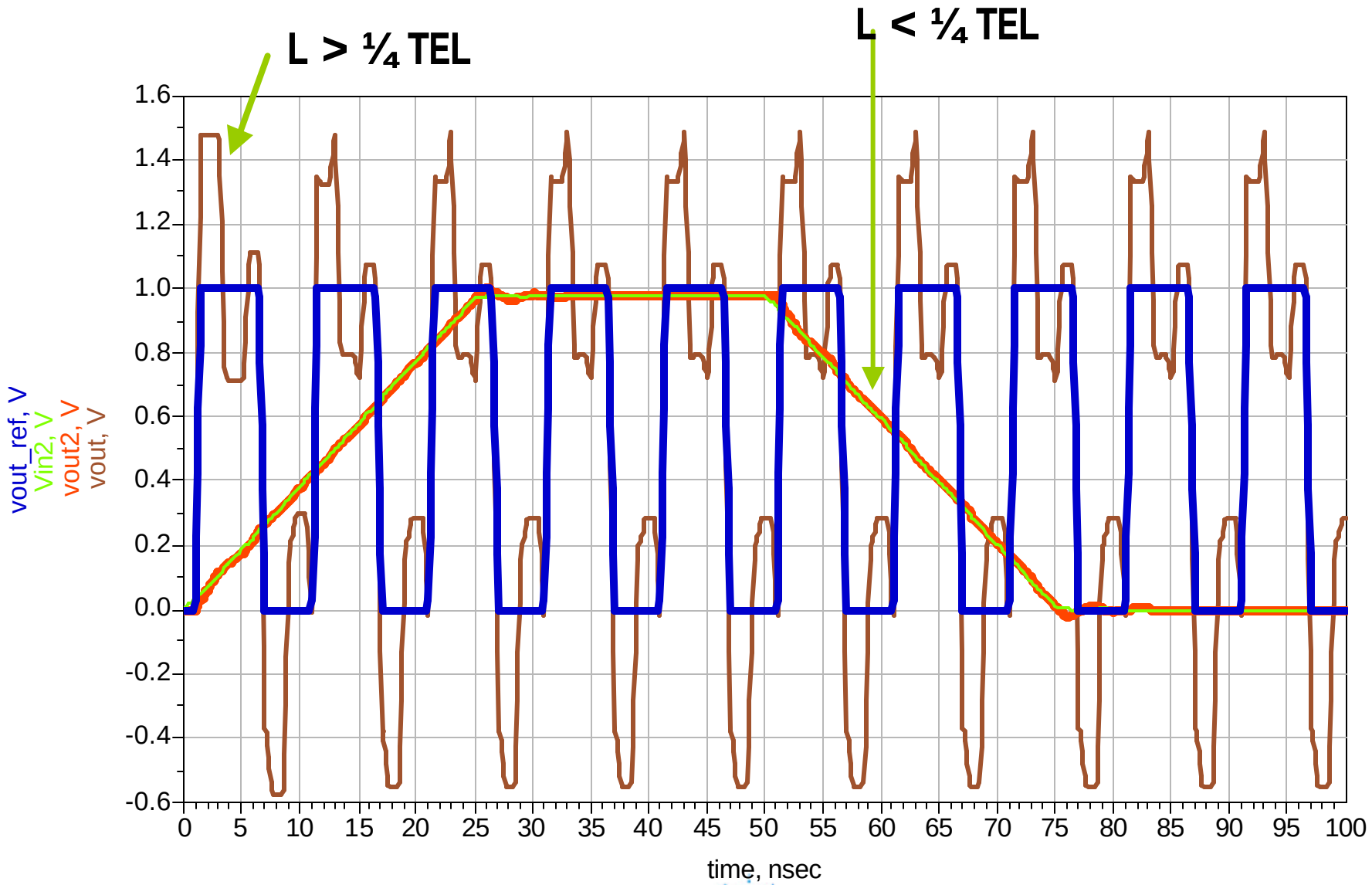


Rise time=25ns

Period=100ns



Reflection at Vo cause by Electrical length is longer than rise time without proper termination



Frequency / VNA VS. Time Domain / TDR / Scope

Frequency Domain

Steady state

Narrow Bandwidth

Better dynamic range

More accurate

Calibrate out fixture

Can convert to time domain

Data analysis more insightful

Require calibration

Longer to setup

For lump parameter

Time Domain

Transition Analysis

Large Bandwidth

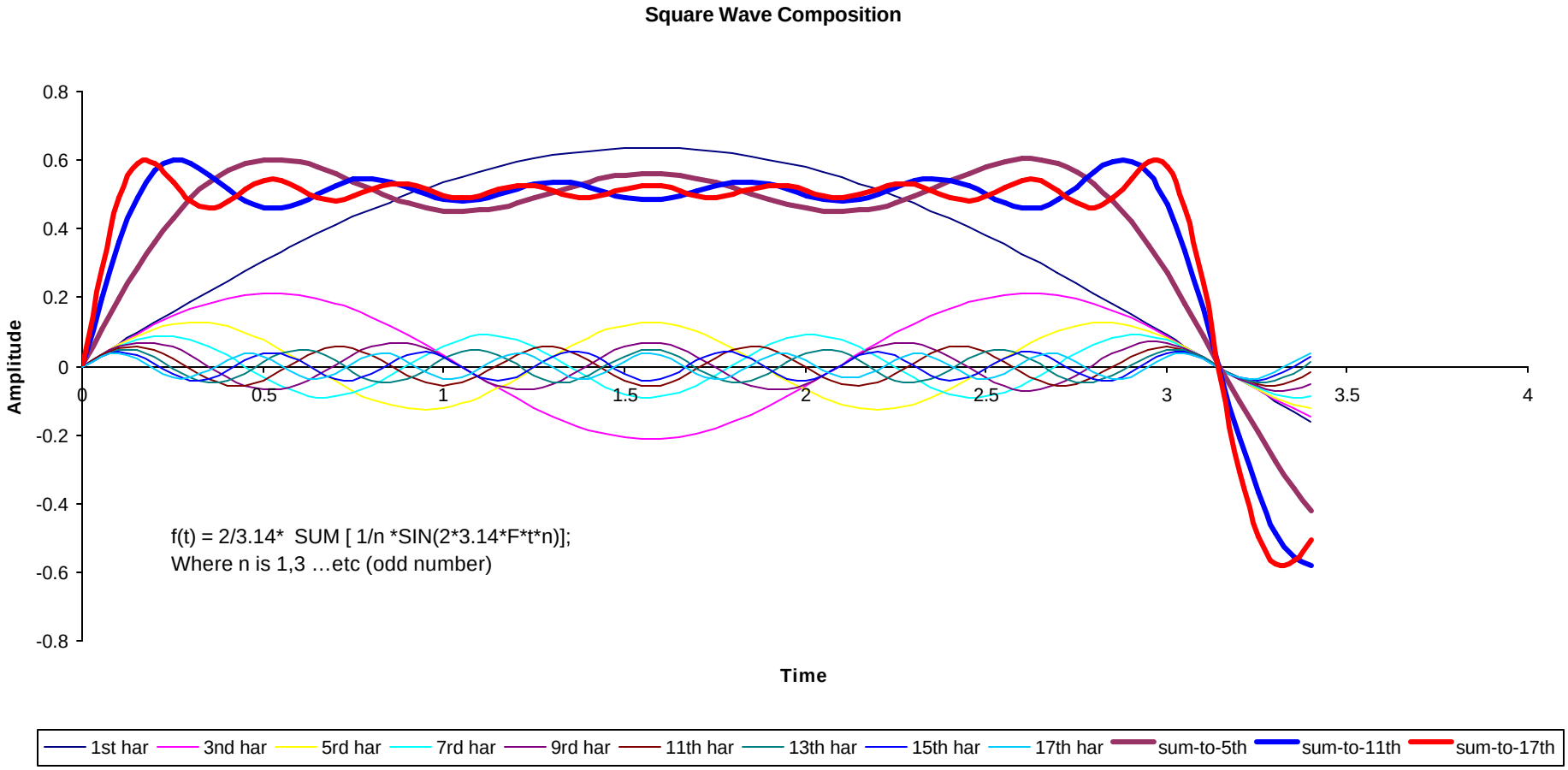
Faster setup

Less expensive / more common

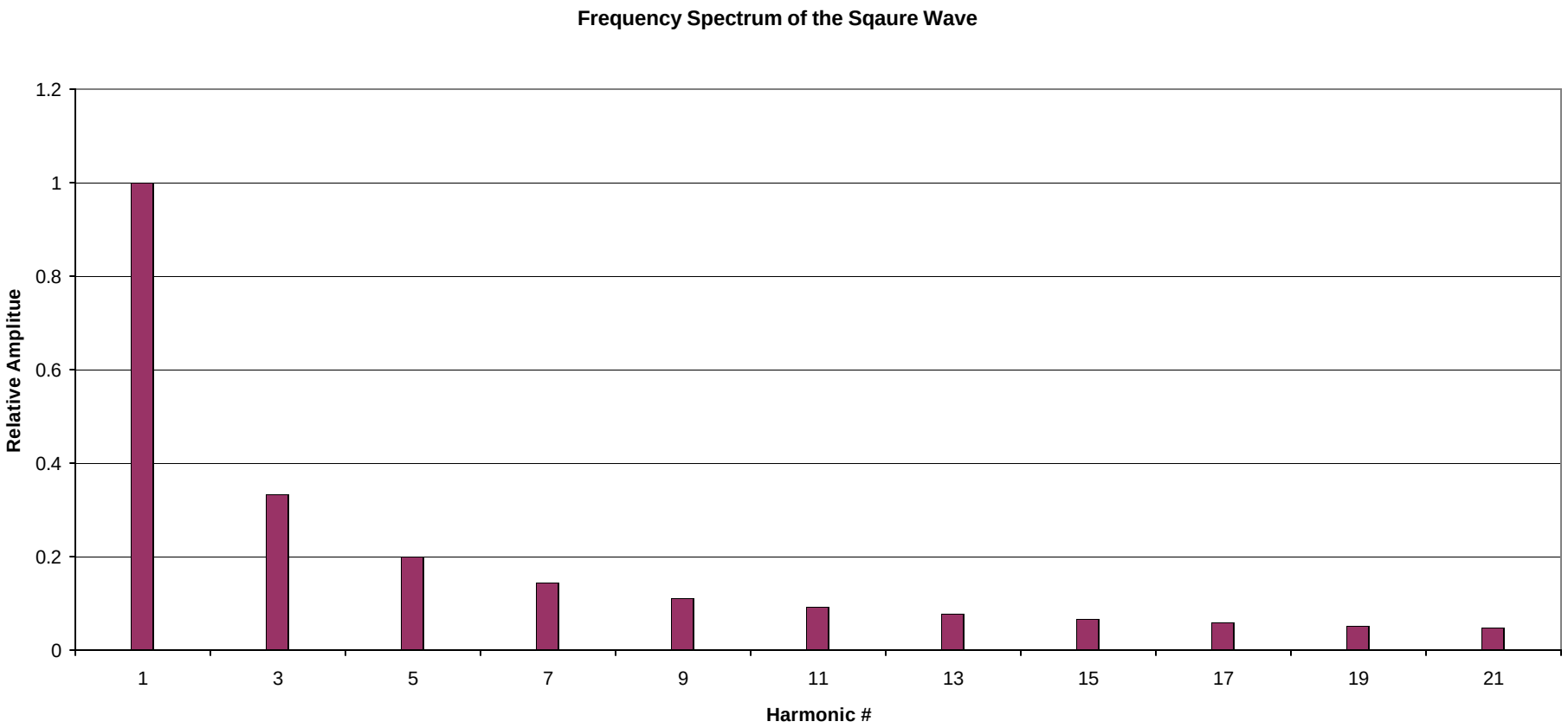
Direct representation

For long transmission line

Square wave composition



Frequency Spectrum of square wave



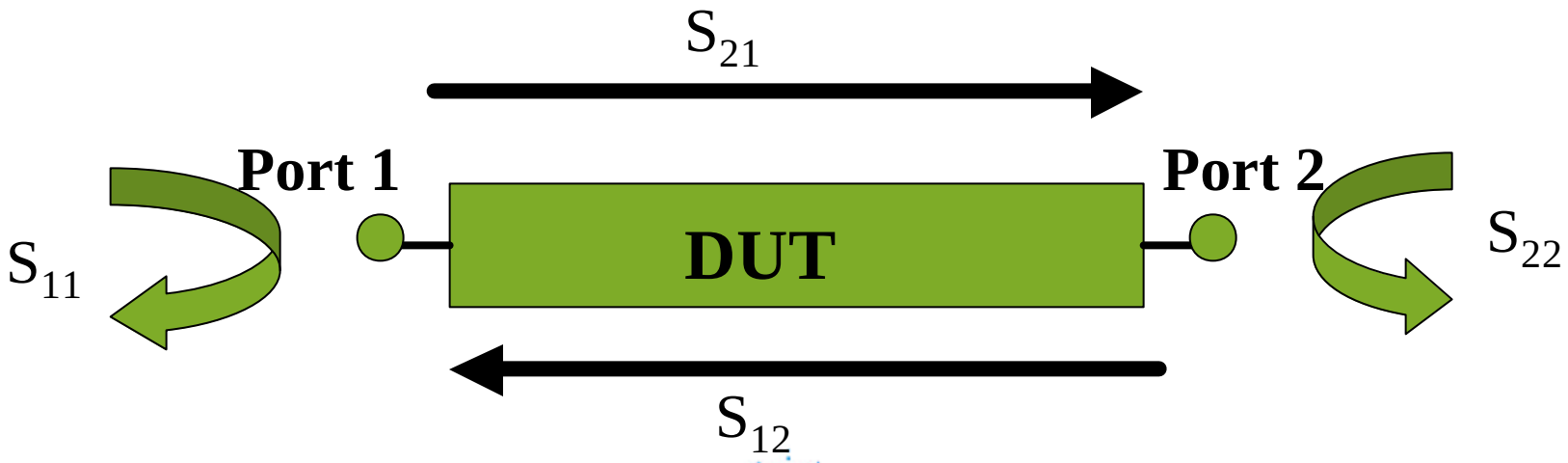
S parameter Definition

$S_{11} = V_{ref,1} / V_{inc,1}$; $S_{11db} = 20 \log (V_{ref,1} / V_{inc,1})$

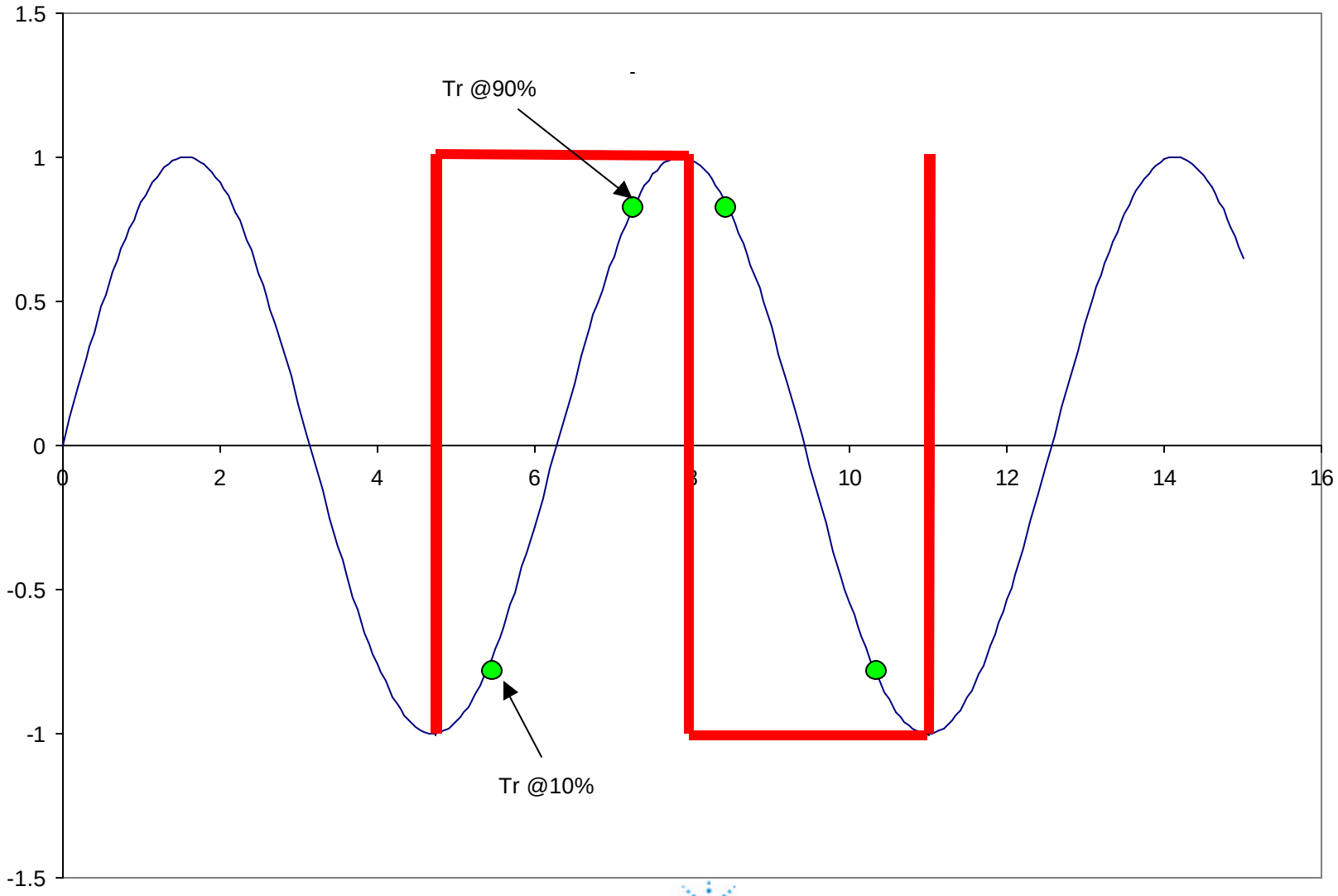
$S_{21} = V_{port2} / V_{port1}$; $S_{21db} = 20 \log (V_{port2} / V_{port1})$

For passive DUT (linear system)

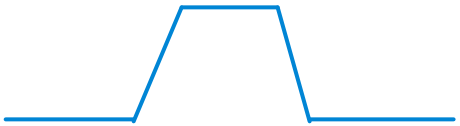
$S_{22} = S_{11}$; $S_{12} = S_{21}$



Edge Rate VS Frequency
$Tr = 0.35 / F_{3db}$



Bandwidth Selection



Rise Time
Frequency

$BW_{rise\ time} = 0.35 / Tr$

$BW1_{system} = 3 * BW_{rise\ time}$

$BW2_{system} = 6 * Frequency$

$BW_{system} = MAX (BW1 , BW2)$

Bandwidth Selection

Clock Frequency @ Rise Time Tr.

$BW_{rise\ time} = 0.35 / Tr$

Interconnect BW with minimum signal distortion and loss

$BW_{interconnect} = MAX (3 X BW_{rise\ time} , 6 X Clock\ Frequency)$

400MHz frequency with:

Rise time	*3 X $BW_{rise\ time}$*	*6 X BW_{signal}*	*$BW_{interconn}$*
200ps	5.25 GHZ	2.4 GHZ	5.25 GHZ
400ps	2.62 GHZ	2.4 GHZ	2.62 GHZ
800ps	1.31 GHZ	2.4 GHZ	2.4 GHZ

Bandwidth Selection

Clock Frequency @ Rise Time Tr.

$BW_{rise\ time} = 0.35 / Tr$

Interconnect BW with minimum signal distortion and loss

$BW_{interconnect} = MAX (3 X BW_{rise\ time} , 6 X Clock\ Frequency)$

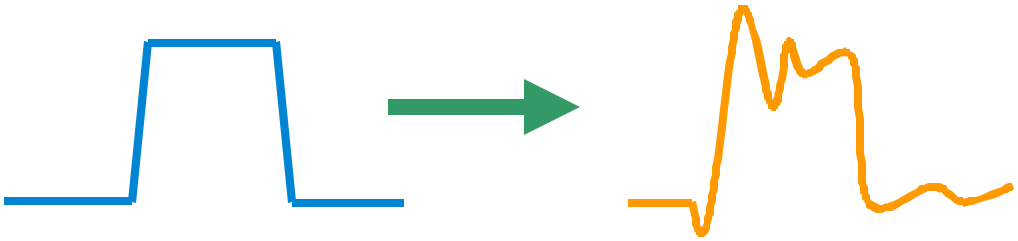
Results from simulation:

$3 X BW_{rise\ time}$ causes approximately 3 % rise time degradation

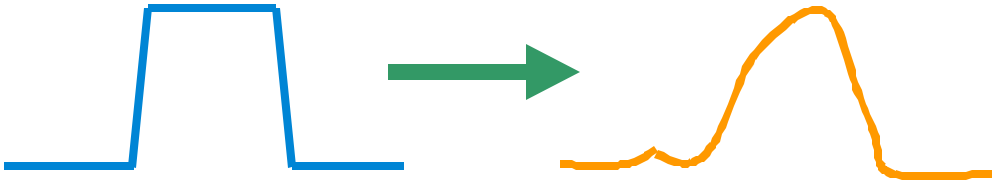
6 X Frequency causes approximately 2 % amplitude loss

Signal Integrity Issues

- Impedance mismatch
- Reflection
- Crosstalk
- Ground bounce
- Inadequate power bus decoupling



- Propagation delay
- Dispersion
- Loss

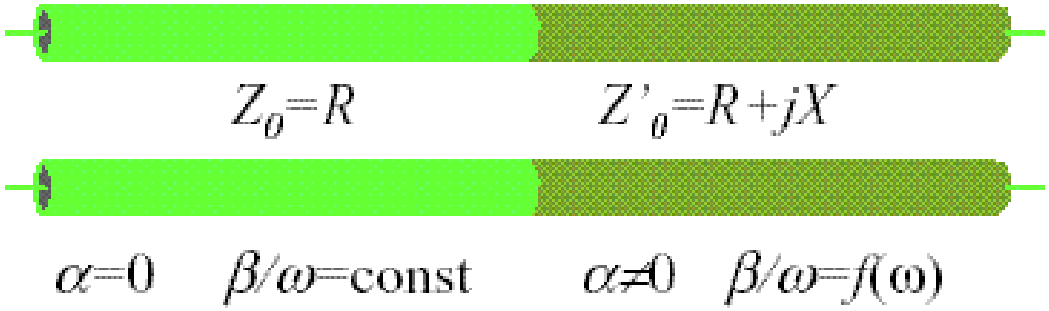


Signal Integrity Components

- **Signal Integrity**
  - **Discontinuity (Connectors, via)**
  - **Dispersion**
  - **AC loss**
    - Skin Effect
    - Dielectric Loss (loss tangent)
  - **Ground Bounce**
  - **Inadequate power bus decoupling**
- **Differential Pair**
  - **Less sensitive to components above**

Dispersive Loss

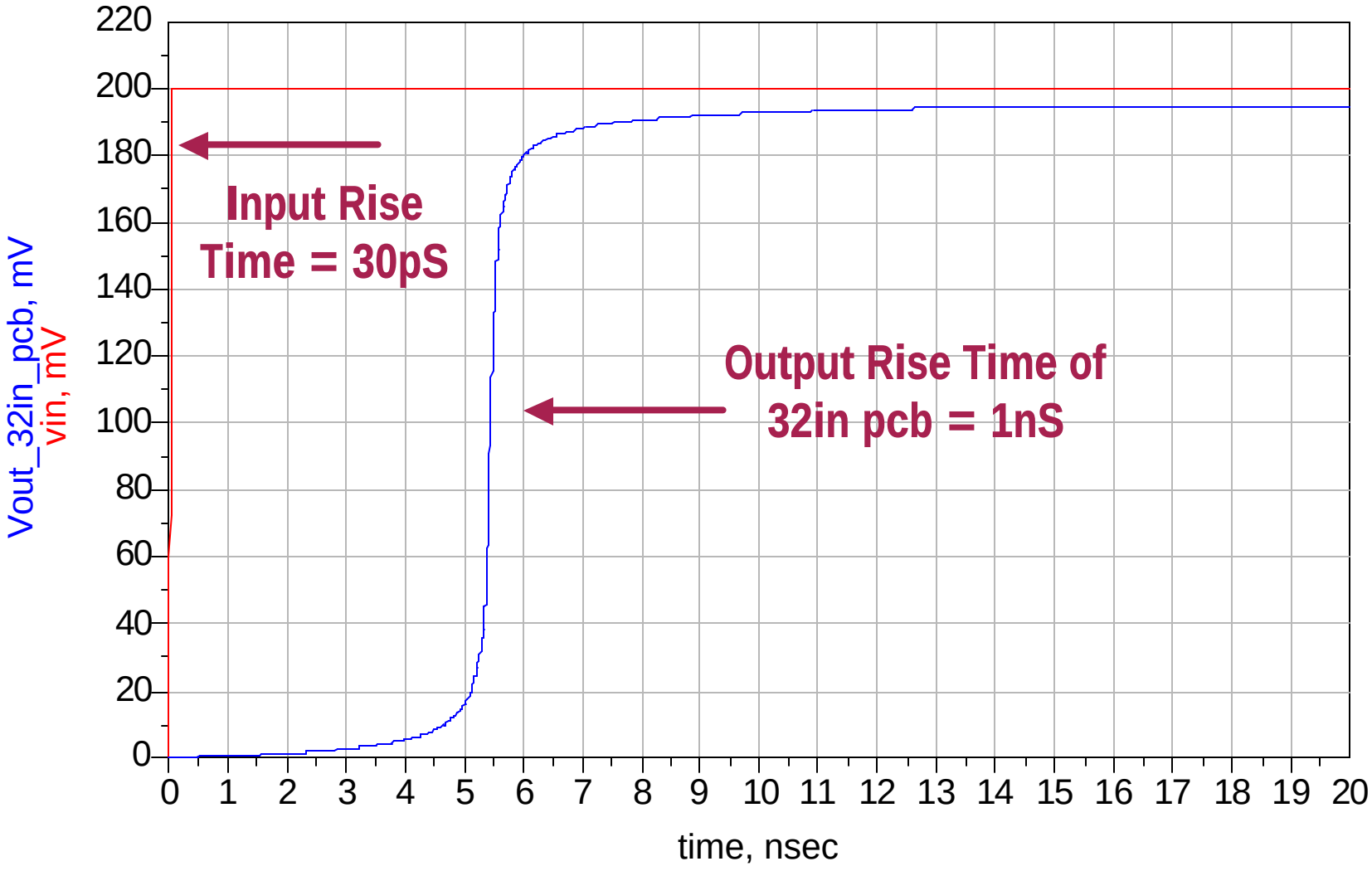
- **Reflection at the Interface of 2 Transmission lines:**
  - **One cable is different loss than the other (Even the characteristics impedance is the same)**
    - **Reflection coefficient is not zero and also frequency dependence.**



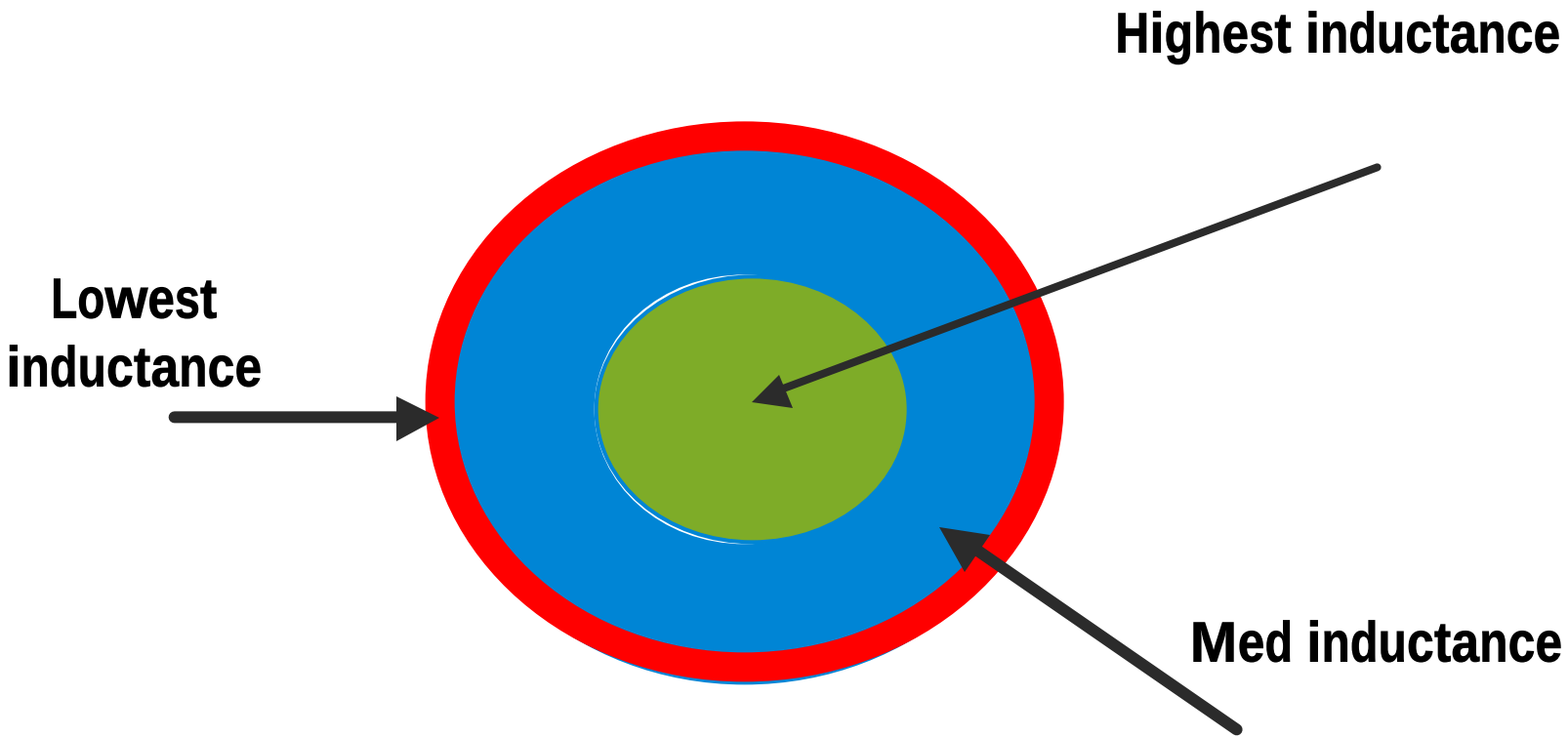
AC LOSS

- **Skin Effect Loss**
- **Dielectric Loss**

Rise Time Degradation After Signal Propagates Through 5mil Width, 32” Long for the FR4 PCB



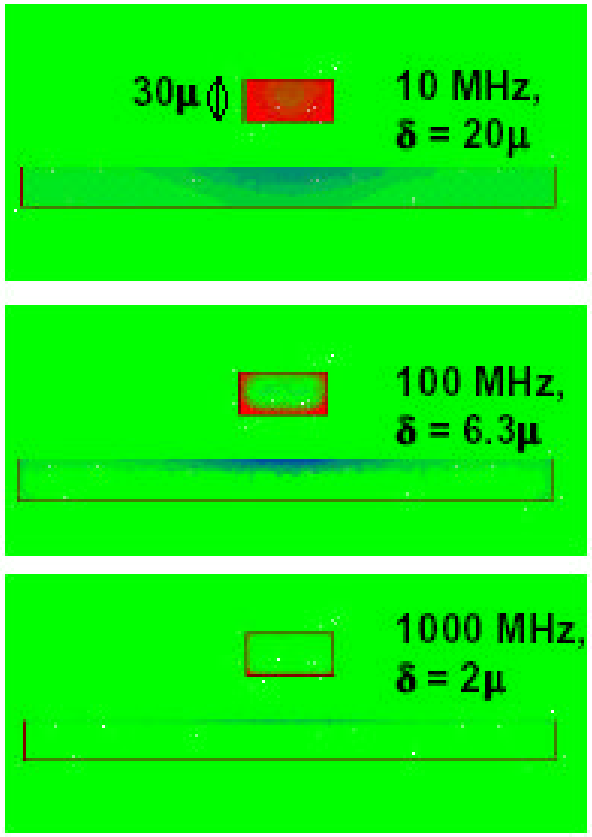
Skin Effect



$$Zo = \sqrt{\frac{(R+jWL)}{(G+jWC)}}$$

Excerpt from PCB Design West Conf
3/21/ 2001 (GigaTest Labs)

Inductance is Frequency Dependent



Internal self inductance decreases with increasing frequency

Account for this by using a complex resistance

$$\tilde{R}_L(f) = R_{DC} + R_{AC}\sqrt{f}(1+i)$$

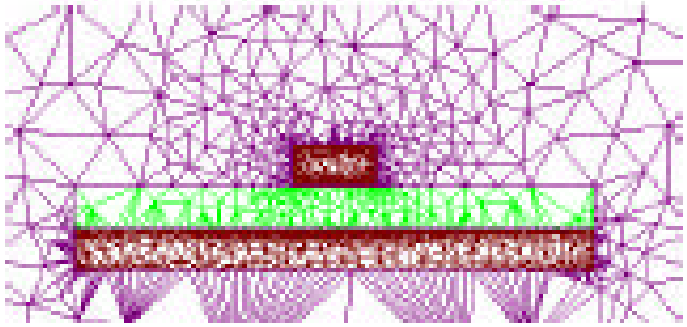
Real part is the resistive loss
Imaginary part is the frequency dependent inductance

$$\tilde{R}_L + i\omega L_L$$

$$= \left(R_{DC} + R_{AC}\sqrt{f}\right) + i\omega\left(L + \frac{R_{AC}}{2\pi\sqrt{f}}\right)$$

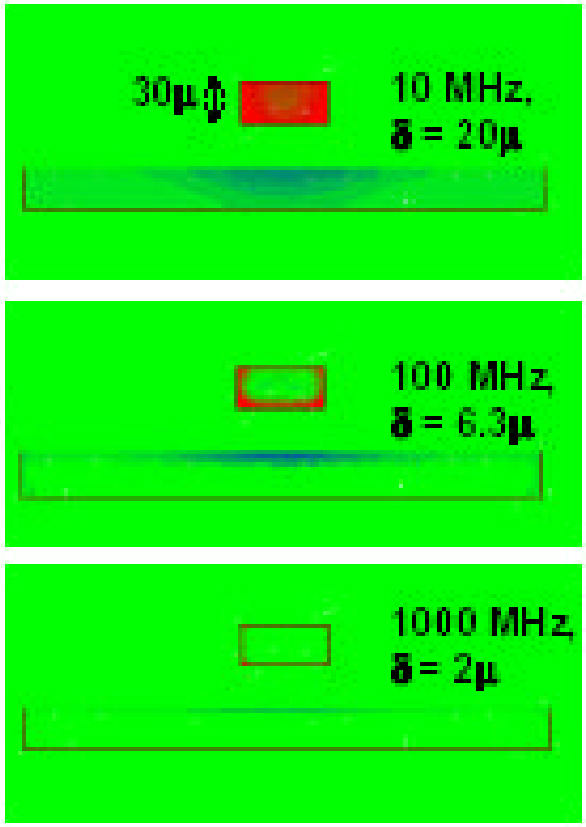
Skin Depth Limited Current Distributions

$$\delta = \sqrt{\frac{1}{\sigma \pi \mu_0 \mu_r f}} = 63\mu\sqrt{\frac{1}{f}} \qquad f \text{ in MHz}$$



Ansoft's Maxwell 2D Extractor

Microstrip:
50 Ohm, FR4
$\varepsilon_r = 4.2$
h = 38 µ
t = 30 µ (1 oz)
w = 75 µ



The Practical Part: A Simple Approximation

Current on one side of signal path

$$R_L = \frac{\rho}{tw} + \frac{\rho}{\delta w}$$

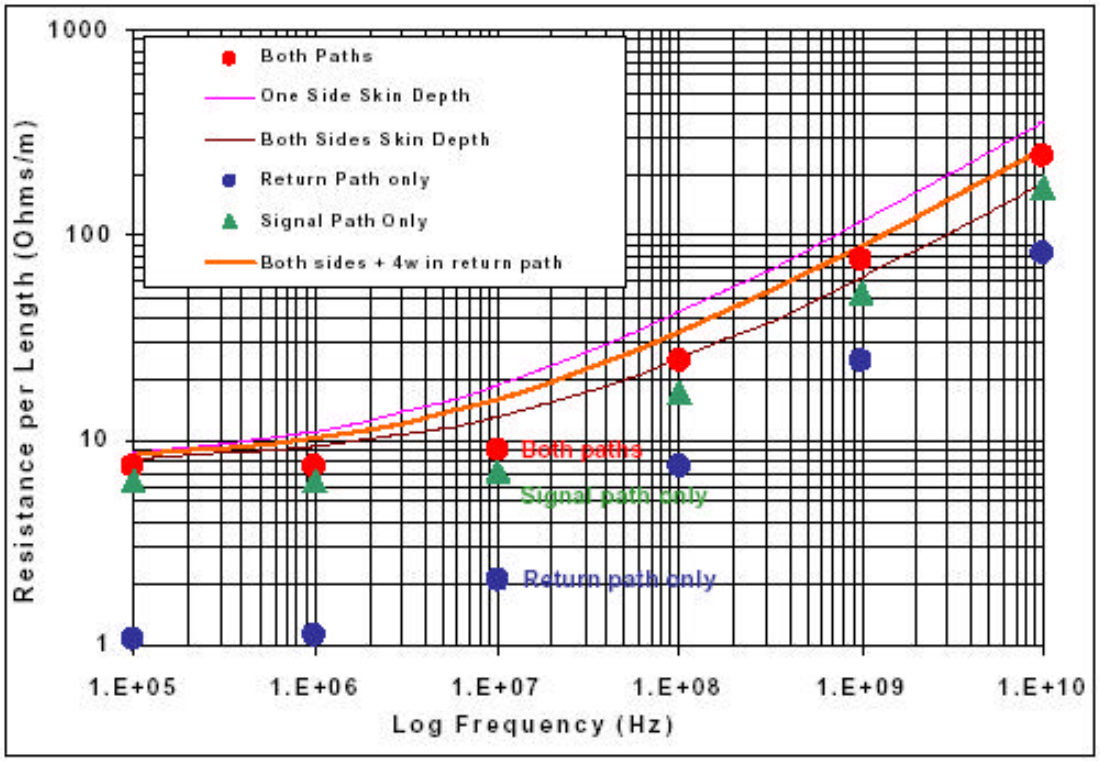
R_{DC} R_{AC}

Current on both sides of signal path

$$R_L = \frac{\rho}{tw} + \frac{\rho}{2\delta w}$$

Current on both sides of signal path
And return current path = 4 x w

$$R_L = \frac{\rho}{tw} + \frac{\rho}{2\delta w} + \frac{\rho}{\delta 4w} = \frac{\rho}{tw} + 0.75\frac{\rho}{\delta w}$$



Dots are from 2D field solver
Lines are the simple models

AC Loss (Cont)

- **Skin Effect Loss**
- **Dielectric Loss**

Complex Dielectric Constant

$C = \varepsilon C_0$ C_0 is the empty space capacitance

describe ε as complex: $\varepsilon(\omega)=\varepsilon'(\omega) - i\,\varepsilon''(\omega)$ $\tan(\delta) = \frac{\varepsilon''}{\varepsilon'}$

Dissipation Factor

Loss Tangent

$$I = C\frac{dV}{dt} = C_0(i\omega V)\{\varepsilon(\omega)\}$$

$$I = i\omega C_0 V(\varepsilon'(\omega) + i\varepsilon''(\omega))$$

$$= i\omega C_0 V\varepsilon'(\omega) + \omega C_0 V\varepsilon''(\omega)$$

imaginary current *real current*

The real part of the dielectric constant relates to "dielectric" or "displacement" currents
The imaginary component of the dielectric constant relates to "resistive" or lossy currents through the capacitor.

$$Zo = \sqrt{\frac{(R+jWL)}{(G+jWC)}}$$

Dissipation Factor and Conductance

$$I = i\,\omega C_0 V\varepsilon'(\omega) + \omega C_0 V\varepsilon''(\omega)$$

imaginary current *real current*

$$I = C\frac{dV}{dt} + \frac{1}{R}V$$

$$R = \frac{1}{\varepsilon''(\omega)\ \omega\ C_0}$$

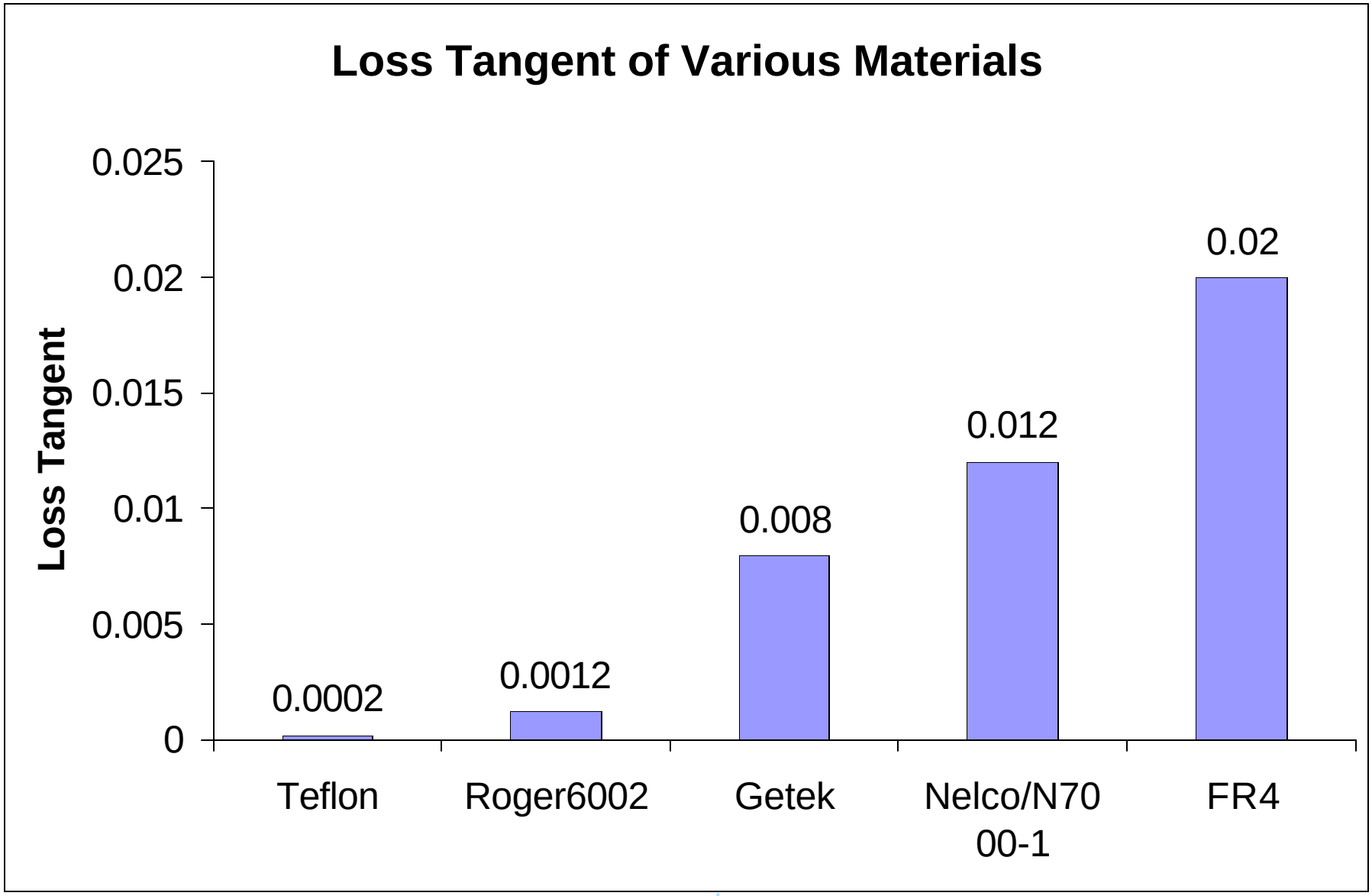
Define conductance as: $I = C\frac{dV}{dt} + GV$

$$G \equiv \frac{1}{R} = \varepsilon''(\omega)\ \omega\ C_0 = \omega\ \tan(\delta)\ C$$

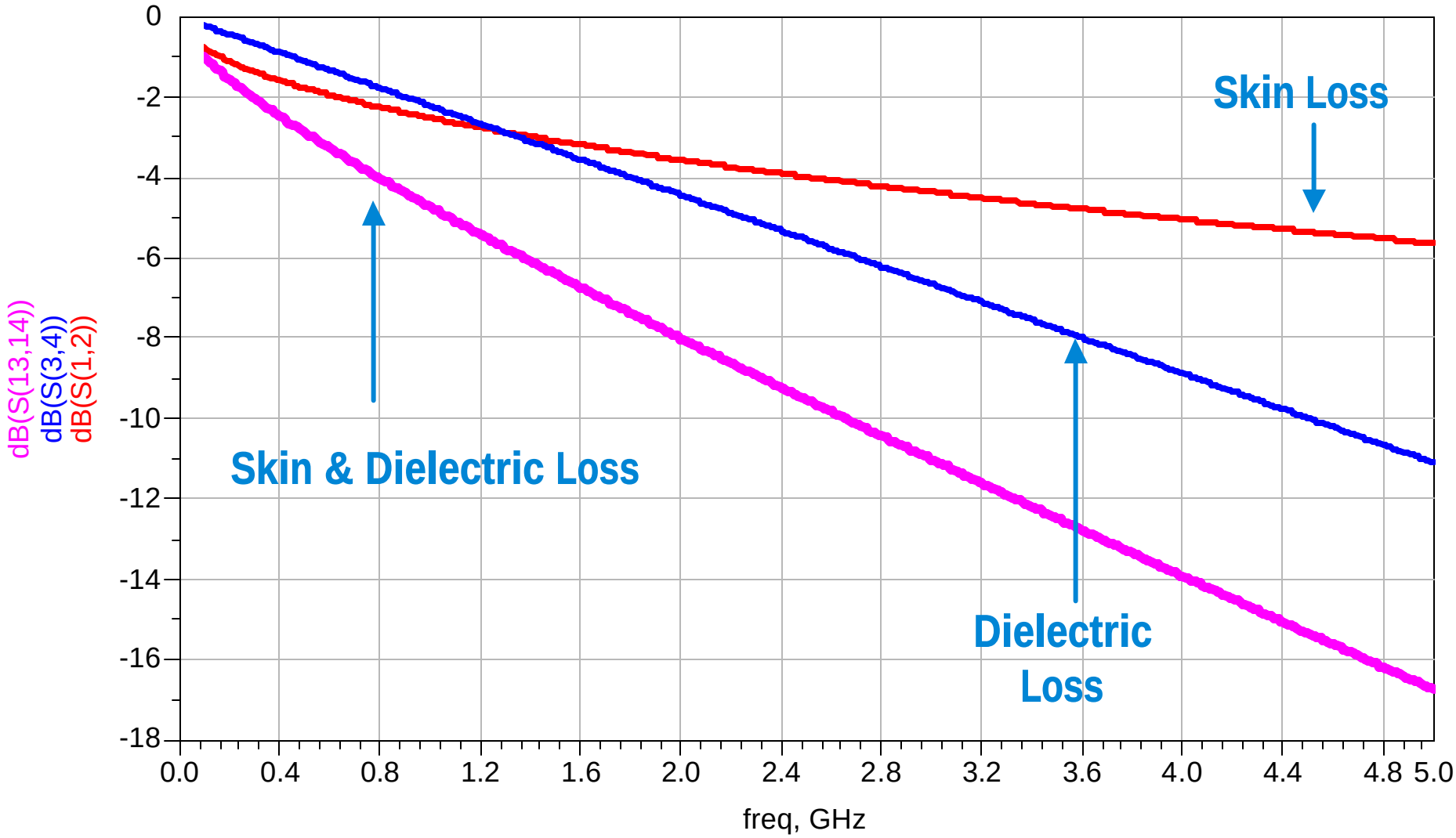
$$G = \frac{\sigma}{\varepsilon_0}C_0 \qquad \sigma = \omega\varepsilon_0\varepsilon_r'' = \omega\varepsilon_0\varepsilon_r'\tan(\delta)$$

Even if tan(δ) is constant in frequency, G is linear in frequency

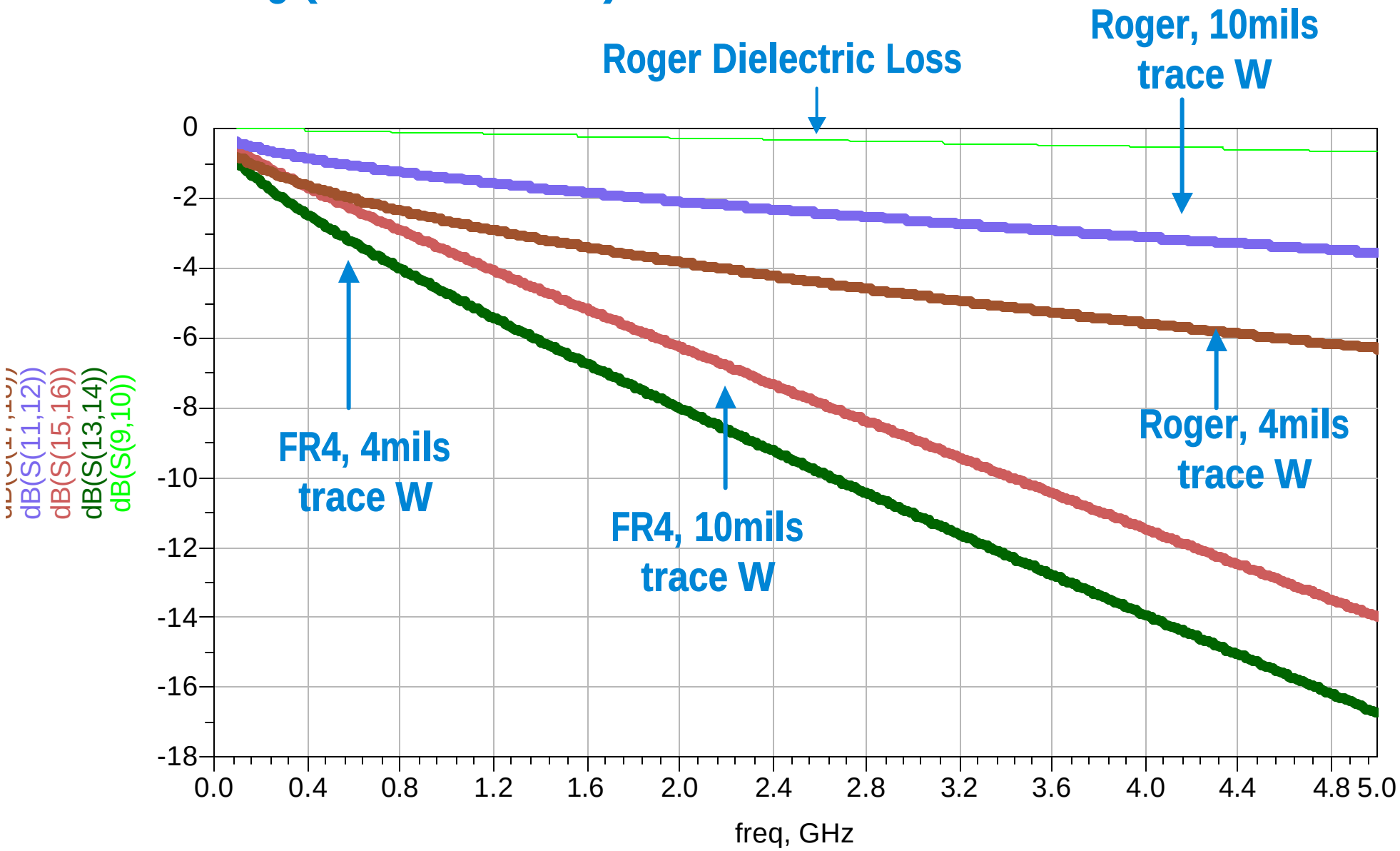
Dielectric Loss



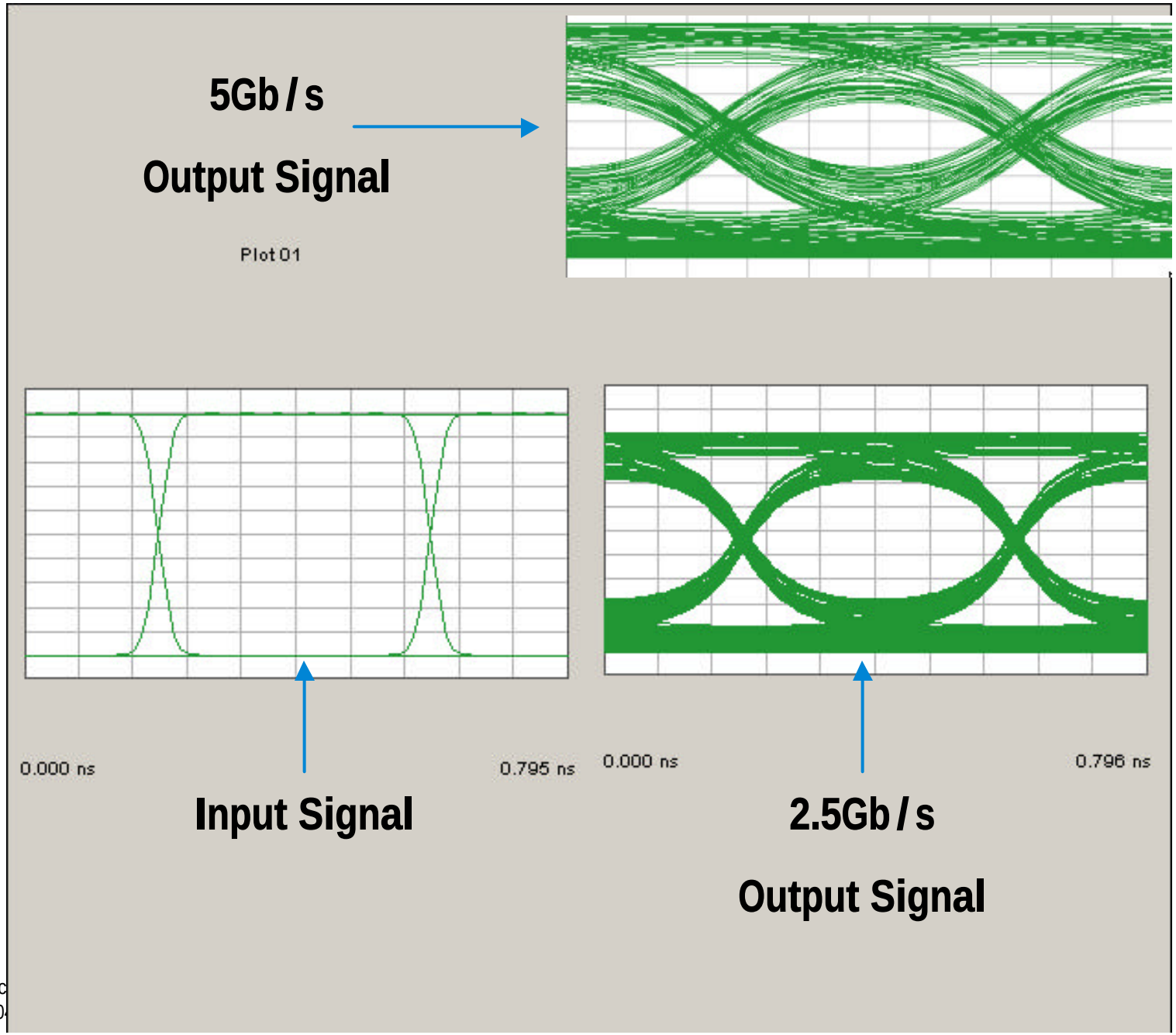
Skin Effect & Dielectric Loss of an FR4, 4 mils, 10mils trace width and 24 in length (ADS simulation)



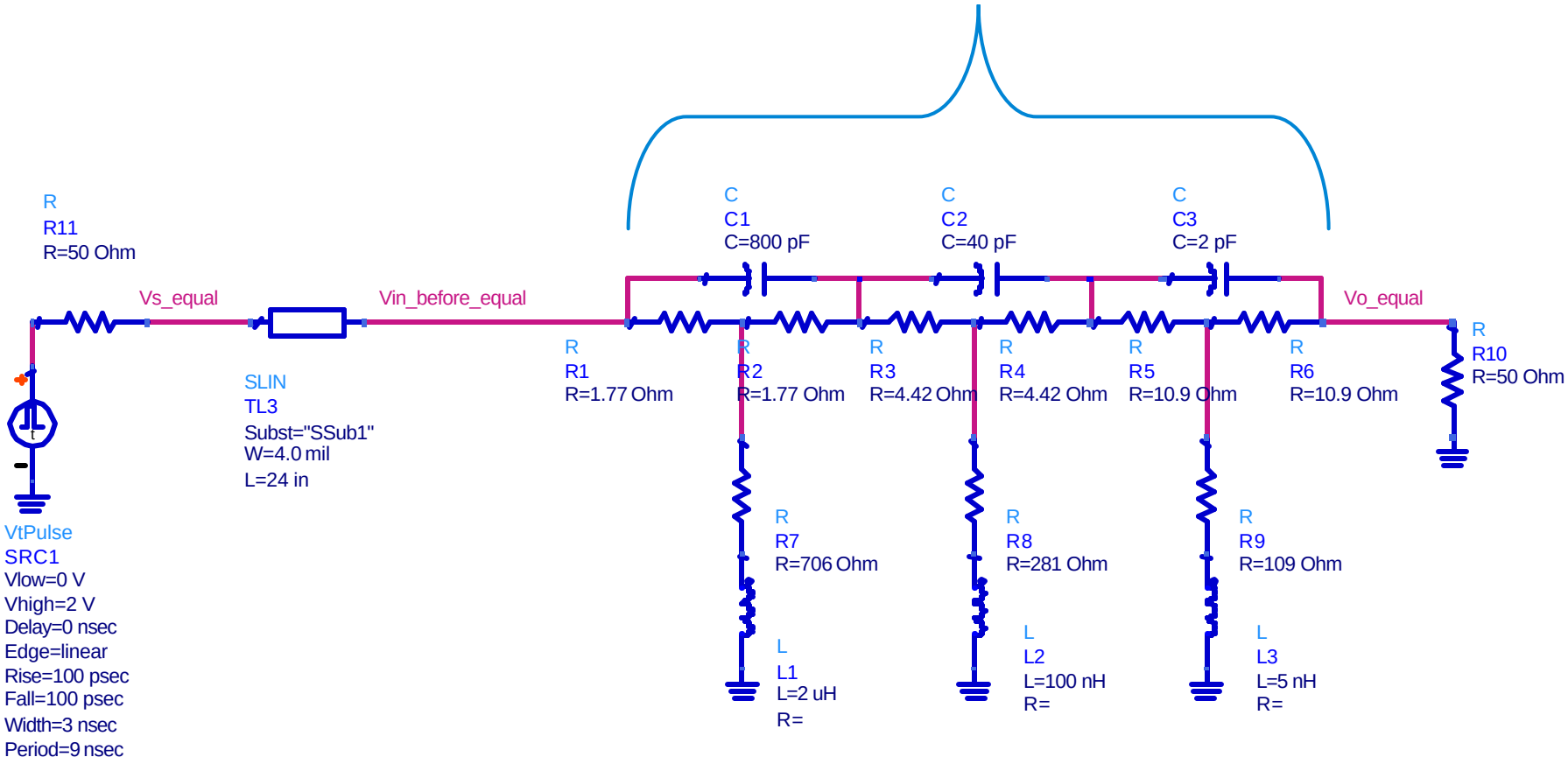
Skin & Dielectric Loss of an FR4, Roger of 4mils and 10mils Width, and 24” long (ADS simulation)



2.5Gb/s data for FR4 PCB with 4mils trace width, 24” long.

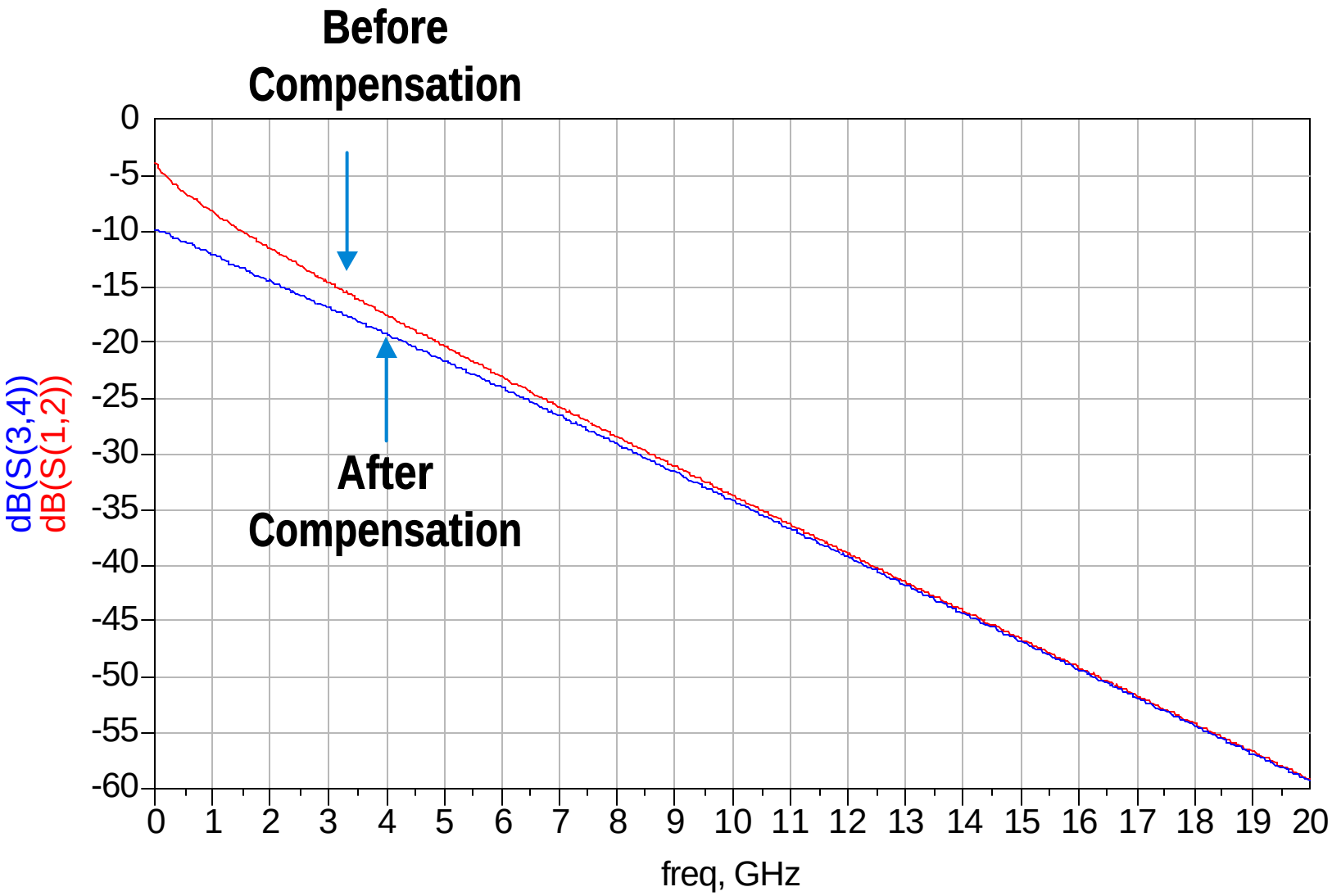


Compensation Circuits

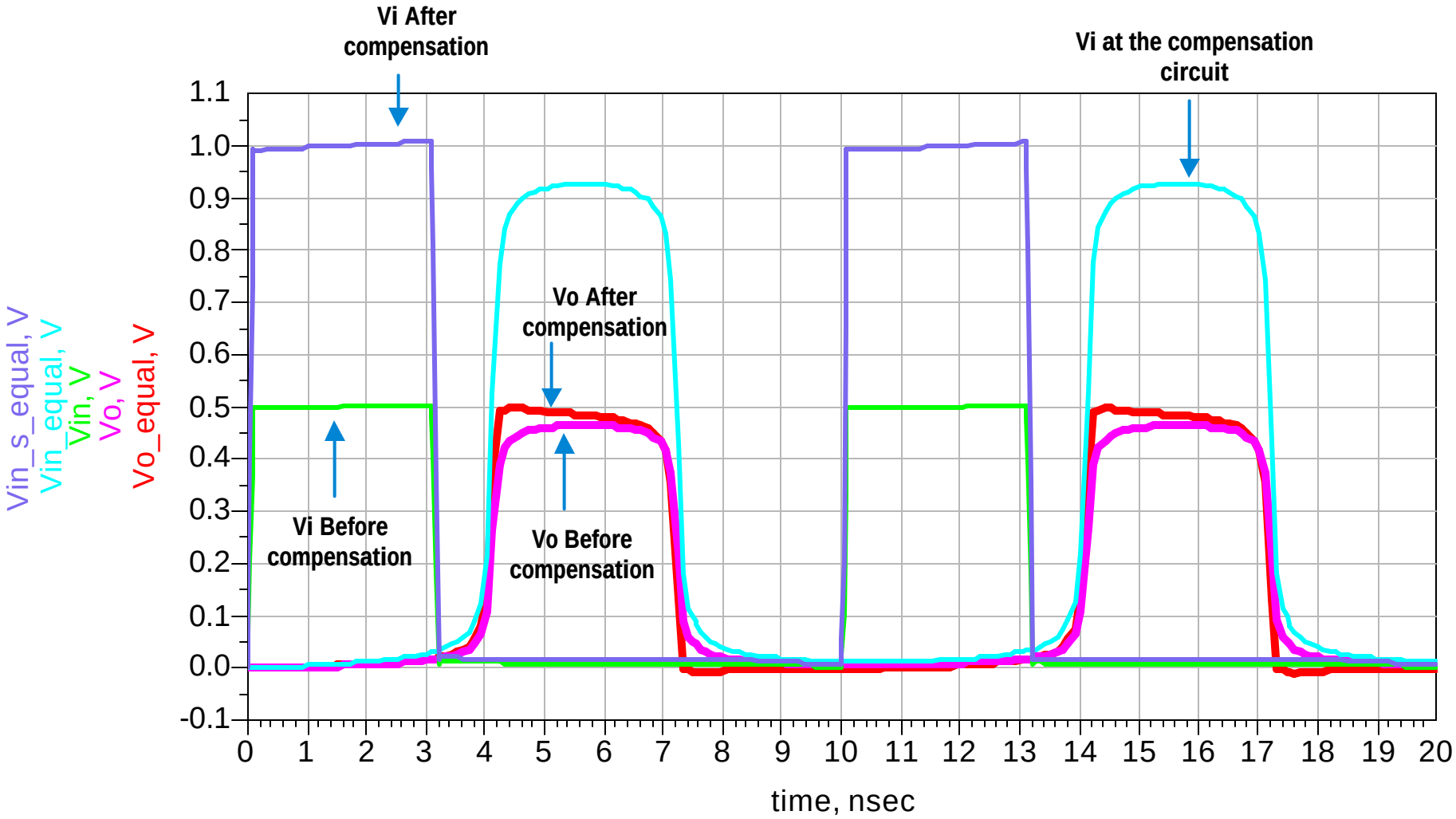


Compensation circuit from ITC 2002 by Wolfram Humann, Agilent Technologies

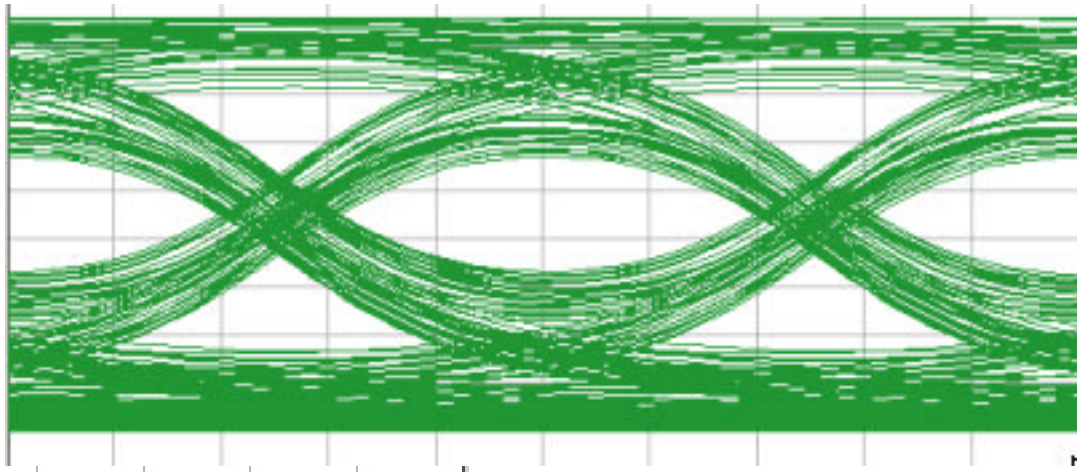
S-Par of before and after compensation



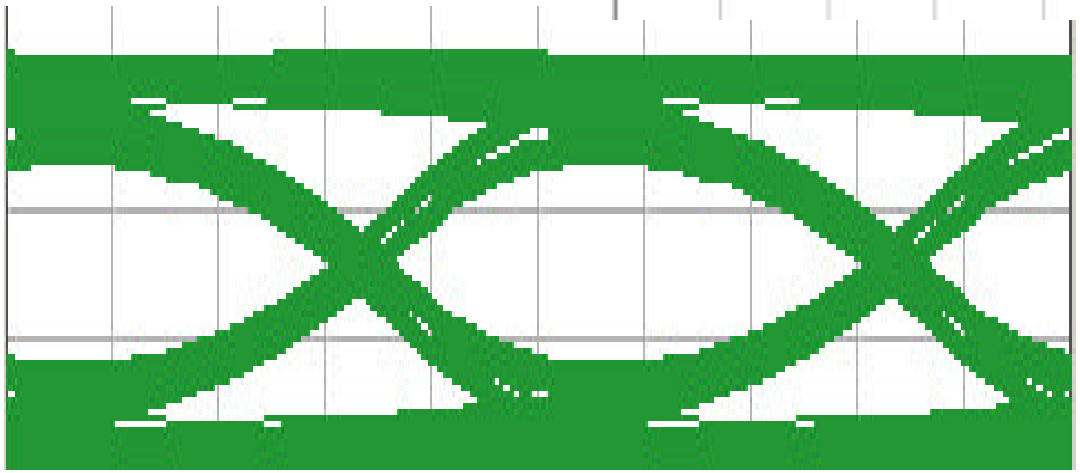
Time Domain of Before and After Compensation
Vi compensation = 2 Vin



5Gb/s data for FR4 PCB with 4mils trace width, 24” long.



Before Compensation



After Compensation

Plot excerpt from the High-Speed Signal Propagation book,
By Howard Johnson . Martin Graham

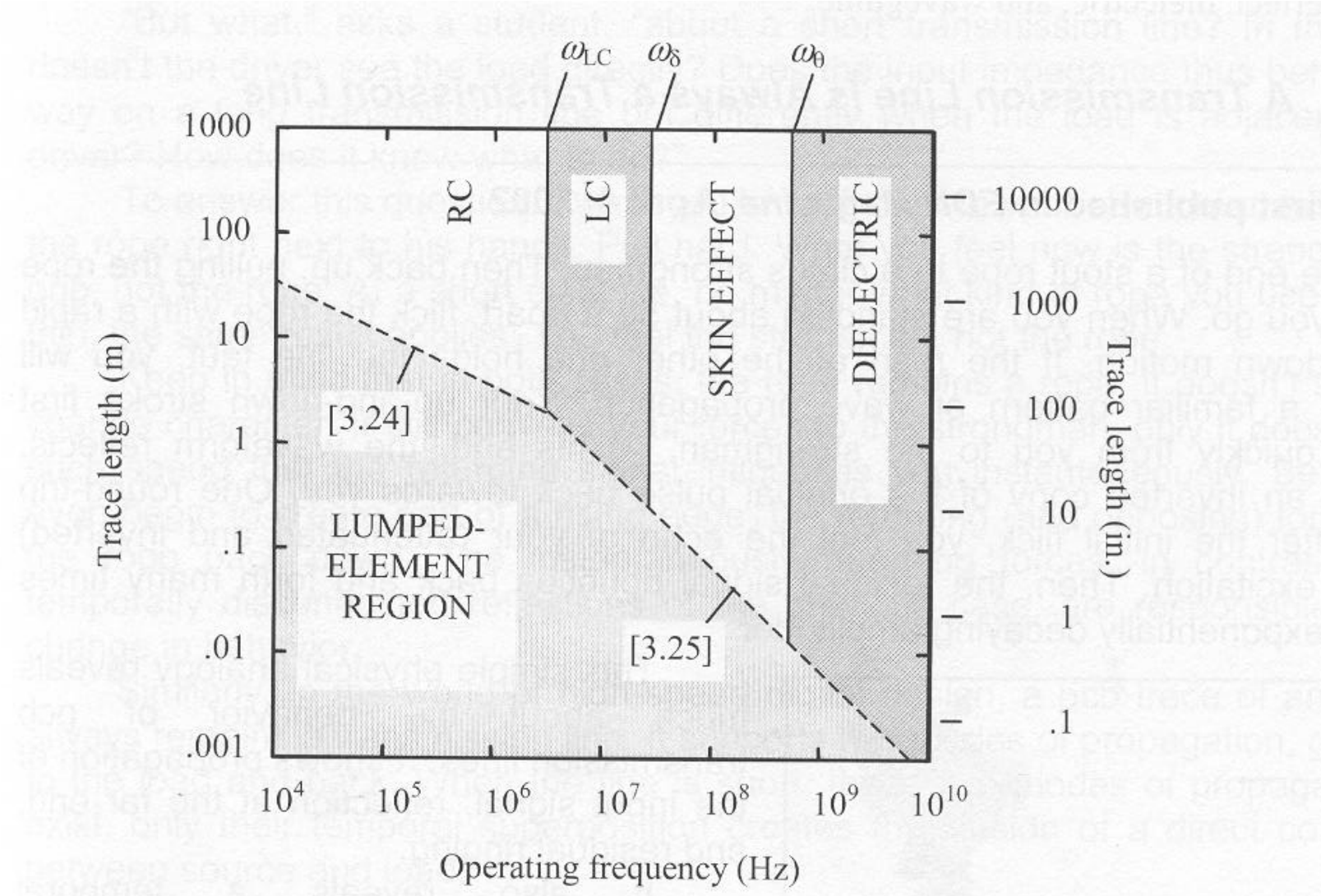


Figure 3.2—Performance regions for a 150-µm (6-mil), 50-Ω, FR-4 stripline.

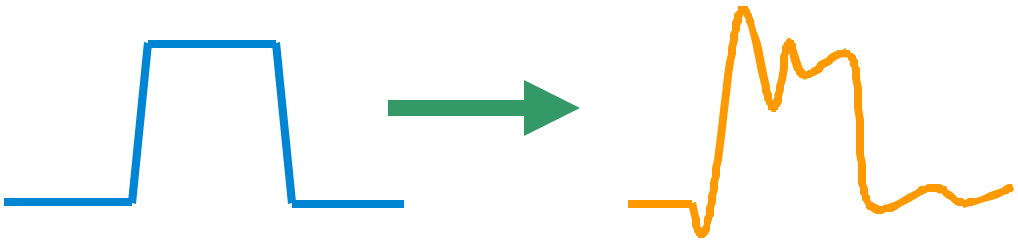
Critical Interconnect Components

- PCB via
- Connectors and Cable Connectors
- Socket
- Probe tips
- Packages and Multichip modules
- PCB trace
  - Single Run
  - Differential Run

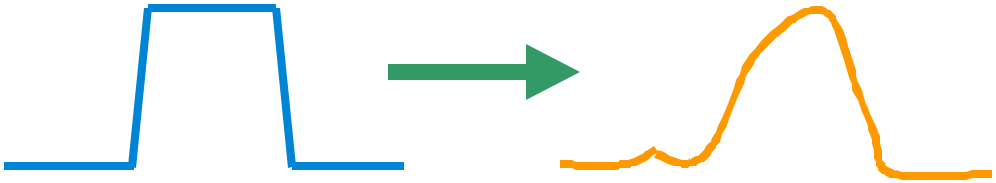
Q / A

Signal Integrity Issues

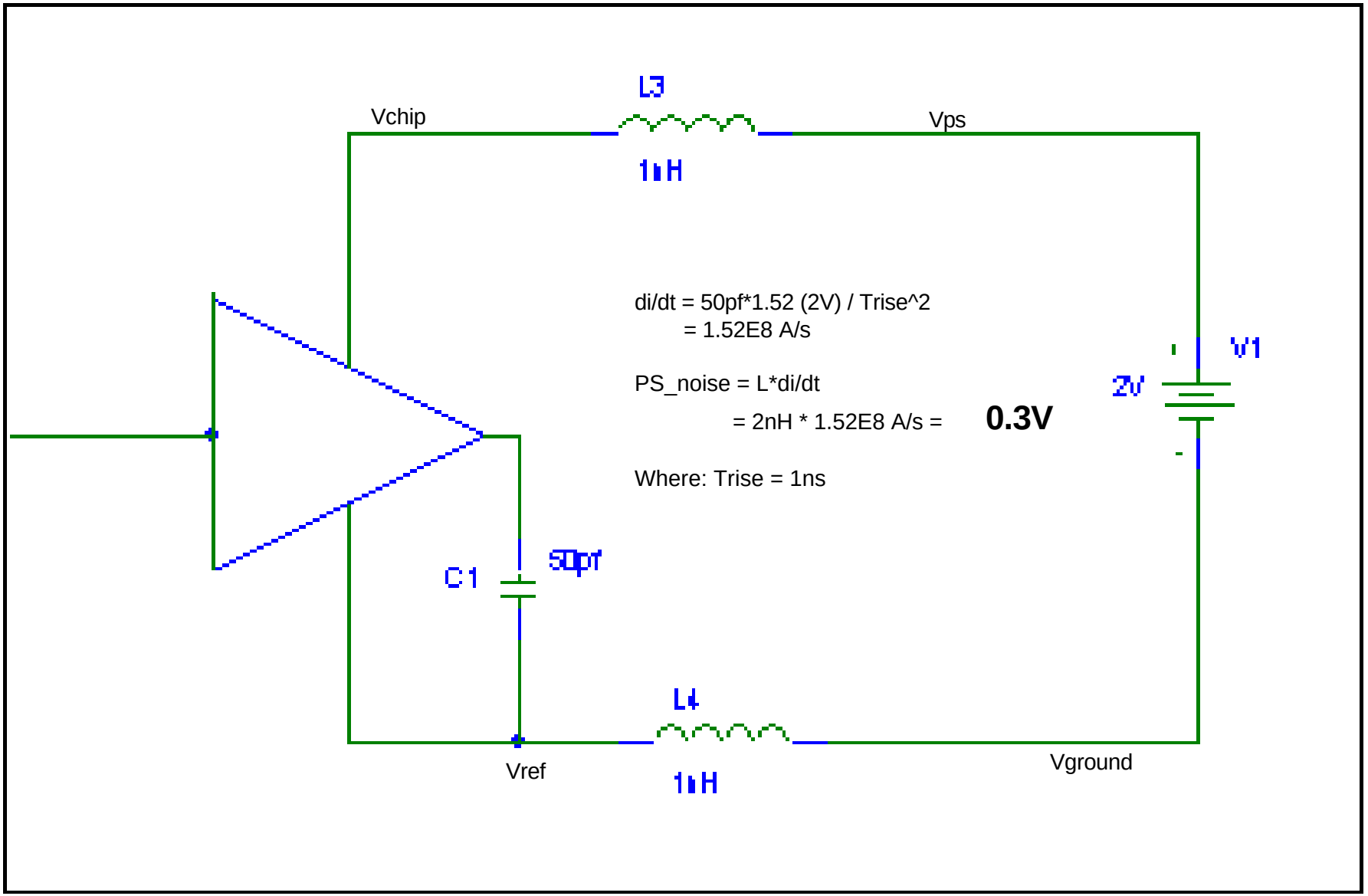
- Impedance mismatch
- Reflection
- Crosstalk
- Ground bounce
- Inadequate power bus decoupling



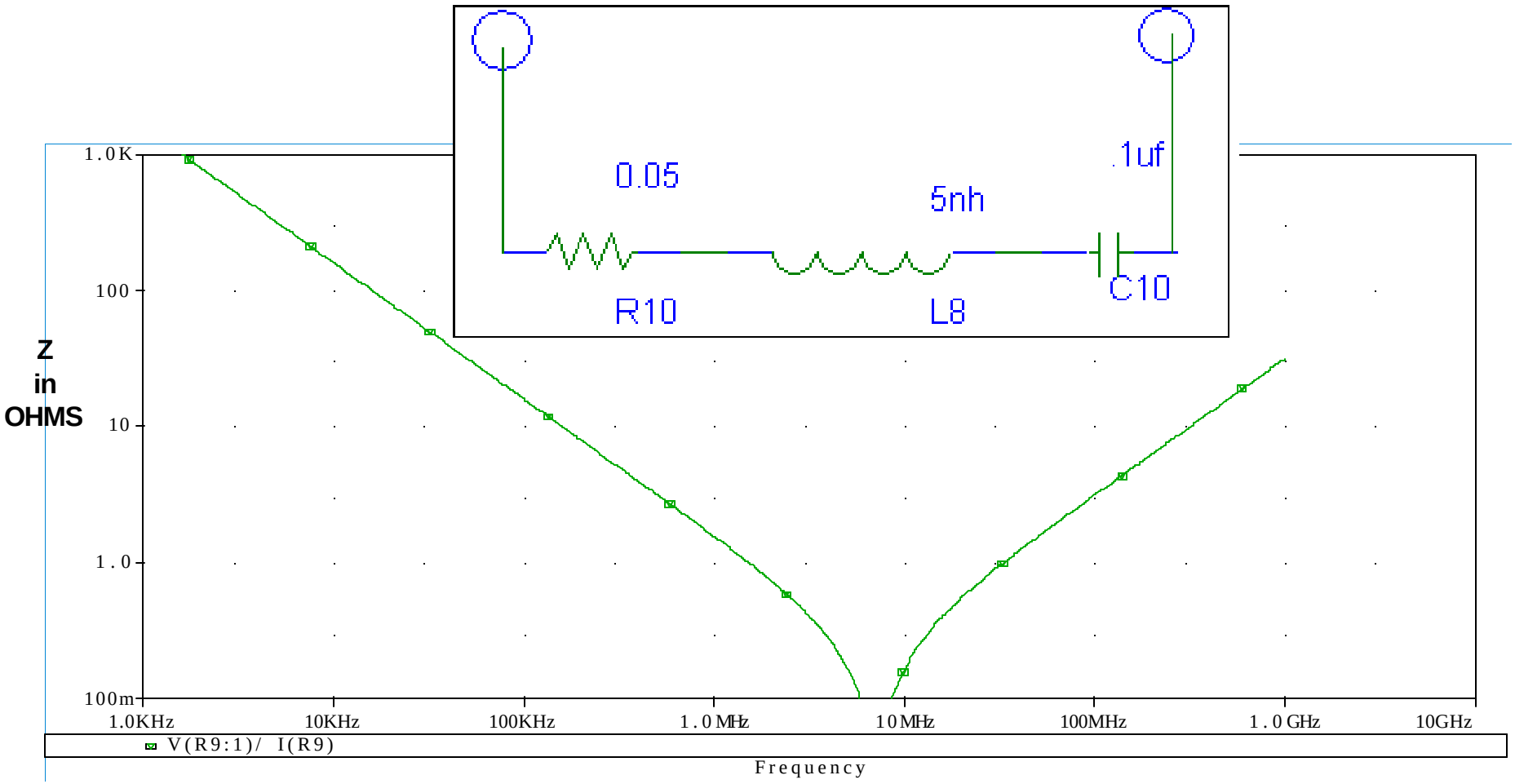
- Propagation delay
- Dispersion
- Loss



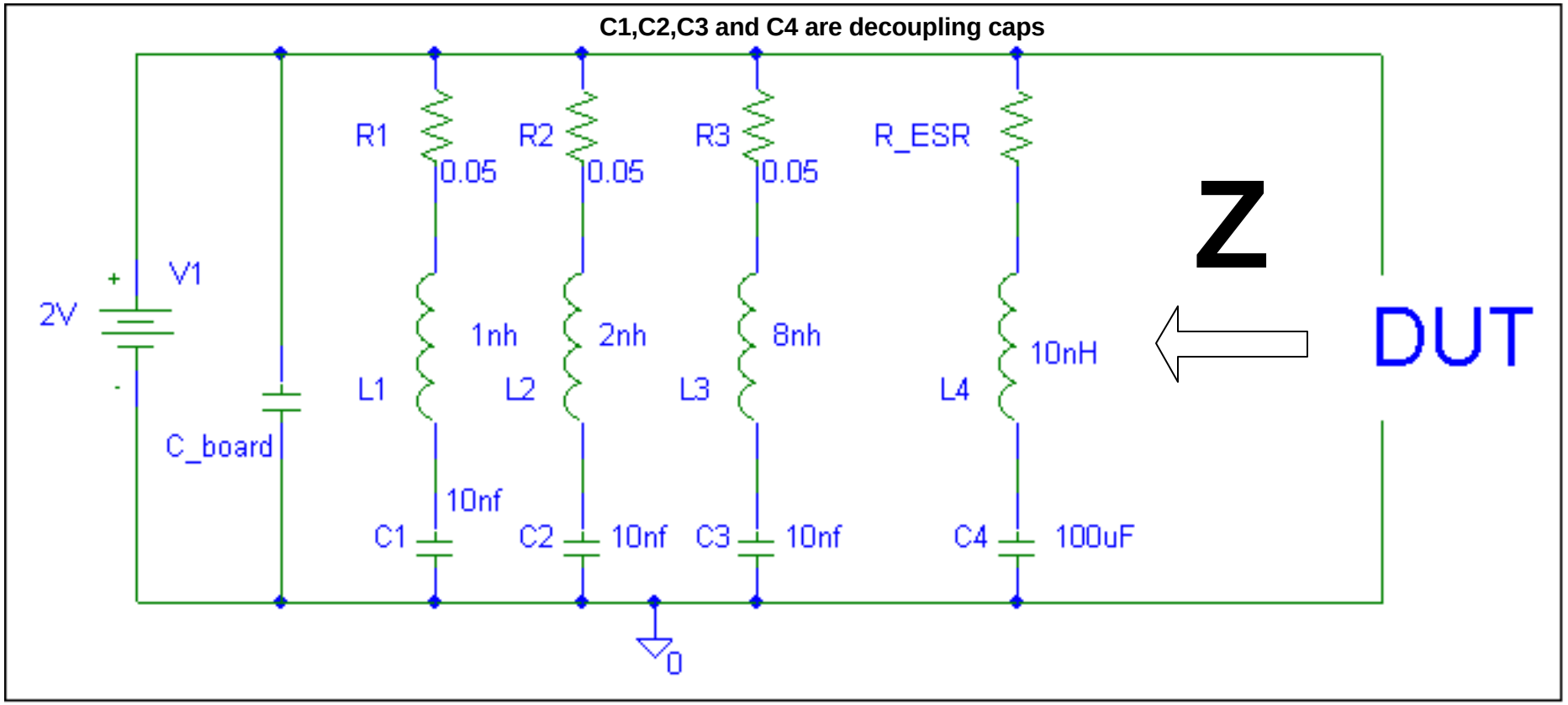
Ground Bounce / Power Droop



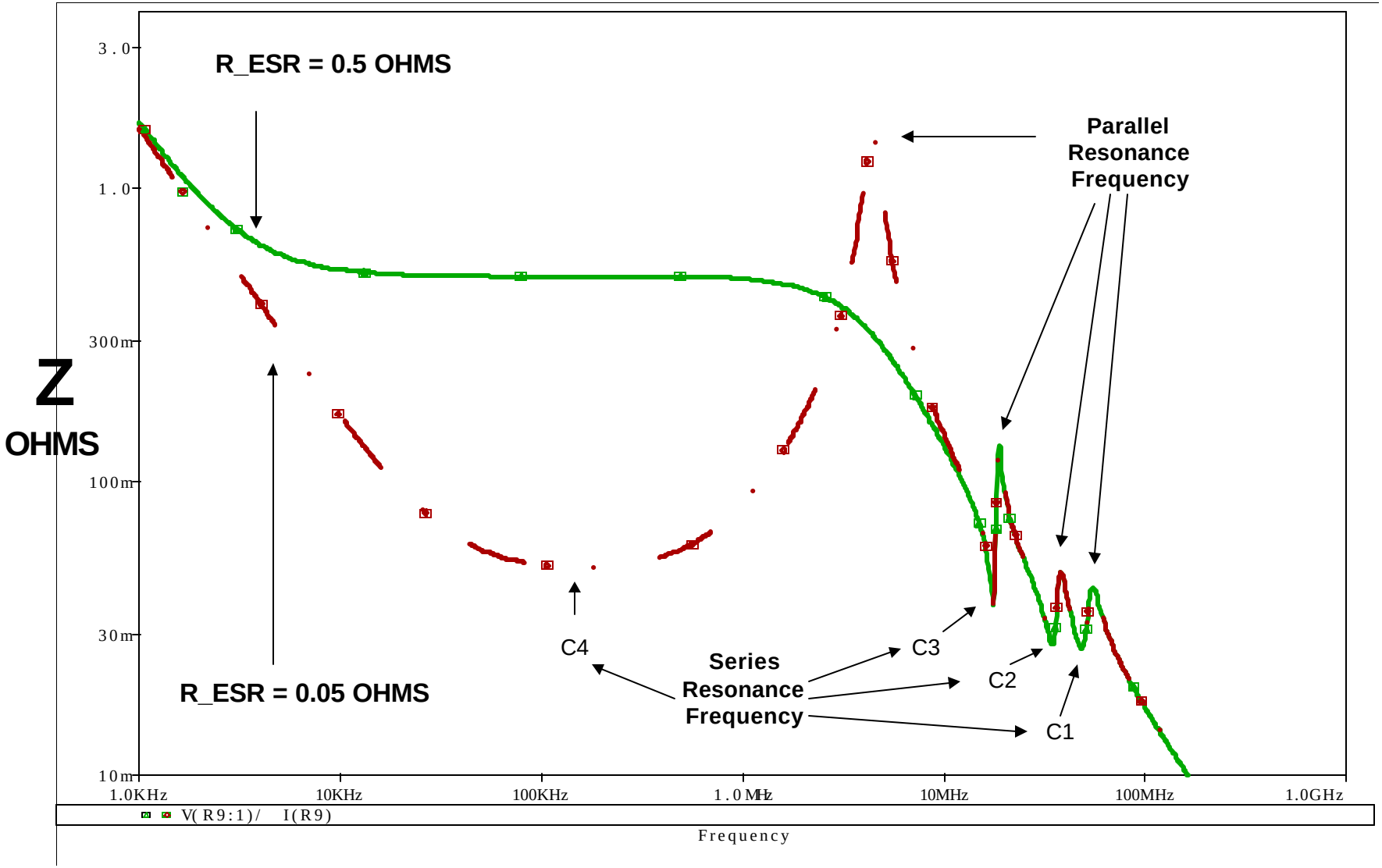
Impedance VS Frequency of Real capacitor model



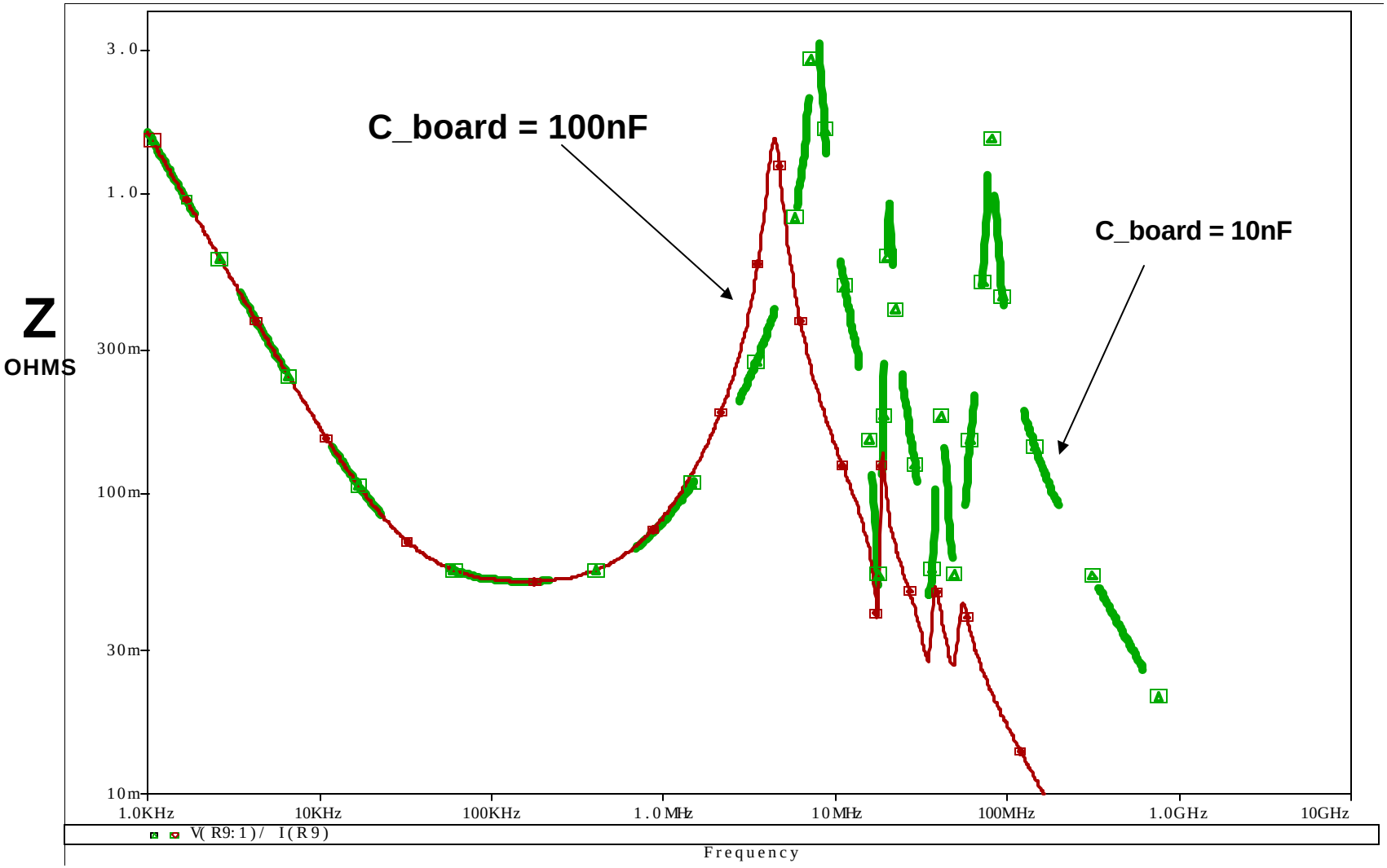
Decoupling and Board Capacitors



Impedance Response of Decoupling and Board Capacitance



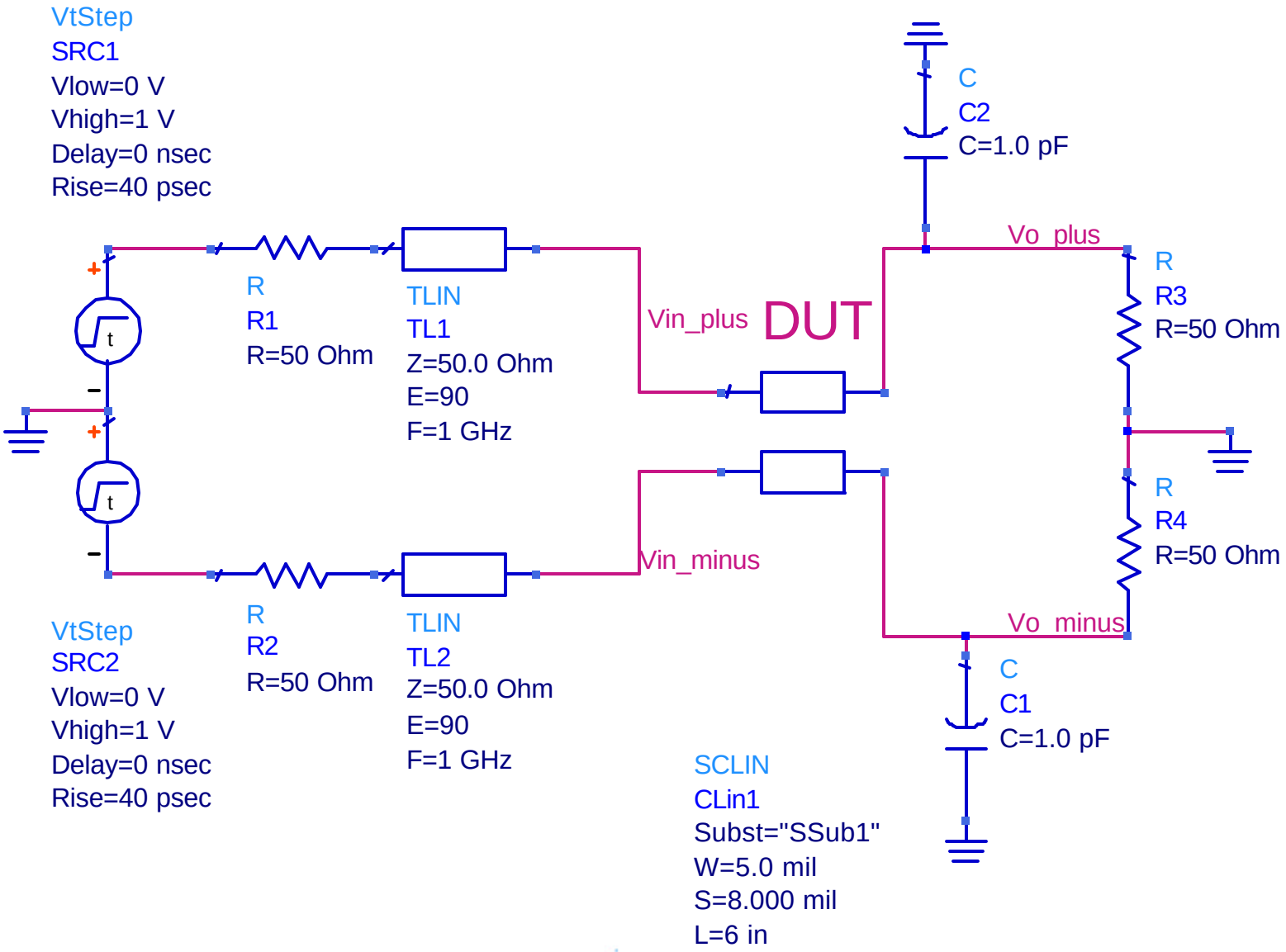
Impedance Response of Decoupling and Board Capacitance



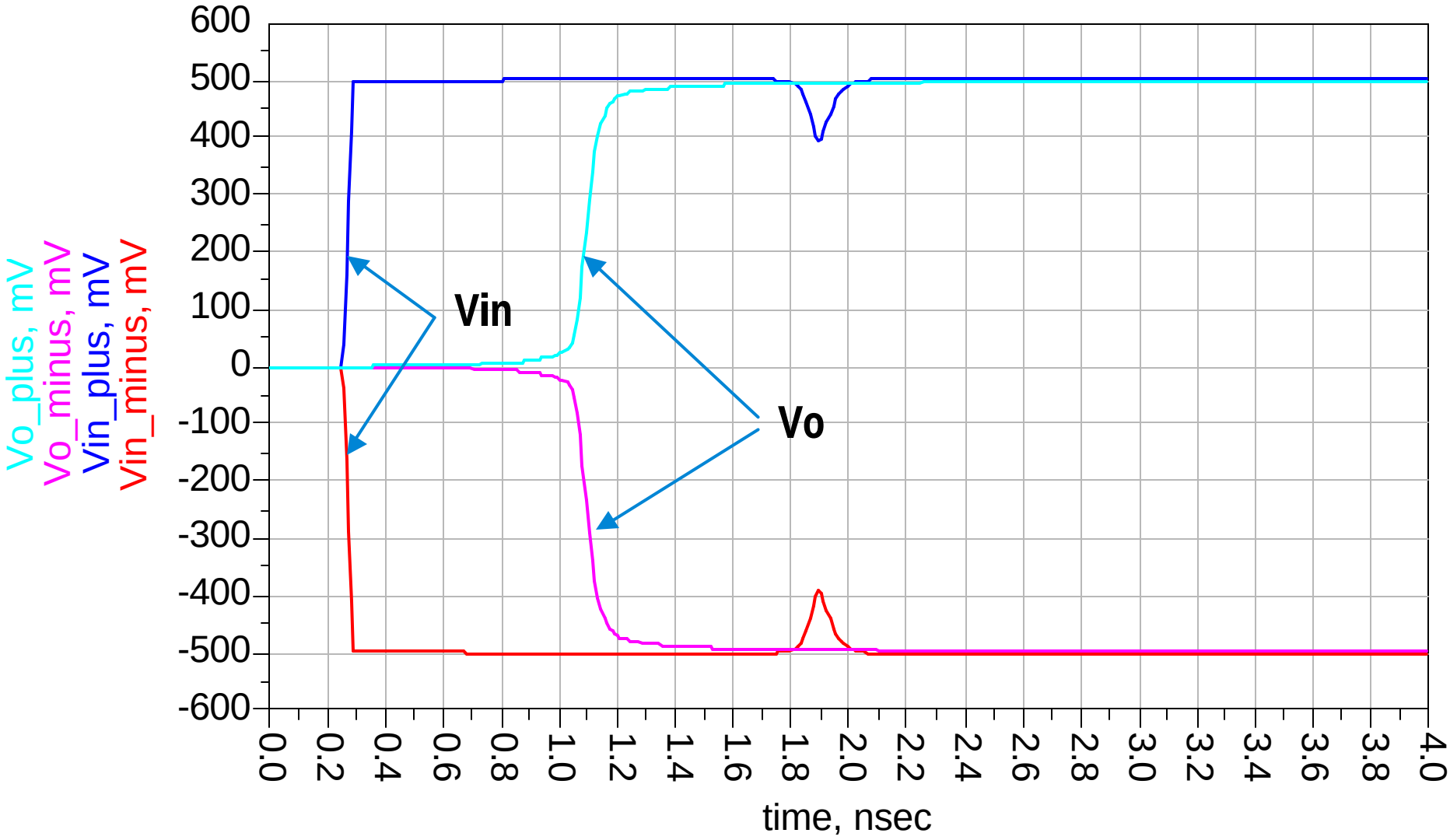
Differential pairs on PCB

- Not very good in common mode rejection with local cross talk.
  - Coupling about 20% to 50%
- Match to an external balanced differential transmission medium.
- Defeat Ground Bounce
- Improve routability
  - Can be pushed very closed together to save board space.
    - Compensate for differential impedance
    - Once signals are paired, they can not be separated without messing up the impedance.

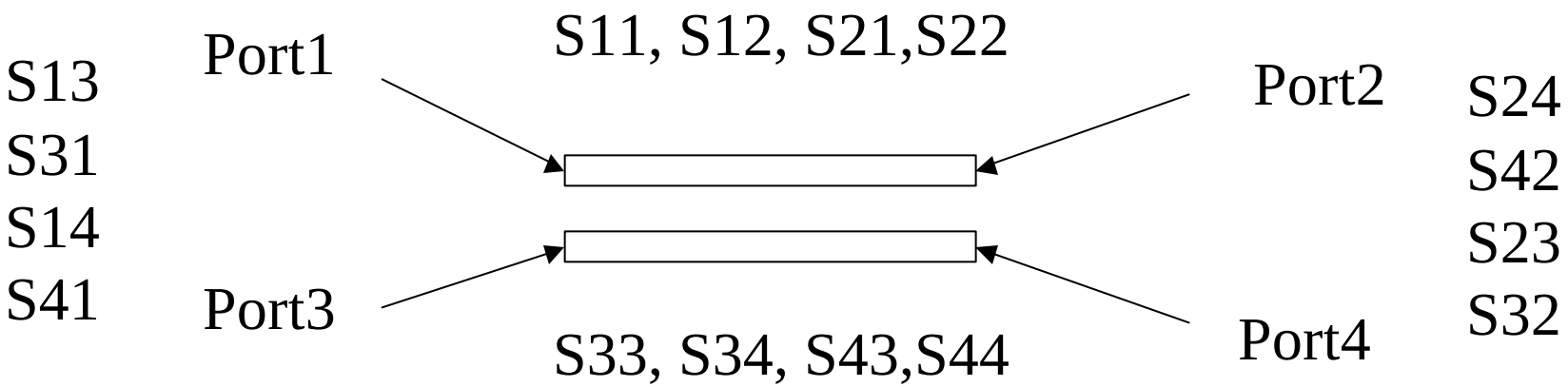
TDR Differential Measurement



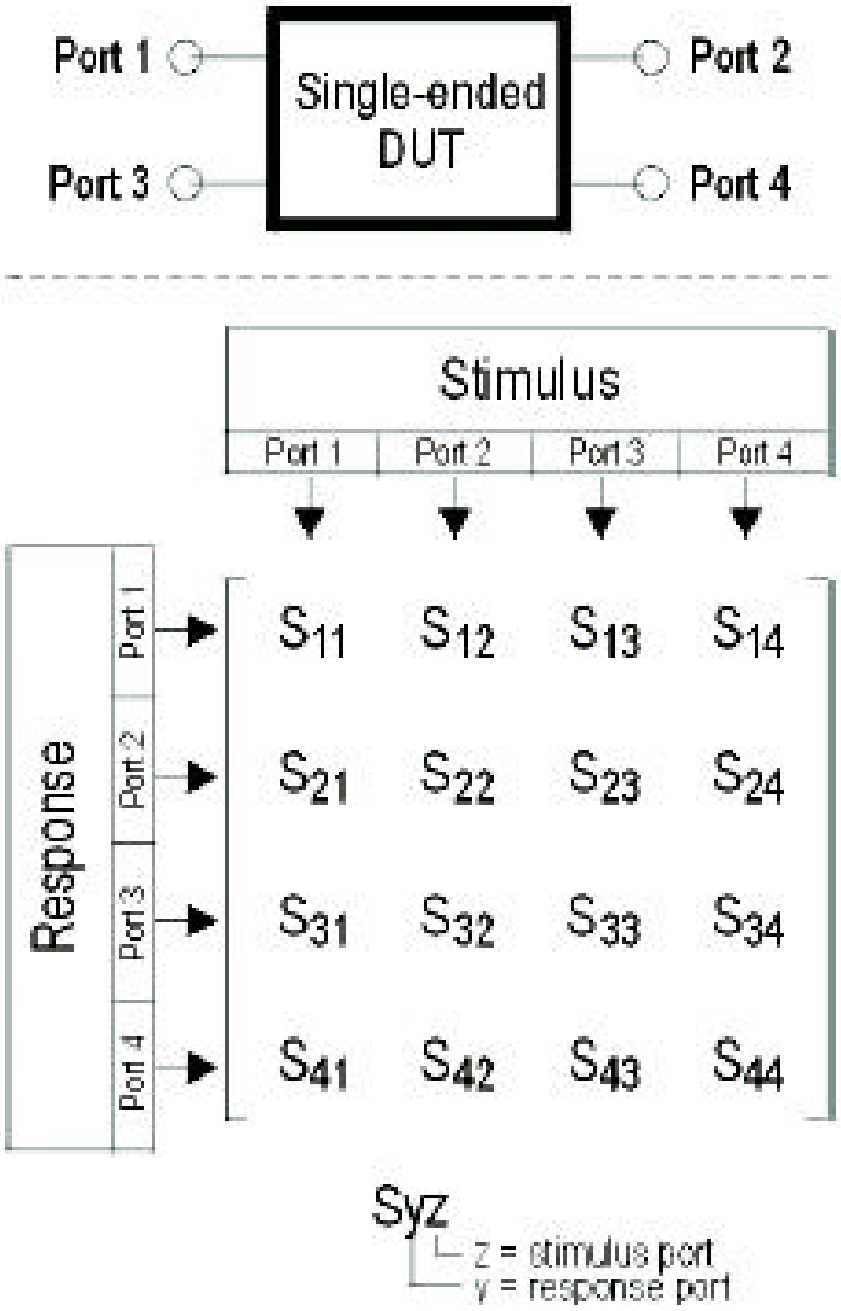
TDR Differential Waveforms



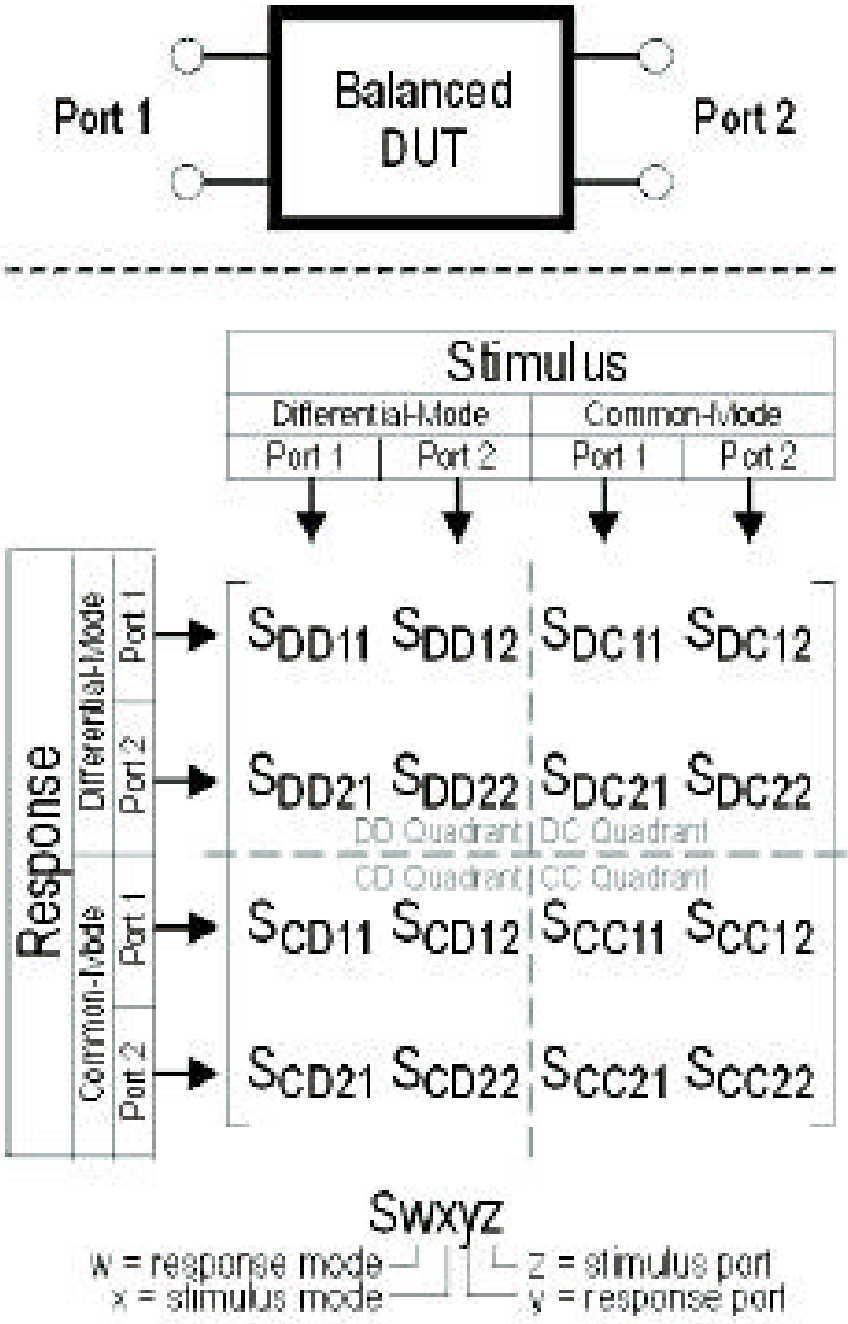
4 Port single ended to differential S parameters



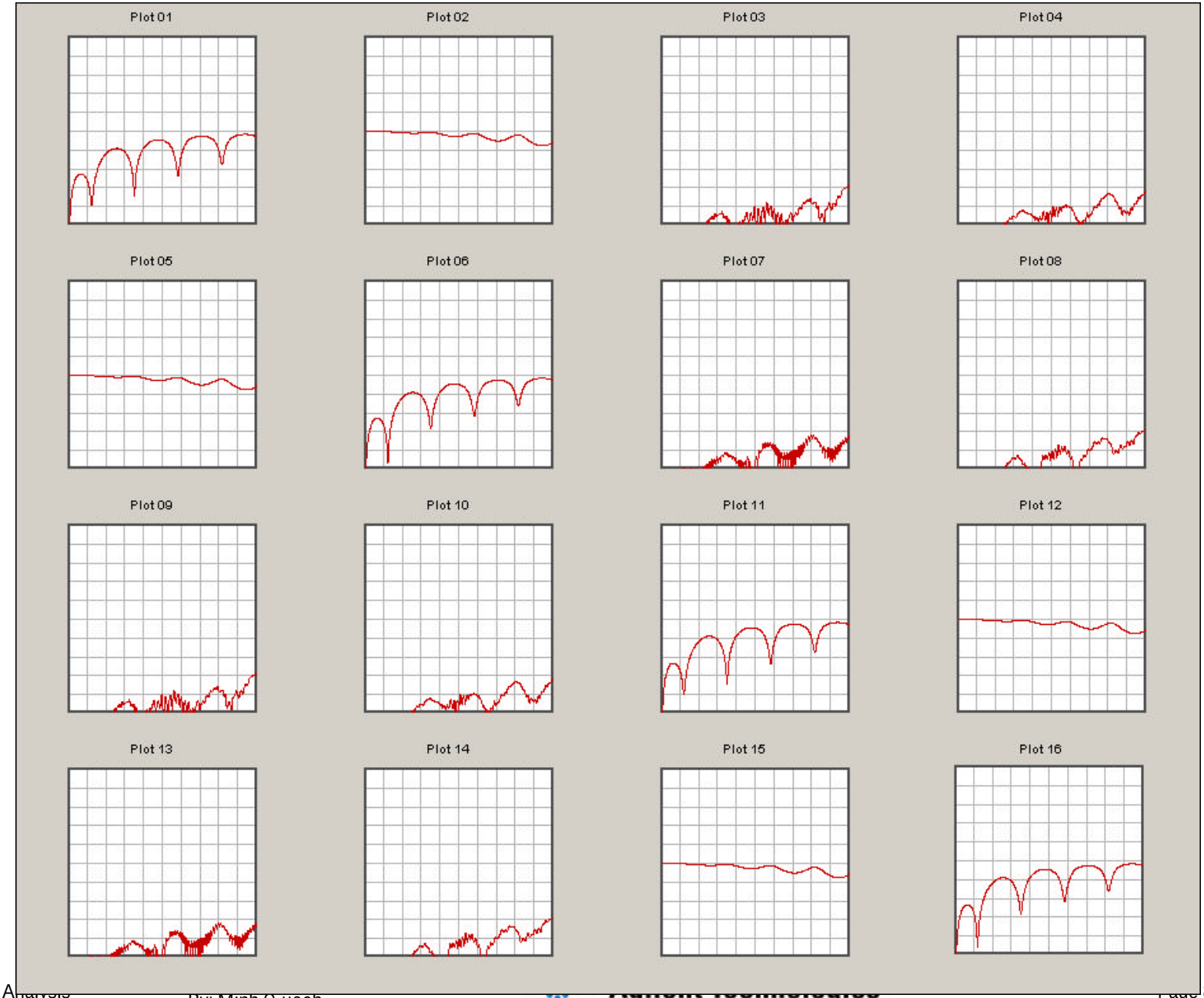
4 Ports single ended S parameters



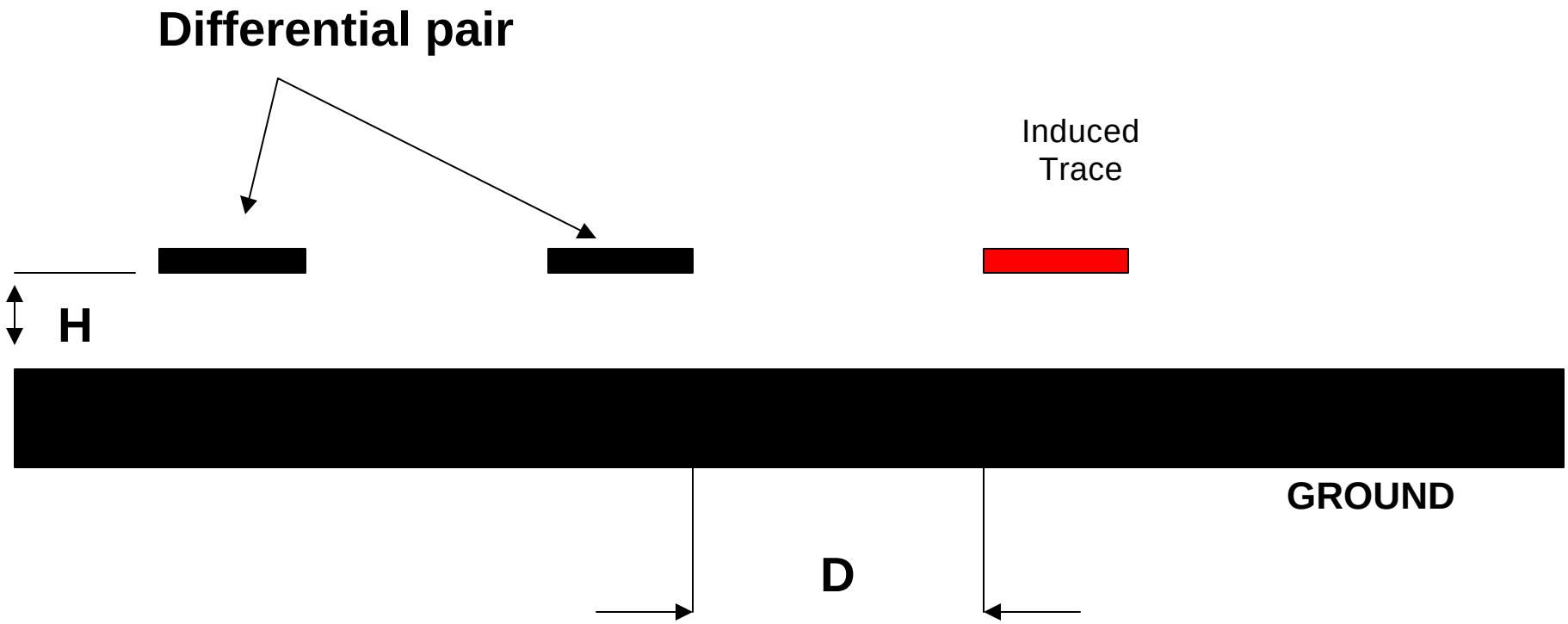
2 Balanced Mode S parameters



Differential S parameters 10mils 2in

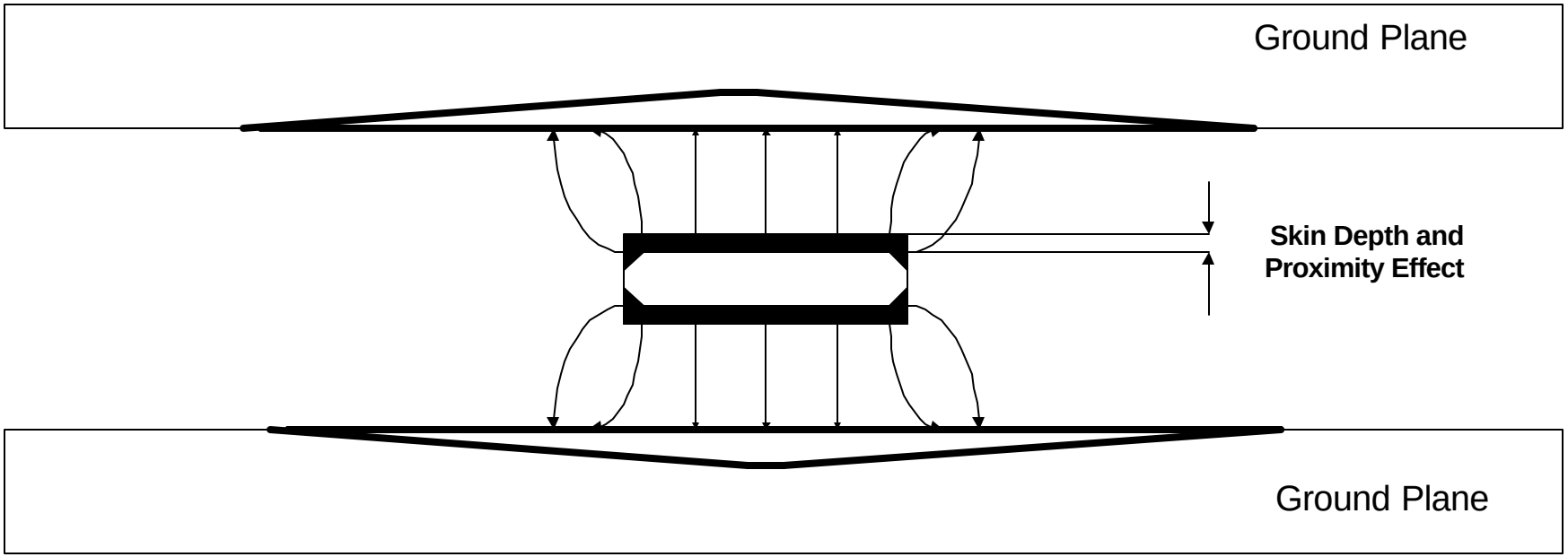


Poor Common Mode Rejection for PCB differential Pair

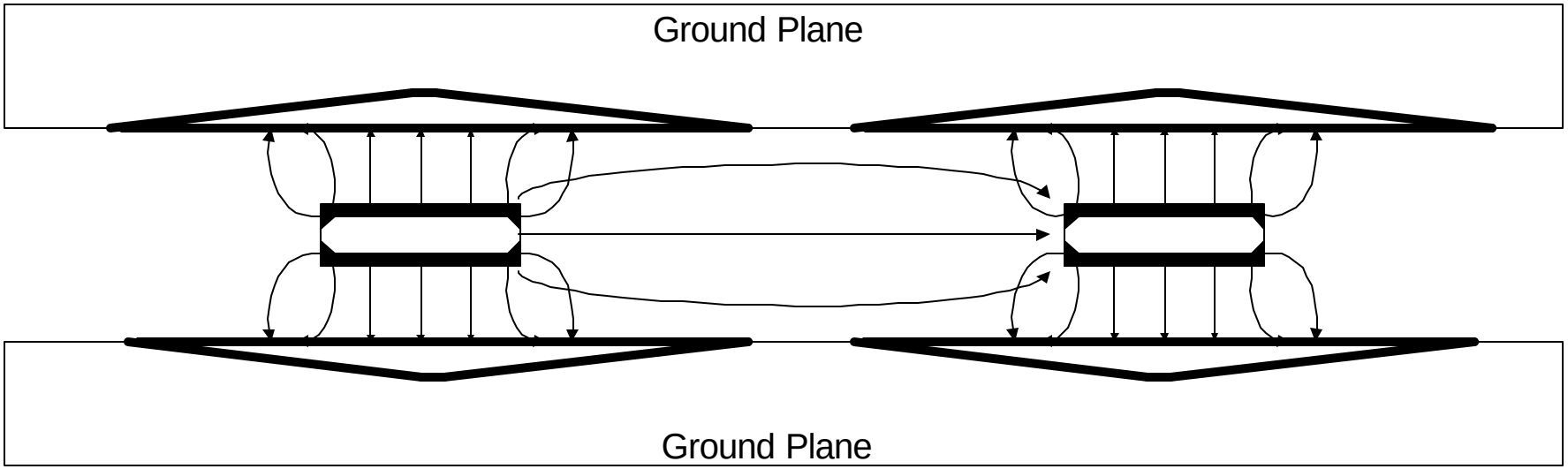


$$\text{Crosstalk} = \frac{K}{1+(D/H)^2}$$; Where K is always less than 1

Proximity Effect

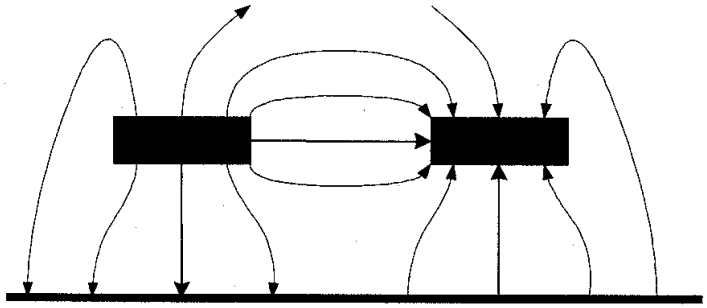


Proximity Effect (Cont)



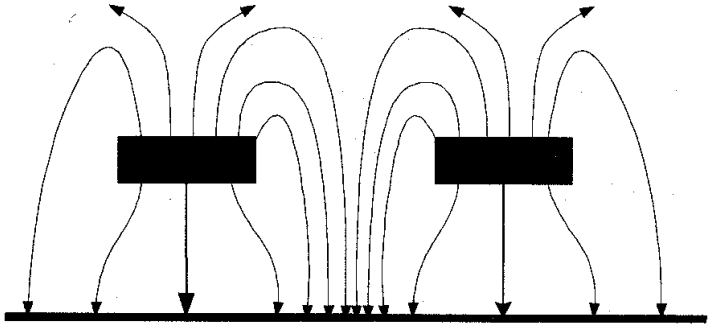
Odd and Even mode characteristic impedance

C increases



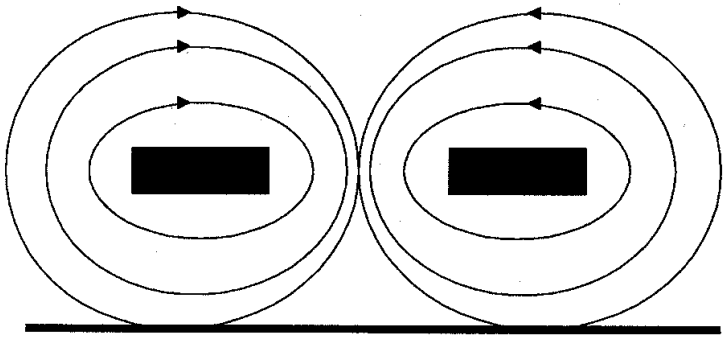
Electric field: Odd mode

C decreases

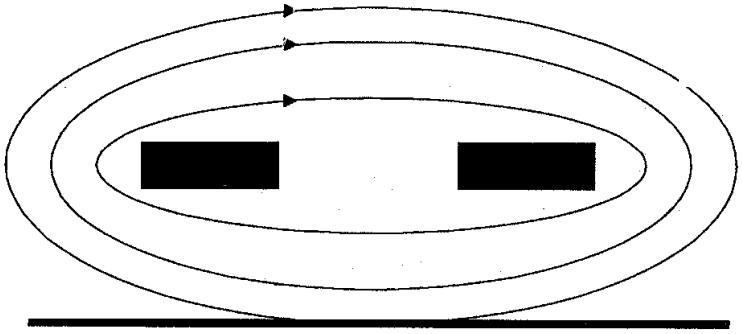


Electric field: Even mode

$$Z_o = \sqrt{\frac{L_c}{C_c}}$$



Magnetic field: Odd mode



Magnetic field: Even mode

L decreases

L increases

Impedance of Differential Pair

$$Z_{odd} = \sqrt{\frac{L_{self} - L_m}{C_{self} + C_m}}$$

$$Z_{even} = \sqrt{\frac{L_{self} + L_m}{C_{self} - C_m}}$$

$$t_{odd} = \sqrt{(L_{self} - L_m)(C_{self} + C_m)}$$

$$t_{even} = \sqrt{(L_{self} + L_m)(C_{self} - C_m)}$$

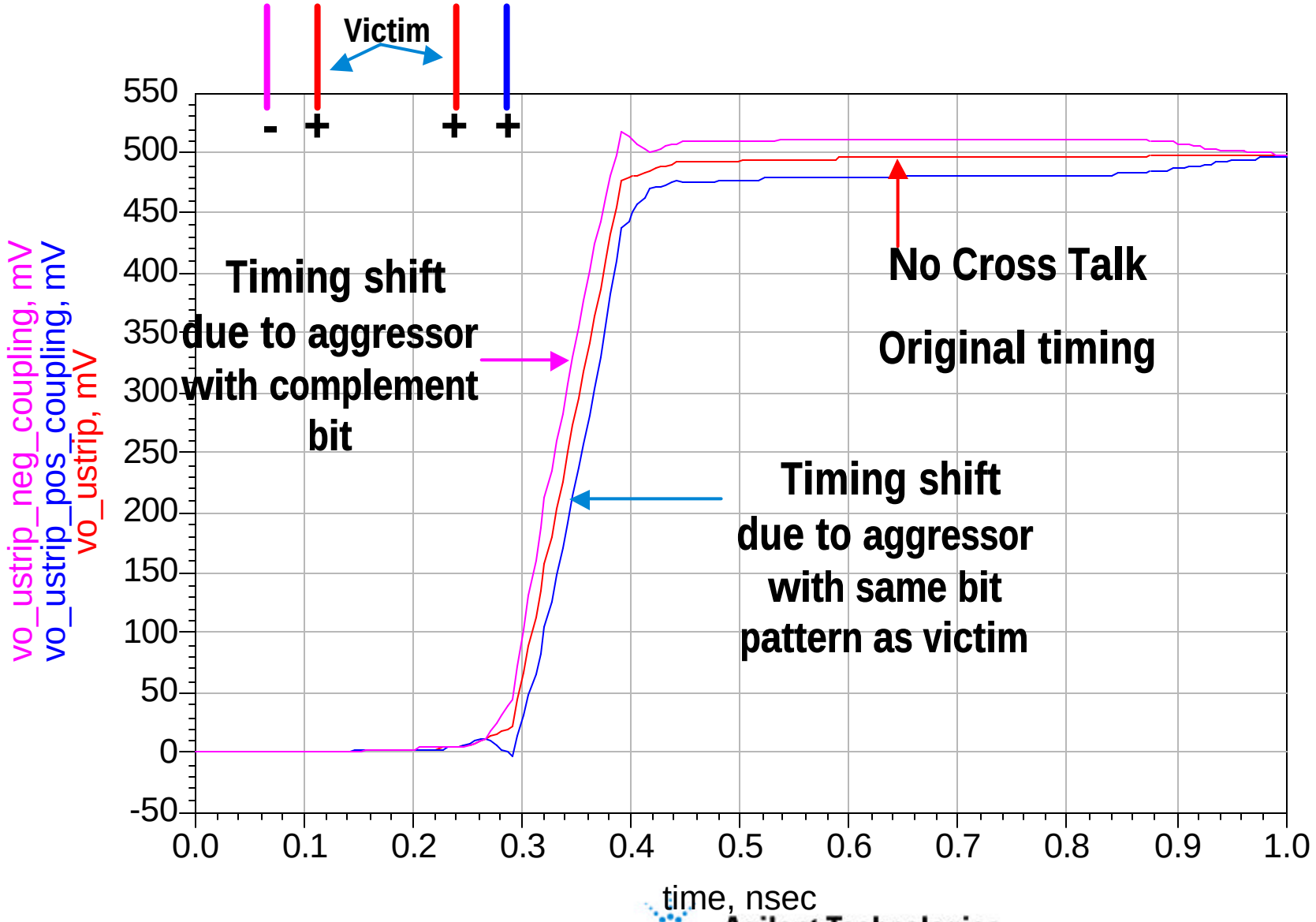
$Z_{odd} =< Zo$

$Z_{diff} = 2 * Z_{odd}$

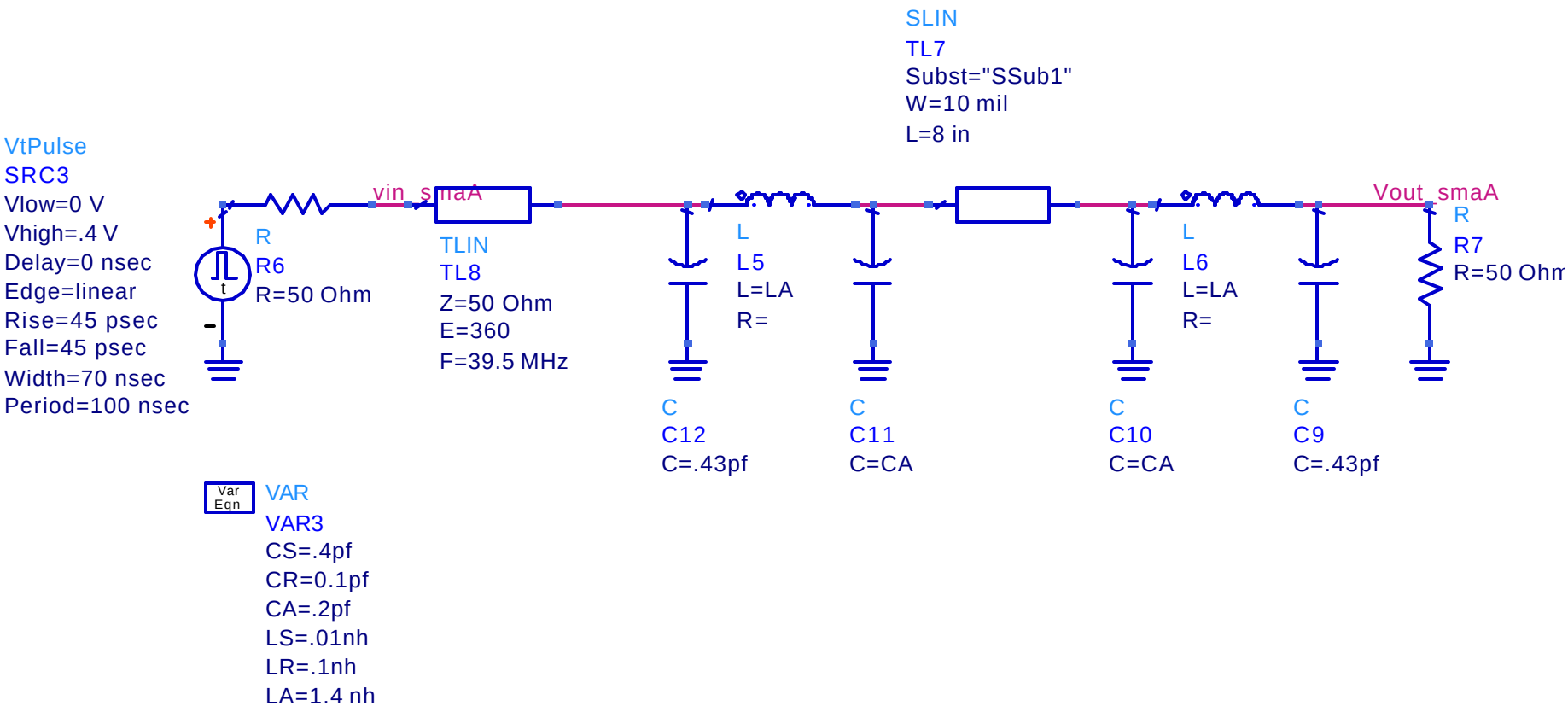
$Z_{even} >= Zo$

$Z_{common} = 1/2\ Z_{even}$

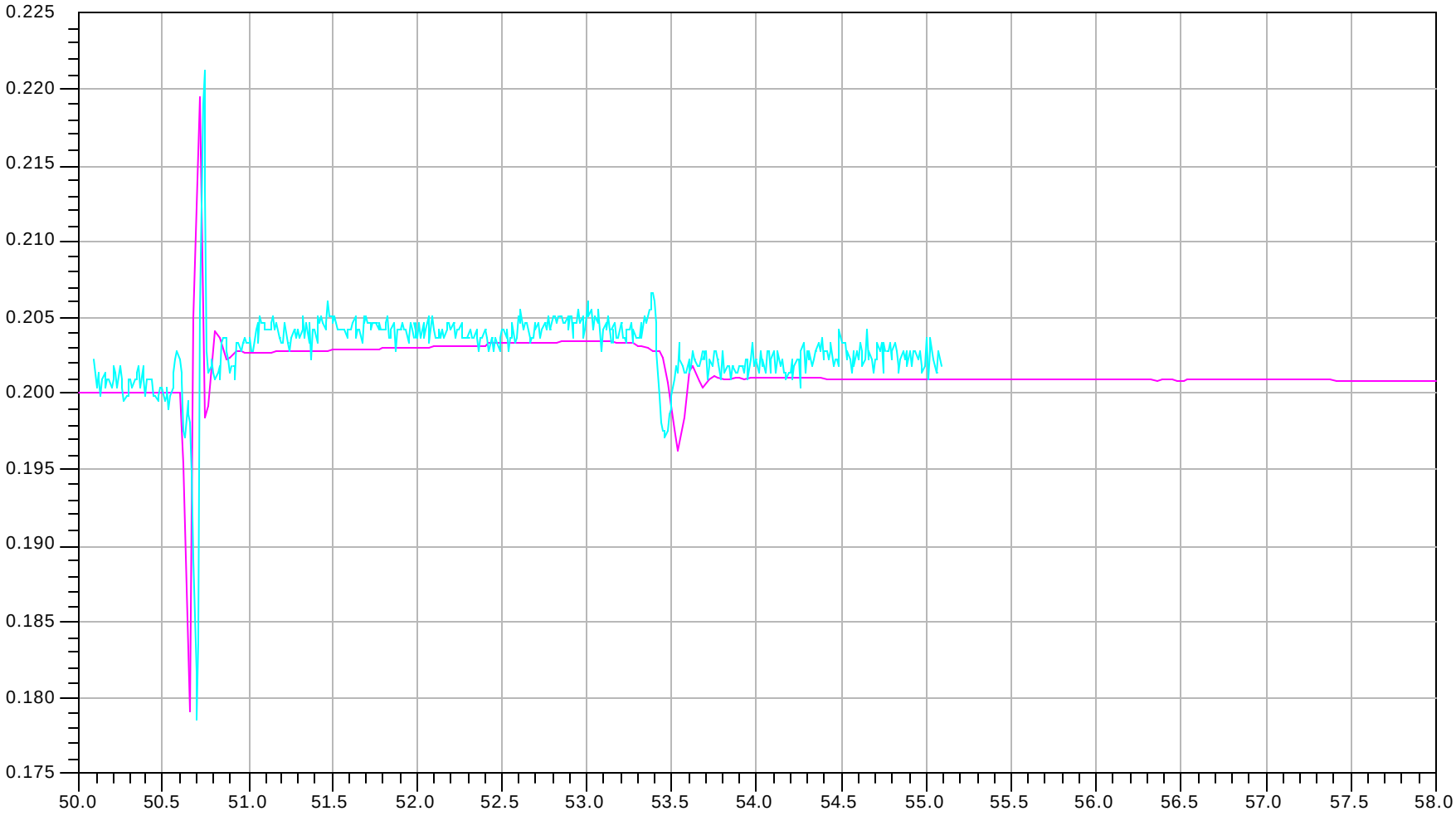
Cross Talk Between PCB Traces Causing Shift in Propagation Delay



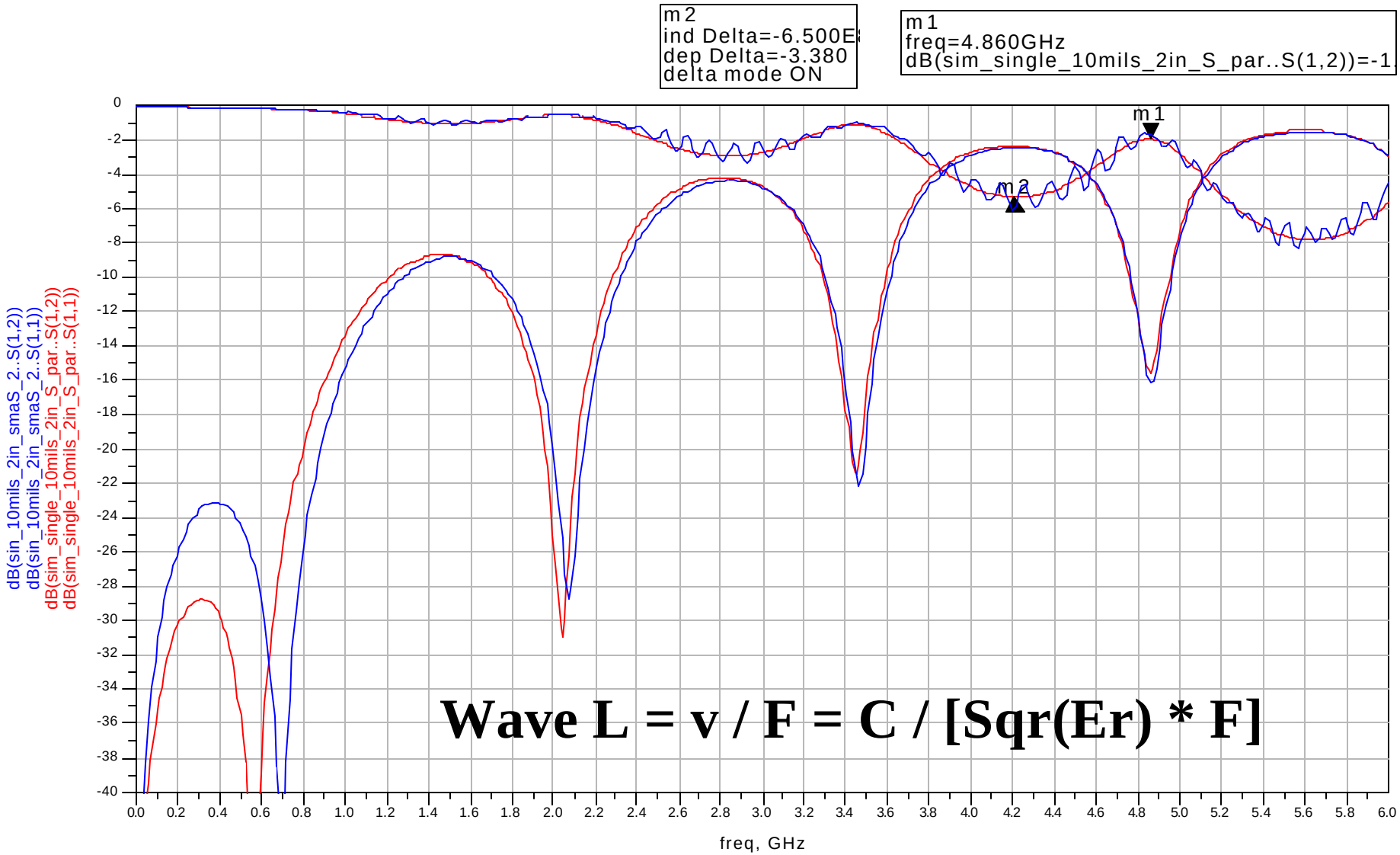
Modeling Circuit



Modeling: TDR simulation VS. Measurement



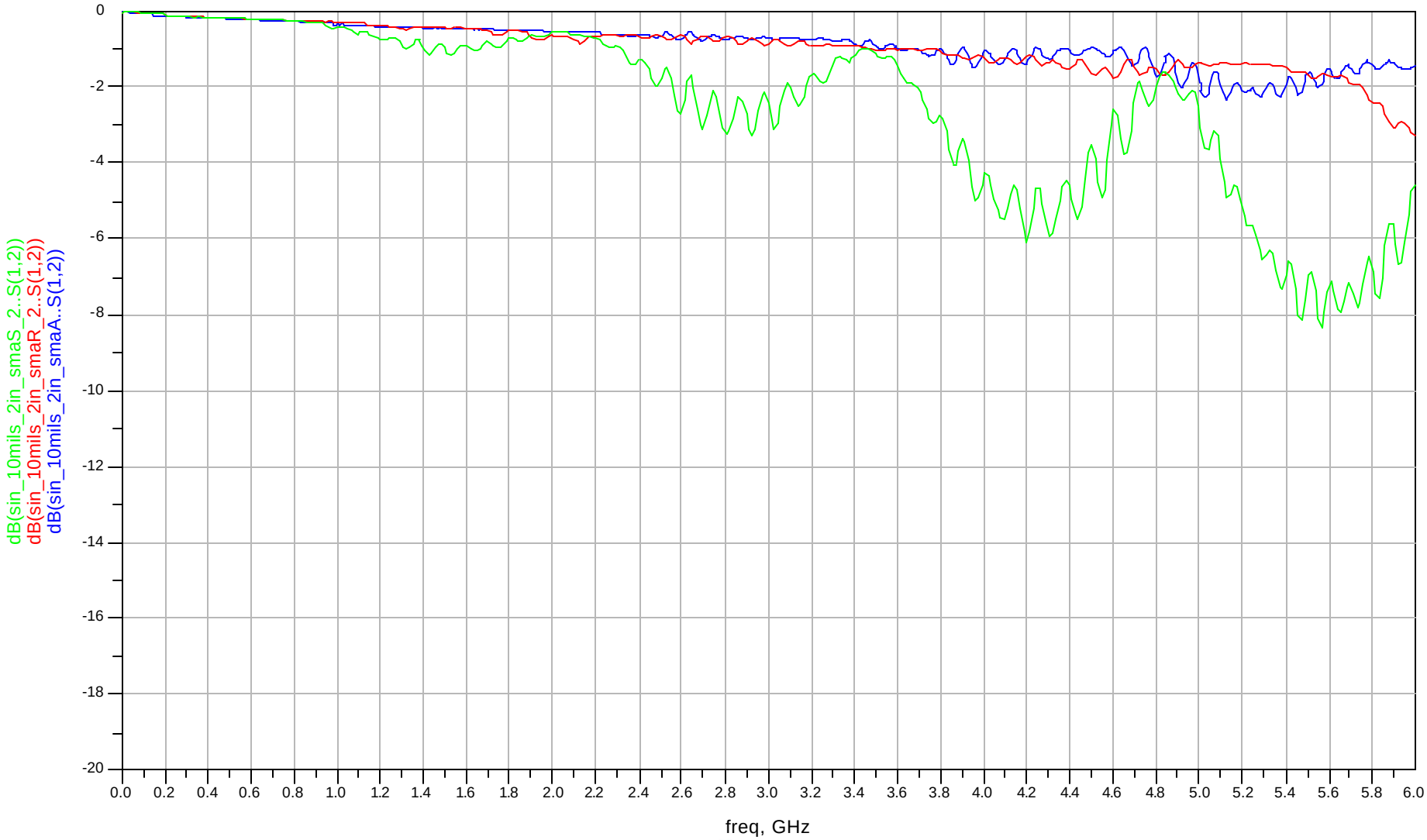
Simulation and measurements of S11 and S12 of w=10mils and L=2in; standard sma



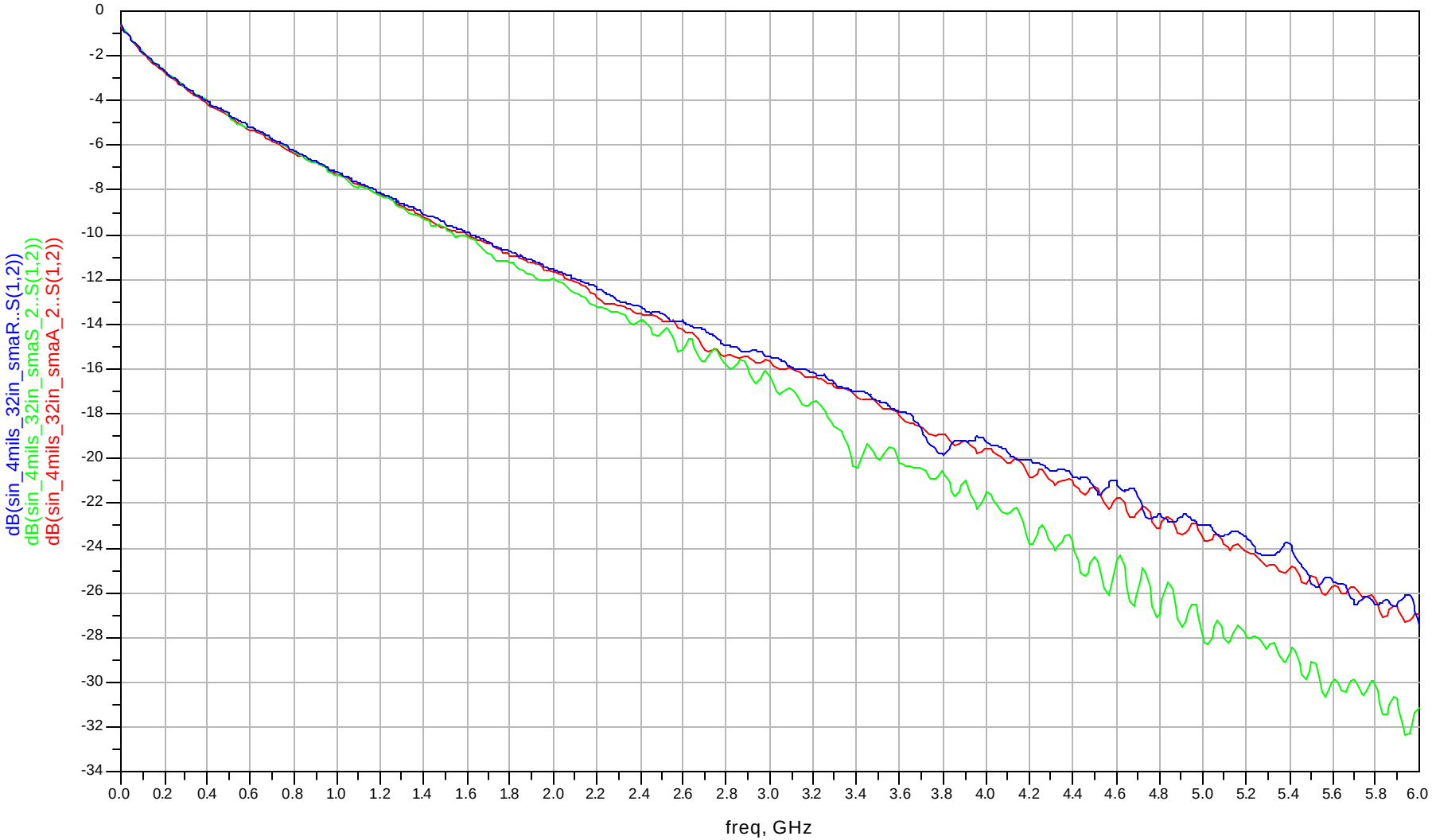
Critical Interconnect Components
Which one is important ?

- PCB via
- Connectors and Cable Connectors
- Socket
- Probe tips
- Packages and Multichip modules
- PCB trace
  - Single Run
  - Differential Run

S12 of 10mils width and 2in length of 3 types of sma connectors



S12 of 4mils width and 32in length of 3 types of sma connectors



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