Minh Quach.
Signal Integrity Consideration and Analysis
4/30/2004

Frequency & Time Domain Measurements/Analysis
Outline

• Three Measurement Methodologies
  - Direct
  - TDR (Time Domain Reflectometry)
  - VNA (Vector Network Analyzer)

• Fundamental Transmission line & TDR Theory
  - Lossless and lossy line
  - Filter Rise Time calculation
  - Bandwidth Interpretation
Outline (Cont)

• **Signal Integrity**
  - Ground Bounce
  - Inadequate power bus decoupling
  - Dispersion
  - AC loss (skin effect and dielectric loss)
  - Cross Talk

• **Differential Pair**
  - Common & Differential Mode
  - Even & Odd Mode
Interconnect

V1Step
SRC 4
Vlow=0 V
Vhigh=1 V
Delay=0 nsec
Rise=1 nsec

R
R=50 Ohm

L
L=0.01 nH
C
C=0.3 pF

SLIN
TL9
Subst="SSub2"
W=10.0 mil
L=6 in

L
L=0.01 nH
C
C=0.3 pF

SLIN
TL10
Subst="SSub2"
W=10.000 mil
L=3 in

L
L=4.34 nH

R
R=50 kOhm
Measurement Methods

- Direct Measurement
- TDR (Time Domain Reflectometry, Time Domain)
- VNA (Vector Network Analyzer, Frequency Domain)
Measurement Method

DUT

Incident Wave $V_{inc}$

Transmitted Signal TDT

Reflected Signal TDR

Load ZLoad
Direct Measurements

SCOPE

sma cable and tester fixture

POGO Tower

Probe Card

SOURCE IN

Solder at tip of probe card
Freq = 100 MHz
Freq = 200 MHz
Freq = 400 MHz
Fundamental Differences Between Analog and Digital in Interconnect Applications

Analog

- Impedance Matching for max power transfer
- Frequency Domain
- VNA
- Amplitude loss
- Frequency

Digital

- Impedance Matching to minimize signal distortion
- Time Domain
- TDR
- Edge timing degradation
- Edge rate and frequency
Using the Reflected Waveform to Construct the Spice Model

Direct Measurement

TDR (Time Domain Reflectometry, Time Domain) Using the Reflected Waveform to construct the spice model

Using ADS (Advanced Design Software)

Transmission Line Theory

VNA (Vector Network Analyzer, Frequency Domain)
Lump or Distributed

**LUMPED**

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>A capacitor - sometimes</td>
</tr>
<tr>
<td>L</td>
<td>An inductor - sometimes</td>
</tr>
</tbody>
</table>

**V, I RELATIONSHIPS:**

\[
V = L \frac{\Delta i}{\Delta t} \quad i = C \frac{\Delta v}{\Delta t}
\]

**DISTRIBUTED**

\[
\frac{\Delta L}{\Delta C} = \frac{\Delta C}{\Delta C} = \frac{\Delta C}{\Delta C}
\]

**V, I RELATIONSHIPS:**

\[
\frac{V_I}{I_I} = \sqrt{\frac{\Delta L}{\Delta C}} = Z_0
\]

\[
V_{TOTAL} = V_I + \sum (V_{RR} + V_{RI})
\]
Lump or Distributed

Lump Parameter if: \( T_{\text{rise}} > T_{\text{prop delay}} \times 6 \)
High Frequency Socket Model in Lump Parameters Valid up to 7GHz

\[
\begin{align*}
L_1 &= 0.80 \, \text{nH} \\
L_2 &= 0.10 \, \text{nH} \\
L_3 &= 0.10 \, \text{nH} \\
R_1 &= 300 \, \text{Ohm} \\
C_1 &= 0.170 \, \text{pF} \\
C_2 &= 0.170 \, \text{pF} \\
R_4 &= 0 \, \text{Ohm}
\end{align*}
\]
What is a transmission line

- A transmission line is any pair of conductor that are used to move electromagnetic energy from one place to another.
- In printed circuit boards, this is typically a trace and one or more power planes.
- Power lines are transmission lines.
- Coaxial cable is a transmission lines.
- Twisted pairs are transmission lines.
- Electromagnetic waves are moving in a transmission line not electron
Characteristic Impedance Zo

\[ V = (R + jWL)I \quad \text{Short circuit} \]
\[ I = (G + jWC)V \quad \text{Open circuit} \]

For Low Loss

\[ Zo = \sqrt{\frac{(R + jWL)}{(G + jWC)}} \]

\[ \sqrt{\frac{L}{C}} \]
Transmission Line Fundamental Software
Time Domain Reflectometry (TDR)
Transmission Line Basic

Interconnect Analysis
30 April 2004
By: Minh Q.uach

Agilent Technologies

\[ \rho = \frac{V_{\text{reflected}}}{V_{\text{incident}}} = \frac{Z_{\text{load}} - Z_0}{Z_{\text{load}} + Z_0} \]

\[ V_{\text{reflected}} = V_{\text{incident}} \cdot \rho \]

\[ Z_{DUT} = Z_0 \cdot \frac{1 + \rho}{1 - \rho} = Z_0 \cdot \frac{V_{\text{incident}} + V_{\text{reflected}}}{V_{\text{incident}} - V_{\text{reflected}}} = Z_0 \cdot \frac{V_{\text{measured}}}{2 \cdot V_{\text{incident}} - V_{\text{measured}}} \]
Discontinuity Examples

Shunt C discontinuity

\[ \frac{1}{2} \text{ V} \quad \downarrow \quad \text{Z}_0 \quad \text{Z}_0 \]

Series L discontinuity

\[ \frac{1}{2} \text{ V} \quad \downarrow \quad \text{Z}_0 \quad \text{Z}_0 \]

L-C discontinuity

\[ \frac{1}{2} \text{ V} \quad \downarrow \quad \text{Z}_0 \quad \text{Z}_0 \]

C-L discontinuity

\[ \frac{1}{2} \text{ V} \quad \downarrow \quad \text{Z}_0 \quad \text{Z}_0 \]
Discontinuity Examples

L-C-L discontinuity

Capacitive termination

Inductive termination
Reflection Response is a function of System Rise Time
Impedance Profile

$Z_1$ $Z_2$ $Z_3$

Propagation
TDR responses different due to lossy line

![Graph showing TDR responses with SMA connectors and PCB connections.](image-url)
Filter Rise Time Calculation

\[ T_{\text{risetime}} = 2.2 \ T_c = 2.2 \ RC \]

Rise time of RC filter

\[ T_{\text{risetime}} = 2.2 \ T_c = 2.2 \ \frac{L}{R} \]

Rise time of RL filter

\[ T_{\text{risetime}} = 3.4 \ (LC)^{\frac{1}{2}} \]

Rise time of LC filter
Filter Rise Time Calculation (cont)

C = 0.5pF   R=50

\[ T_{\text{rise composite}} = \left( T_{\text{in}}^2 + T_{\text{filter}}^2 \right)^{1/2} \]

\[ T_{\text{rise composite}} = 403.8 \, \text{pS} \quad T_{\text{rise composite}} = 400.9 \, \text{pS} \]

Tr in = 400ps   Tr filter = 2.2 X 50 X 0.5 pf = 55pS   Tr filter = 2.2 X 25 X 0.5 pf = 27.5pS
\[ T_{\text{risetime}} = 2.2 \ T_c = 2.2 \ \frac{R}{C} \]
\[ R = \frac{Z_0}{2} \]

\[ T_{\text{risetime}} = 2.2 \ T_c = 2.2 \ \frac{L}{R} \]
\[ R = 2 \times Z_0 \]
Filter Rise Time Calculation (cont)

\[ C = 0.5\text{pF} \quad R = 50 \]

\[ T_{\text{rise composite}} = \left( T_{\text{in}}^2 + T_{\text{filter}}^2 + T_{\text{scope}}^2 \right)^{1/2} \]

\[ T_{\text{rise composite}} = 403.8\text{pS} \quad \text{Output of filter} \]

\[ T_{\text{rise composite}} = \left( T_{\text{in}}^2 + T_{\text{filter}}^2 + T_{\text{scope}}^2 \right)^{1/2} \]

\[ T_{\text{rise composite}} = 421\text{pS} \quad \text{Scope Display} \]

Note: \( T_r = \frac{k}{B W_{3\text{db}}} \)

Where: \( k \) from 0.338 to 0.35 for gaussian pulse and single pole exponential decay respectively

Note: \( T_r = \frac{k}{B W_{\text{rms}}} \)

Where: \( k \) from 0.36 to 0.549 for gaussian pulse and single pole exponential decay respectively
Transmitted Rise Time of 2 different type of SMA cables

\[ y = 0.032x^2 \]

\[ T_{\text{risetime}} = K \times L^2 \]

Transmitted Rise Time of 2 different type SMA cables

Rise Time in ps vs Cable Length in inches

- 20GHZ BW SMA cable
- Low BW SMA cable
Cable Length VS Rise Time of high BW sma cable. Using Reflected Signal to Predict Transmitted Signal

Rise Time VS SMA (18GHZ Bandwidth) Cable Length

\[ \text{Tr} = KL^2; \text{Reflect signal travels twice as the distance on the same cable (2L);} \]

\[ \text{Reflect rise time} / \text{Transmit rise time} = 4 \]

\[ \text{TR}=0.016L^2 \]

\[ \text{TR}=0.004L^2 \]

\[ \text{Tr} = K*L^2 \]

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TDR indicates a large Capacitor presents at the load causing rise time to degrade to 5ns
Q/ A
When Speed or Wire/Net length are important

- The edge rate (rise or fall time) of a signal is fast enough that the signal can change from one logic state to the other less time than it takes the signal to travel the length of the wire/net.

- Example: Rise time = 1ns, pcb trace length = 6 inch.
  \[ v = \frac{\text{6 inch}}{\text{ns}} \]

- Overshoot and undershoot begins to show at \( \frac{1}{4} \) of this length (1.5 inch).
When should impedance be controlled

- When the length of the transmission line exceeds $\frac{1}{4}$ of the transition electrical length ($TEL = Tr \times Velocity$)

- $Tr = 1\text{ns}$, $Velocity = 6\text{ inch/ns}$; $TEL = 6\text{ “}$

And

- When reflections may cause malfunction from:
  - Overshoot or undershoot and
  - The logic technology support termination
Reflection causes by un-proper termination with fast rise time

Rise time=0.5ns  
Period=10ns

(6” FR4 PCB)

t_{prop} = 1ns

Rise time=25ns  
Period=100ns
Reflection at Vo cause by Electrical length is longer than rise time without proper termination

\[ L > \frac{1}{4} \text{ TEL} \]

\[ L < \frac{1}{4} \text{ TEL} \]
Frequency/ VNA VS. Time Domain/ TDR/ Scope

**Frequency Domain**

- Steady state
- Narrow Bandwidth
- Better dynamic range
- More accurate
- Calibrate out fixture
- Can convert to time domain
- Data analysis more insightful
- Require calibration
- Longer to setup
- For lump parameter

**Time Domain**

- Transition Analysis
- Large Bandwidth
- Faster setup
- Less expensive/ more common
- Direct representation
- For long transmission line
Square wave composition

\[ f(t) = \frac{2}{3.14} \sum \left( \frac{1}{n} \sin(2 \times 3.14 \times F \times t \times n) \right) \]

Where \( n \) is 1, 3, … etc (odd number)
S parameter Definition

\[ S_{11} = \frac{V_{\text{ref},1}}{V_{\text{inc},1}}; \quad S_{11\text{db}} = 20 \log \left( \frac{V_{\text{ref},1}}{V_{\text{inc},1}} \right) \]

\[ S_{21} = \frac{V_{\text{port}2}}{V_{\text{port}1}}; \quad S_{21\text{db}} = 20 \log \left( \frac{V_{\text{port}2}}{V_{\text{port}1}} \right) \]

For passive DUT (linear system)

\[ S_{22} = S_{11}; \quad S_{12} = S_{21} \]
Edge Rate VS Frequency

$Tr = \frac{0.35}{F_{3db}}$
Bandwidth Selection

Rise Time

Frequency

\[ \text{BW}_{\text{rise time}} = \frac{0.35}{\text{Tr}} \]

\[ \text{BW1}_{\text{system}} = 3 \times \text{BW}_{\text{rise time}} \]

\[ \text{BW2}_{\text{system}} = 6 \times \text{Frequency} \]

\[ \text{BW}_{\text{system}} = \text{MAX} (\text{BW1}, \text{BW2}) \]
Bandwidth Selection

Clock Frequency @ Rise Time Tr.

\[ BW_{rise\ time} = \frac{0.35}{Tr} \]

Interconnect BW with minimum signal distortion and loss

\[ BW_{interconnect} = \text{MAX} \left( 3 \times BW_{rise\ time}, 6 \times \text{Clock Frequency} \right) \]

400MHz frequency with:

<table>
<thead>
<tr>
<th>Rise time</th>
<th>3 X BW (_{rise\ time})</th>
<th>6 X BW (_{signal})</th>
<th>BW (_{interconn})</th>
</tr>
</thead>
<tbody>
<tr>
<td>200ps</td>
<td>5.25 GHZ</td>
<td>2.4 GHZ</td>
<td>5.25 GHZ</td>
</tr>
<tr>
<td>400ps</td>
<td>2.62 GHZ</td>
<td>2.4 GHZ</td>
<td>2.62 GHZ</td>
</tr>
<tr>
<td>800ps</td>
<td>1.31 GHZ</td>
<td>2.4 GHZ</td>
<td>2.4 GHZ</td>
</tr>
</tbody>
</table>
Bandwidth Selection

Clock Frequency @ Rise Time Tr.

\[ BW_{\text{rise time}} = 0.35/\text{Tr} \]

Interconnect BW with minimum signal distortion and loss

\[ BW_{\text{interconnect}} = \text{MAX}(3 \times BW_{\text{rise time}}, 6 \times \text{Clock Frequency}) \]

Results from simulation:

\[ 3 \times BW_{\text{rise time}} \text{ causes approximately 3\% rise time degradation} \]

\[ 6 \times \text{Frequency} \text{ causes approximately 2\% amplitude loss} \]
Signal Integrity Issues

- Impedance mismatch
- Reflection
- Crosstalk
- Ground bounce
- Inadequate power bus decoupling
- Propagation delay
- Dispersion
- Loss
Signal Integrity Components

• Signal Integrity
  - Discontinuity (Connectors, via)
  - Dispersion
  - AC loss
    - Skin Effect
    - Dielectric Loss (loss tangent)
  - Ground Bounce
  - Inadequate power bus decoupling
• Differential Pair
  - Less sensitive to components above
Dispersive Loss

- Reflection at the Interface of 2 Transmission lines:
  - One cable is different loss than the other (Even the characteristics impedance is the same)
  - Reflection coefficient is not zero and also frequency dependence.

\[
\begin{align*}
Z_0 &= R \\
Z'_0 &= R + jX \\
\alpha &= 0 \quad \beta/\omega = \text{const} \\
\alpha' &= 0 \quad \beta/\omega = f(\omega)
\end{align*}
\]
AC LOSS

- **Skin Effect Loss**
- **Dielectric Loss**
Rise Time Degradation After Signal Propagates Through 5mil Width, 32” Long for the FR4 PCB

Input Rise Time = 30pS

Output Rise Time of 32in pcb = 1nS
Skin Effect

Highest inductance

Lowest inductance

Med inductance
\[
Z_0 = \sqrt{\frac{(R + jWL)}{(G + jWC)}}
\]

**Inductance is Frequency Dependent**

Internal self inductance decreases with increasing frequency. Account for this by using a complex resistance:

\[
\tilde{R}_L(f) = R_{DC} + R_{AC}\sqrt{f}(1 + i)
\]

Real part is the resistive loss, imaginary part is the frequency dependent inductance.

\[
\tilde{R}_L + j\omega L_L = (R_{DC} + R_{AC}\sqrt{f}) + j\omega\left(L + \frac{R_{AC}}{2\pi\sqrt{f}}\right)
\]
Skin Depth Limited Current Distributions

\[ \delta = \sqrt{\frac{1}{\sigma \mu_0 \mu_r f}} = 63 \mu \sqrt{\frac{1}{f}} \text{ in MHz} \]

Microstrip:
- 50 Ohm, FR4
- \( \varepsilon_r = 4.2 \)
- \( h = 38 \mu \)
- \( t = 30 \mu \text{(1 oz)} \)
- \( w = 75 \mu \)

- 30 MHz, \( \delta = 20 \mu \)
- 100 MHz, \( \delta = 6.3 \mu \)
- 1000 MHz, \( \delta = 2 \mu \)
The Practical Part: A Simple Approximation

Current on one side of signal path

\[ R_L = \frac{\rho}{t \delta W} + \frac{\rho}{\delta W} \]

\[ R_{DC} + R_{AC} \]

Current on both sides of signal path

\[ R_L = \frac{\rho}{t \delta W} + \frac{\rho}{2 \delta W} \]

Current on both sides of signal path
And return current path = 4 x w

\[ R_L = \frac{\rho}{t \delta W} + \frac{\rho}{2 \delta W} + \frac{\rho}{\delta 4W} = \frac{\rho}{t \delta W} + 0.75 \frac{\rho}{\delta W} \]

Log Frequency (Hz)

Resistance per Length (Ohms/m)

Dots are from 2D field solver
Lines are the simple models
AC Loss (Cont)

- Skin Effect Loss
- Dielectric Loss
Complex Dielectric Constant

\[ C = \varepsilon C_0 \]

\[ C_0 \] is the empty space capacitance

describe \( \varepsilon \) as complex: \( \varepsilon(\omega) = \varepsilon'(\omega) - i \varepsilon''(\omega) \)

\[ l = \frac{C}{dV}{dt} = C_0 (i\omega V)[\varepsilon(\omega)] \]

\[ l = i\omega C_0 V (\varepsilon'(\omega) + i\varepsilon''(\omega)) \]

imaginary current  real current

Dissipation Factor

Loss Tangent

\[ \tan(\delta) = \frac{\varepsilon''}{\varepsilon'} \]

The real part of the dielectric constant relates to “dielectric” or “displacement” currents.
The imaginary component of the dielectric constant relates to "resistive" or lossy currents through the capacitor.
\[ Zo = \sqrt{\frac{(R+jWL)}{(G+jWC)}} \]

**Dissipation Factor and Conductance**

\[ I = i \omega C_0 \sqrt{\varepsilon'(\omega)} + \omega C_0 \sqrt{\varepsilon''(\omega)} \]  
imaginary current

\[ I = C \frac{dV}{dt} + \frac{1}{R} V \]  
real current

\[ R = \frac{1}{\varepsilon''(\omega)} \frac{1}{\omega C_0} \]

Define conductance as: \[ I = C \frac{dV}{dt} + GV \]

\[ G = \frac{1}{R} = \varepsilon''(\omega) \omega C_0 = \omega \tan(\delta) C \]

\[ G = \frac{\sigma}{\varepsilon_0} C_0 \quad \sigma = \omega \varepsilon_0 \varepsilon'_r = \omega \varepsilon_0 \varepsilon'_r \tan(\delta) \]

*Even if \( \tan(\delta) \) is constant in frequency, \( G \) is linear in frequency*
Dielectric Loss

Loss Tangent of Various Materials

- Teflon: 0.0002
- Roger6002: 0.0012
- Getek: 0.008
- Nelco/N7000-1: 0.012
- FR4: 0.02
Skin Effect & Dielectric Loss of an FR4, 4 mils, 10mils trace width and 24 in length (ADS simulation)
Skin & Dielectric Loss of an FR4, Roger of 4mils and 10mils Width, and 24" long (ADS simulation)
2.5Gb/ s data for FR4 PCB with 4mils trace width, 24” long.

Input Signal

Output Signal

5Gb/ s

Plot 01

0.000 ns

0.795 ns

0.000 ns

0.796 ns

2.5Gb/ s

Output Signal
Compensation Circuits

Compensation circuit from ITC 2002 by Wolfram Humann, Agilent Technologies

Interconnect Analysis
30 April 2004

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S-Par of before and after compensation

Before Compensation

After Compensation

freq, GHz

dB(S(3,4))

dB(S(1,2))
Time Domain of Before and After Compensation

Vi compensation = 2 Vin

![Graph showing time domain comparison between before and after compensation](image)
5Gb/s data for FR4 PCB with 4mils trace width, 24” long.
Plot excerpt from the High-Speed Signal Propagation book, by Howard Johnson and Martin Graham.

Figure 3.2—Performance regions for a 150-μm (6-mil), 50-Ω, FR-4 stripline.
Critical Interconnect Components

- PCB via
- Connectors and Cable Connectors
- Socket
- Probe tips
- Packages and Multichip modules
- PCB trace
  - Single Run
  - Differential Run
Signal Integrity Issues

- Impedance mismatch
- Reflection
- Crosstalk
- Ground bounce
- Inadequate power bus decoupling
- Propagation delay
- Dispersion
- Loss
Ground Bounce / Power Droop

\[
\frac{\text{di/dt}}{\text{Trise}} = \frac{50\text{pF} \times 1.52 (2\text{V})}{\text{Trise}^2} = 1.52 \times 10^8 \text{ A/s}
\]

\[
\text{PS}_{\text{noise}} = L \times \frac{\text{di/dt}}{\text{Trise}} = 2n\text{H} \times 1.52 \times 10^8 \text{ A/s} = 0.3\text{V}
\]

Where: Trise = 1ns
Impedance VS Frequency of Real capacitor model

- Frequency: 1.0KHz, 10KHz, 100KHz, 1.0MHz, 10MHz, 100MHz, 1.0GHz, 10GHz
- V(R9:1)/I(R9)
- Z in OHMS

Diagram showing a circuit with components R10, L8, 0.05, 5nh, .1uf connected.
Decoupling and Board Capacitors

C1, C2, C3, and C4 are decoupling caps
Impedance Response of Decoupling and Board Capacitance

R_{ESR} = 0.5 \text{ OHMS}

R_{ESR} = 0.05 \text{ OHMS}

Parallel Resonance Frequency

Series Resonance Frequency

C1

C2

C3

C4
Impedance Response of Decoupling and Board Capacitance

- **C\_board = 100nF**
- **C\_board = 10nF**
Differential pairs on PCB

• Not very good in common mode rejection with local cross talk.
  ✤ Coupling about 20% to 50%
• Match to an external balanced differential transmission medium.
• Defeat Ground Bounce
• Improve routability
  ✤ Can be pushed very close together to save board space.
  ✤ Compensate for differential impedance
  ✤ Once signals are paired, they can not be separated without messing up the impedance.
TDR Differential Measurement

VtStep
SRC1
Vlow=0 V
Vhigh=1 V
Delay=0 nsec
Rise=40 psec

R
R1
R=50 Ohm

TLIN
TL1
Z=50.0 Ohm
E=90
F=1 GHz

R
R2
R=50 Ohm

TLIN
TL2
Z=50.0 Ohm
E=90
F=1 GHz

SCLIN
CLin1
Subst="SSub1"
W=5.0 mil
S=8.000 mil
L=6 in

R
R3
R=50 Ohm

R
R4
R=50 Ohm

C
C2
C=1.0 pF

C
C1
C=1.0 pF

VtStep
SRC2
Vlow=0 V
Vhigh=1 V
Delay=0 nsec
Rise=40 psec

R
R4
R=50 Ohm

TLIN
TL2
Z=50.0 Ohm
E=90
F=1 GHz

R
R1
R=50 Ohm

R
R2
R=50 Ohm

R
R3
R=50 Ohm

Vo_plus

Vo_minus
4 Port single ended to differential S parameters

S11, S12, S21, S22

Port 1

S13
S31
S14
S41

Port 3

S33, S34, S43, S44

Port 2

S24
S42
S23
S32

Port 4

SDD11, SDD12, SDD21, SDD22

Port 1

SCC11, SCC12, SCC21, SCC22

Port 2
4 Ports single ended S parameters
2 Balanced Mode S parameters

![Diagram of Balanced Mode S parameters]

- **Stimulus**
  - **Differential-Mode**
    - Port 1
    - Port 2
  - **Common-Mode**
    - Port 1
    - Port 2

- **Response**
  - **Differential-Mode**
    - Port 1
    - Port 2
  - **Common-Mode**
    - Port 1
    - Port 2

- **S parameters**
  - $S_{DD11}$, $S_{DD12}$, $S_{DC11}$, $S_{DC12}$
  - $S_{DD21}$, $S_{DD22}$, $S_{DC21}$, $S_{DC22}$
  - $S_{CD11}$, $S_{CD12}$, $S_{CC11}$, $S_{CC12}$
  - $S_{CD21}$, $S_{CD22}$, $S_{CC21}$, $S_{CC22}$

- **Legend**
  - $w = \text{response mode}$
  - $x = \text{stimulus mode}$
  - $z = \text{stimulus port}$
  - $v = \text{response port}$
Differential S parameters 10mils 2in
Poor Common Mode Rejection for PCB differential Pair

Differential pair

\[
\text{Crosstalk} = \frac{K}{1 + (D/H)^2} \quad \text{; Where } K \text{ is always less than 1}
\]
Proximity Effect

Skin Depth and Proximity Effect

Ground Plane

Ground Plane
Proximity Effect (Cont)
Odd and Even mode characteristic impedance

C increases

C decreases

L decreases

L increases

\[ Z_0 = \sqrt{\frac{L_c}{C_c}} \]
**Impedance of Differential Pair**

\[
Z_{\text{odd}} = \sqrt{\frac{L_{\text{self}} - L_m}{C_{\text{self}} + C_m}}
\]

\[
Z_{\text{even}} = \sqrt{\frac{L_{\text{self}} + L_m}{C_{\text{self}} - C_m}}
\]

\[
t_{\text{odd}} = \sqrt{(L_{\text{self}} - L_m)(C_{\text{self}} + C_m)}
\]

\[
t_{\text{even}} = \sqrt{(L_{\text{self}} + L_m)(C_{\text{self}} - C_m)}
\]

\[
Z_{\text{odd}} = < Z_0
\]

\[
Z_{\text{diff}} = 2 \times Z_{\text{odd}}
\]

\[
Z_{\text{even}} \geq Z_0
\]

\[
Z_{\text{common}} = \frac{1}{2} Z_{\text{even}}
\]
Cross Talk Between PCB Traces Causing Shift in Propagation Delay

Timing shift due to aggressor with complement bit

Timing shift due to aggressor with same bit pattern as victim

No Cross Talk

Original timing
Modeling Circuit

VtPulse
SRC3
Vlow=0 V
Vhigh=.4 V
Delay=0 nsec
Edge=linear
Rise=45 psec
Fall=45 psec
Width=70 nsec
Period=100 nsec

VAR
VAR3
CS=.4 pf
CR=.1 pf
CA=.2 pf
LS=.01 pf
LR=.1 pf
LA=.14 pf
Modeling: TDR simulation VS. Measurement
Simulation and measurements of S11 and S12 of w = 10mils and L = 2in; standard sma

Wave \( L = \frac{v}{F} = \frac{C}{\sqrt{Er} \times F} \)
Critical Interconnect Components
Which one is important?

- PCB via
- Connectors and Cable Connectors
- Socket
- Probe tips
- Packages and Multichip modules
- PCB trace
  - Single Run
  - Differential Run
S12 of 10mils width and 2in length of 3 types of sma connectors
S12 of 4mils width and 32in length of 3 types of sma connectors