Purpose

• Provide background:
  - Quick introduction to digital test

• Describe the problem:
  - Testing “digital” circuits that have analog issues

• Describe a solution:
  - Selective application of analog test & measurement techniques
Outline

• Digital Test 101
• Problems with Testing Today’s “Digital” Chip
• Some Solutions for Analog Test Issues
• Conclusions
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Digital Test 101: Common Test Questions

• Why test?
• What do we test?
• How are tests applied to a chip?
• What kinds of tests are there? How created?
• How good is a test?
• What upcoming test issues do we expect?
Manufacturing Isn’t Always Perfect
Missing Contacts

- Missing contacts
Open Metal Line
Why do we test ICs?

• Simply, because Yield is not 100%
• Shipping defective chips to a customer: bad idea
• \( DL = 1 - Y^{(1 - DC)} \)
  - \( DL \) is Defect Level (0 is good)
  - \( Y \) is Yield (1 is good)
  - \( DC \) is Defect Coverage (1 is good)
• Until IC Manufacturing becomes perfect, we’ll test
What Do We Test?

- What are the options?
  - Functionality
    - If chip operates correctly, it must be good
  - Structural correctness
    - If chip has no defects, it must be good
- Functional test vs. Structural test debate
- Defect-Based Test (DBT)
  - Another angle on the debate: different == bad
- Best approach: all 3, heavily biased toward structural + DBT
Structural Test: Automated Test Pattern Generation

- Circuit netlist: gate level model
- Fault model: abstracted defect behavior
  - Stuck-at: line in circuit acts permanently stuck
  - Delay: gate(s) in circuit operate too slowly
    - Transition (== Gate Delay): lumped delay
    - Path Delay: distributed delay
  - Iddq: high static current (pseudo-stuck-at)
- I/O parametric specs (freq, timing, levels, ...)
- Signal constraints

• Test patterns
• Fault coverage
• Undetected faults
What Do We Test Structurally?

- Defect-free presence of every gate
  - Logical operation
  - Connections to predecessors, successors
  - Capability of transitioning at speed
- Chip specifications
  - I/O parameters (e.g. Vol, Voh, Iol, Ioh, Vil, Vih, I1kg, Iz, Tck_q, Tsu, Th)
- Functional operation of BISTed circuits
  - RAMs, Latch Arrays, TCAMs, etc.
  - SerDes high speed I/O channels
How Are Tests Applied to a Chip?

- Traditional Tester Hardware
  - Power supplies, tester channels
  - Parametric Measurement Units
  - Stored stimulus and response data
- On-chip Design-For-Test (DFT) hardware
  - Scan flops stitched into scan chains
  - Test control signals via TAP
  - Built-In Self Test (BIST) structures
- Almost all DFT these days is built around scan
What is Scan DFT?

- Connect all flip-flops into a serial scan chain
  - Extra scan-in input for each flop
  - Q of one flop becomes scan-in of the next
  - Distribute all flops across several scan chains
- Reduce sequential test problem to combinational
- Serial shifting access is slow, but effective
Scan DFT: Original Circuit

combinational logic

D1

Q1

D2

Q2

CK
Scan DFT: Scan Circuit (mux-d)

combinational logic

D1 Q1 D2 Q2
SIN
CK
scan_enable
SOUT
FAST-lean Flip-Flop Views

DFF-based view:

Latch-based view:
FAST-lean Flip-Flop Schematic
What Kinds of Tests are There?

• Functional: some coverage of stuck-at and delay
• Scan
  - Boundary: for chip-to-chip tests on boards
  - Continuity: scan chains can shift serially
  - Static: stuck-at and lddq faults
  - Dynamic: delay faults (transition, path delay)
• BIST: for RAMs, SerDes, I/Os, Logic
• Pad parametrics: analog measurements
Scan Continuity

Serial scan shifting to verify continuity

flip-flops

logic cloud
Stuck-at Fault Testing

Combinational logic tested

source flip-flops

logic cloud

destination flip-flop
Iddq Testing

Combinational logic tested via monitoring current through VDD

VDD

logic cloud

source flip-flops
Delay Fault Testing: System Clock Launch

Transitions on functionally sensitizable paths are tested
How is a Dynamic Scan Test Applied?

Scanin | Step | Scanout

NORM
SIN
SFTMA
CK+SFTSL
SOUT
M1
S1

V1

v1 logic cloud
source flip-flops

V2

v2 logic cloud
predecessor flip-flops

edge
destination flip-flop
How Good is a Test (metrics)?

- Fault Coverage = faults detected / total faults
- Untestable faults
  - Structurally untestable
    - Tied, Blocked, Unused, Redundant
  - Structurally at-best-potentially testable
    - Clocks, resets, tristate bus enables, wired
  - Constrained: test signals
- Testable Fault Coverage = detected / (total – untestable)
- Coverage is a predictor of escape rate (the real metric)
Which Tests Work Best?

• Test Effectiveness Study (Maxwell, ITC ’00)

![Venn Diagram](image)
What are the Trends in Testing?

• Widespread usage of DFT: scan and BIST
• Widespread usage of ATPG (Automated Test Pattern Generation)
• Less usage of functional testing
• Drive to reduce the cost of test
• Cheaper testers

Risky!  Test is getting more complex!
What are Upcoming Test Challenges?

- Solidifying AC Scan tests (better fault models)
- Quantifying new defect spectra (Al bridges -> Cu voids)
- Mitigating growth of subthreshold conduction Iddq leakage
- Addressing dominance of interconnect faults over device faults
- Managing scan test length and time for multimillion transistor chips
- Testing high speed signal integrity
- Testing for layout-induced marginalities

Analog!
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I/O Parametric Test (the traditional analog test)

- Many parameters
  - Vol, Voh, Iol, Ioh, Vil, Vih, Ilkg, lz, Tck_q, Tsu, Th
- Many interfaces (CMOS, SSTL, HSTL, LVDS, many serial specs)
- Challenging specs (10Gb/s, 200mV swing, multilevel logic)
- Many pins (1000 – 2000 signal pins not uncommon)
- Few tester channels (2048 pin testers can cost almost $10M)
- Programmable values (impedance, slew rate, termination, etc.)
Driver Impedance Range
Deli ASIC Measurements

I/O Circuit

\[ R_u \]
\[ R_d \]

Measurement Data

- vector label deli_io_imp_00 resistance = 78.2882 Ohms
- vector label deli_io_imp_01 resistance = 73.4972 Ohms
- vector label deli_io_imp_02 resistance = 69.2707 Ohms
- vector label deli_io_imp_03 resistance = 65.0682 Ohms
- vector label deli_io_imp_04 resistance = 61.3653 Ohms
- vector label deli_io_imp_05 resistance = 57.677 Ohms
- vector label deli_io_imp_06 resistance = 54.4292 Ohms
- vector label deli_io_imp_07 resistance = 51.2053 Ohms
- vector label deli_io_imp_08 resistance = 48.342 Ohms
- vector label deli_io_imp_09 resistance = 45.5273 Ohms
- vector label deli_io_imp_10 resistance = 43.0223 Ohms
- vector label deli_io_imp_11 resistance = 40.5314 Ohms
- vector label deli_io_imp_12 resistance = 38.3388 Ohms
- vector label deli_io_imp_13 resistance = 36.1582 Ohms
- vector label deli_io_imp_14 resistance = 34.2239 Ohms

4 PVT control bits
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Path Length Example
Defect Tolerance as a Function of Path Length

(Digital)
Path through fault site should be long

(After)
Clock period is the metric used to test the path

Slack
Long path
Faulty

Slack
Short path
Fault-free

Slack
Short path
Fault-free

Slack
Long path
Fault-free

Slack
Long path
Faulty

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Dynamic Scan Test: Theory

- NORM
- SIN
- SFTMA
- CK+SFTSL
- SOUT
- M1
- S1

scanin  step  scanout
Dynamic Scan Test : Reality

Power supply droop causes clock period stretch
Clock Double Pulse and Vdd

270 MHz
Free-running Clock and Vdd

312.5 MHz
Delay Testing is Analog

- $312.5 - 270 = 42.5$ (~15%)
- Typical frequency margin is 5-10%
- Clock period measurement and adjustment crucial

- Other internal analog issues on the horizon: crosstalk
Crosstalk Test: Simulation

victim

aggressors
Tester Results

- Overlay shmoo:
  - $1/f$ vs. Vdd
- 6 tests
  - 2 aggressors
  - ...
  - 7 aggressors
- -> No differences
  i.e. \#aggressors had no effect
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Iddq Testing with Current Ratios

- CMOS has low leakage (quiescent current) in static state
- Defects cause static current to be drawn
- Measurement of Idd during static state allows defect detection
Does Iddq Have a Future?

- Issue: signal-to-noise ratio
  - Signal = current from defect
  - Noise = leakage current from everybody else
- Leakage currents rising as geometries shrink
- Intel presentation last month: leakage power was huge!
- Likely to lose Iddq as a test method
Iddq Testing with Current Ratios

- Single-threshold Iddq tests do not work for deep submicron chips
- Solution: Current Ratios method (Maxwell, ITC 1999)
- Self-scaling solution: max/min ratio + guardband : find outliers
- Extends usability of Iddq into .13u, even 90nm designs

$Iddq$ Histogram

![Iddq Histogram](image)

$Iddq$ (uA)

Defective

Good

Original regression:

$$y = 12.536 + 1.063x$$
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WLRS: Wafer Level Reliability Screening

• Latent defects detectable by clever test methods
  - LVS : Low Voltage Sweep
  - DVS : Dynamic Voltage Stress (30% over nominal voltage)
  - EVS : Enhanced Voltage Stress (80% over nominal voltage)
• Iddq is a very sensitive measure of stress-induced performance shift
• Study: WLRS with statistical defect-based test for outliers identified latent defects at wafer test (Quach, ITC 2002)
Test Types and Applications
LVS Timing Diagram

Minimum passing supply voltage
DVS Timing Diagram

VStress

VNom

Data

SCAN-IN

T1

T2
EVS Timing Diagram

VStress

VNom

Data

Scan-In

VBump Setup & Eval

T1

T2
Voltage Acceleration Factor \( (AF_V) \)

- Stress Voltage in V:
  - DVS = 1.95V, \( AF_V = 37 \)
  - EVS = 2.7V, \( AF_V = 15,000 \)
Low Voltage Sweep (LVS)

Die A before EVS stress
Die B before EVS stress
Die A after EVS stress
Die B after EVS stress
$I_{DDQ}$ Outliers Before Voltage Stress

Die A: 10mA

Min $I_{DDQ}$ in mA

Max $I_{DDQ}$ in mA
**I_{DDQ} Outliers Before & After Stress**

Die F: Was 0.28mA
After Stress 1.26mA

Die A: Was 10mA
After Stress 5mA
Defect-Based Testing is Analog

• Correlation of test results as continuous variables
  - Iddq
  - Vdd

• Measurement over large sample size using statistics
  - Outliers
  - Distributions
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... if only data were really this digital...
Limitations in High-Speed I/O Test Observability

Transmit ASIC

Receive ASIC

Conventional Probe Access

Internal Signal

Solder Ball, Package, Wire Bond

Package

Equalization

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“Eye” at Receiver Pins at 6.25 Gb/S, 34” Trace
Data Bit View: Negative Eye Opening
Bit Error Rate Testing

• Bit Error Rate is the bottom-line measure of communication quality
  • BER = #errors / #bits transmitted
    • $10^{-12}$ BER => ~1 minute for 1 error at 10 Gb/s
    • $10^{-15}$ BER => ~1 day for 1 error at 10 Gb/s
    • $10^{-17}$ BER => ~Fiscal Quarter for 1 error at 10 Gb/s
  • > 400 errors required for 95% confidence
  • $T = \frac{3}{r}$ seconds with 0 errors for 95% confidence that error rate < $r$
  • Stress the channel (ie. reduce SNR) to cause more errors; extrapolate

**Problem:** if BER too high, what was the cause?
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Eye Mapping (to produce eye diagrams)

Move through the (Phase, Offset) space to map eye opening
Boundary Scan in GHz Channel

data[0:n-1] → parallel to serial converter → TX+ RX+ TX- RX- → rxdata

Good place for on-chip instruments
IEEE 1149.6 : AC Extest

- IEEE 1149.1 extensions for advanced I/O
  - AC-coupled nets
  - Differential nets
  - Adjustable I/O
- Agilent provided technical leadership in working group
- First silicon implementation of 1149.6
AC Scan Shmoo: Clock Stretch Compensation
Process Skew Methodology
Force the Process Drift prior to Characterization

Fast and Slow Targets (Outer Box) Represent PCM Specification Limits for a Given IC Process Technology
Skew Lot vs Process Distribution

Production Data
Skew Lot Data
On-Chip Instrumentation
Accessing Analog Information Inside
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Digital == Analog

- The strictly digital test problem is well understood
  - Temptation is to simplify the digital test manufacturing flow
- Real digital test issues are often analog in nature
  - Test equipment must keep pace (speed, power, data volume)
  - Some test equipment must find its way on chip
- Characterization of analog nature of process drift is important
- Clever design-for-testability and manufacturability is essential!