Negative Bias Temperature Instability (NBTI)

Physics, Materials, Process, and Circuit Issues

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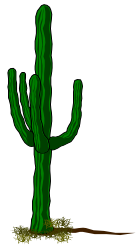
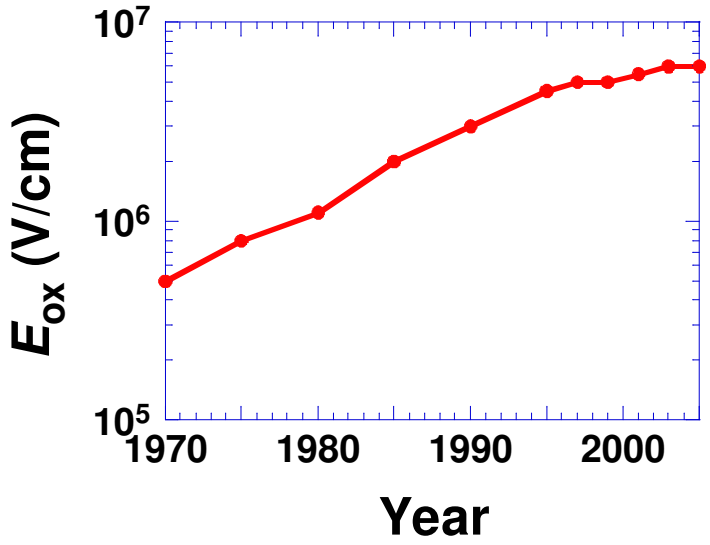


Introduction

- What is NBTI?
- Material Issues
- Device Issues
- Circuit Issues
- Effect of
  - Hydrogen
  - Nitrogen
  - Water
  - Fluorine
  - Deuterium
  - Boron
  - Stress
- NBTI Minimization

What Is NBTI?

- Negative bias temperature instability occurs mainly in *p*-channel MOS devices
- Either *negative gate voltages* or *elevated temperatures* can produce NBTI, but a stronger and faster effect is produced by their combined action
  - Oxide electric fields typically below 6 MV/cm
  - Stress temperatures: 100 - 250°C
  - Drain current, transconductance, and "off" current decrease
  - Absolute threshold voltage increase
- Such fields and temperatures are typically encountered during *burn in*, but are also approached in high-performance ICs during routine operation

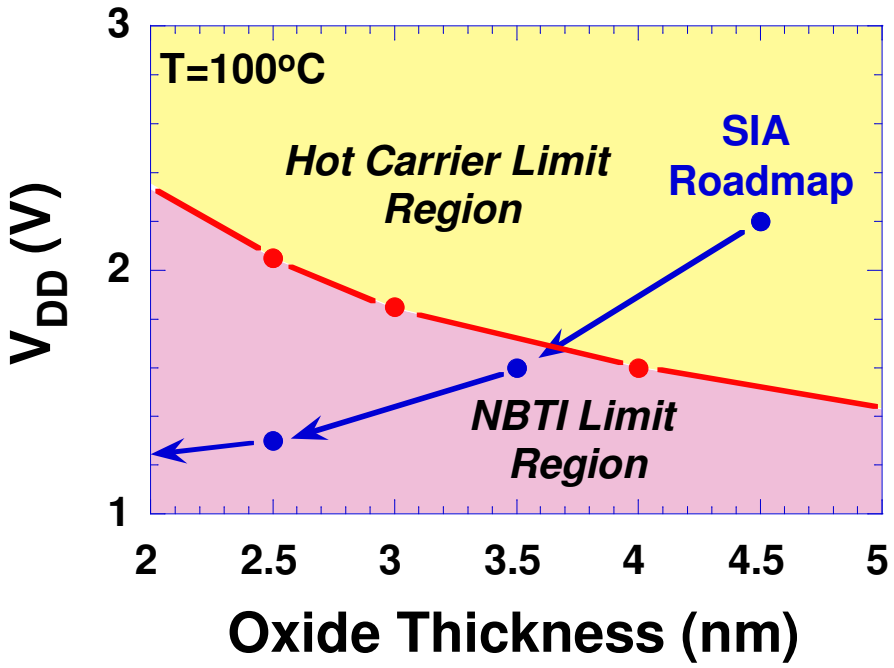


Parametric Impact

- **Material**
  - Interface traps, D_{it}
  - Oxide charges, N_{ot}
- **Device**
  - Threshold voltage, V_T
  - Transconductance, g_m
  - Subthreshold slope, S
  - Mobility, μ_{eff}
  - Drain current, $I_{D,lin}$, $I_{D,sat}$
- **Circuit**
  - Gate-to-drain capacitance, C_{gd}
  - Delay time, t_d

Device Lifetime Limits

- **NBTI – key reliability issue**



N. Kimizuka et al., *IEEE VLSI Symp.* 73 (1999)

MOSFET Performance

- MOSFET drain current depends on
  - Dimensions: W, L, $C_{ox} \sim 1/t_{ox}$
  - Mobility: μ_{eff}
  - Voltages: V_G, V_D, V_T

$$I_D = (W/2L)\mu_{eff} C_{ox}(V_G - V_T)^2$$

- Delay time: t_d

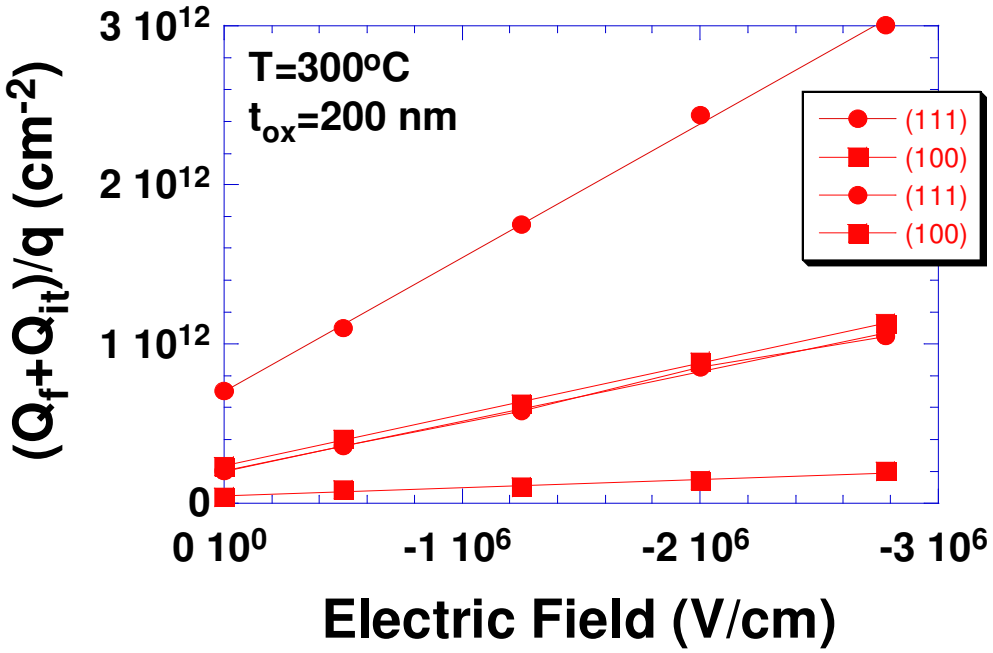
$$t_d = \frac{CV_{DD}}{I_D} = \frac{C}{(W/2L)\mu_{eff} C_{ox} V_{DD}(1 - V_T/V_{DD})^2}$$

$I_D \Downarrow$ and $t_d \Uparrow$ if $V_T \Uparrow$ and $\mu_{eff} \Downarrow$

When device parameter change exceeds a certain value $\Rightarrow$ *failure*

Earliest NBTI

- **Generation of fixed charge and interface states with *negative* gate bias was observed very early during MOS development – *in 1967*!**

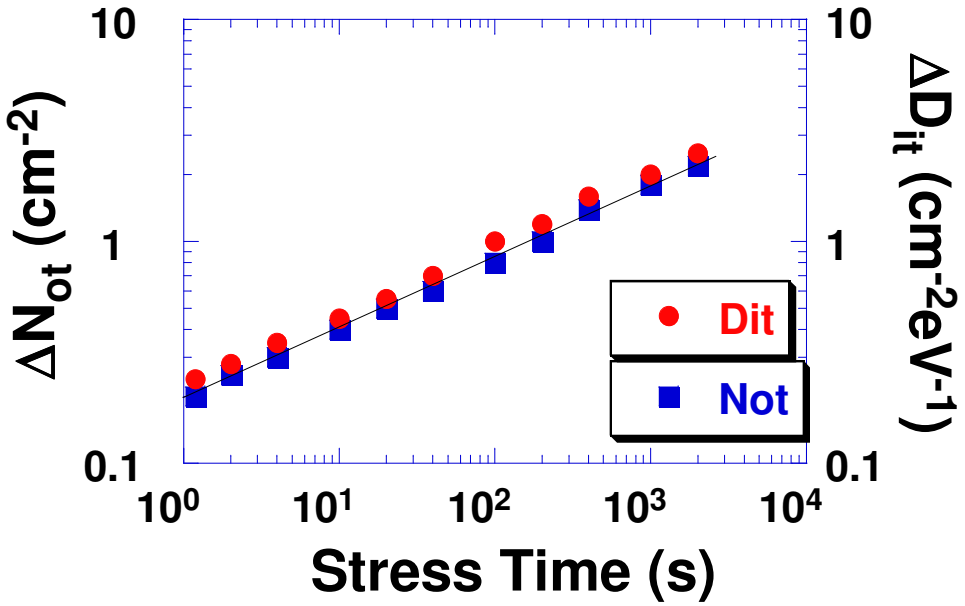


B.E. Deal et al., *J. Electrochem. Soc.* **114**, 266 (1967)

Typical NBTI Features

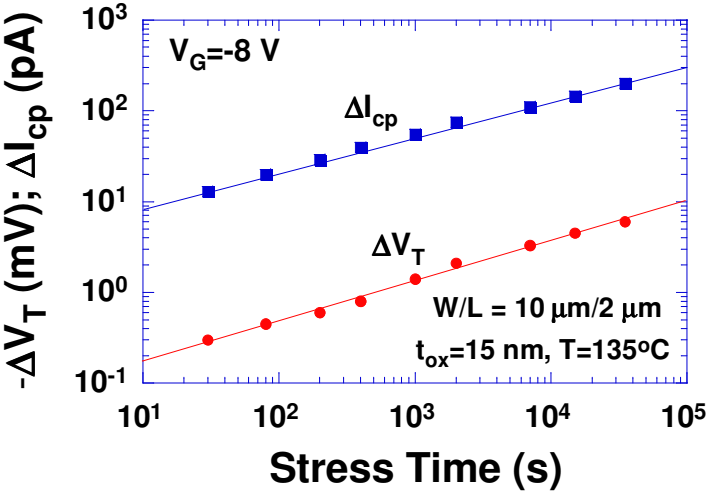
- Interface traps, D_{it}, and positive oxide charges, N_{ot}, are generated at similar rates

$$\Delta D_{it} \approx \Delta N_{ot}$$

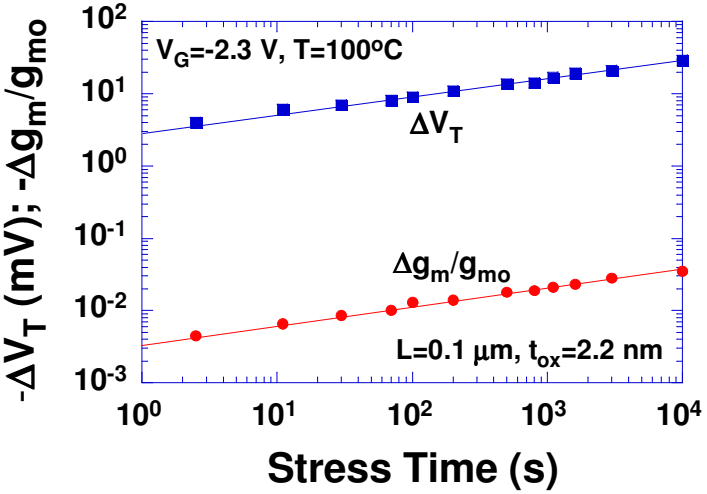


V_T, *Transconductance*

- **Charge pumping current I_{cp} ~ interface state density D_{it}**
- **Transconductance g_m ~ effective mobility μ_{eff} ~ D_{it}**



C. Schlünder et al. *Microelectron. Rel.* **39**, 821 (1999)

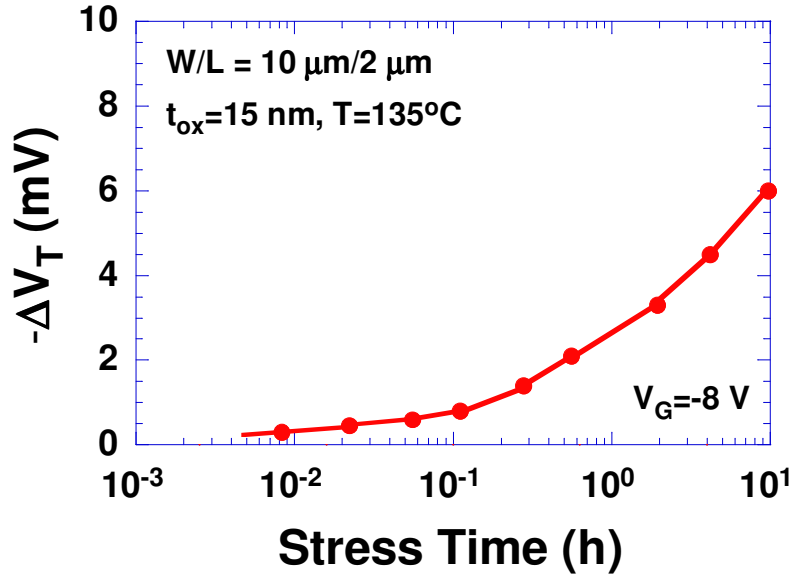


N. Kimizuka et al., *IEEE VLSI Symp.* 92 (2000)

Threshold Voltage

- **Threshold voltage of *p*-channel MOSFETs decreases with stress time. Why?**

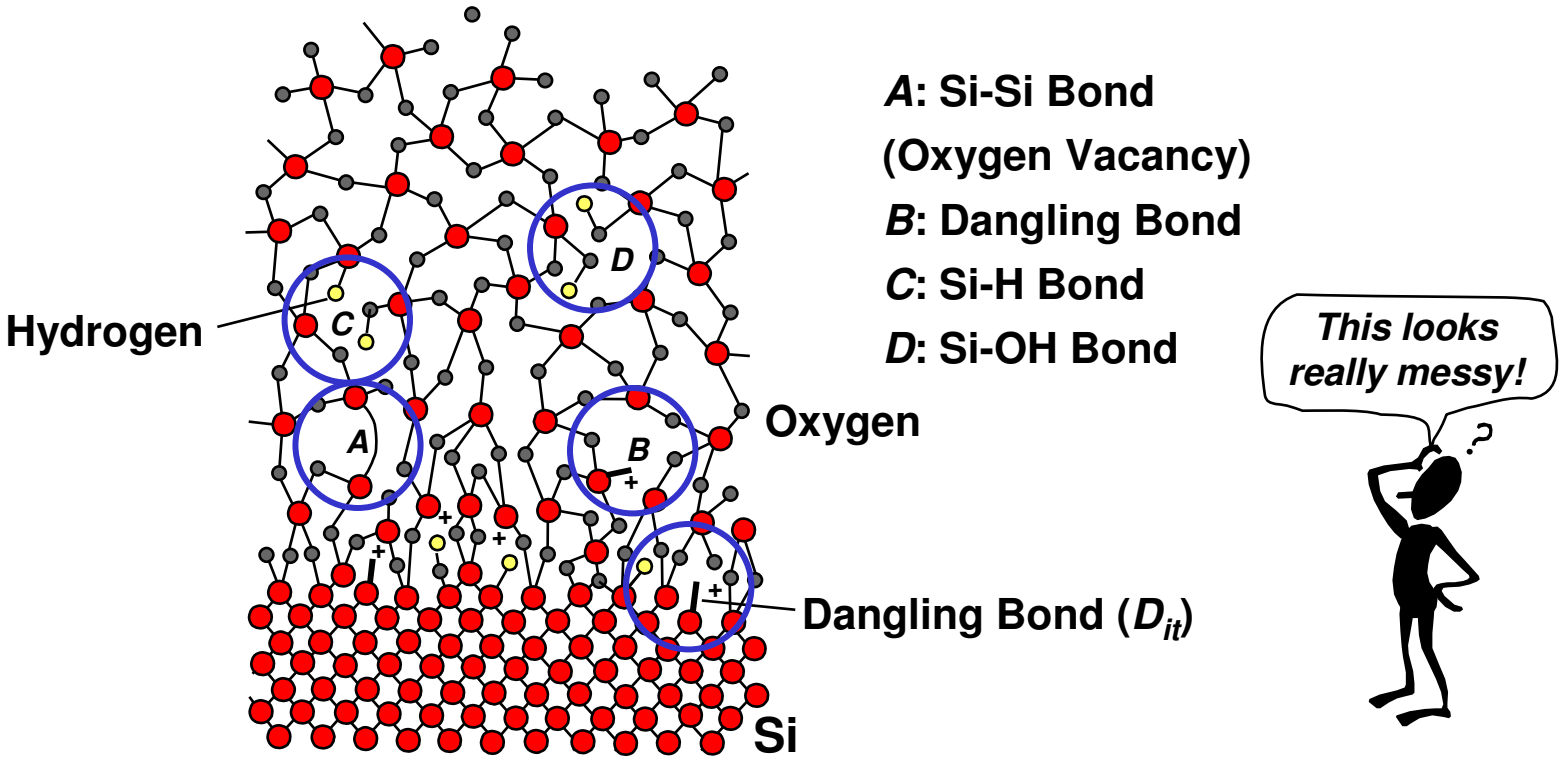
$$V_T = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} + 2\phi_F + \frac{Q_S}{C_{ox}}$$



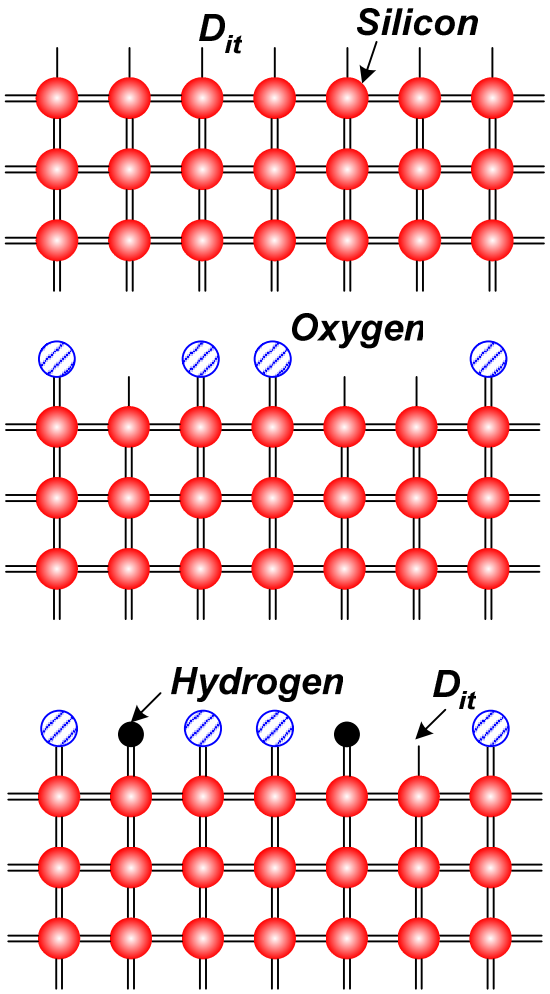
C. Schlünder et al. *Microelectron. Rel.* **39**, 821 (1999)

SiO_2 and SiO_2/Si Interface

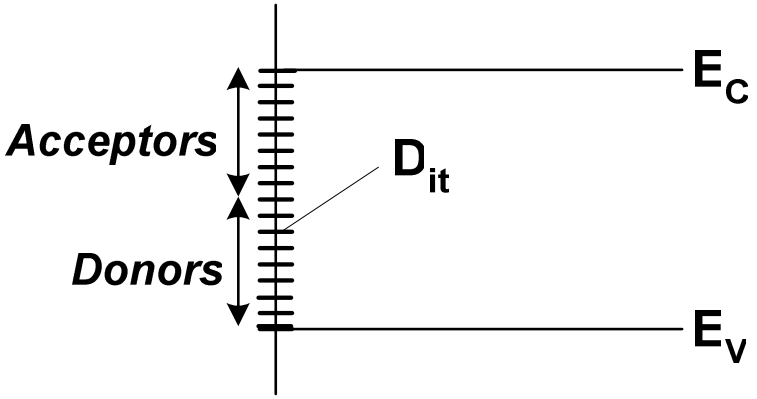
- Si, Si/SiO_2 interface, SiO_2 bulk, and oxide defect structure



Interface Traps

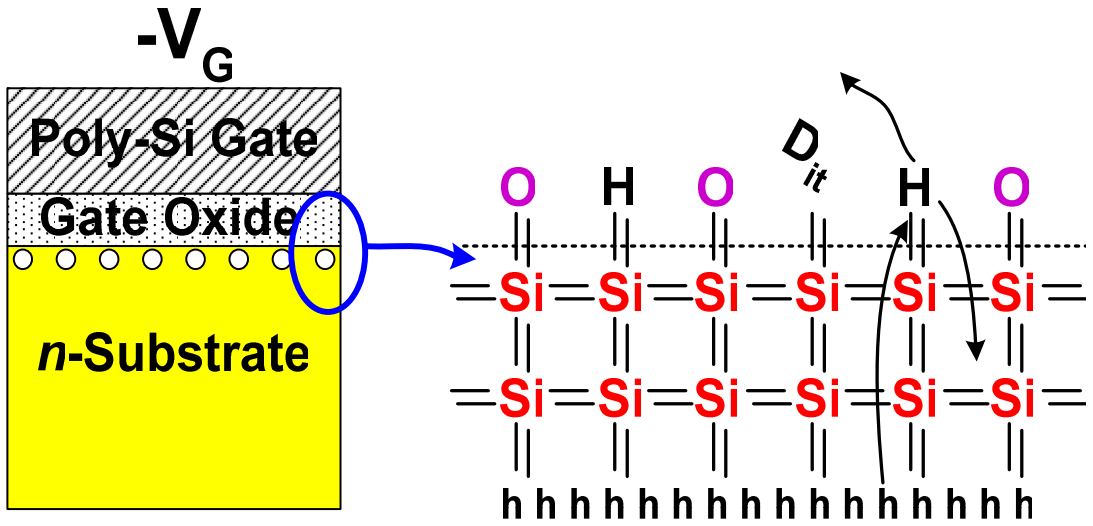


- Si has 4 electrons
- At the surface, Si atoms are missing: $D_{it} \sim 10^{14}$ cm^{-2}eV^{-1}
- After oxidation: $D_{it} \sim 10^{12}$ cm^{-2}eV^{-1}
- After forming gas (H_2/N_2) anneal: $D_{it} \sim 10^{10}$ cm^{-2}eV^{-1}
- D_{it} *are* energy levels in the band gap at the Si surface
- Hydrogen is very important?

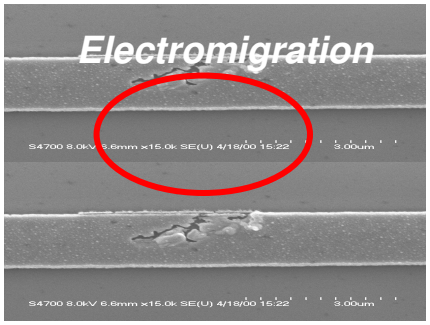


NBTI Mechanism

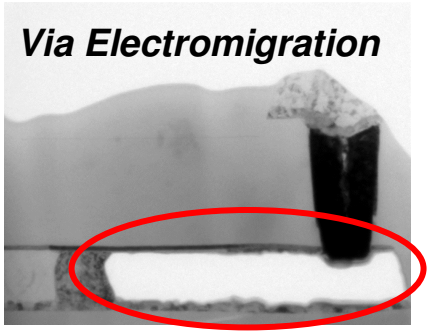
- A hole (*h*) is attracted to the Si/SiO_2 interface
- It weakens the Si-H bond until it breaks
- The hydrogen (*H*) diffuses into the oxide or Si substrate
  - If *H* diffuses into the Si, it can passivate boron ions
- Leaves an interface trap (D_{it})



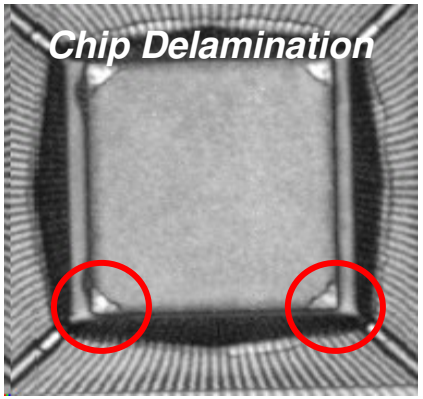
Holes Are The Problem !



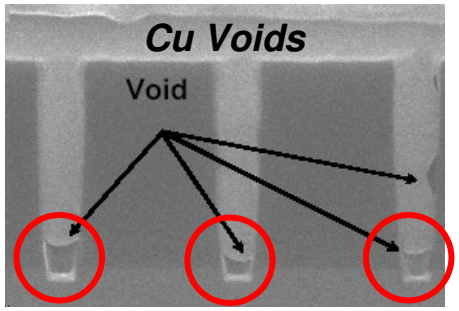
P. Nguyen, ASU



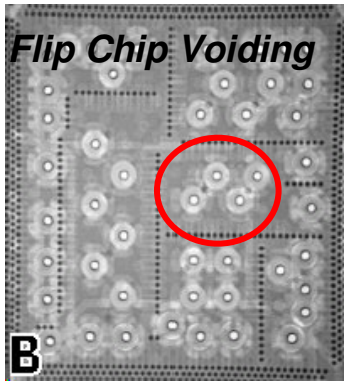
T.S. Sriram and E. Piccioli
Compaq



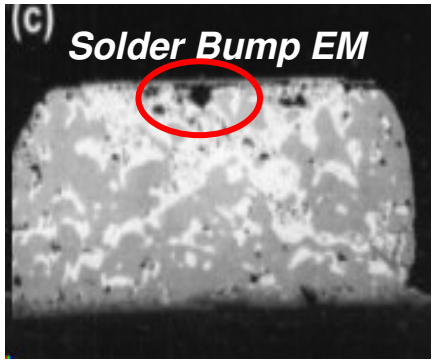
L. Wagner, IRPS 2004



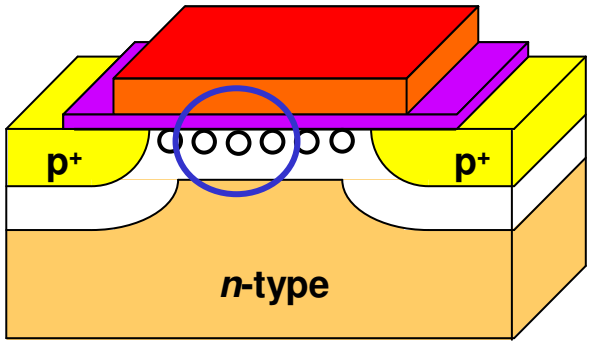
G. Dixit, IRPS 2004



L. Wagner, IRPS 2004



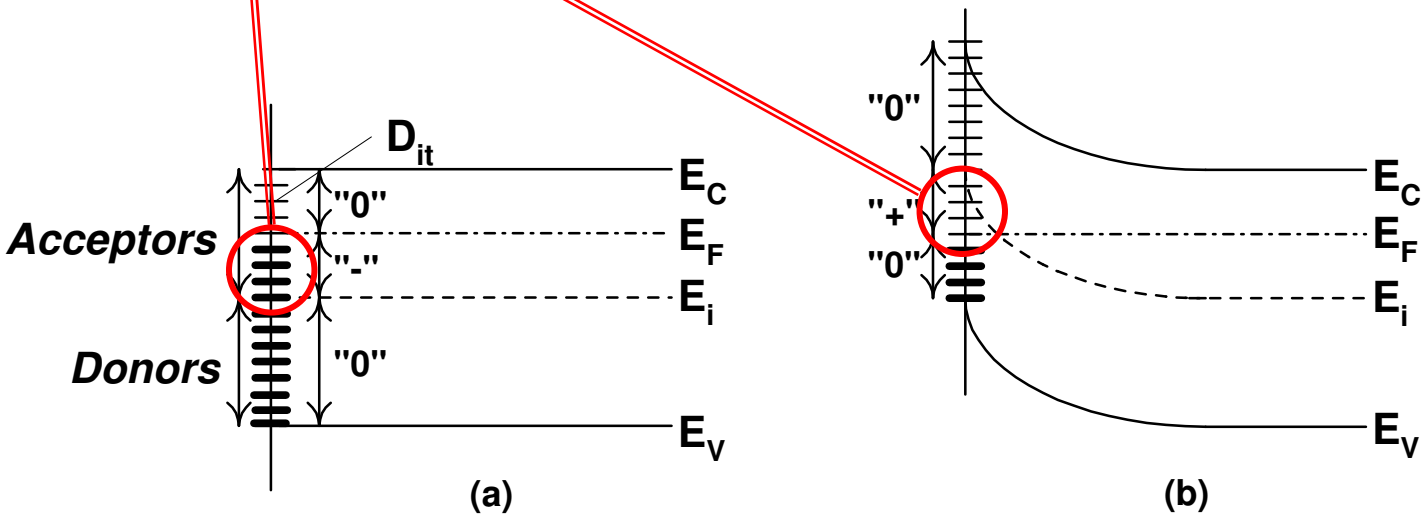
K. Tu, UCLA



Interface Trap Charge

- Band diagrams of the Si substrate of a *p*-channel MOS device shows the occupancy of interface traps and the various charge polarities for an *n*-substrate
- Acceptor with electron: *negative charge*
- Donor without electron: *positive charge*
  - (a) negative interface trap charge at flat band
  - (b) positive interface trap charge at inversion

(Heavy line: interface trap occupied by an electron; light line: unoccupied by an electron)



Threshold Voltage

- N_{it} and $N_f \approx 10^{10}$ cm^{-2}; 0.1 μm x 1.0 μm gate ($A = 10^{-9}$ cm^2), there only 10 interface traps and 10 fixed oxide charges at the SiO_2/Si interface under the gate $\Rightarrow \Delta V_T$

$$\Delta V_T = -\frac{Q_{it} + Q_f}{C_{ox}} = -\frac{20q}{K_{ox}\varepsilon_o A} t_{ox} = -\frac{1.6x10^{-19}\,x20}{3.45x10^{-13}\,x10^{-9}} t_{ox} = -9.2x10^3\, t_{ox}$$

- For t_{ox} = 5 nm $\Rightarrow \Delta V_T \approx$ -5 mV. For ΔV_T = -50 mV, device failure $\Rightarrow \Delta N_{it} = \Delta N_f = 10^{11}$ cm^{-2}
- Suppose that in a matched analog circuit, one MOSFET experiences $\Delta V_T \approx$ -10 mV and the other $\Delta V_T \approx$ -25 mV. This 15 mV mismatch in a V_T = -0.3 V technology $\Rightarrow$ 5% mismatch. High performance analog transistor pairs that require mismatch tolerances of 0.1% to 0.01%.

Reaction – Diffusion Model

- Holes interact with Si-H bond
- Holes weaken Si-H bond
- At elevated temperature, the Si-H bonds dissociate

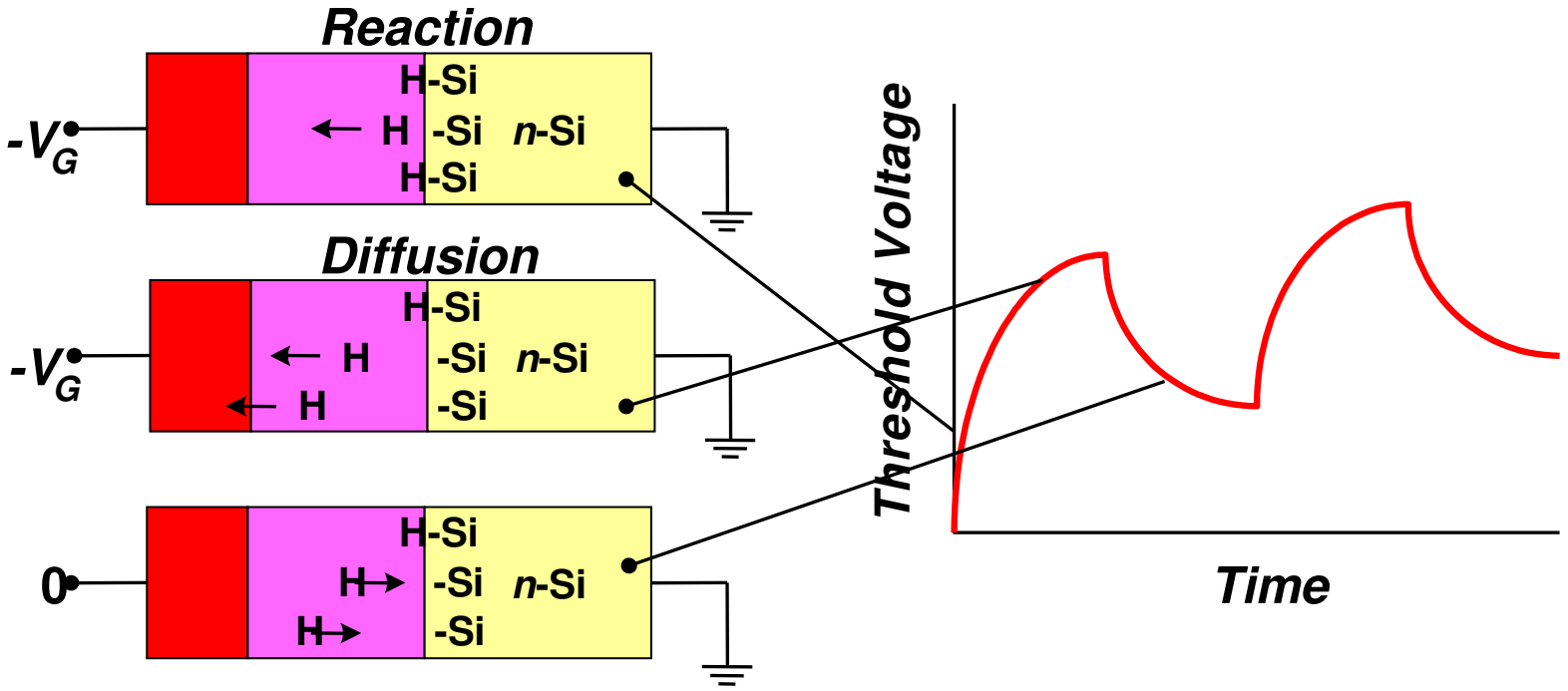
$$Si_3 \equiv SiH + h^+ \rightarrow Si_3 \equiv Si\bullet + H^+$$

- Initially
  - D_{it} generation ~ Si-H dissociation rate (reaction limited)
- Later
  - D_{it} generation ~ hydrogen diffusion rate (diffusion limited)

M.A. Alam, *IEDM*, 2003; IRPS 2005

Reaction – Diffusion Model

$$\frac{dN_{it}}{dt} = k_f(N_{Si-H} - N_{it}) - k_r N_{it} N_H(x=0)$$

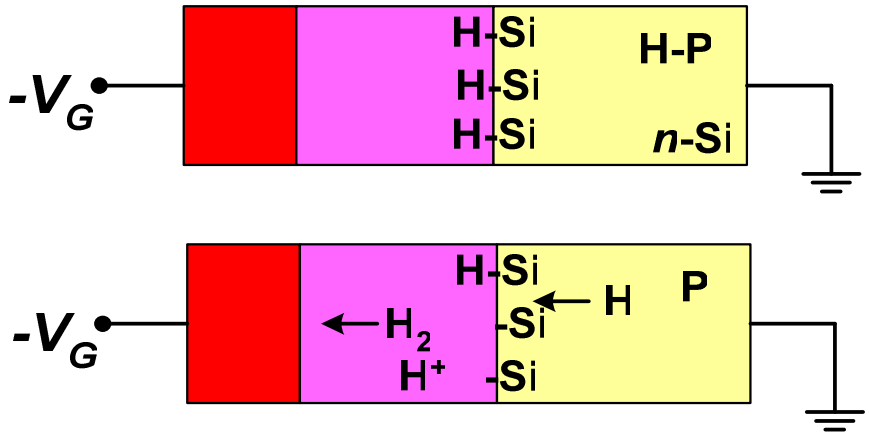


Hydrogen Model

- Hydrogen from *Si substrate* drifts to SiO_2/Si interface
- H^o near/at SiO_2/Si interface traps a hole $\Rightarrow$ H^+
- H^+ depassivates Si-H bond $\Rightarrow$ D_{it} and H_2

$$Si_3 \equiv SiH + H^+ \Rightarrow Si_3 \equiv Si\bullet + H_2$$

- Some H^+ drifts into SiO_2 $\Rightarrow$ N_{ot}



D.M. Fleetwood et al. *Appl. Phys. Lett.* **86**, 142103 (2005)

Device Dependence

$$I_{D,lin} = \frac{W\mu_{eff}C_{ox}/L}{1+V_D/\varepsilon_{lat}L}(V_G - V_T - V_D/2)V_D$$

$$\Rightarrow \frac{\delta I_{D,lin}}{I_{D,lin}} = -\frac{\delta V_T}{V_G - V_T}$$

$$I_{D,sat} = Wv_{sat}C_{ox}\frac{(V_G - V_T)^2}{V_G - V_T + \varepsilon_{sat}L} \approx Wv_{sat}C_{ox}(V_G - V_T)^n$$

$$\Rightarrow \frac{\delta I_{D,sat}}{I_{D,sat}} = -n\frac{\delta V_T}{V_G - V_T}$$

L dependence

- Long channel: $n \approx 2$, short channel: $n \approx 1$
- Hence long channel degradation worse

I_D dependence

- $I_{D,sat}$ worse than $I_{D,lin}$ due to n

Device Dependence

t_{ox} dependence

- With scaling, $t_{ox} \Downarrow$ and V_G-V_T (headroom) $\Downarrow$
- Hence thin oxide degradation worse for same V_T

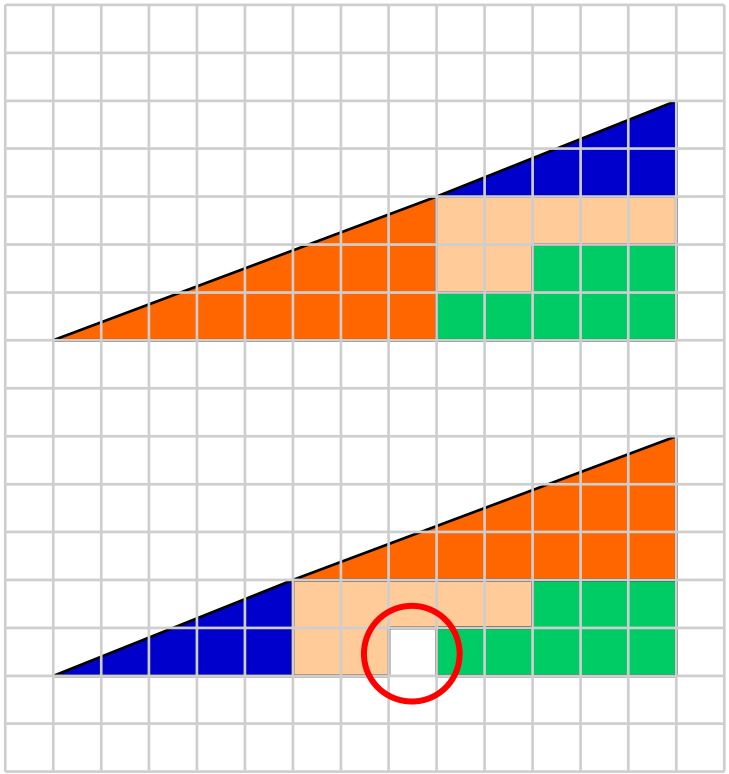
μ_{eff} dependence

$$C_{it} = qD_{it} \qquad \delta V_T = \frac{q\delta D_{it}}{C_{ox}} = \frac{q\delta D_{it}}{K_{ox}\varepsilon_o} t_{ox}$$

- For same V_T, as $t_{ox} \Downarrow$ $\delta D_{it} \Uparrow$, $\Rightarrow \mu_{eff} \Downarrow$
- Hence mobility degradation worse for thin oxides

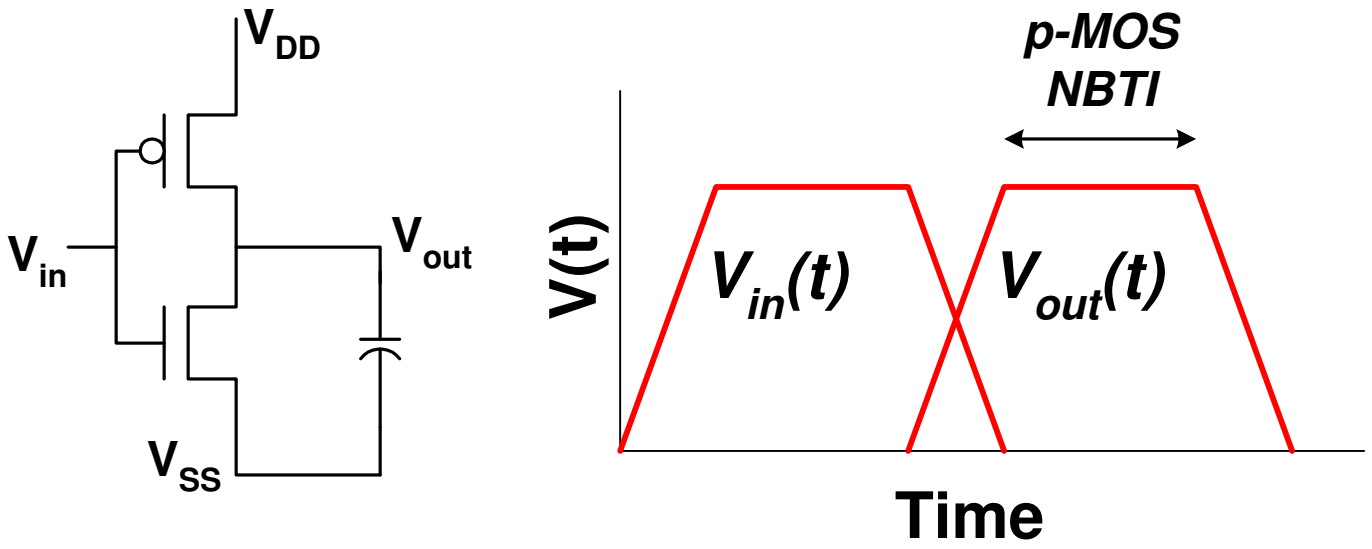
How Can This Be ?

- The lower picture is after the parts are moved
- Where does the missing hole come from?



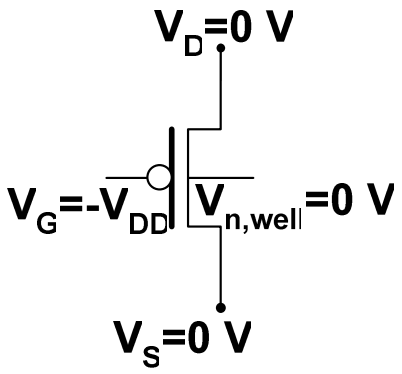
Effect on Circuits

Inverter Bias	V_{in}	V_{out}	*n*-MOS Stress	*p*-MOS Stress
1	V_{DD}	0 V	PBTI	*Off* State
2	0 V	V_{DD}	*Off* State	NBTI

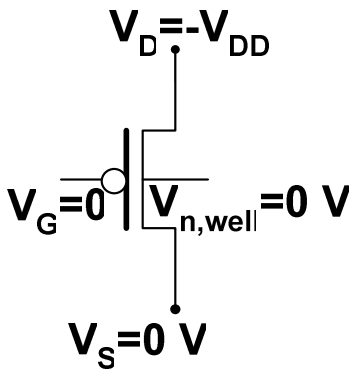


CMOS Inverter Degradation

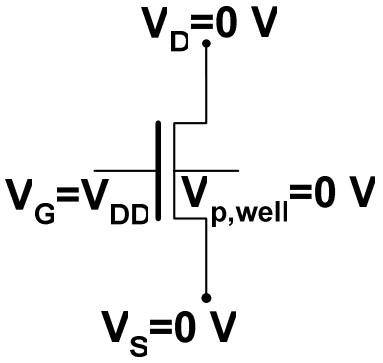
_p_-MOS NBTI



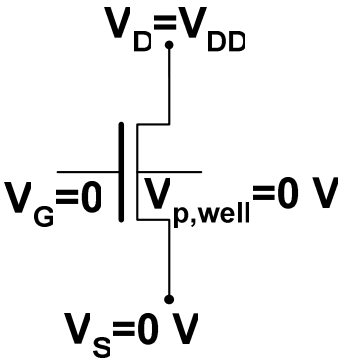
_p_-MOS *Off* State



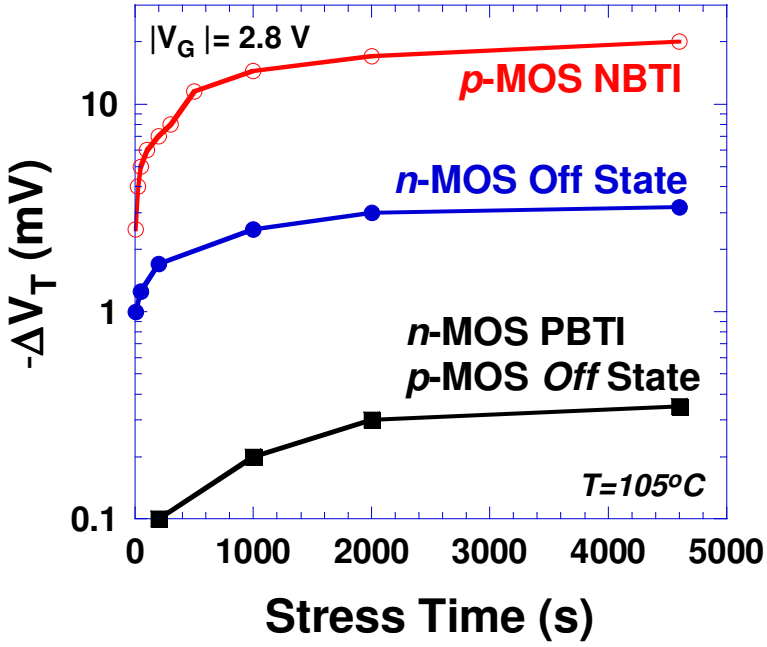
_n_-MOS PBTI



_n_-MOS *Off* State



- ***p*-MOS NBTI degradation is dominant degradation mechanism during static inverter stress**



V. Reddy et al. *IEEE 40th Ann. Int. Rel. Symp.*, 248 (2002)

Effect on Circuits

- **Occurs primarily in *p*-channel MOSFETs with negative gate voltage bias and is negligible for positive gate voltage**
- **In MOS circuits, it occurs most commonly during the "high" state of *p*-channel MOSFETs inverter operation**
- **Leads to timing shifts and potential circuit failure due to increased spreads in signal arrival in logic circuits**
- **Asymmetric degradation in timing paths can lead to non-functionality of sensitive logic circuits $\Rightarrow$ product field failures**

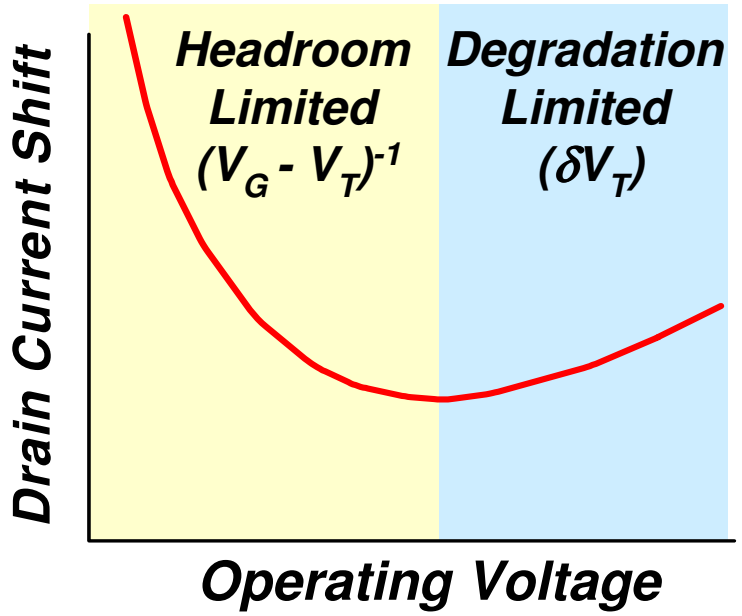
Circuit Dependence

t_d dependence

$$t_d = \frac{CV_{DD}}{I_D} \Rightarrow \frac{\delta t_d}{t_d} = n\frac{\delta V_T}{V_G - V_T}$$

$$\frac{\delta t_d}{t_d} = \frac{Kt^{0.25}}{V_G - V_T}\sqrt{E_{ox}\exp\left(\frac{E_{ox}}{E_0}\right)}$$

- Circuit delay degrades with V_T increase
  - ISCAS C423: 10% after 10 yrs*



A.T. Krishnan et al., *IEDM* 14.5.1, 2003

C_{GD} dependence

- With stress, $D_{it} \Uparrow$, $C_{it} \Uparrow$, $\Rightarrow C_{GD} \Uparrow$
- Important for analog circuits (Miller effect)

* B.C. Paul et al., *IEEE Electron Dev. Lett.* **26**, 560 (2005)

Circuit Degradation

Model	Accounts for NBTI impact on	RO Frequency Degradation (Digital)	Change in Unity Gain Bandwidth (Analog)
V_T Shifted Model	Channel charge	-3.2%	-1.0%
Degraded *I- V* only	Channel charge + Mobility	-4.5%	-1.3%
Including C_{GD} Degradation	Channel charge + Mobility + C_{GD}	**-4.9%**	**-4.4%**

- **V_T shifted model captures only ~60% (20%) of the degradation for digital (analog) circuits**

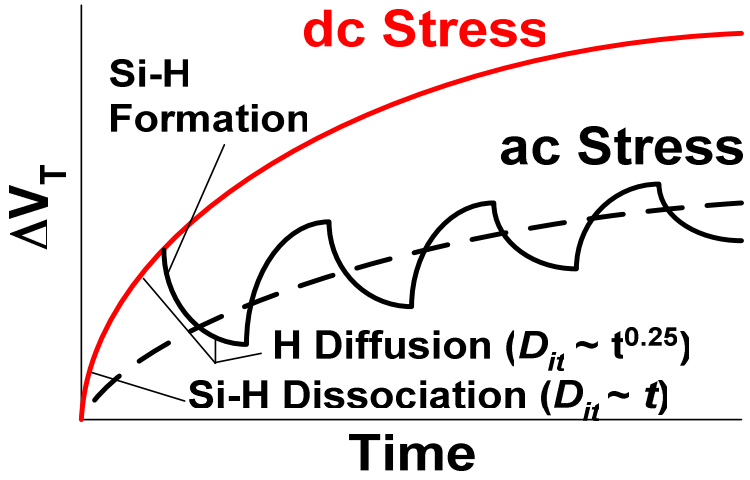
A.T. Krishnan *IRPS* 2004

Circuit Degradation

- **Degradation in digital circuits**
  - **FPGA performance**
  - **Ring oscillator f_{max}**
  - **SRAM static noise margin**
  - **Microprocessor**
- **Degradation in analog circuits**
  - **Current mirror**
  - **Operational amplifier**

DC Versus AC Stress

- Stress creates interface traps ($Si_3 \equiv Si\bullet$)
- D_{it} generation
  - Initially determined by Si-H dissociation rate
  - Later determined by hydrogen diffusion from interface
- When stress is terminated hydrogen diffuses back
  - Interface traps are passivated
- dc: D_{it} generation
- ac: D_{it} generation, passivation

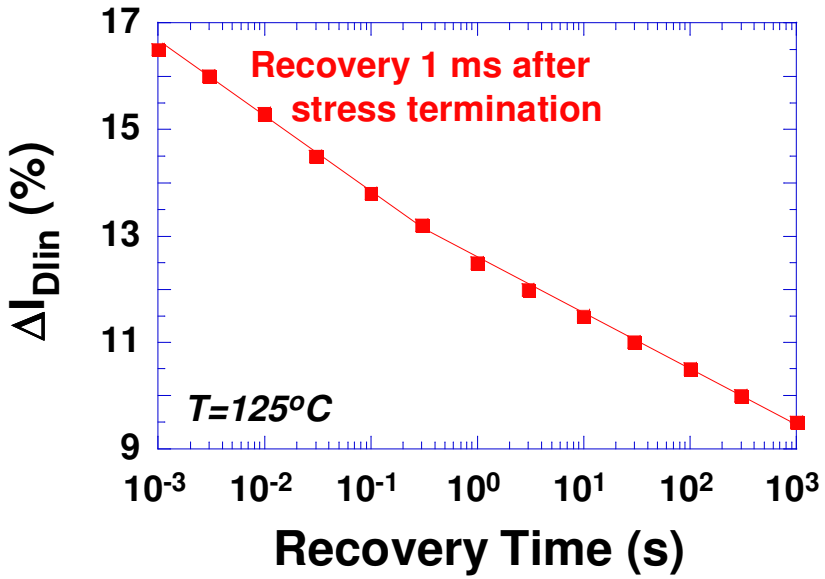


M.A. Alam, *IEDM*, 2003

ac stress leads to reduced degradation!

Damage Relaxation

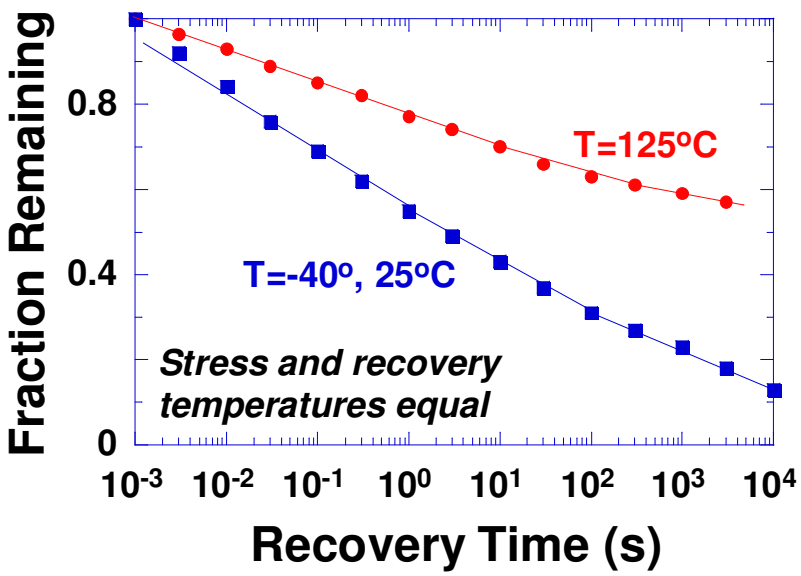
- When stress is terminated, degradation relaxes
- For sufficiently long times, all damage is "healed"
- Important to indicate the time between stress termination and NBTI measurements
  - Threshold voltage
  - Drain current
  - Transconductance
  - Interface traps
  - Mobility



S. Rangan et al., *IEDM*, 2003

Damage Relaxation

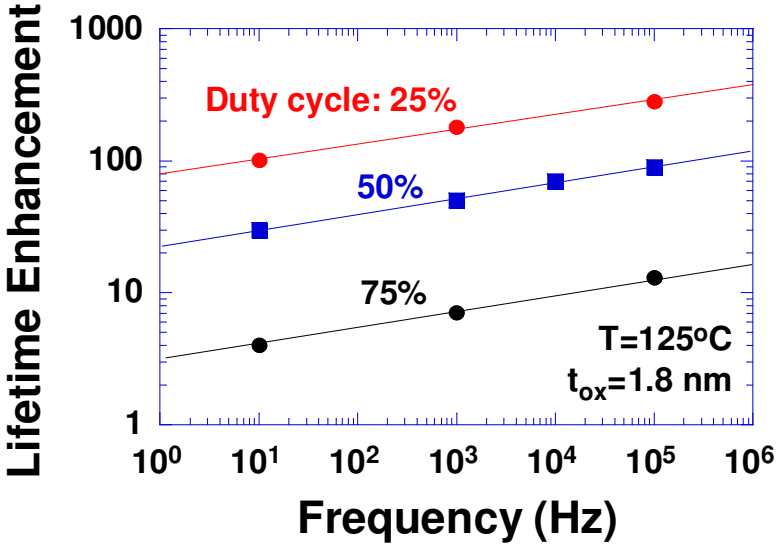
- For sufficiently long recovery time, damage disappears
- Temperature dependent
- Higher temperature, less recovery
  - Hydrogen diffuses further from SiO_2/Si interface and is not available during recovery
  - If hydrogen diffuses all the way to the poly-Si gate, it may "disappear"

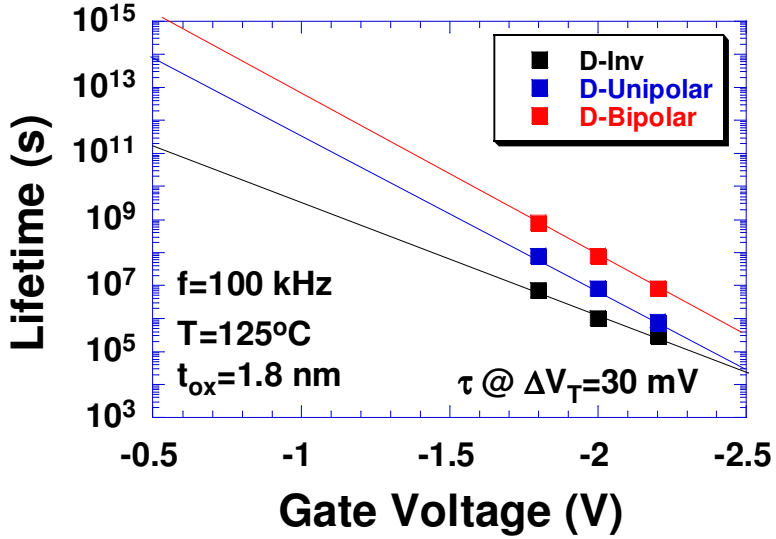


S. Rangan et al., *IEDM*, 2003

DC Versus AC Stress

- Dynamic stress ⇒ lifetime ⇑
- Transistors in circuit switch at different frequencies
  - Some transistors may not switch out of NBTI state
  - Could increase mismatch between paths switching at different rates





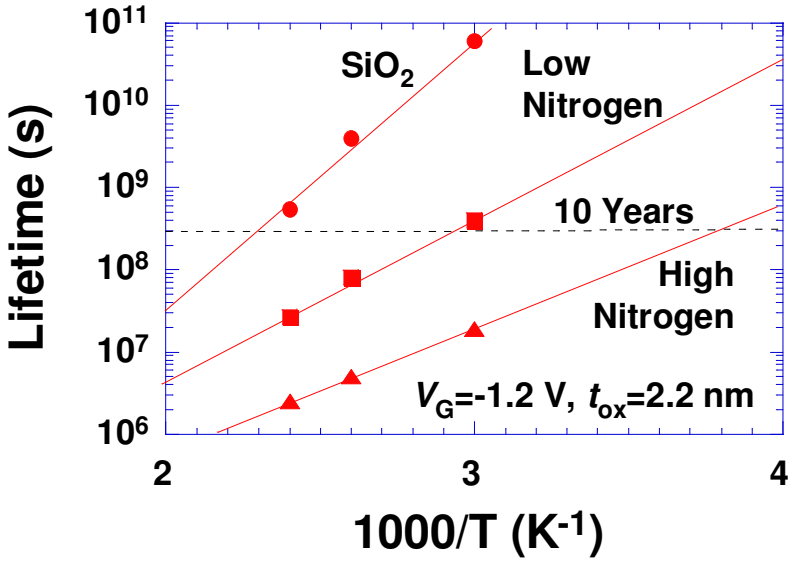
S.S. Tan et al. *IRPS*, 35 (2004)

Effect of Hydrogen

- **Hydrogen commonly used for interface trap passivation (~400-450°C, 20-30 min)**
- **Hydrogen can exist as**
  - **Atomic hydrogen H^0**
  - **Molecular hydrogen, H_2**
  - **Positively charged hydrogen or proton, H^+**
  - **Part of the hydroxyl group, OH**
  - **Hydronium, H_3O^+**
  - **Hydroxide ions, OH^-**
- **Hydrogen is believed to be the main passivating species for Si dangling bonds and plays a major role during NBTI stress, when SiH bonds are depassivated $\Rightarrow$ interface traps**

Effect of Nitrogen

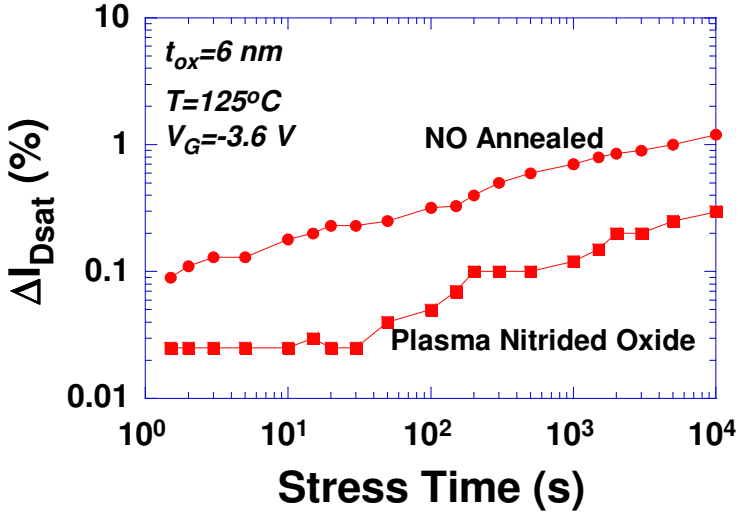
- Nitrogen may improve or degrade NBTI
- NBTI enhanced by nitrogen
- Nitrogen lowers activation energy
- Nitrogen profile affects impact
  - Lower N at interface is better
- Plasma nitridation gives least NBTI

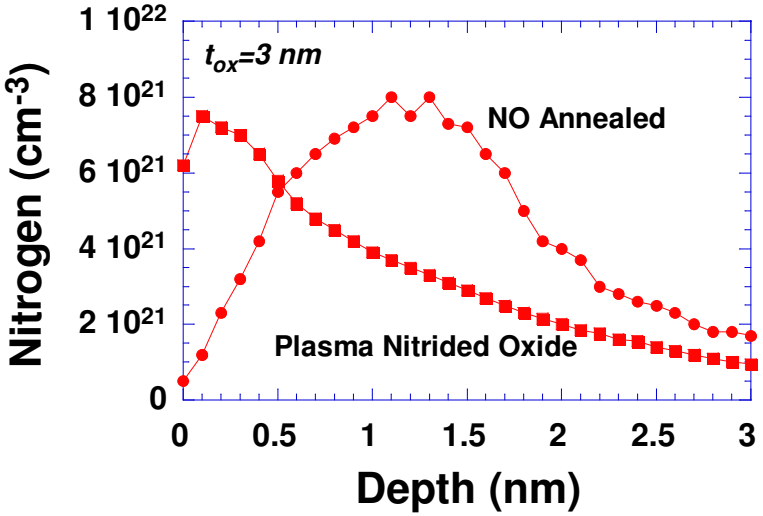


N. Kimizuka et al., *IEEE VLSI Symp.* 92 (2000)

Effect of Nitrogen

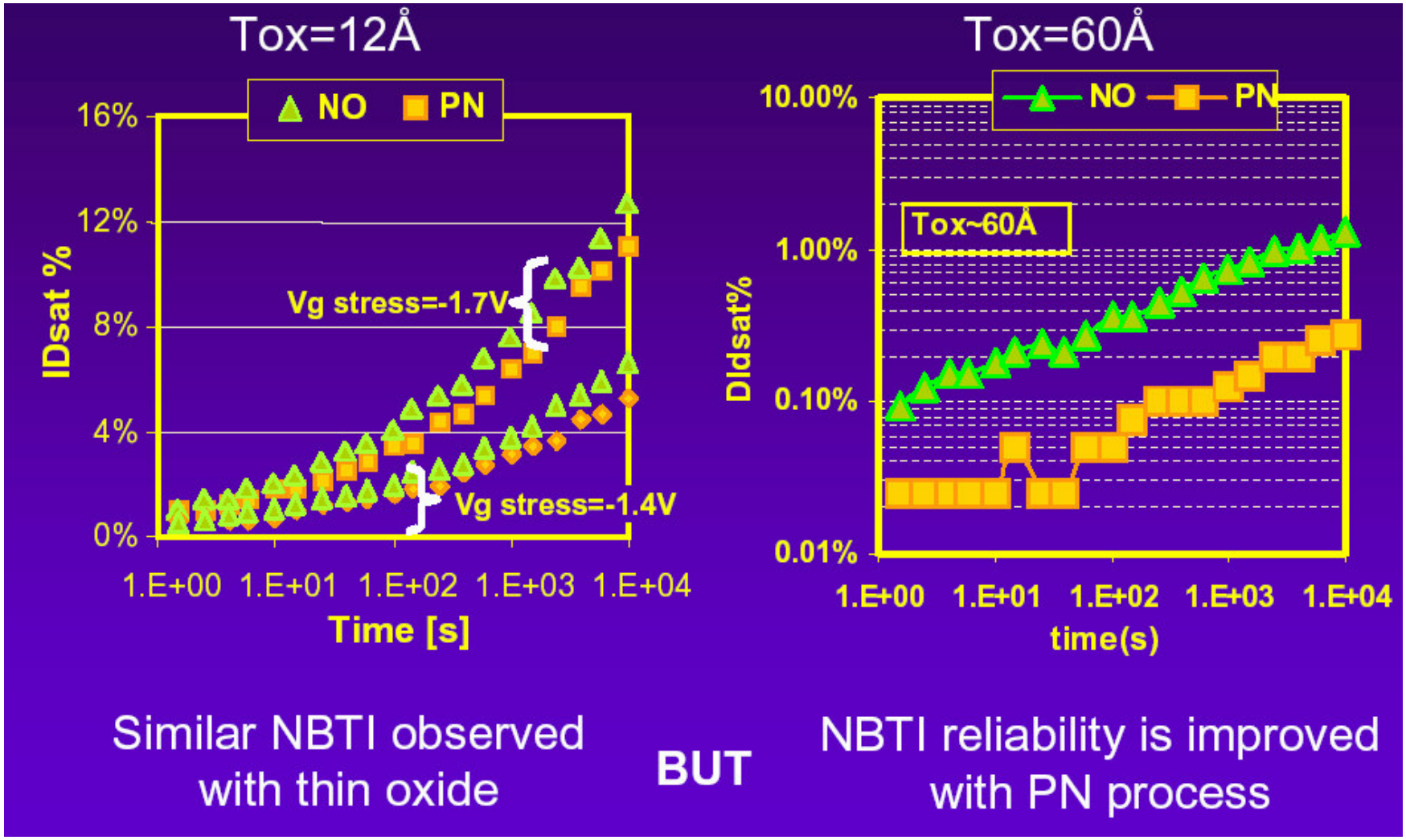
- Grow thermal oxide
- NO anneal or plasma nitridation
- Reduced gate leakage current (same oxide thickness)
- Similar reliability
- Improved NBTI with plasma nitridation
- Improves both digital and mixed-signal performance





B.Tavel et al., IEDM, 2003

Effect of Nitrogen



B.Tavel et al., IEDM, 2003

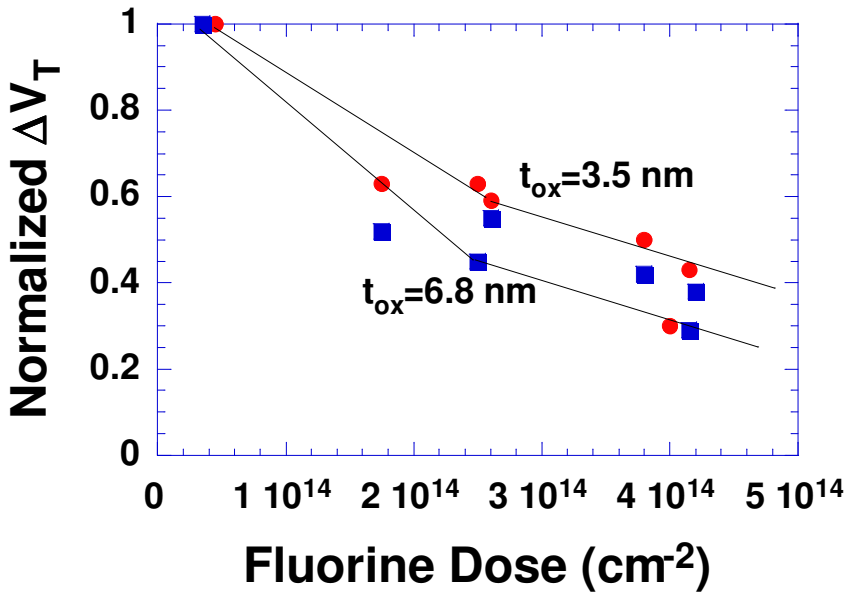
Effect of Water

- Water in the oxide enhances NBTI
- D_{it} and Q_{ox} increases are observed in damp and wet oxides; diffusion species is water
- Wet H_2-O_2 grown oxide to exhibit worse NBTI than dry O_2 grown oxides
- Water is often present on wafers from contact and via formation
- Water and moisture mostly travel along interfaces
- Water-originated reaction has lower energy at the Si/SiO_xN_y interface than at the Si/SiO_2 interface

$\Rightarrow$ NBTI is enhanced by water incorporation in oxide

Effect of Fluorine

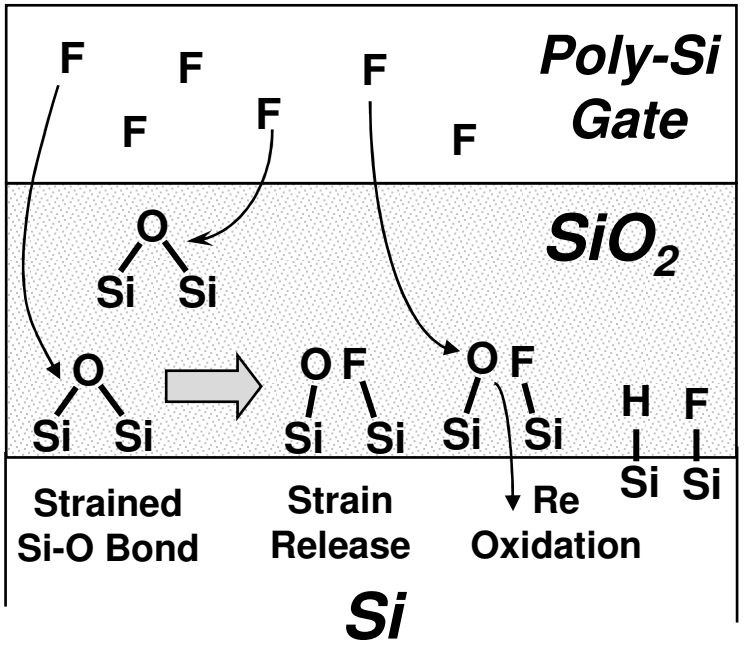
- **Fluorine improves NBTI**
- **"Hardens" SiO_2/Si interface**
- **Fluorine is believed to relieve strain at SiO_2/Si interface**



T.B. Hook et al., *IEEE Trans. Electron Dev.* **48**, 1346 (2001)

Fluorine

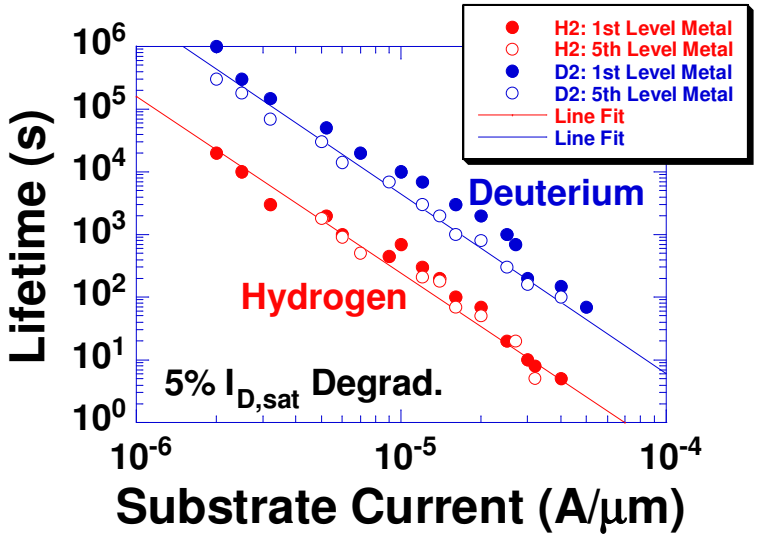
- Incorporation of fluorine atoms into SiO_2 improves Q_{BD}
- SIMS and Fourier transform infrared spectroscopy ⇒ strained layers are localized near the SiO_2/Si interface
- Fluorine releases the distortion of the strained Si-O bonds
- Fluorine diffuses into gate-oxide
- React with the strained Si-O bonds and release the distortion
- Released oxygen atoms re-oxidize the Si-SiO_2 interface
- Forms Si-F instead of Si-H bonds
- Si-F bond stronger than Si-H bond



Y. Mitani et al. "Improvement of Charge-to-Breakdown Distribution by Fluorine Incorporation Into Thin Gate Oxides," *IEEE Trans. Electron Dev.* **50**, 2221, Nov. 2003

Effect of Deuterium

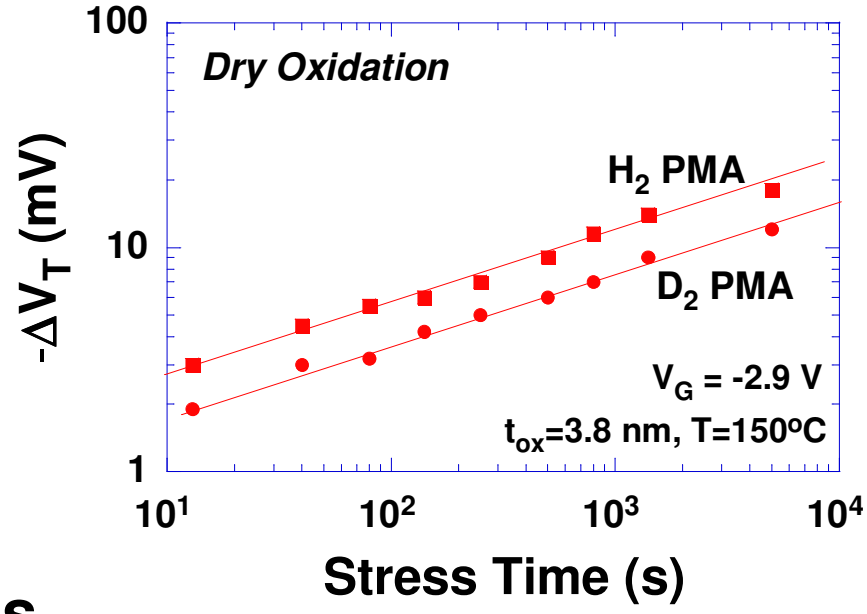
- **Hot carriers degrade devices through: *interface state generation, oxide charge trapping, mobility/transconductance degradation***
- **Post metallization anneal (~450°C/30 min): forming gas or hydrogen**
- **Si-H bonds form at SiO_2/Si interface**
- **Si-H bonds easy to form, but also easy to break**
- **Si-D bonds are stronger (D: deuterium is a stable isotope of hydrogen with natural abundance of 0.0015%)**
- **Hot carrier resistance enhanced by D_2**



W. F. Clark et al., *IEEE Electron Dev. Lett.* **20**, 501 (1999)

Effect of Deuterium

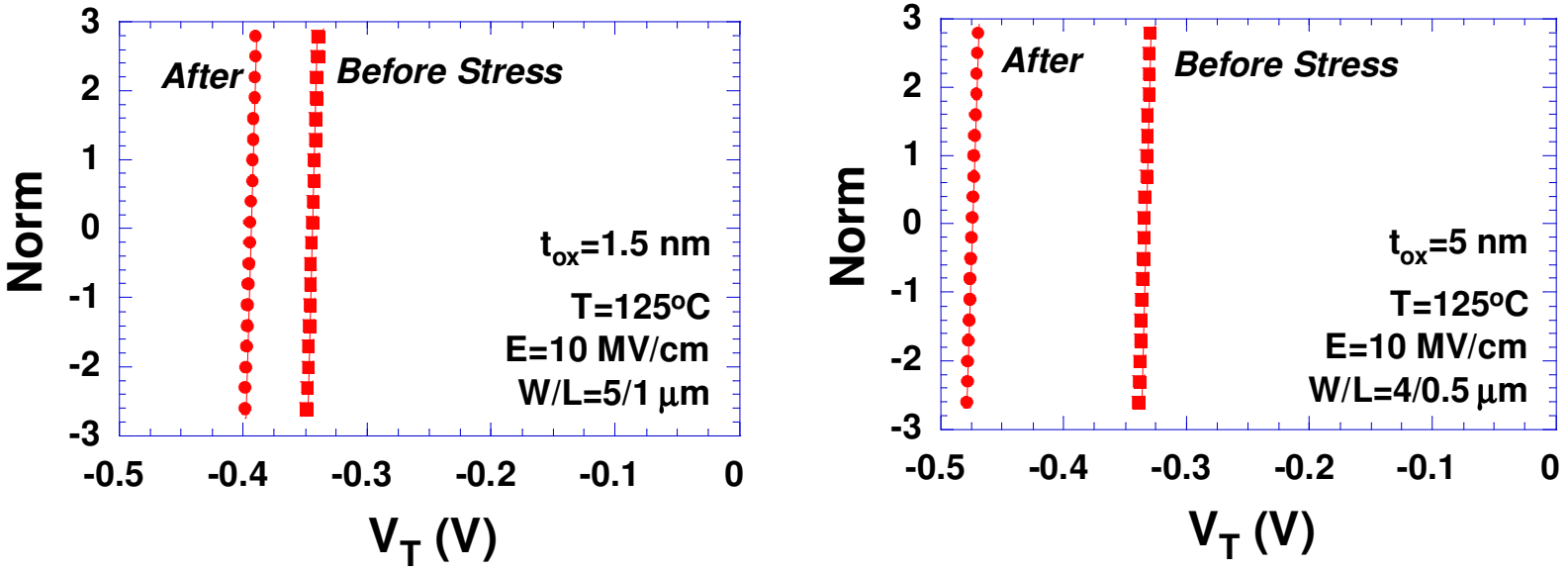
- Deuterium improves NBTI
- A "heavy" variant of hydrogen
- Stable isotope of hydrogen containing a proton as well as a neutron in its nucleus
- Due to its heavier mass, Si-D bonds are more resistant than Si-H bonds to hot carrier stress as well as NBTI



Effect of Oxide Thickness

- V_T shift, ΔV_T, depends on oxide thickness
- $\Delta V_T \sim t_{ox}$ for same interface trap density

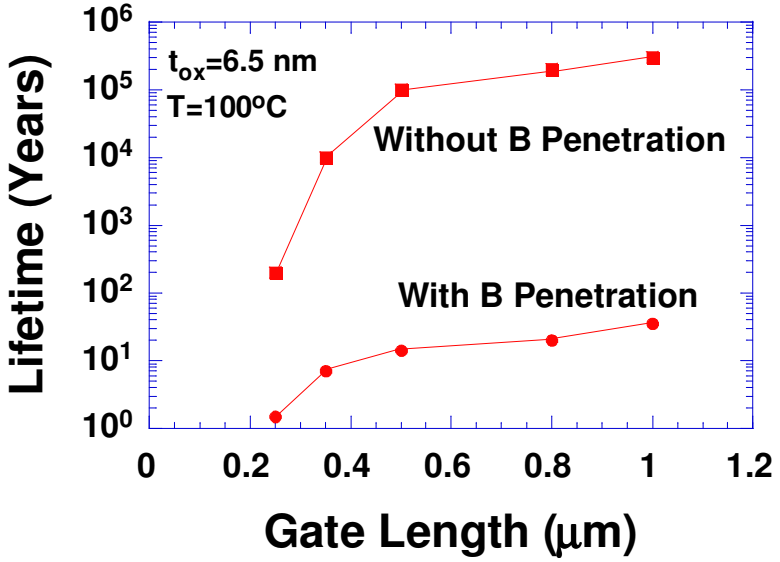
$$\Delta V_T = \frac{Q_{it}}{C_{ox}} = \frac{qN_{it}}{K_{ox}\varepsilon_o} t_{ox}$$



M. Agostinelli et al., *IRPS,* 171 (2004)

Effect of Boron

- **Boron degrades NBTI**
- **Boron diffuses into the gate oxide from the boron-doped gate and from the source/drain implants**
  - **Reduced D_{it} due to Si-F bonds from the BF_2 boron implant**
  - **Enhanced Q_{ox} due to increased oxide defects due to boron in the oxide**



Yamamoto et al. *IEEE Trans. Electron Dev.* **46**, 921 (1999)

NBTI Minimization

- Have initially low densities of electrically active defects at the SiO_2/Si interface and keep water out of the oxide
- Silicon nitride encapsulation layer has been found effective in keeping water away from the active CMOS devices, improving NBTI performance
- Minimize stress and hydrogen content
- Keep damage at the SiO_2/Si interface to a minimum during processing
- Plasma damage degrades NBTI in *p*-MOSFETs, but not *n*-MOSFETs
- Deuterium improves both hot carrier stress and NBTI
- Important to ensure deuterium can get to the SiO_2/Si interface and passivate dangling bonds or replace the hydrogen with deuterium in existing Si-H bonds

NBTI Minimization

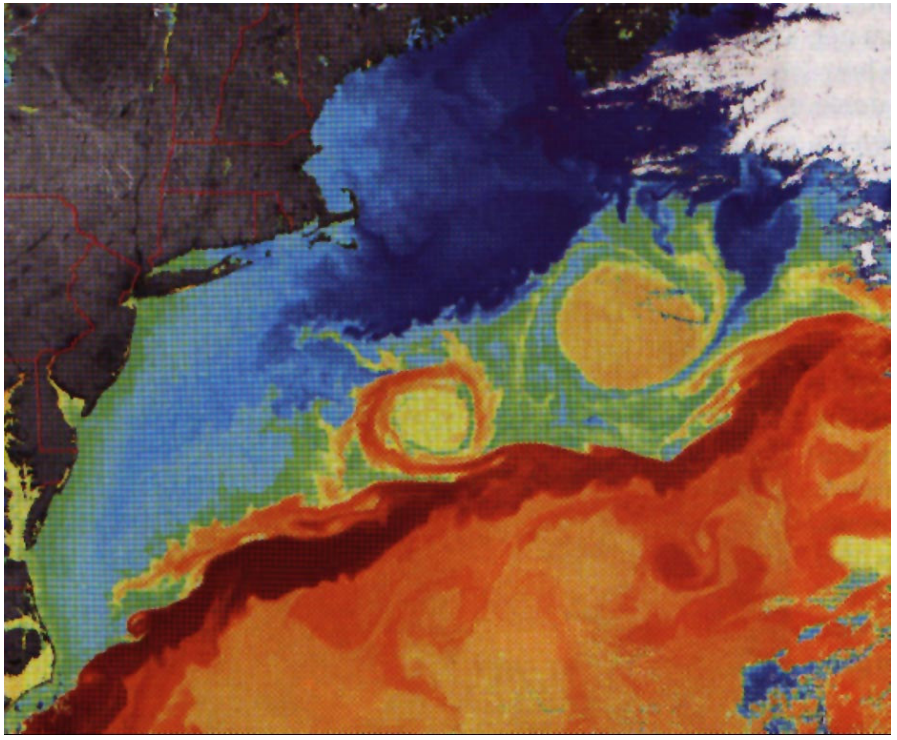
- Nitrogen incorporation has given conflicting results. Some authors claim an NBTI improvement, while others observe degradation
- The method and chemistry of oxide growth has significant effects on NBTI
- Wet oxides show worse NBTI degradation then dry oxides
- Fluorine leads to an improvement. F in the gate oxides can significantly improve NBTI and 1/*f* noise performance
- Boron degrades NBTI
- Oxide electric field important

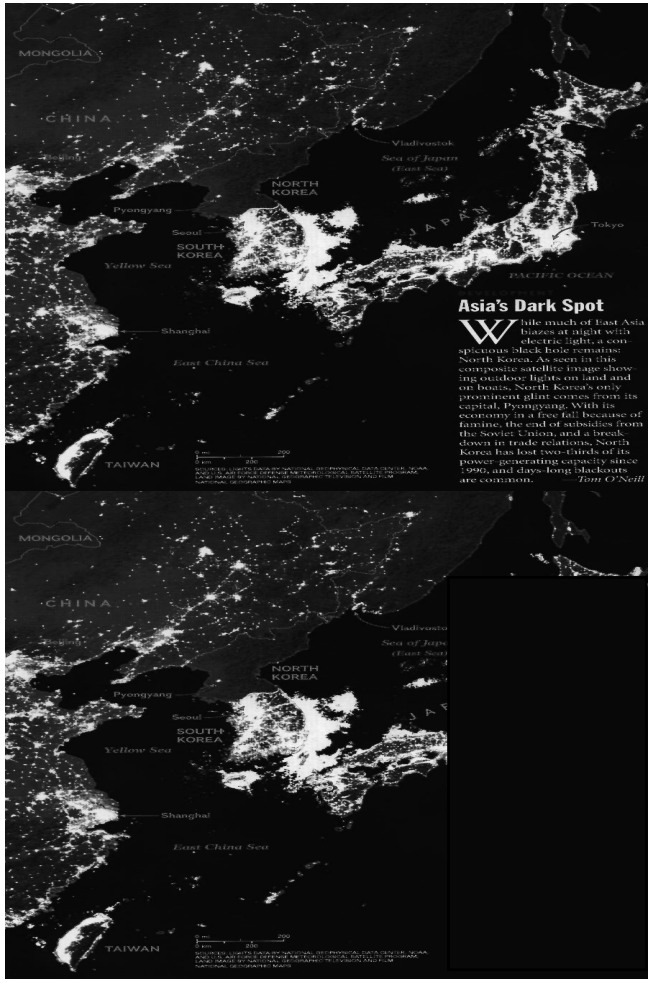
Summary

NBTI

- Can be a significant contributor to *p*-MOSFET degradation in submicron devices
- Needs to be considered during optimization between device reliability and circuit performance
- Sensitive to a variety of process parameters, *e.g.,* hydrogen, nitrogen, fluorine, boron, etc.
- Can occur during *burn in*
- Can occur during circuit operation at elevated temperatures

What Is It?




MONGOLIA
CHINA
NORTH KOREA
Pyongyang
Seoul
SOUTH KOREA
Yellow Sea
Shanghai
East China Sea
TAIWAN
Vladivostok
Sea of Japan (East Sea)
Tokyo
PACIFIC OCEAN
Asia's Dark Spot
While much of East Asia blazes at night with electric light, a conspicuous black hole remains: North Korea. As seen in this composite satellite image showing outdoor lights on land and on boats, North Korea's only prominent glint comes from its capital, Pyongyang. With its economy in a free fall because of famine, the end of subsidies from the Soviet Union, and a breakdown in trade relations, North Korea has lost two-thirds of its power-generating capacity since 1990, and days-long blackouts are common. —Tom O'Neill