# Optical Interconnects for Commercial CMOS

Kevin Lear
Colorado State University
Electrical & Computer Engineering Department
kllear@engr.colostate.edu

IEEE SSCS Technical Seminar
Agilent Technologies, Fort Collins, CO
September 2, 2005

This work has been supported by the NSF GOALI program under contract number ECS-0323493 in collaboration with Agilent.

# Acknowledgments


## CSU

- Prof. Tom Chen (Lead P.I.)
- Matheen Raza (fab, model)
- Charles Thangaraj (design)
- Henry Dittmer (REU)
- Tejkiran Balijepalli (design)
- Adrienne Iguchi (test)
- Bob Pownall (test)
- Guangwei Yuan (modeling, NSOM)
- Other students

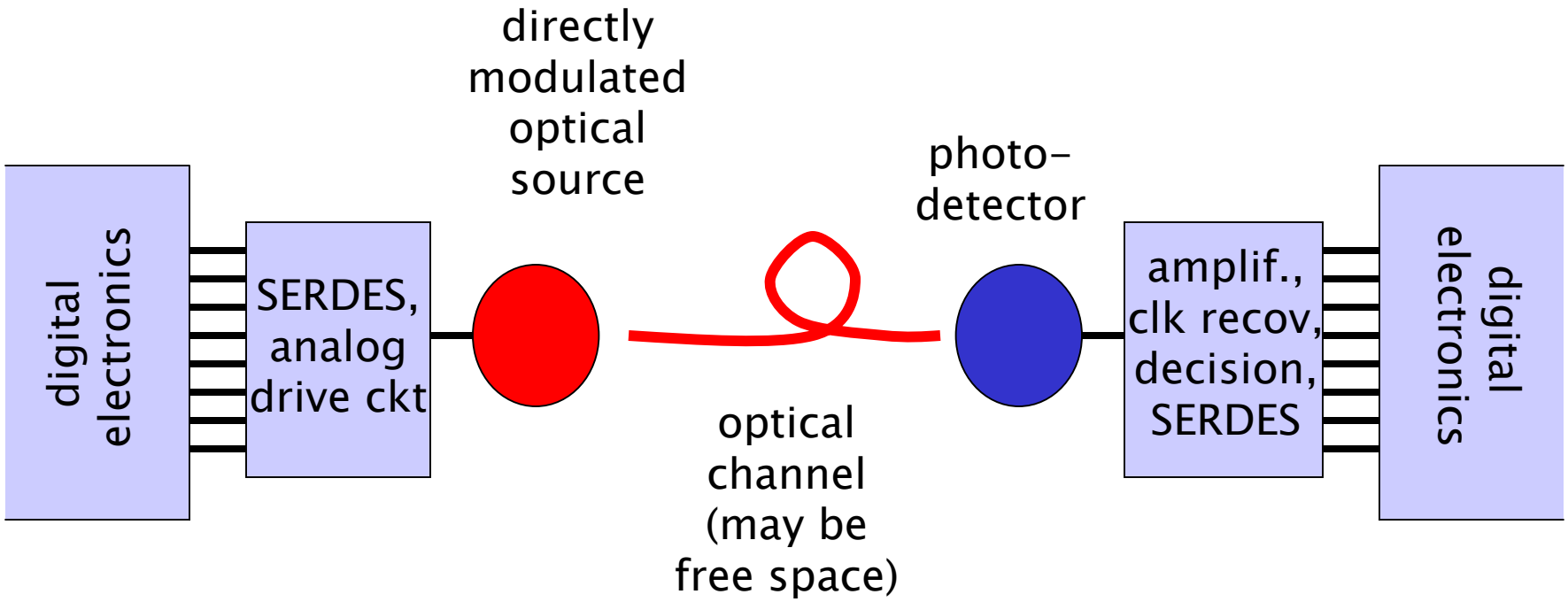
## Agilent

- Phil Nikkel
- Duane Fasen (artwork/mask)
- Glen Taylor (photolith)
- Roger Gehring (etch)
- Brian Defonseka (etch)
- Other fab staff (std. proc.)
- Stan Strathman
- Ceceli Wilhelmi
- Ken Tarbett

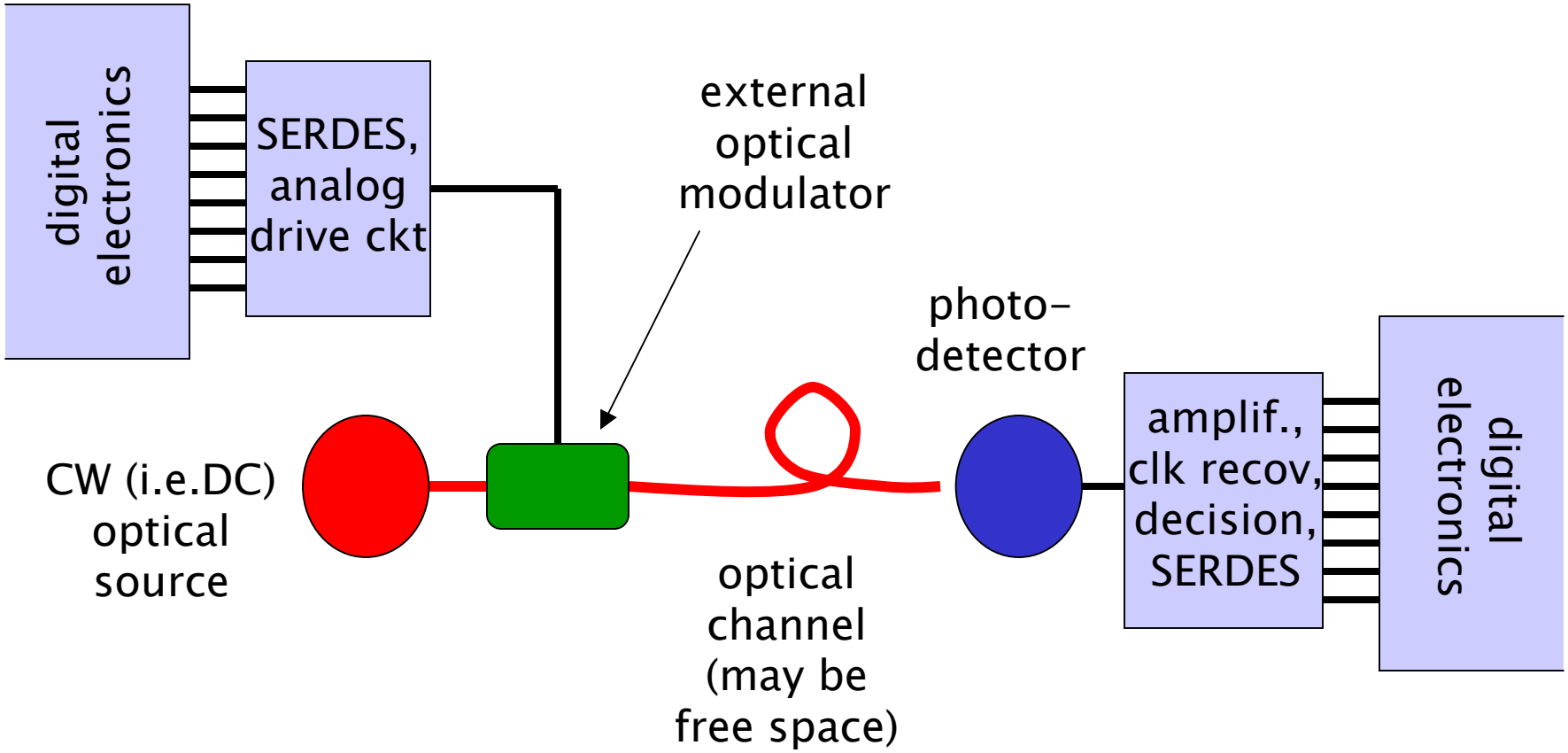
# Outline

- Optical communications background
- On-chip optics motivation and approaches
- CSU-Agilent optical clock chip design and fab
- Initial testing results
- Summary

# Directly Modulated Optical Link



# Externally Modulated Optical Link



# Optical Communication Distance

Optics is progressing to smaller distance applications:

- >100 km: wide area networks (WAN: continental or inter-continental)
- ~10 km: metropolitan area networks (MAN)
- ~1 to 0.1 km: local and storage area networks (LAN & SAN)
- ~10 m: “box to box” in the same room (e.g. telco switch)
- ~1 m: “in the box (or rack)” optical backplane
- ~0.1 m: chip-to-chip optical boards
- ~0.01 m: global on-chip optical interconnects

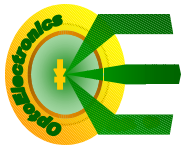
# Optical Communication Advantages

- Low loss
  - Fiber optics ~10 to 0.1 dB/km
  - Planar waveguide ~10 to 0.1 dB/cm
- High bandwidth
  - THz of bandwidth
  - Minimal change in attenuation at 10s of GHz
- High signal velocity (~c/3 or faster)
- Electromagnetic interference immunity
- Isolation / intrinsic impedance matching

# Optical Communication Disadvantages

- Cost
  - Alignment tolerances
  - Non-silicon optoelectronic components
  - Insufficient integration
- Not the incumbent

So a silicon based optoelectronic technology that could be readily integrated with an incumbent technology such as CMOS is very attractive.






Colorado State University

# On-Chip Optics Motivations

- Increasing clock rates and shrinking line width and line spacing are exacerbating the on-chip interconnect bottleneck
  - Takes on the ~10 clock cycles to propagate a signal across a state-of-the-art processor die

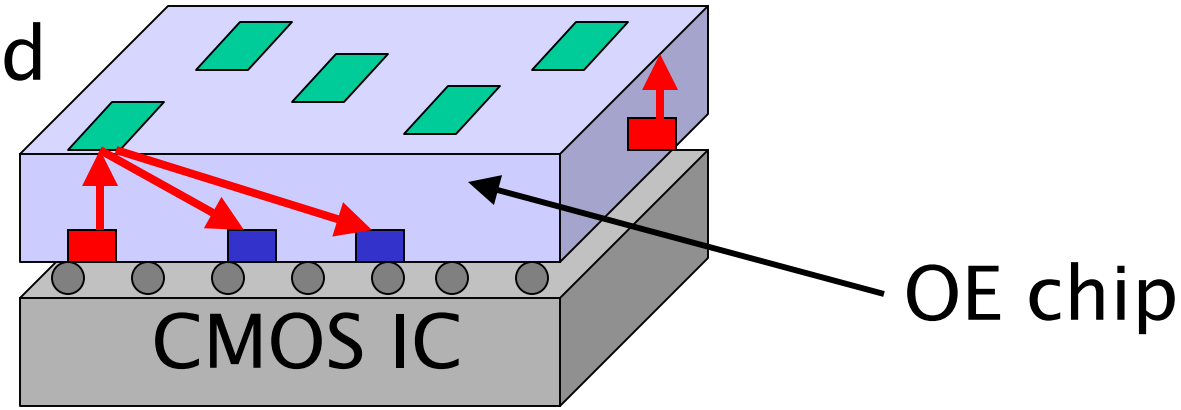
- Desire to bring optical network all the way onto the chip to eliminate intervening optoelectronics chips

# Optical Clock Distribution

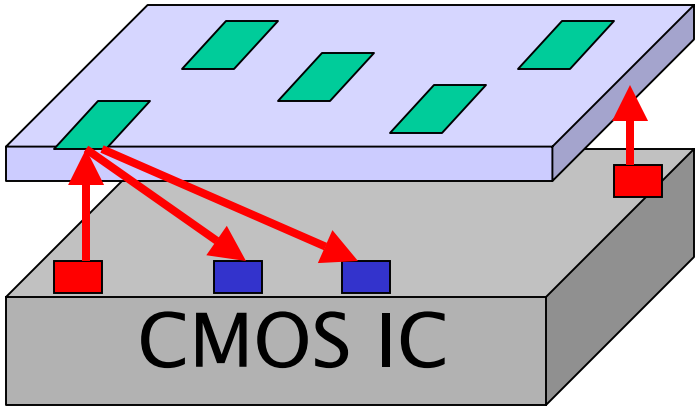
- Eliminates repeater stages
  - Reduces skew due to local process variations in FETs
  - Reduces power consumption
- Good match to optics capability
  - Requires only a single optical source that can be off chip (e.g. a low-jitter mode-locked laser diode).
  - Waveguides and splitters are readily fabricated
  - Photodetectors need to be made with sufficient speed and responsivity

# Integration Approaches

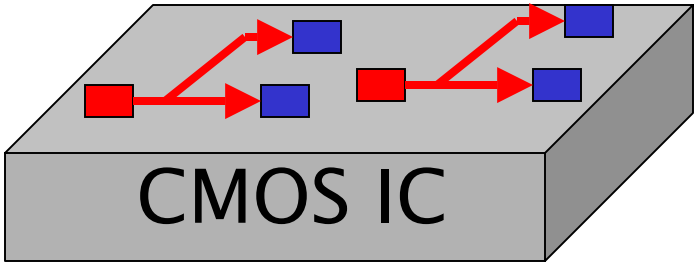
- Hybrid




- Surface normal




- Planar



# CSU-Agilent Approach

- Philosophy: make it as painless as possible for commercial CMOS manufacturers if you want them to adopt it.
- Planar waveguide approach for lower cost packaging
- Use only materials that are already available in CMOS:
  - Waveguide core is SiN use for Cu encapsulation
  - Waveguide cladding is low-k dielectric
  - Detectors are polysilicon used for gates and resistors
  - Put optical interconnect in backend layers where electrical interconnects are.

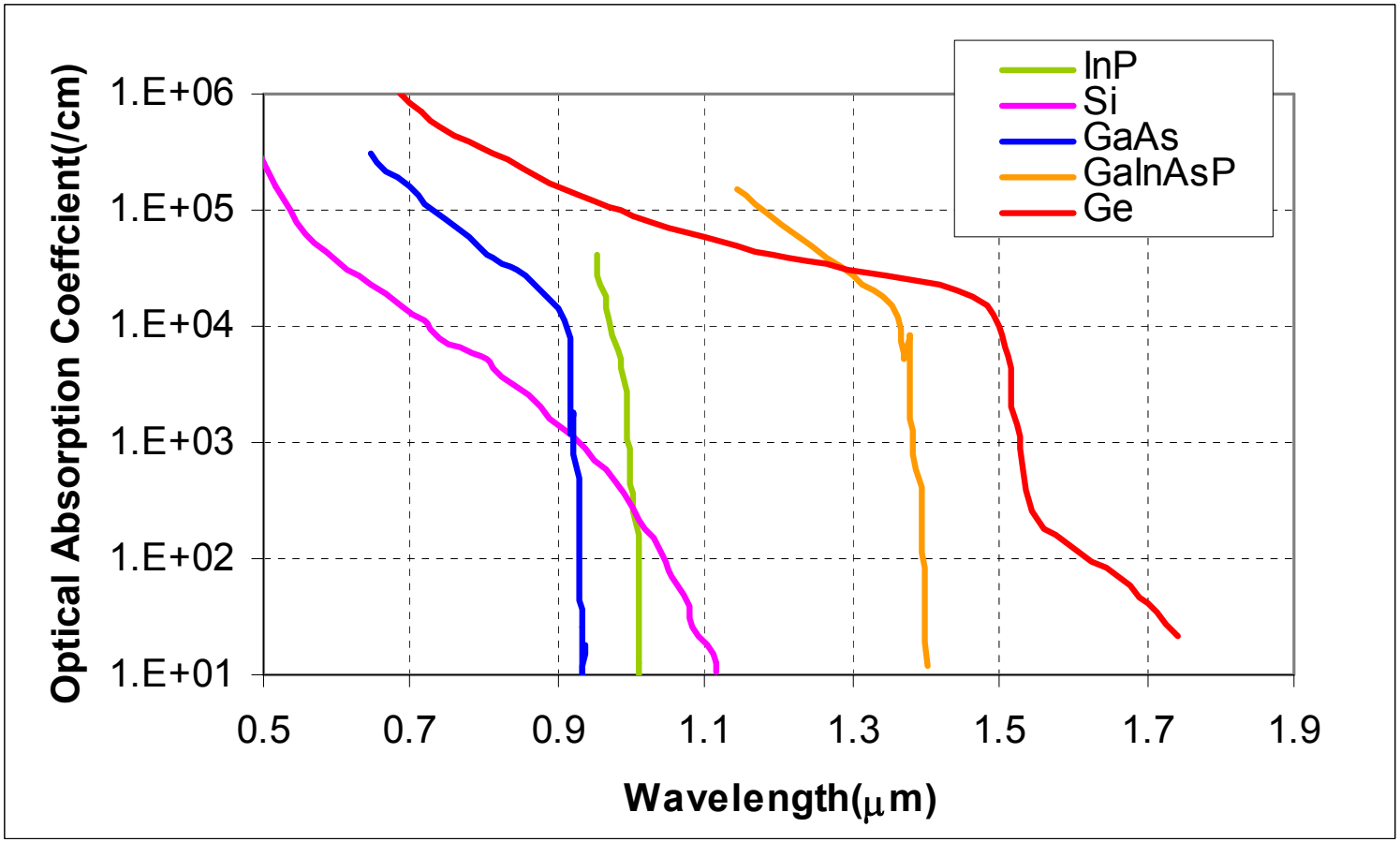
# Materials / Wavelength Choices

- $\lambda$=1310 or 1550 nm
  - Waveguides can be $SiO_2$, SiN, or poly-Si
  - Detector must be an absorbing material at this wavelength, e.g. Ge or SiGe
  - Allows compatability with long-haul networks
- $\lambda$=650 to 980 nm
  - Waveguides can be $SiO_2$, and SiN
  - Detector can be Si or poly-Si
  - May allow compatability with local area networks

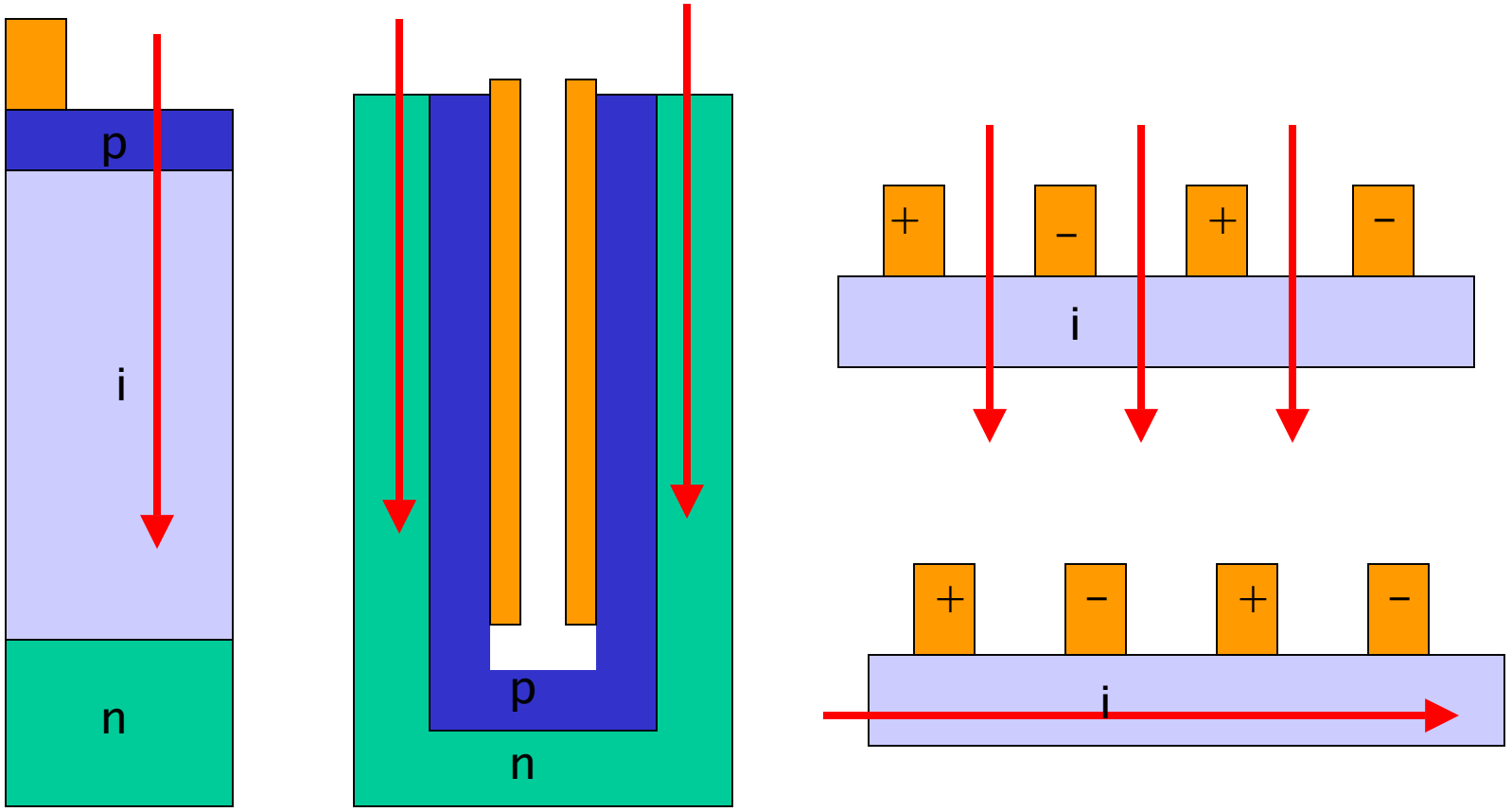
# Silicon based light sources?

- Rare earth doped glass or Si
- Porous Si
- Raman lasers in Si
- External “optical power supply”

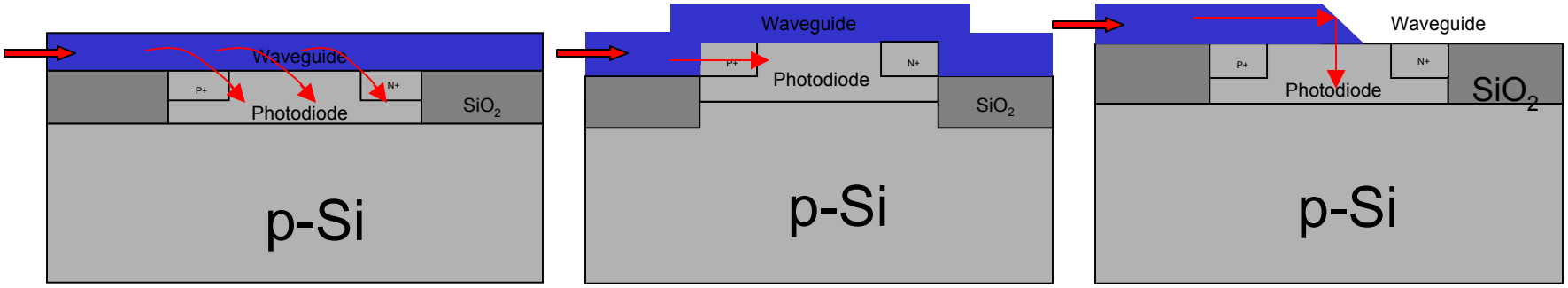
# Semiconductor Absorption Coefficients



# Silicon Photodiode Structures



# Prior Monolithic CMOS Approaches




Leaky mode coupled photodiode | End coupled photodiode | Micromirror coupled photodiode

[1] U. Hilleringmann and K. Goser, "Optoelectronic System Integration on Silicon: Waveguides, Photodetectors, and VLSI CMOS Circuits on One Chip", IEEE transactions on Electron Devices, Vol. 42, No. 5, May 1995

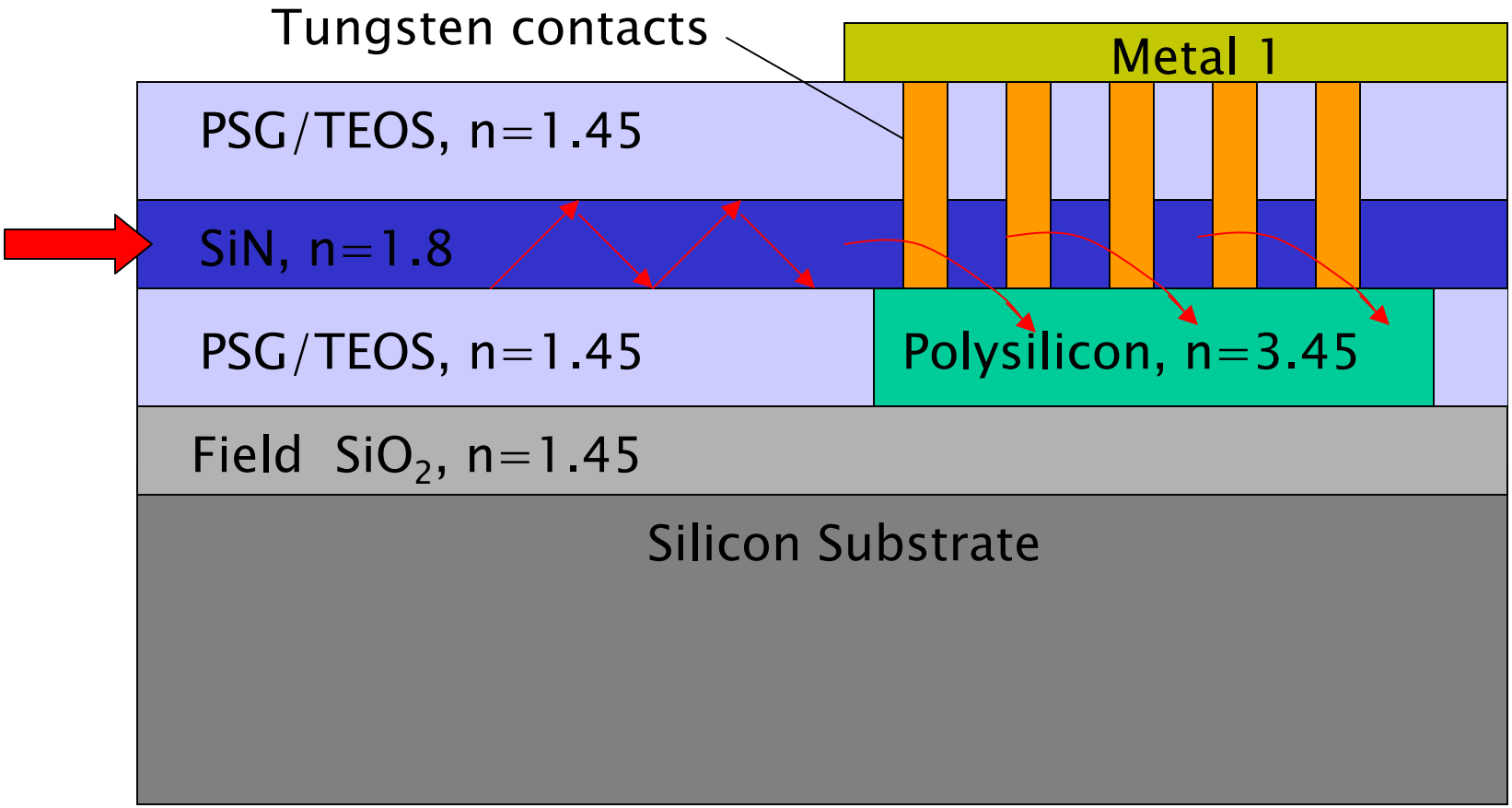
- Low responsivity (12 mA/W)
- Intervening PSG layer

- Low responsivity (12 mA/W)
- Scatter at waveguide step

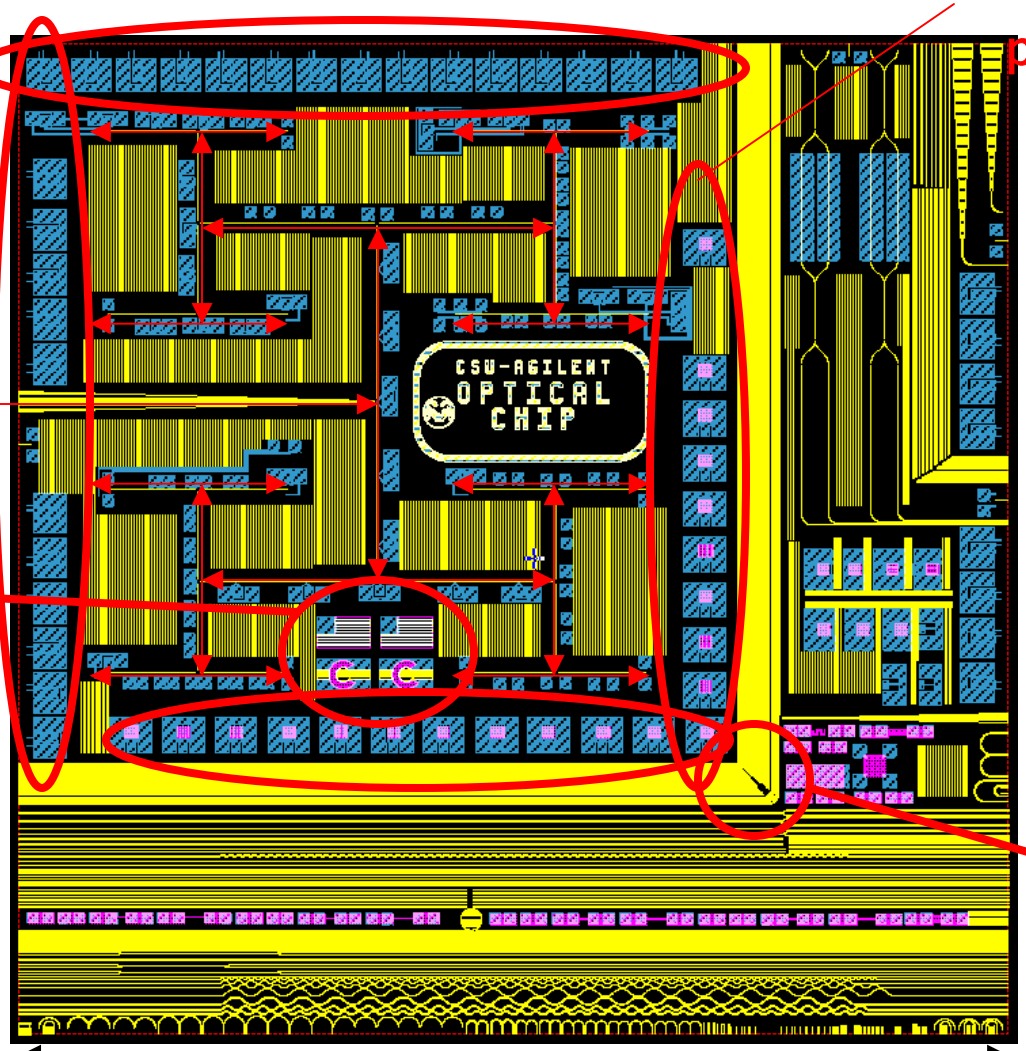
- 30 mA/W responsivity
- requires micro mirrors

- Time response is limited by carriers that are generated in the silicon bulk
- Cross talk due to noise coupling through substrate
- Solution: use isolated polysilicon MSM photodetectors

# Waveguide and Detector Fabrication



# First Generation Chip Layout




waveguide photodetectors

normal MSM photodetectors

H-tree

other test structures

flags

other test structures

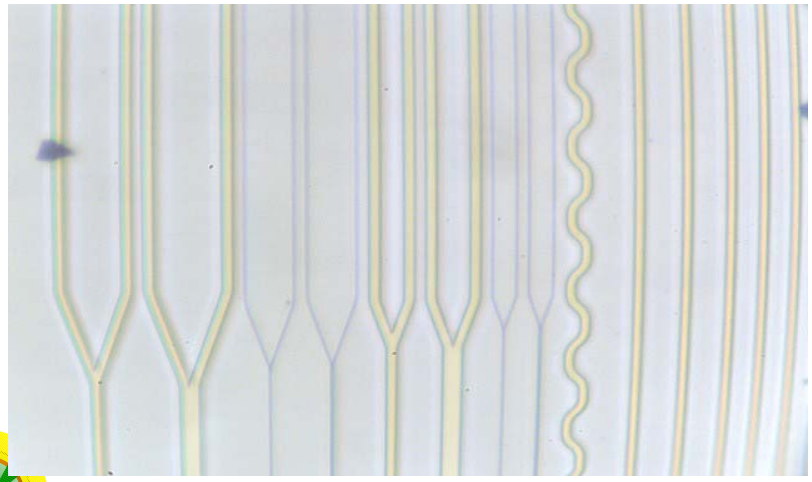
L-bends

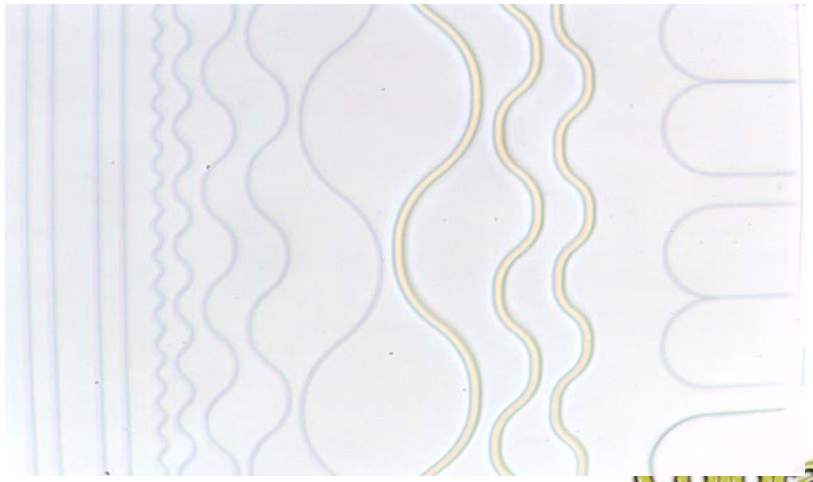
# Waveguide Test Structures

L-bends

splitters

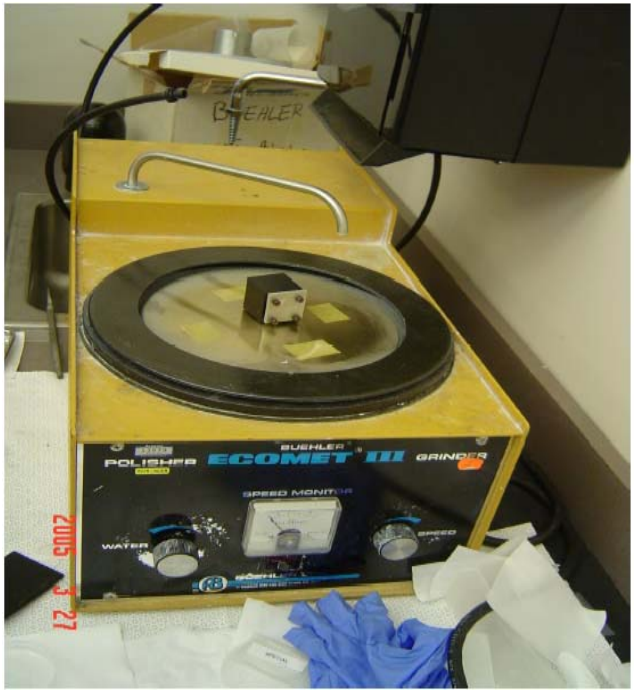
“wigglies”



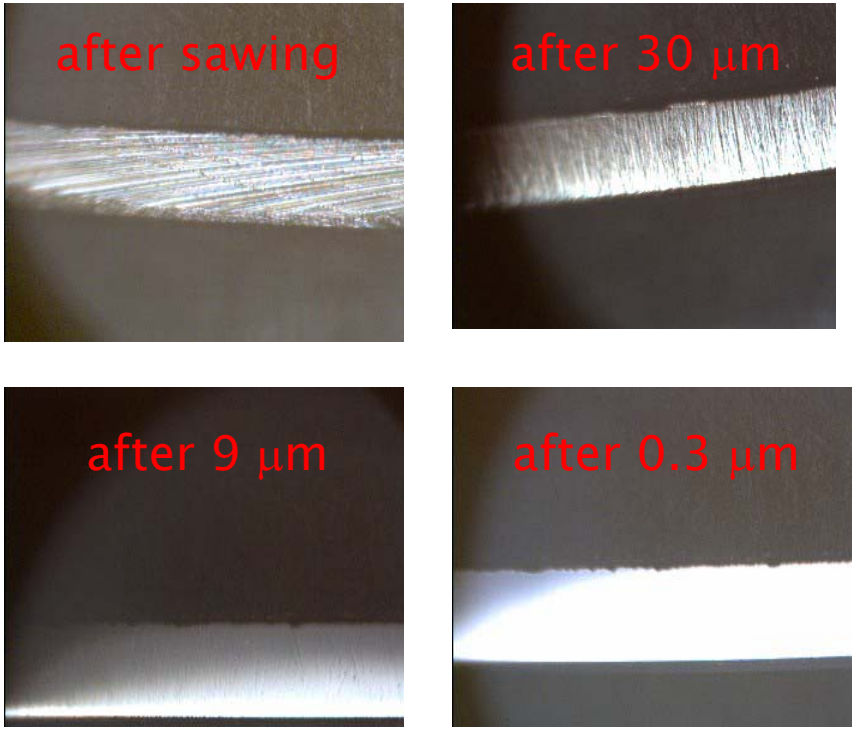


# Edge Polishing

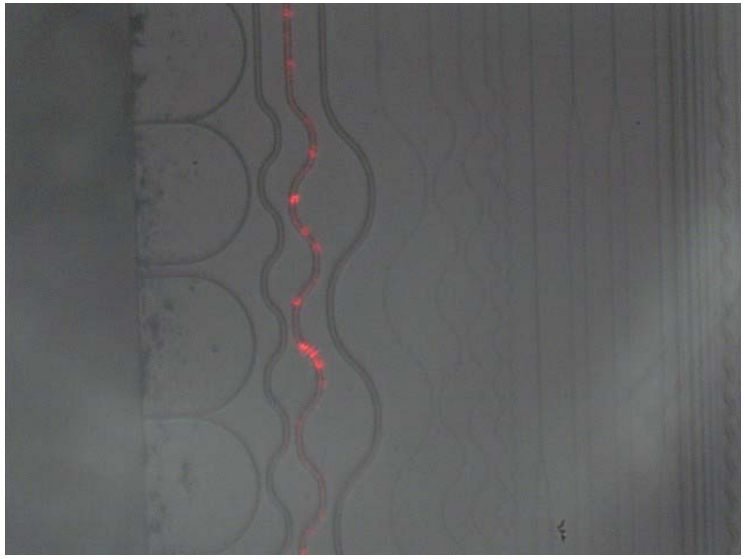
- After dicing, necessary to edge polish

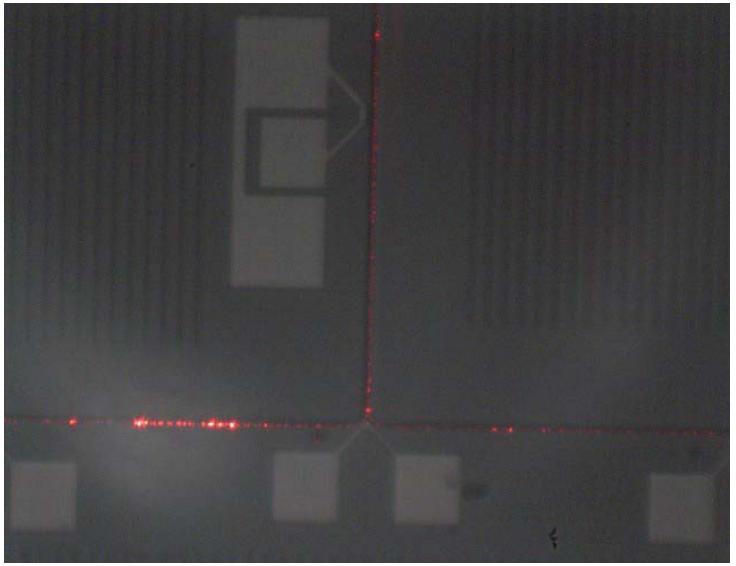



Thanks to Susan Hunter
for arranging donation.

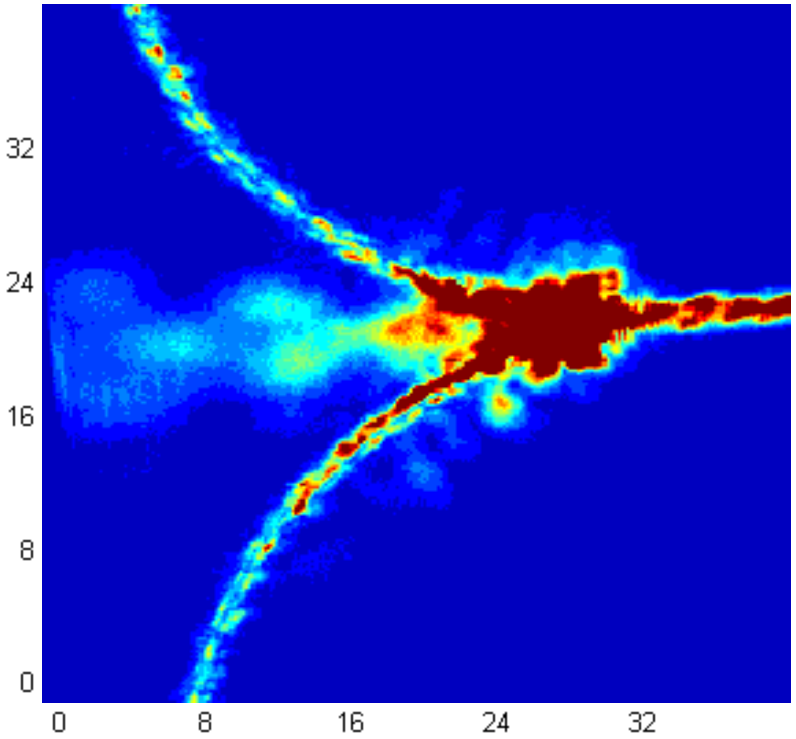


# Light coupled into waveguides





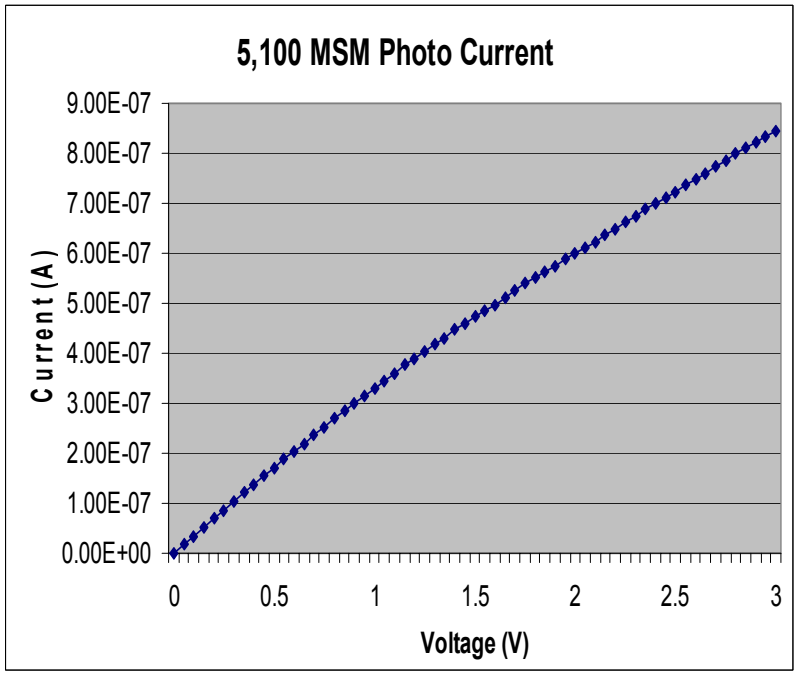
# Near-Field Scanning Optical Microscopy of Splitter Structures

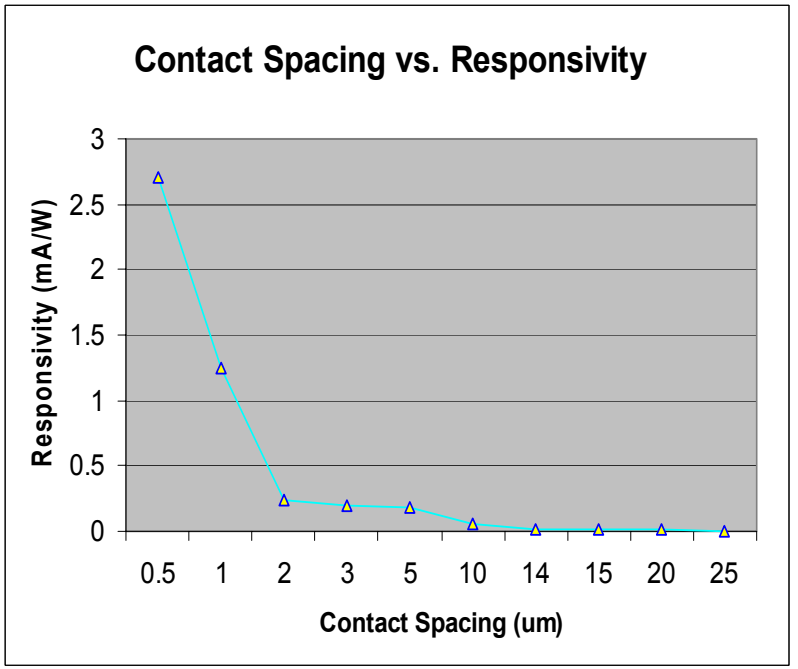



2 μm wide to 2x 1 μm wide Y-splitter

- NSOM measures evanescent field
- Mode beating and scatter are seen
- Can detect power levels
  - Excess splitting loss=2.4dB
  - Branching ratio=0.7dB

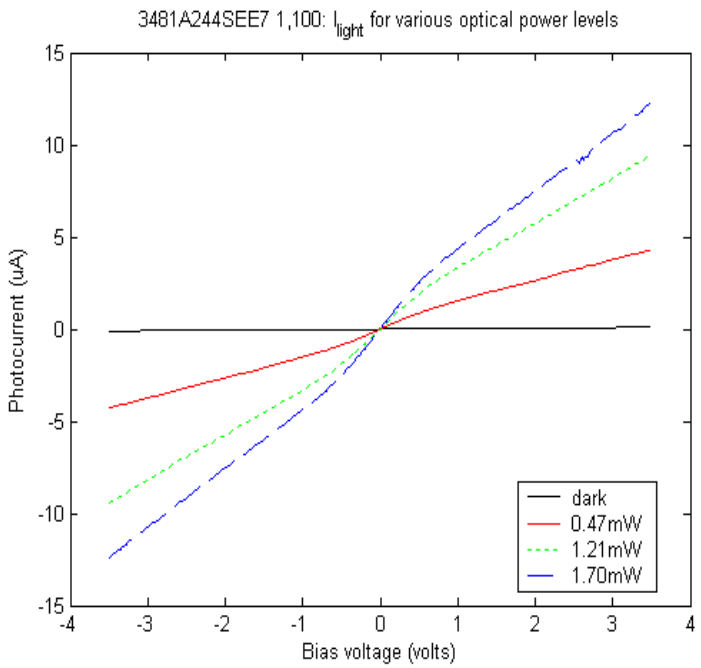
# MSM Photodiode Results

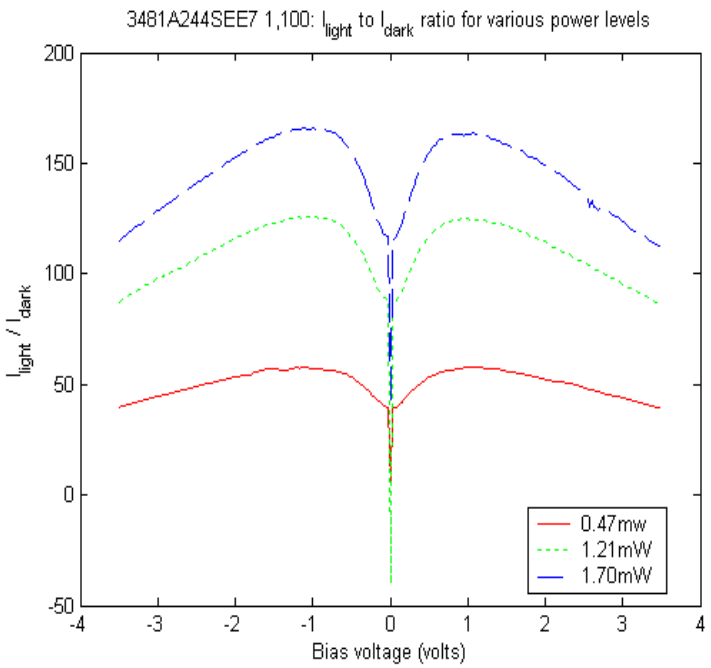



- Linear I vs. V with R dependent on power level
  - Photoconductivity
  - Low carrier collection efficiency
- Responsivity at 3V is ~0.003 A/W

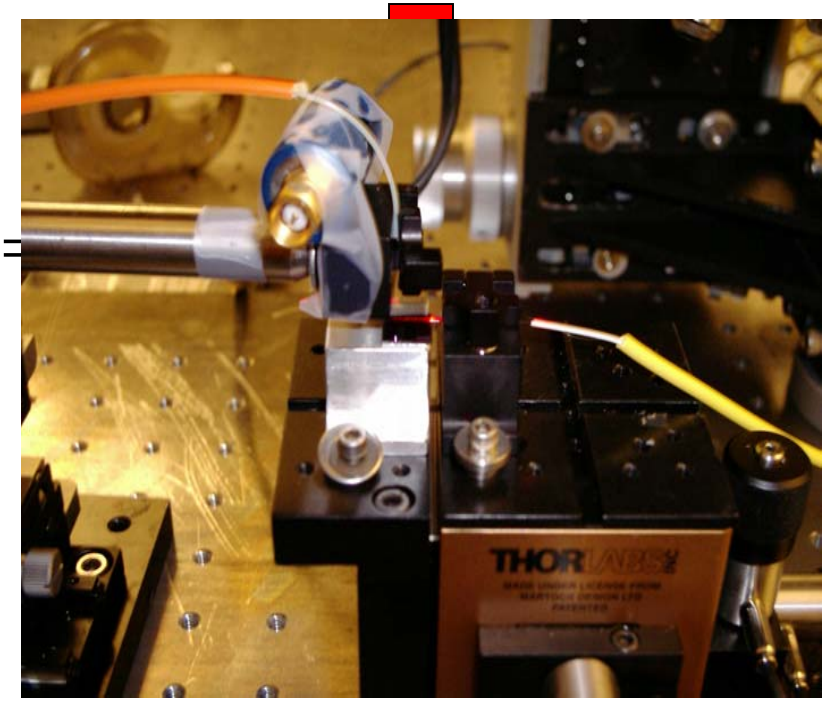
# MSM Photodiode Results



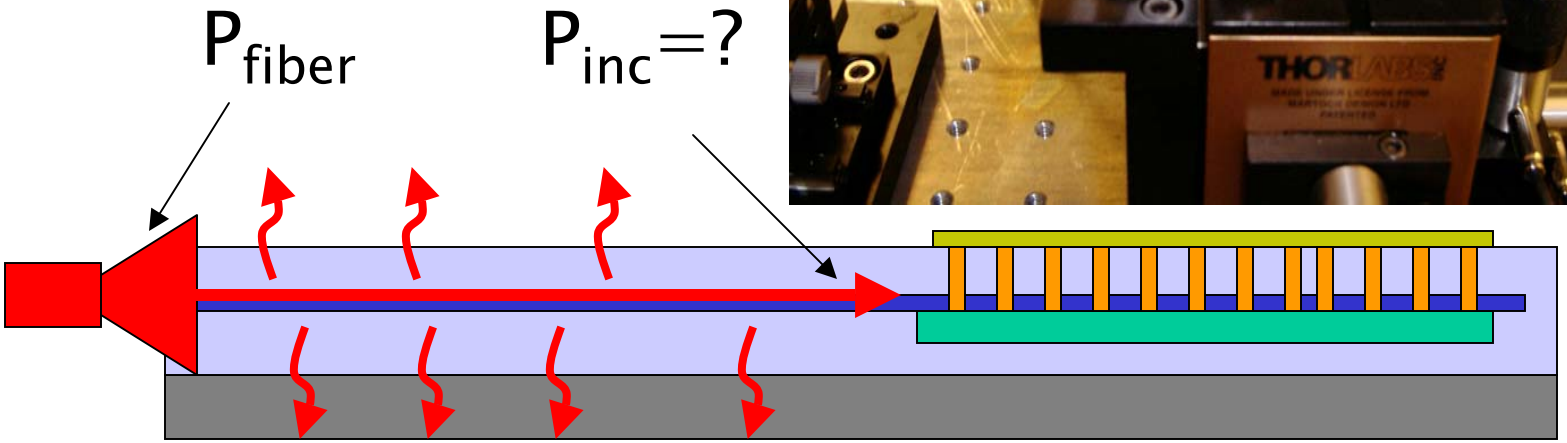




- Responsivity at 3V is ~0.01 A/W at low powers, but saturates at higher powers

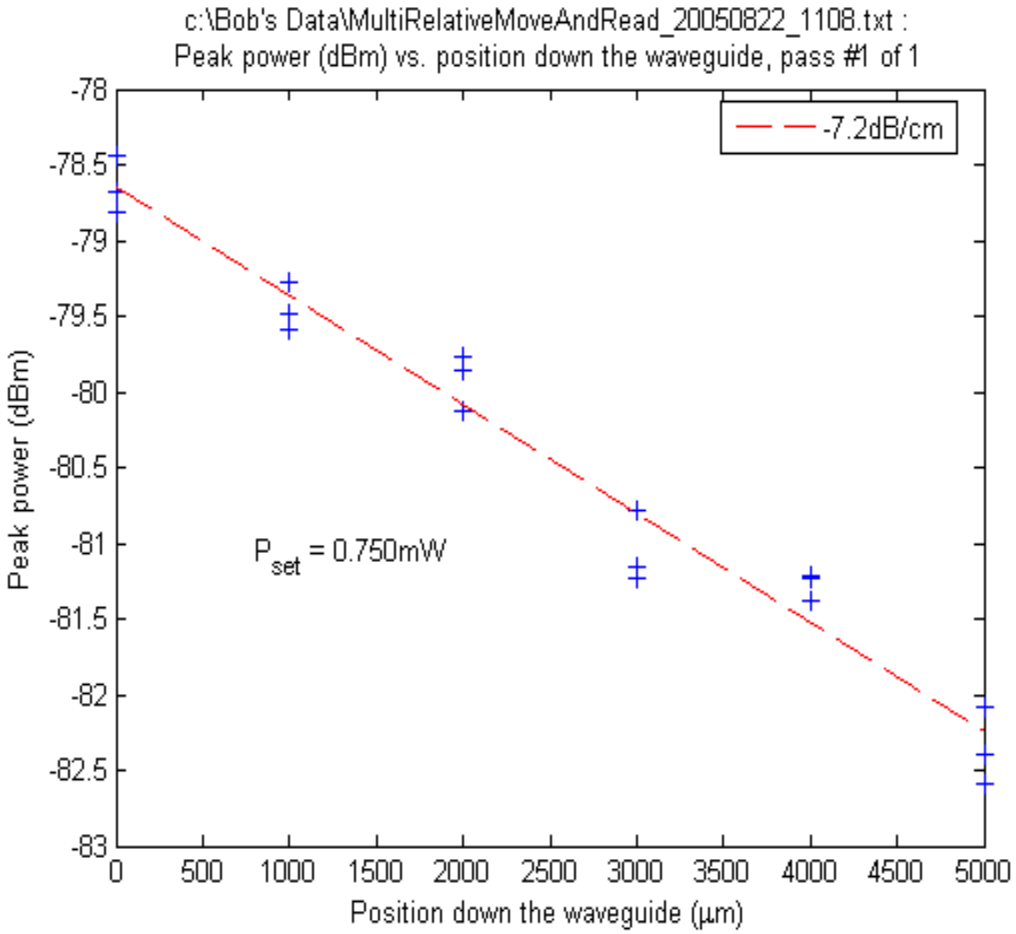
# Photodiode Testing Configurations




$P_{fiber}$ =



# Waveguide loss results

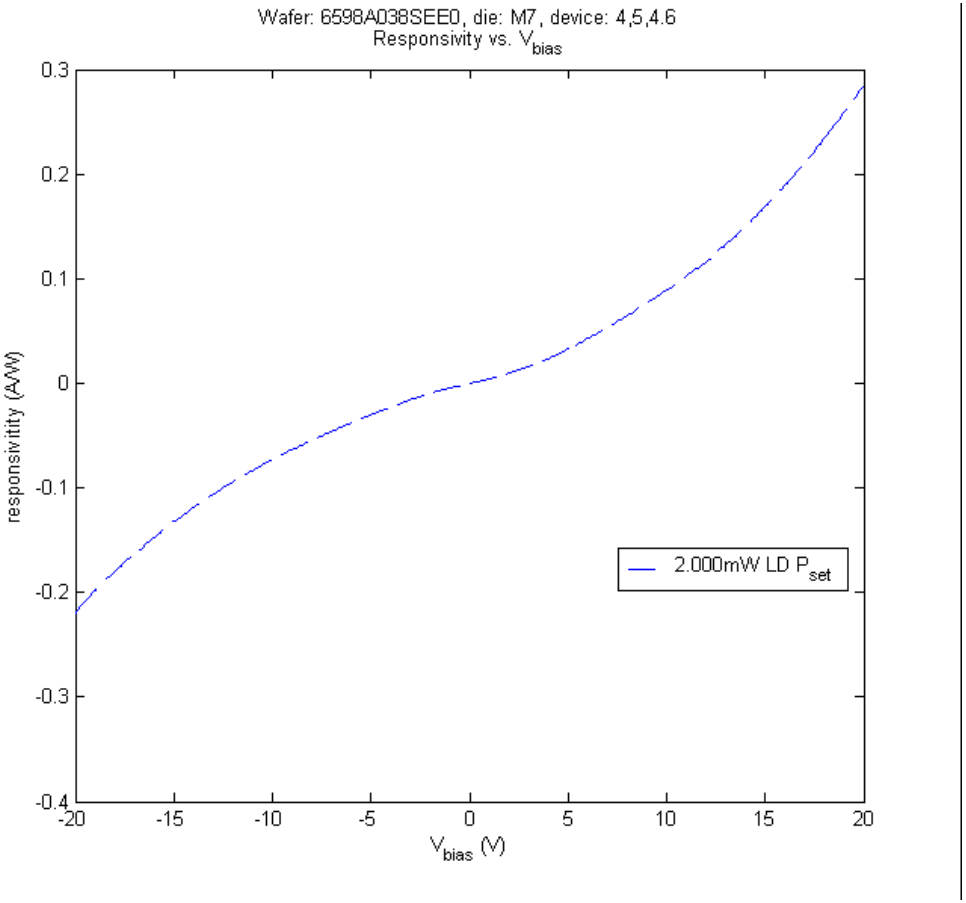


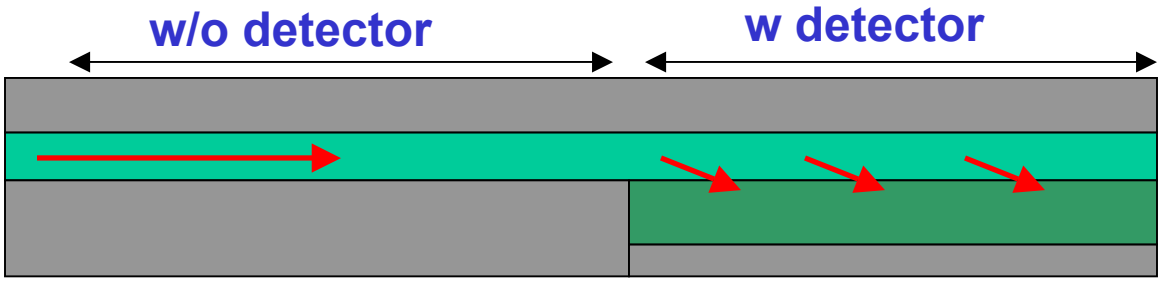

Loss of ~8dB/cm for 4 µm wide WG is high

Loss increases as width decreases implying CMP roughness is less than sidewall roughness

# Waveguide Photodiode Responsivity

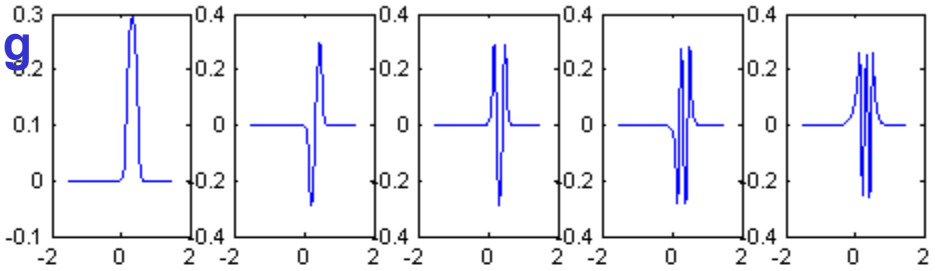
- R=0.2A/W at 20V for 5 μm long detector with 2 μm contact spacing
- Longer detectors with smaller contact spacing should give 0.2A/W at 5-10V bias

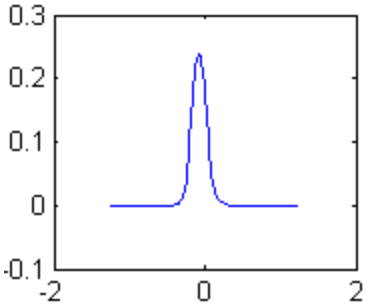




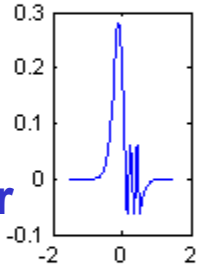

$SiO_2$ 250nm
$SiN_x$ 350nm
Poly Si 400nm

Quick damping Modes 15%





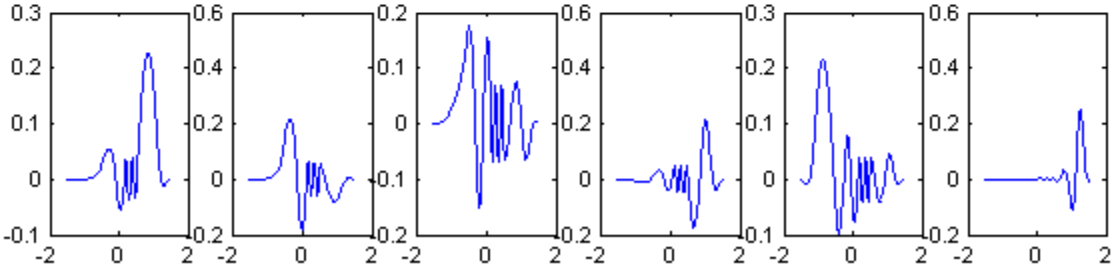
Leaky mode 85%



Attenuation coefficient =4.3dB/10μm
For the leaky mode, comparing with Experimentally obtained value 5.5dB/10μm

Major power preserved

Scattering Modes 5%



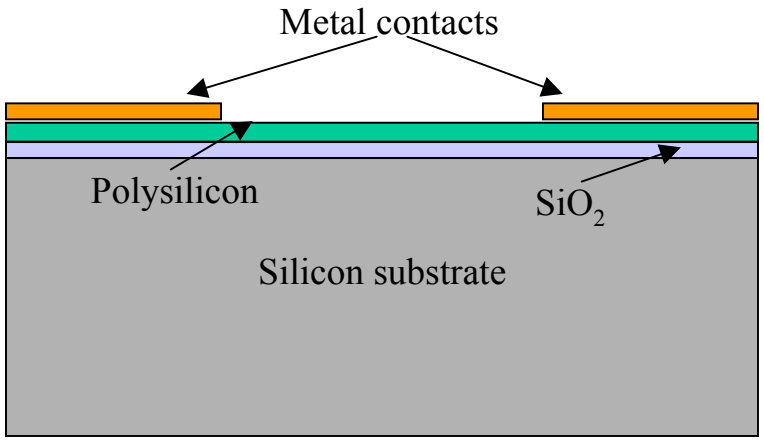
...

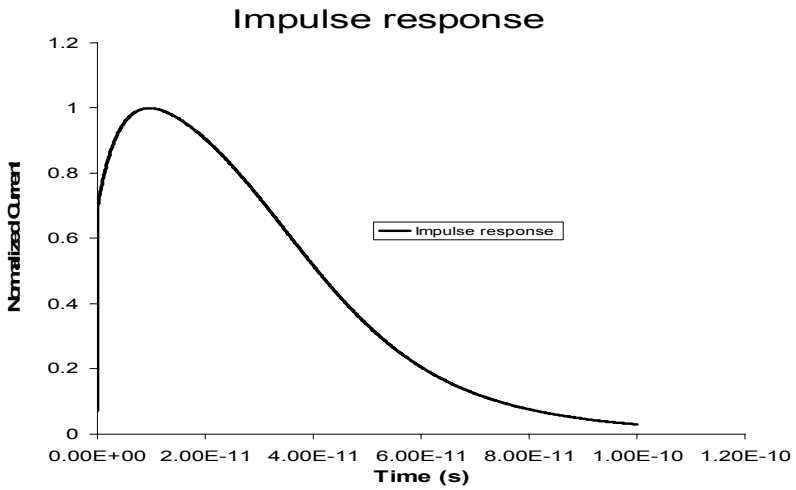
Mode in WG w/o detector

Modes in WG with detector

# Temporal Response

- Simulated using ISE's TCAD



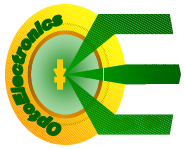

- Impulse response simulated for a 1 fs pulse imput pulse at 780 nm
- $\mu_n$= 100 $cm^2$/ V-s, $\tau_n$=$10^{-9}$s, 1 μm grain size assumed in this case
- For a contact spacing of 1 um, the FWHM is 40.4 ps, corresponding to a device 3-dB bandwidth of 12.3 GHz

# Lessons Learned

- Waveguide and detectors worked well enough for the first generation chip characterization
- Waveguide loss is high, probably due to sidewall roughness, but acceptable
- Need to redesign splitters for lower loss, perhaps more defect tolerant
- Characterizing waveguide photodiode responsivity is difficult
- Need to use longer waveguide photodetectors to allow sufficient leaky mode coupling

# Summary

- There is a developing need for on-chip optical interconnects in CMOS
- Planar, silicon based optoelectronics using standard CMOS materials is most likely to be adopted
- We have successfully demonstrated prototype components for on-chip optical clock distribution using Agilent's CMOS processes
- We should be able to achieve 16-node optical clock distribution in a second generation chip with less than 1 mW of optical power.






Colorado State University