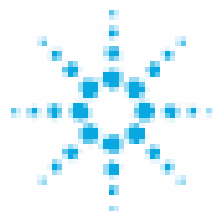


A Versatile Low-Jitter PLL in 90nm CMOS for SerDes Transmitter Clocking

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T. Cynkar, A. Volz, J. Pfiester, R. Martin, R. Miller,
D. Hood, G. Motley, E. Rojas, T. Walley & M. Gilsdorf**

Enterprise ASIC SerDes R&D

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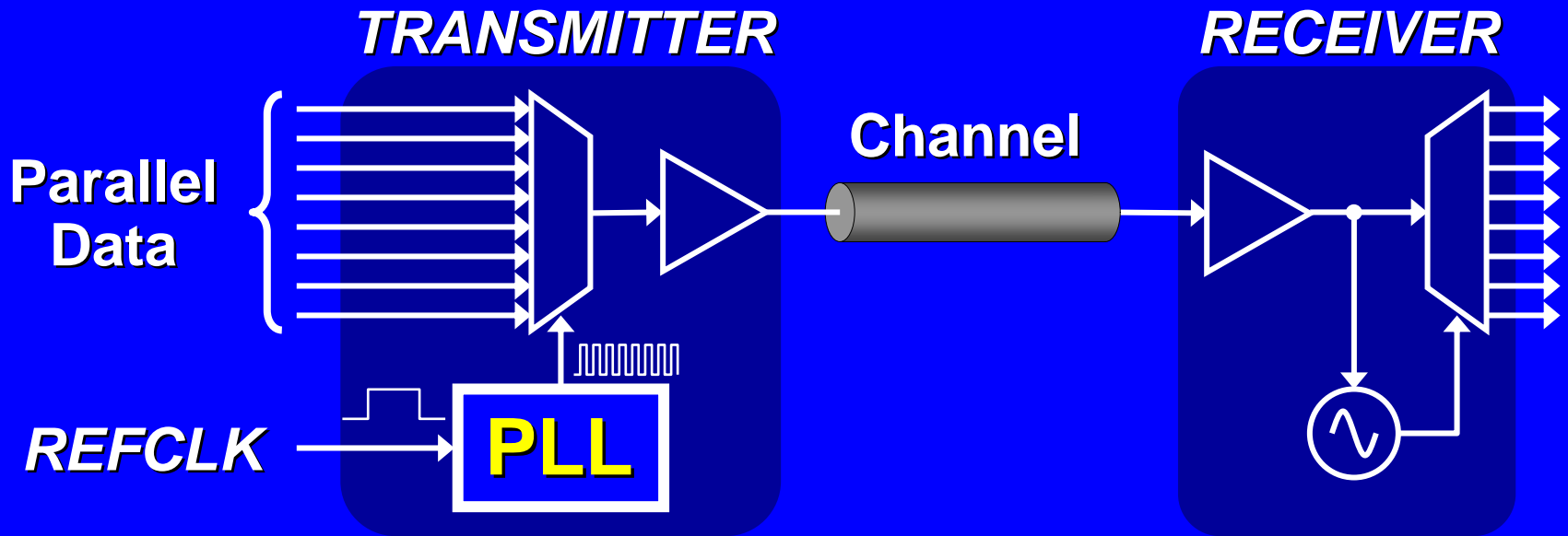


Agilent Technologies

Outline

- **Objective**
- **Dual-Path PLL Architecture**
- **Design Considerations**
- **Measurements**
- **Performance Summary**
- **Conclusions**

Objective

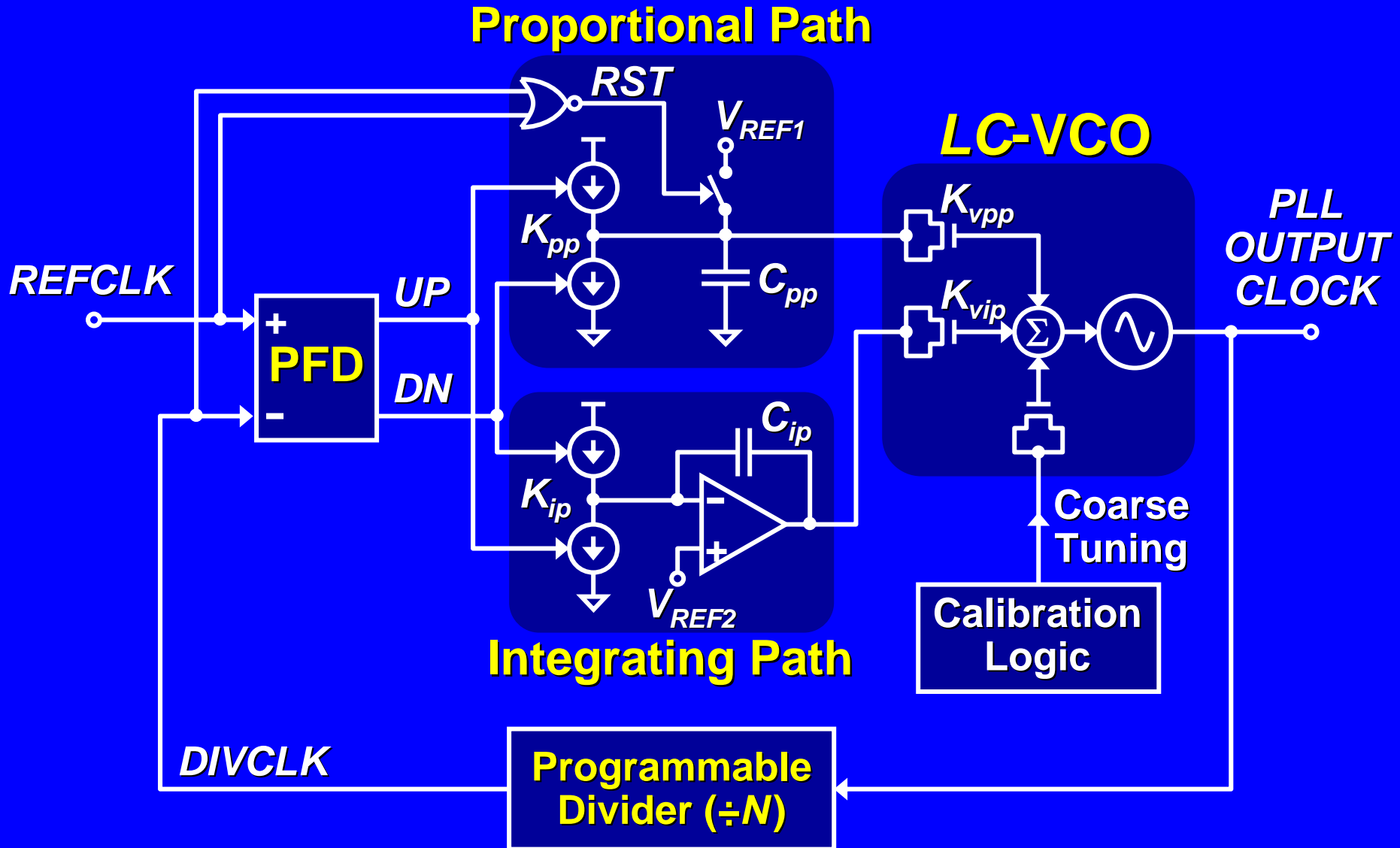


- **Tx clocking for embedded wireline SerDes applications** (Ethernet, FibreChannel, PCIe, SAS/SATA, XFI, SONET, ...)
- Support of multiple rates, protocols & reference clock frequencies per Tx-Rx channel
- Backward compatibility with existing serial links
- **Strategy: flexible loop dynamics, wide tuning range, versatile divider configurations & small size**

Outline

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Dual-Path PLL Architecture



PLL Closed-Loop Dynamics

Transfer function has 1 zero (z) & 2 poles (p_1 & p_2)

$$H(s) \approx \frac{\omega_n^2}{z} \cdot \frac{s + z}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\zeta = \frac{K_{pp} K_{vpp}}{2 \sqrt{N \frac{K_{ip} K_{vip}}{C_{ip}}}} \quad \omega_n = \sqrt{\frac{K_{ip} K_{vip}}{C_{ip} N}}$$

For overdamped case ($\zeta > 1$), z cancels p_1

$$\omega_{-3dB} \approx -p_2 \approx 2\zeta\omega_n = \frac{K_{pp} K_{vpp}}{N}$$

bandwidth

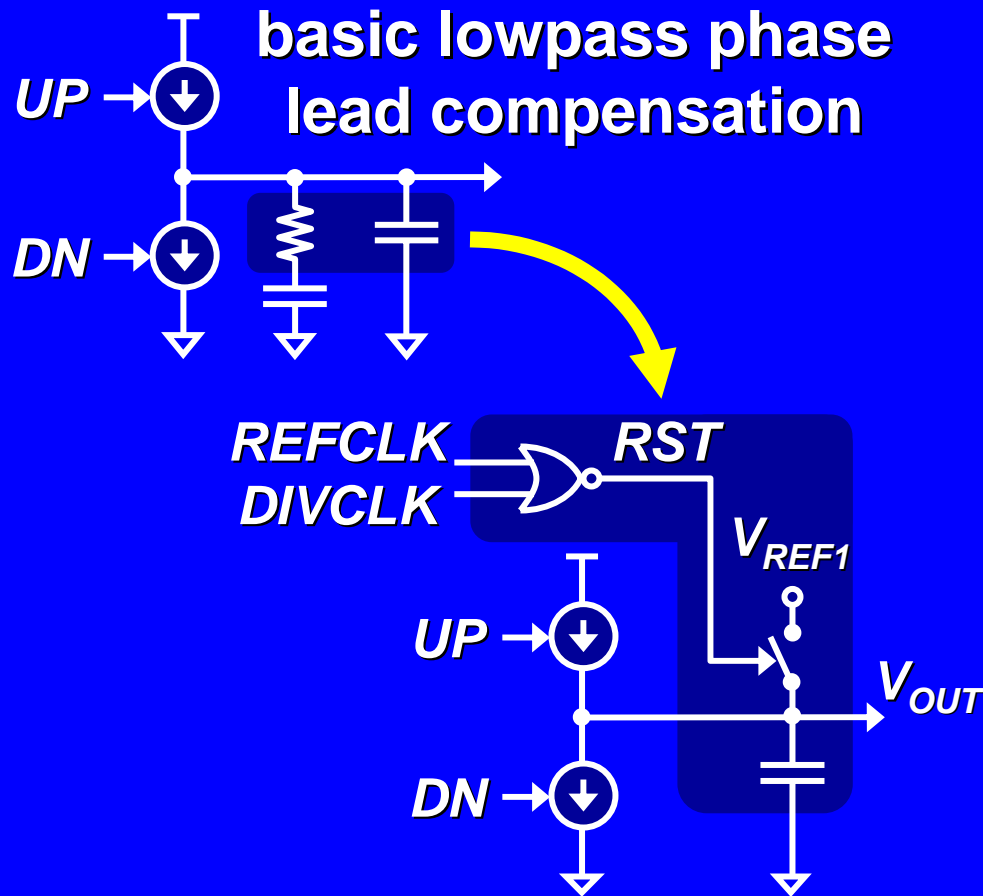
$$\zeta \propto \frac{K_{pp}}{\sqrt{K_{ip}}}$$

inverse peaking

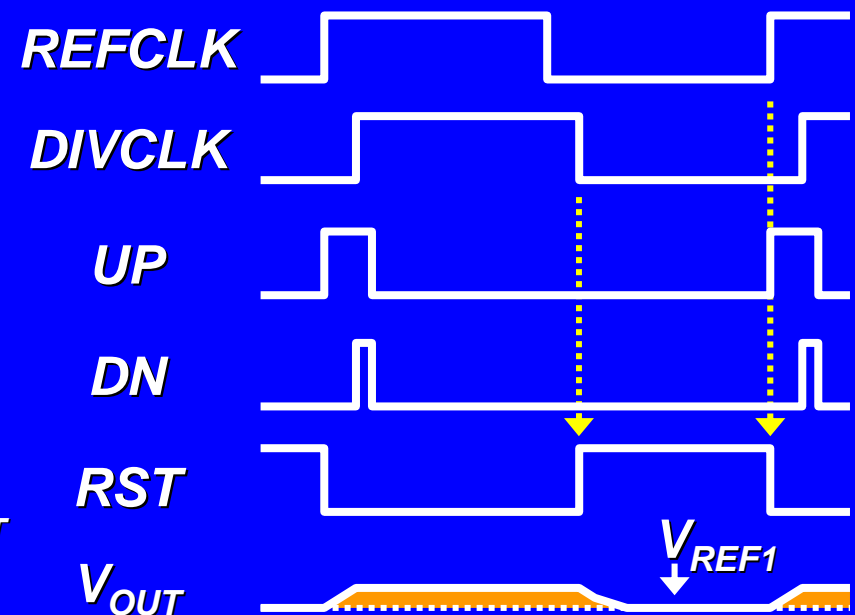
Outline

- Objective
- Dual-Path PLL Architecture
- **Design Considerations**
 - Loop Filter Proportional Path
 - Mismatch in Loop Filter Phase Offsets
 - *LC-VCO* Architecture
 - Inversion-Mode nFET Varactors
 - Tuning Range Factors
- Measurements
- Performance Summary
- Conclusions

Loop Filter Proportional Path

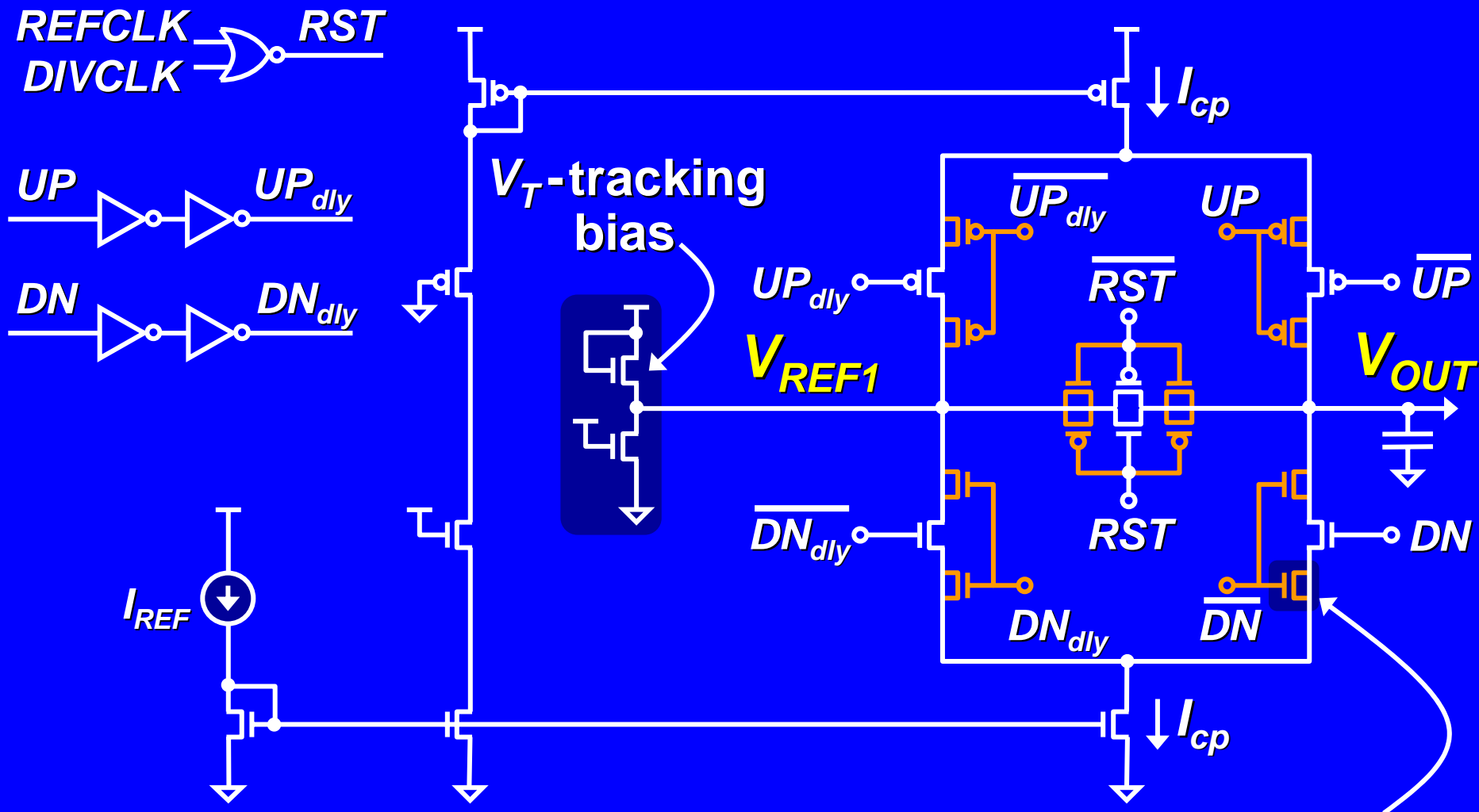


Timing Diagram



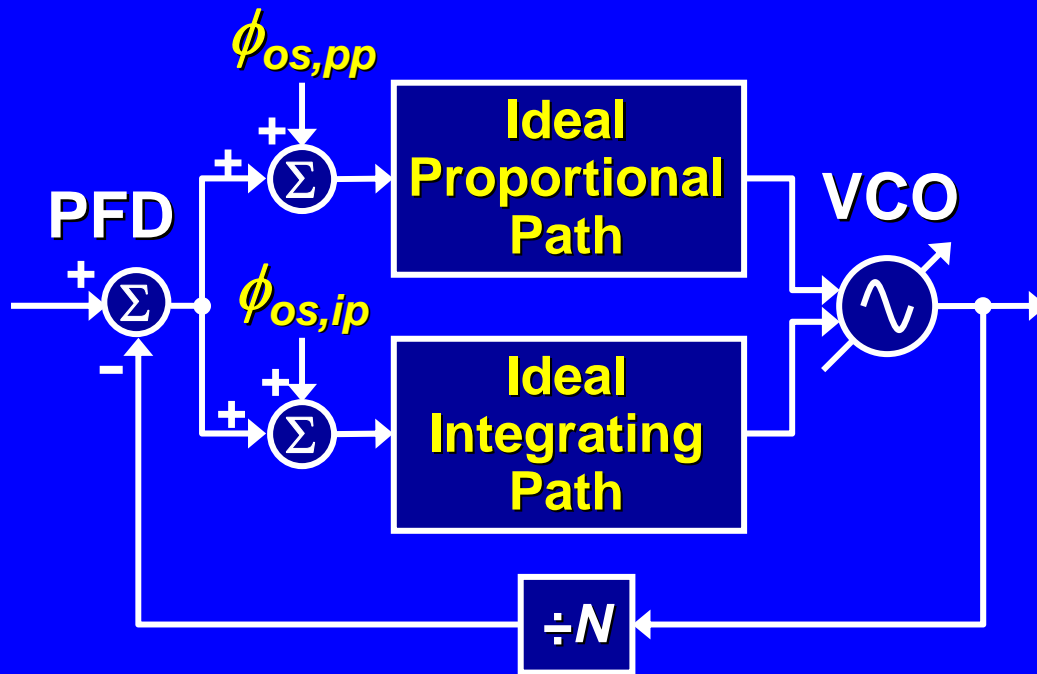
- Stretch V_{OUT} pulse in time to reduce reference spur
- V_{OUT} pulse $\sim 50\%$ duty cycle, independent of divider ratio
- Resistorless \rightarrow area-efficient

Proportional Path Implementation

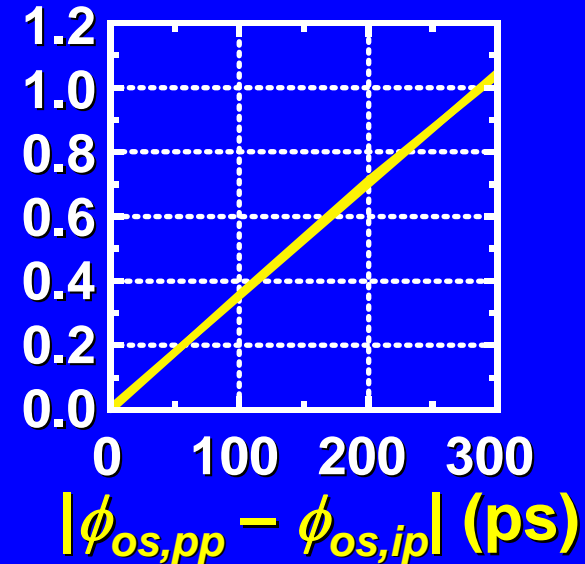


W/2 switch feedthrough & charge cancellation FETs

Effect of Mismatched Loop Filter Phase Offsets

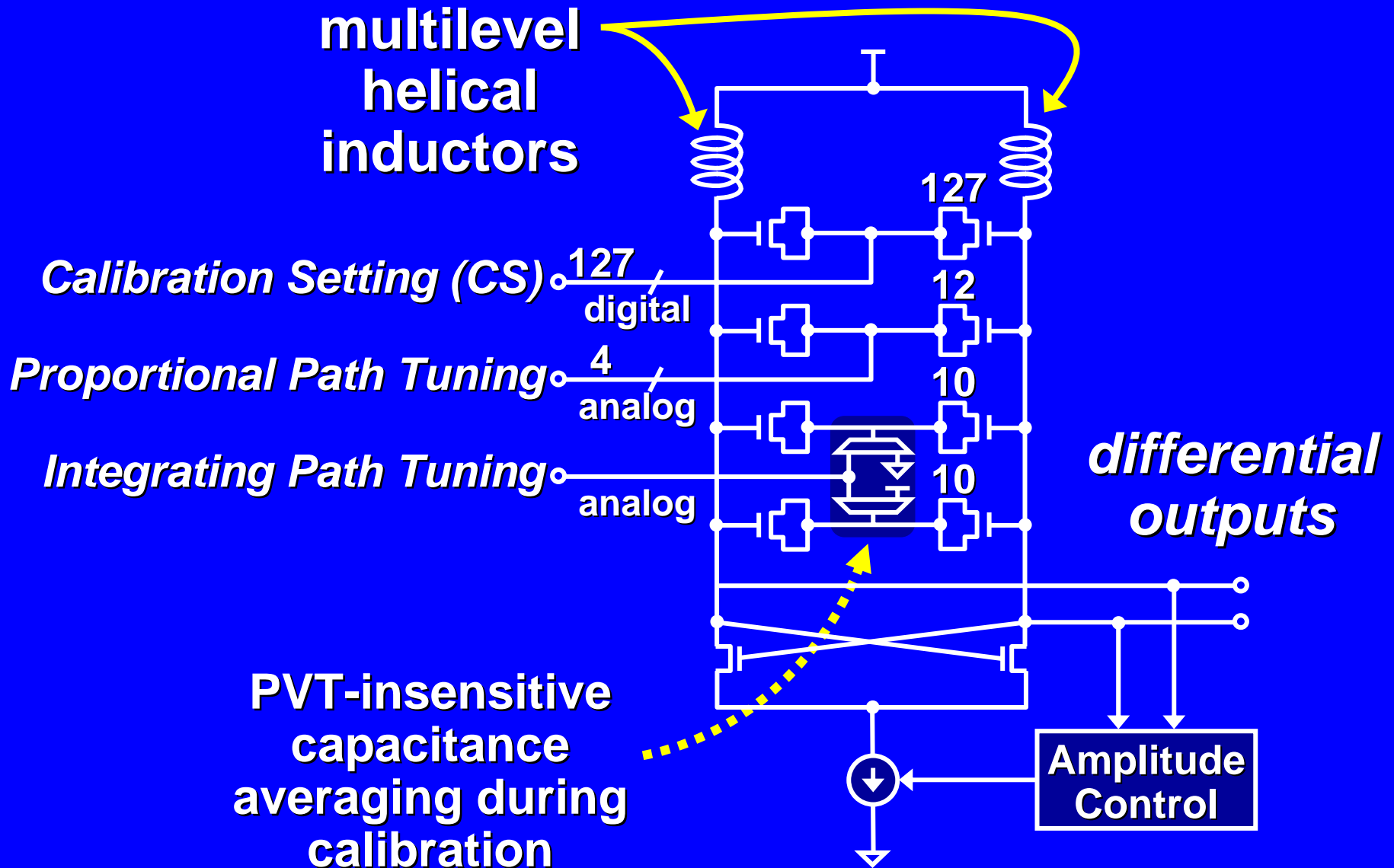


Simulated PLL
RMS Jitter (ps)

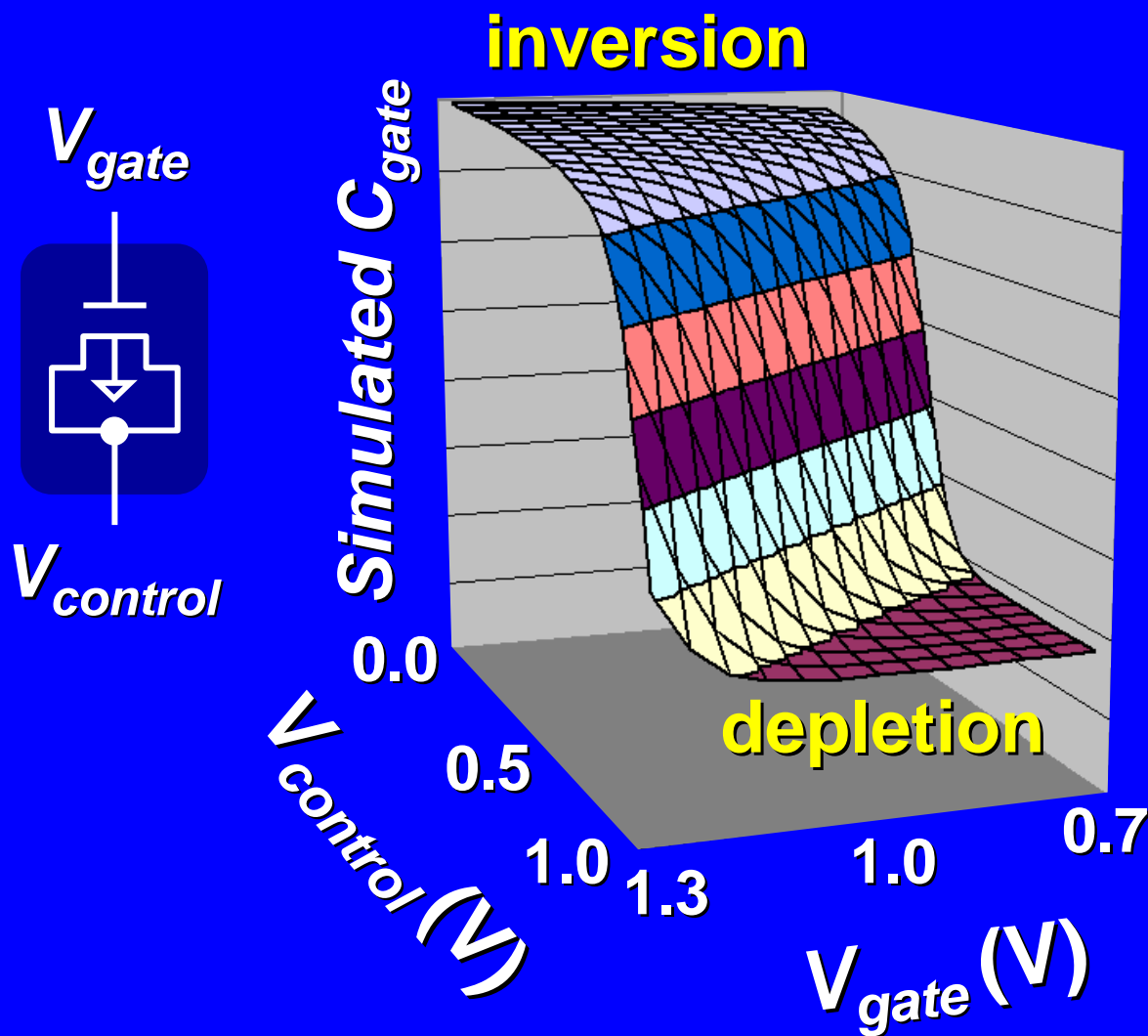


- Minimize ϕ_{os} mismatch between all loop filter paths to reduce PLL jitter
- Charge pump dynamic range issue: need big switches for large I_{cp} but may compromise ϕ_{os} at small I_{cp}

LC-VCO Architecture



Inversion-Mode nFET Varactors

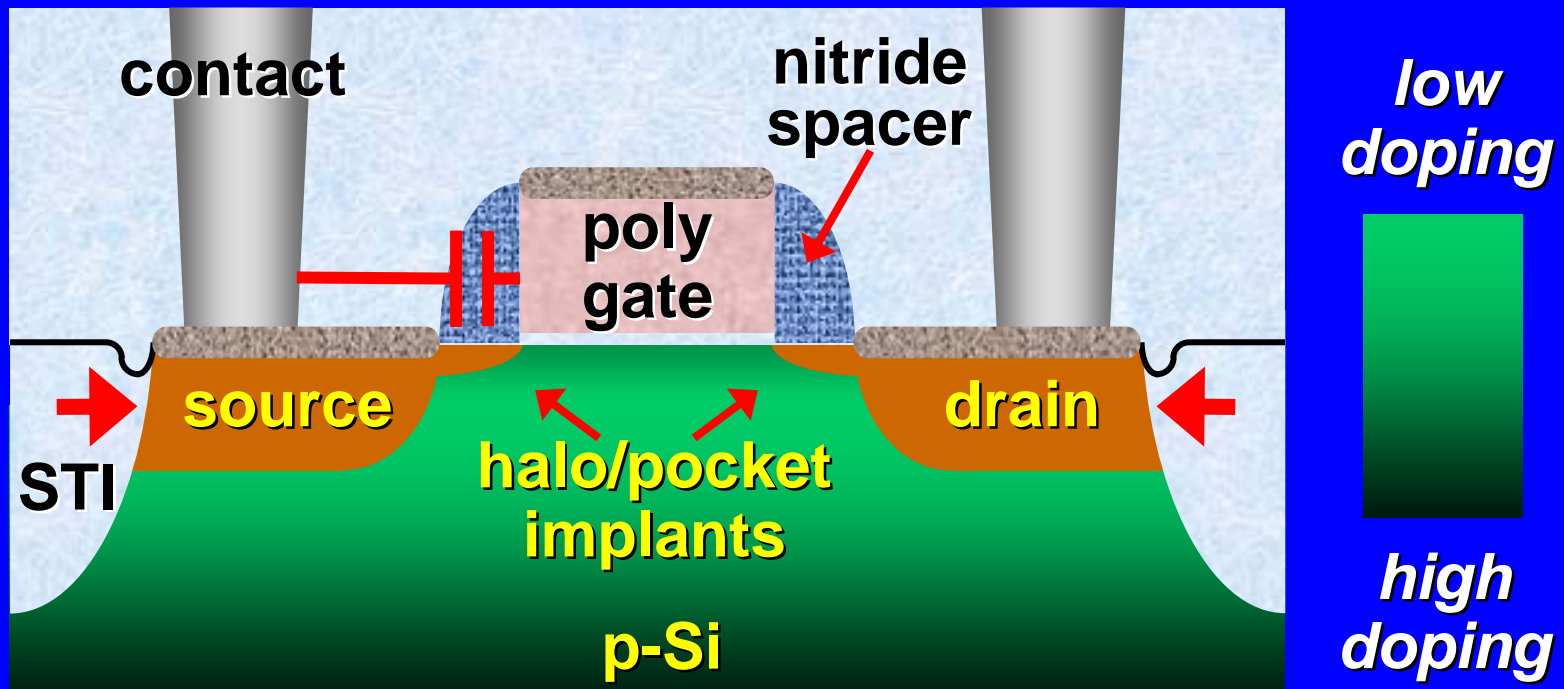


C-V flatness for supply noise rejection

- **Critical for integration with digital systems**

Tuning Range Factors

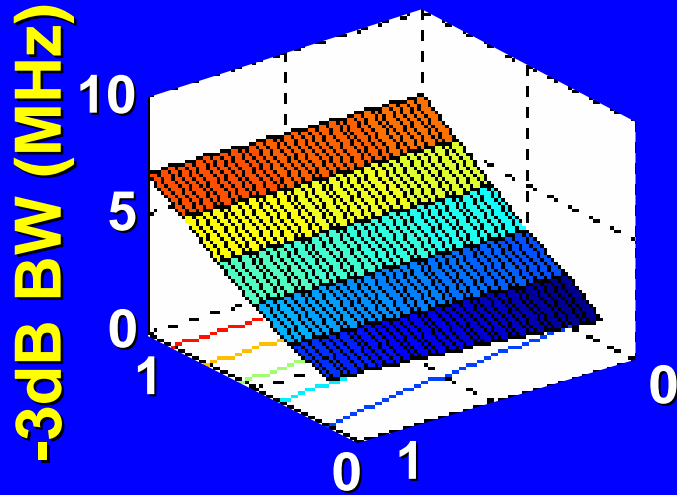
- Large tuning range \rightarrow maximize $C_{max}:C_{min}$ ratio
- Large $C_{max} \rightarrow$ large $W \times L$
- Small $C_{min} \rightarrow$ long L to reduce C_{ov} & C_{sub} , reduced Q_C
 \rightarrow minimize wiring parasitics (contact-to-poly)
- Reduce channel mechanical stress \rightarrow increase Q_C



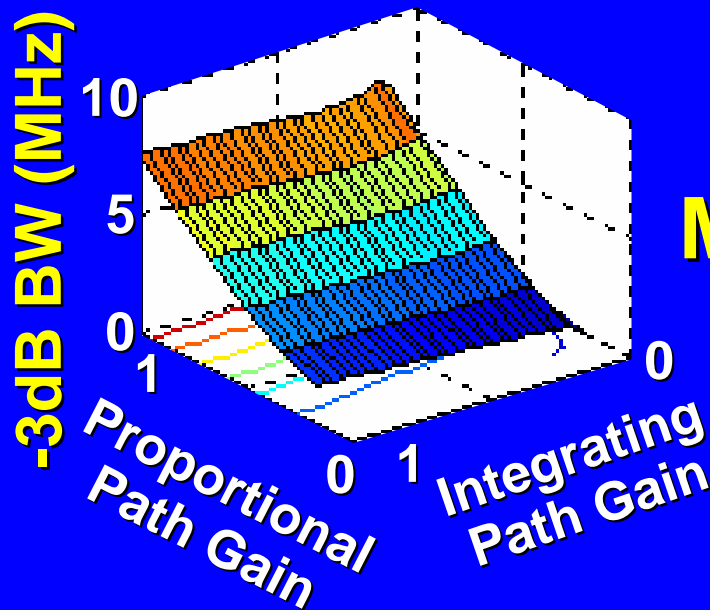
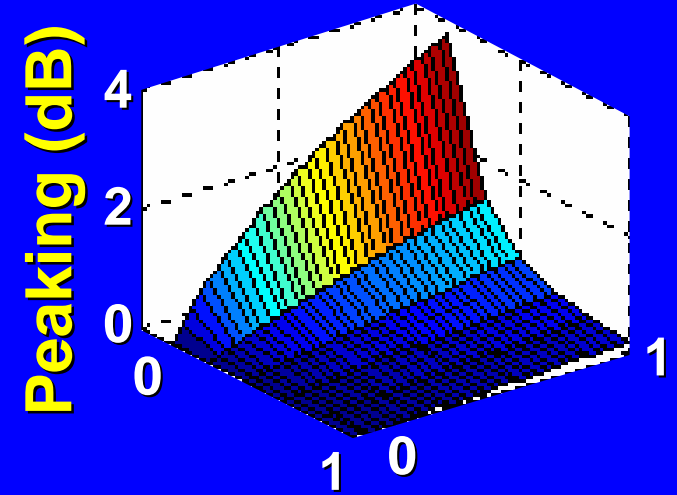
Outline

- Objective
- Dual-Path PLL Architecture
- Design Considerations
- **Measurements**
 - PLL Closed-Loop Dynamics
 - PLL Output Jitter
 - VCO Tuning
 - VDD & Temperature Sensitivities
 - Die Micrograph
- Performance Summary
- Conclusions

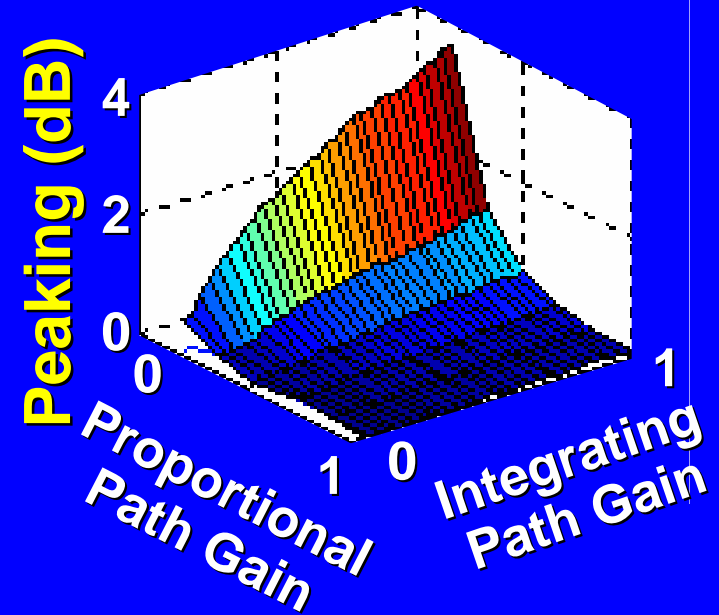
PLL Closed-Loop Dynamics



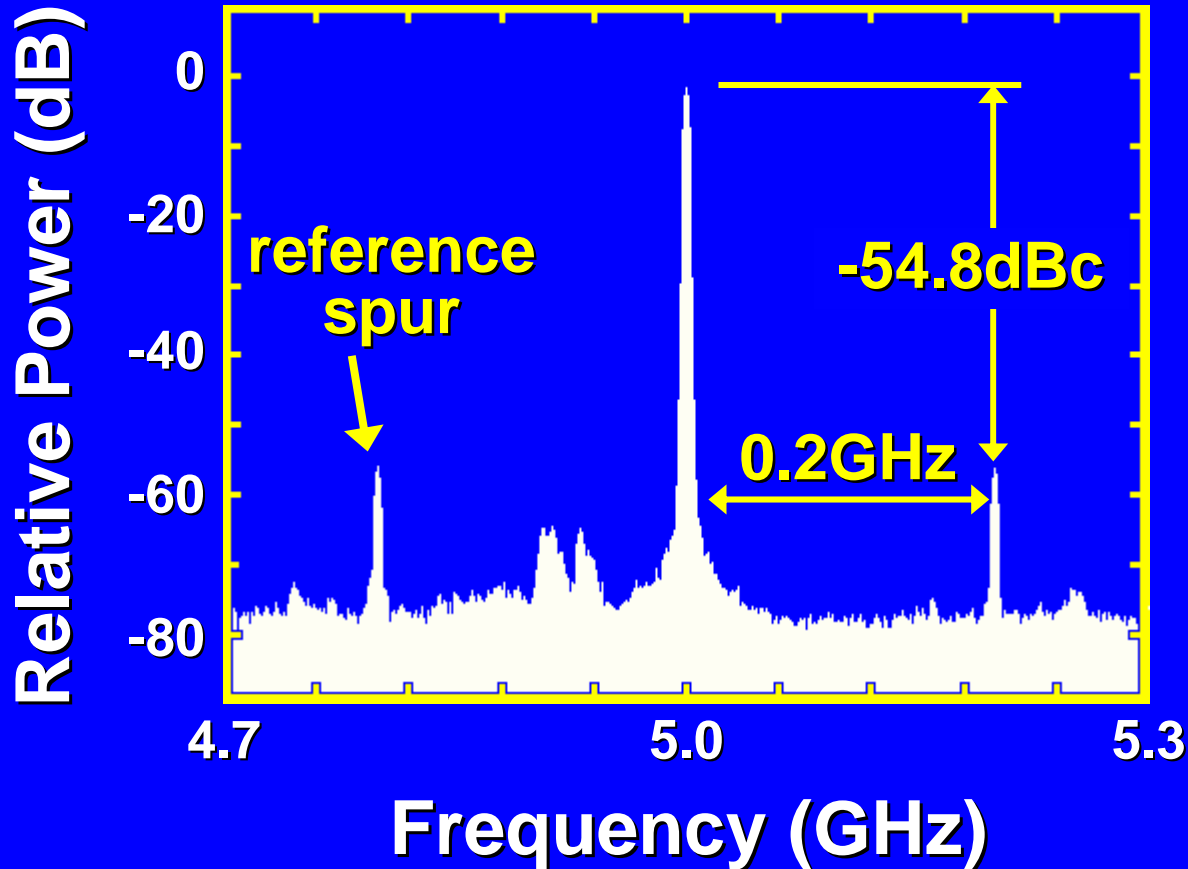
Modeled



Measured

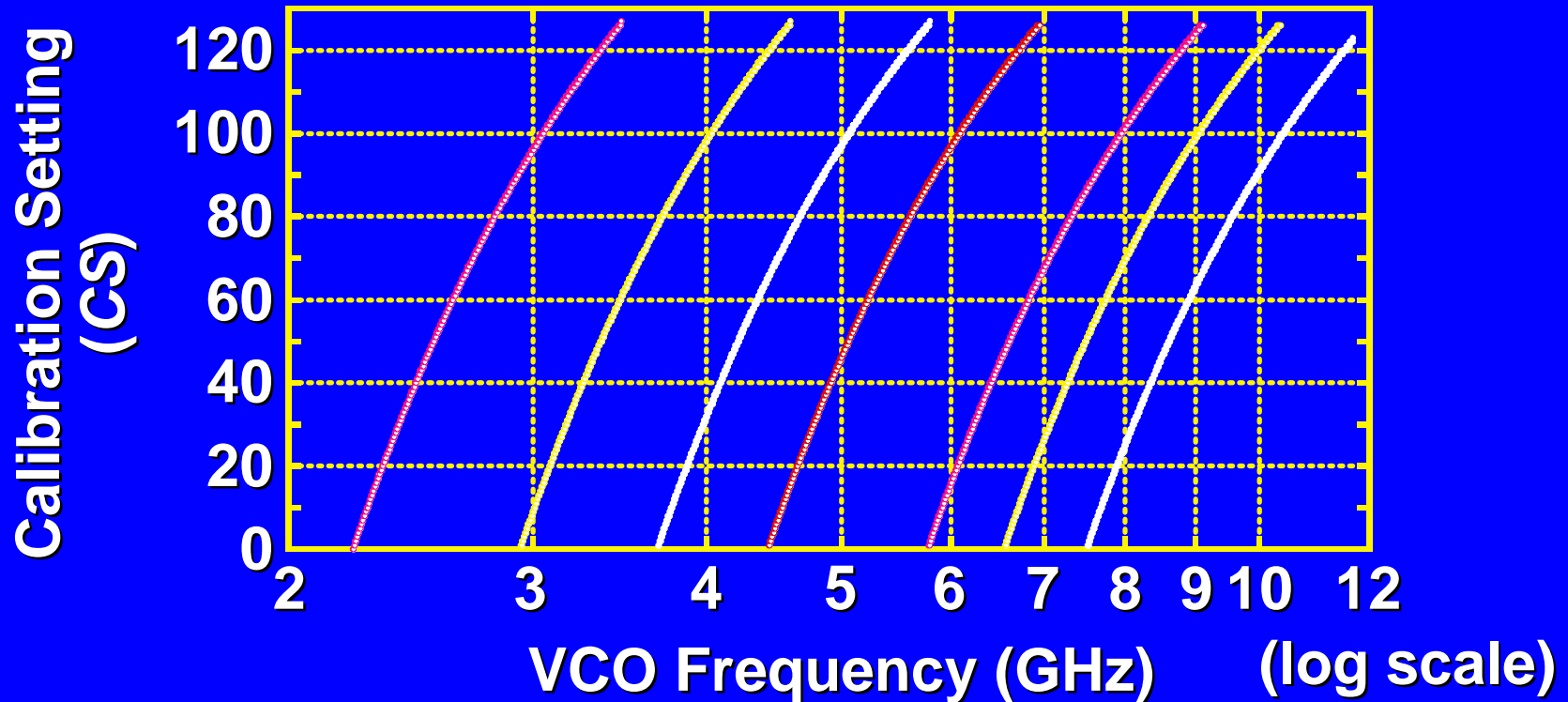


PLL Output Spectrum @ 10Gb/s



- 101010... data pattern (no ISI), $N=50$
- Extracted RMS Jitter = 0.81 ps

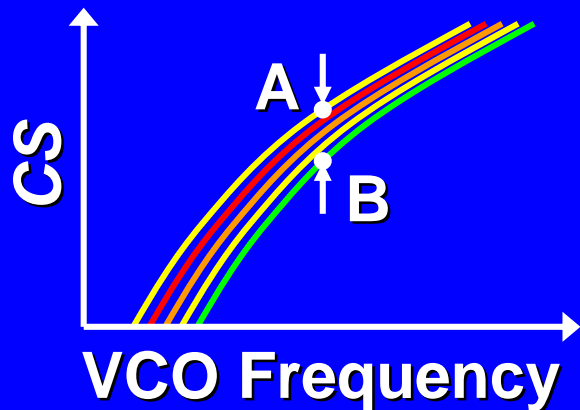
VCO Coarse Frequency Tuning



- CS = coarse-tuning varactor inputs tied to V_{DD}
- 7 VCO variants shown, each with 45% tuning range
- Coverage of practical SerDes protocols
- Loop filter outputs mid-railed during calibration

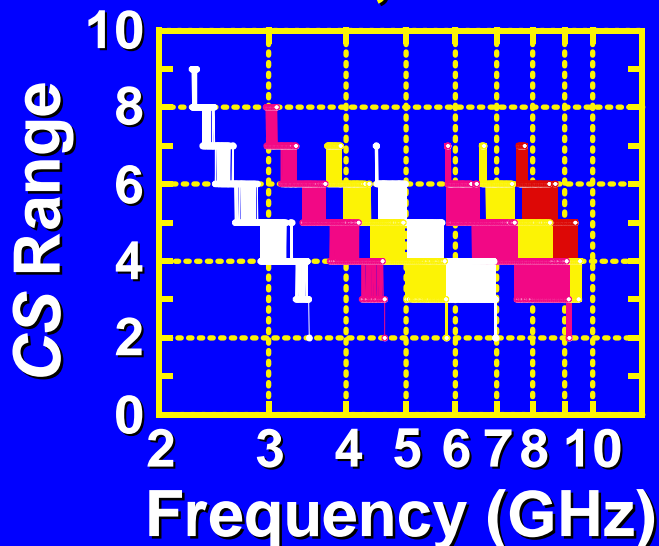
VCO Post-Calibration Tuning

coarse tuning curves
across V_{DD} & Temp corners

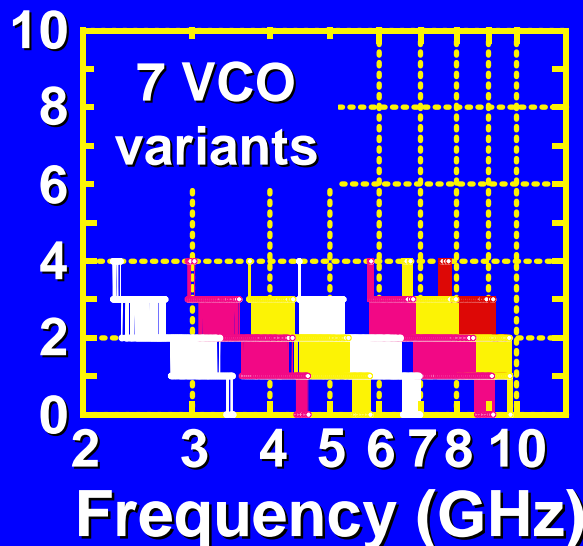


VCO has ± 10 varactors of tuning
to correct for VCO sensitivities to
 V_{DD} & Temp drifts after calibration
→ Measure **CS Range** (A–B)

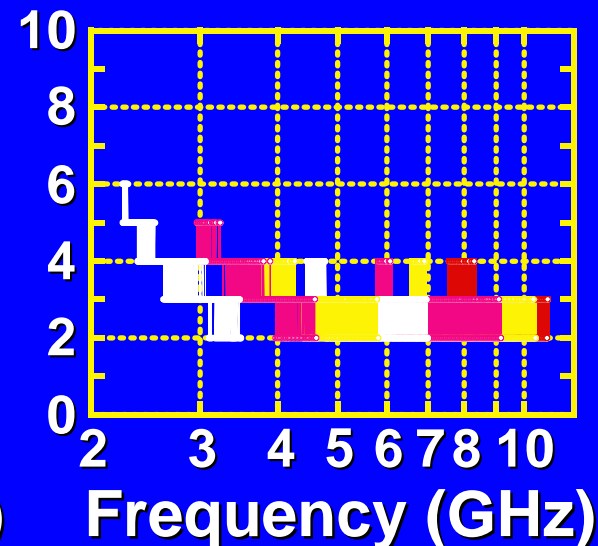
0.9-1.1V, 0-110°C



0.9-1.1V @ 85°C

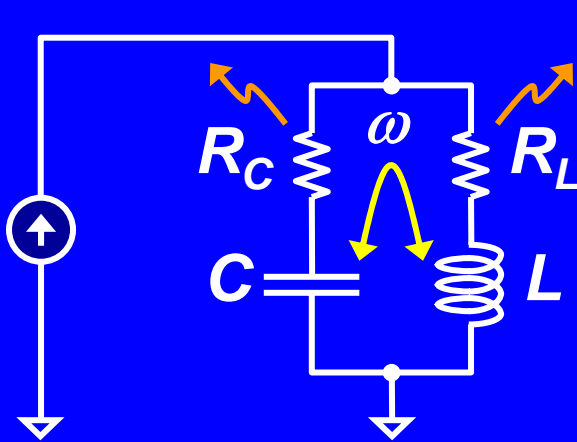


0-110°C @ 1.0V



VCO Temperature Sensitivities

Resonance for lossy LC tank:



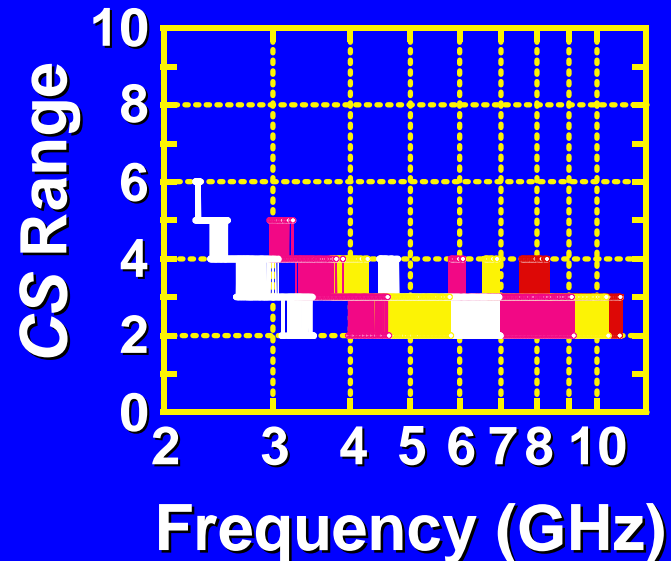
$$\omega^2 = \frac{1}{LC} \cdot \frac{1 - R_L^2 C/L}{1 - R_C^2 C/L} \equiv \frac{1}{LC} \cdot \frac{1 + 1/Q_C^2}{1 + 1/Q_L^2}$$

For $Q_L \ll Q_C$:

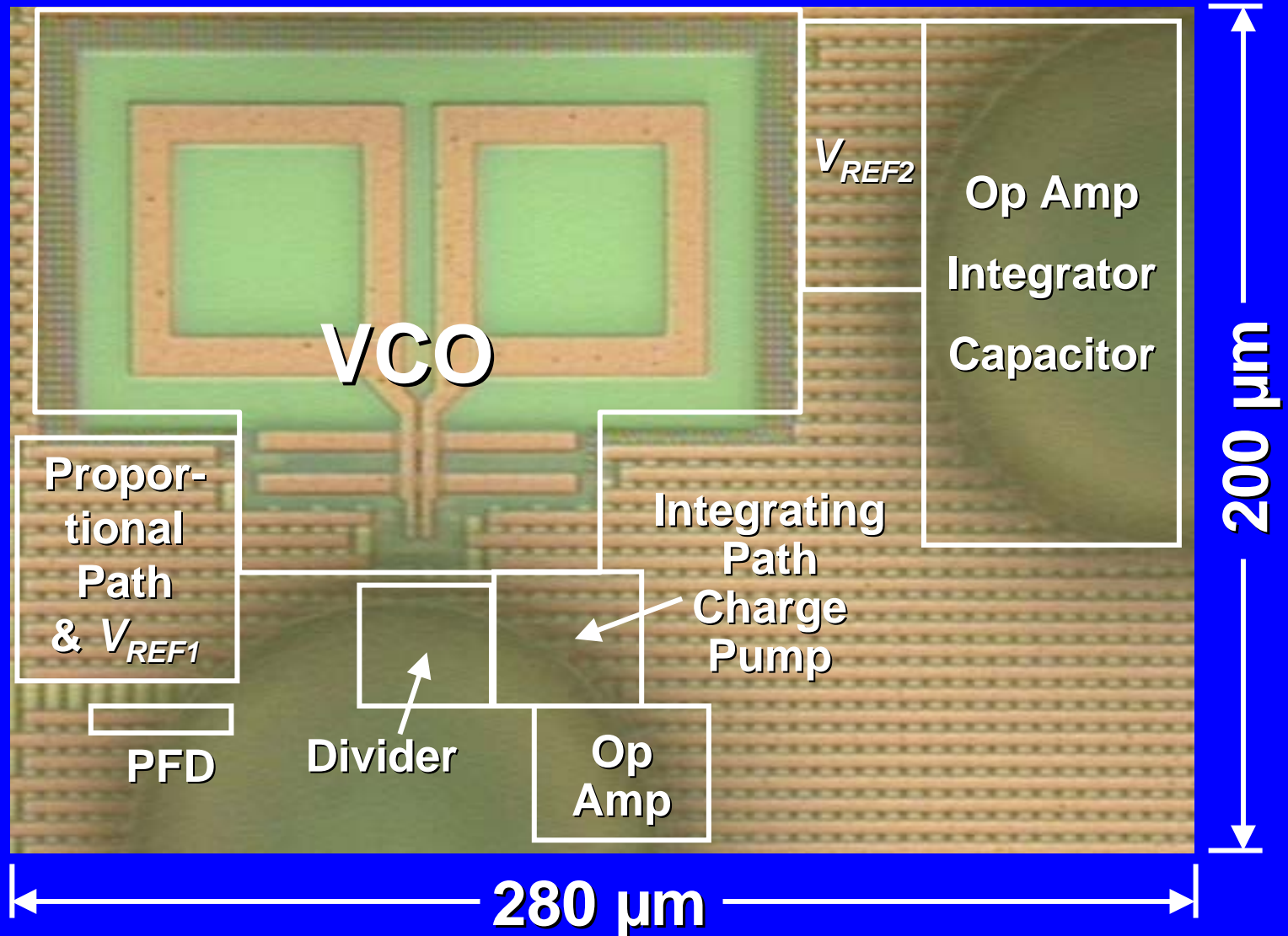
$$\left. \frac{d\omega}{dT} \right|_{C,L} \approx -\frac{R_L^2}{\omega L^2} \cdot TCR$$

$$\left. \frac{dC}{dT} \right|_{\omega,L} \approx -\frac{2R_L^2 C^2}{L} \cdot TCR$$

0-110°C @ 1.0V



Die Micrograph



Performance Summary

Technology	90nm CMOS (8M)
Supply	1.0 V (core)
RMS Jitter	0.81 ps @ 10 Gb/s
Selectable -3dB BW	0.46–7.5 MHz
Peaking	0.0–3.9 dB
Divider Ratio	10, 20, ..., 100
VCO f_{center} Range	2.9–9.8 GHz
Tuning Range	45%
Silicon Area	0.056 mm ²
Power / SerDes Channel	82 mW @ 10 Gb/s

Conclusions

- Presented PLL offers significant versatility to meet variety of SerDes Tx applications
- Resistorless dual-path loop filter provides area-efficient & flexible control of PLL dynamics
- Phase offsets in multiple-path loop filters must be reduced to suppress reference spurs
- Process considerations are critical for VCO tuning range optimization
- VCO inductor loss & varactor C-V flatness determine post-calibration tuning & jitter sensitivity