IJTAG (Internal JTAG): A Step Toward a DFT Standard

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Purpose

- Provide background and motivation for new IEEE standard activity re: *internal access*
- Describe progress of the IJTAG working group during the past year
- Solicit feedback and participation
- *Somehow, some way, make a talk about an IEEE standard interesting and entertaining*

A Background Joke…

Once upon a time, a guy asked a girl "Will you marry me?"

The girl said, "NO!"

And the guy lived happily ever after and went fishing and hunting and played golf a lot and drank beer and belched out loud whenever he wanted.

Moral: If left on their own, guys do silly things that don’t conform with societal norms.

Outline

- Background
- Motivating example
- IJTAG standardization effort
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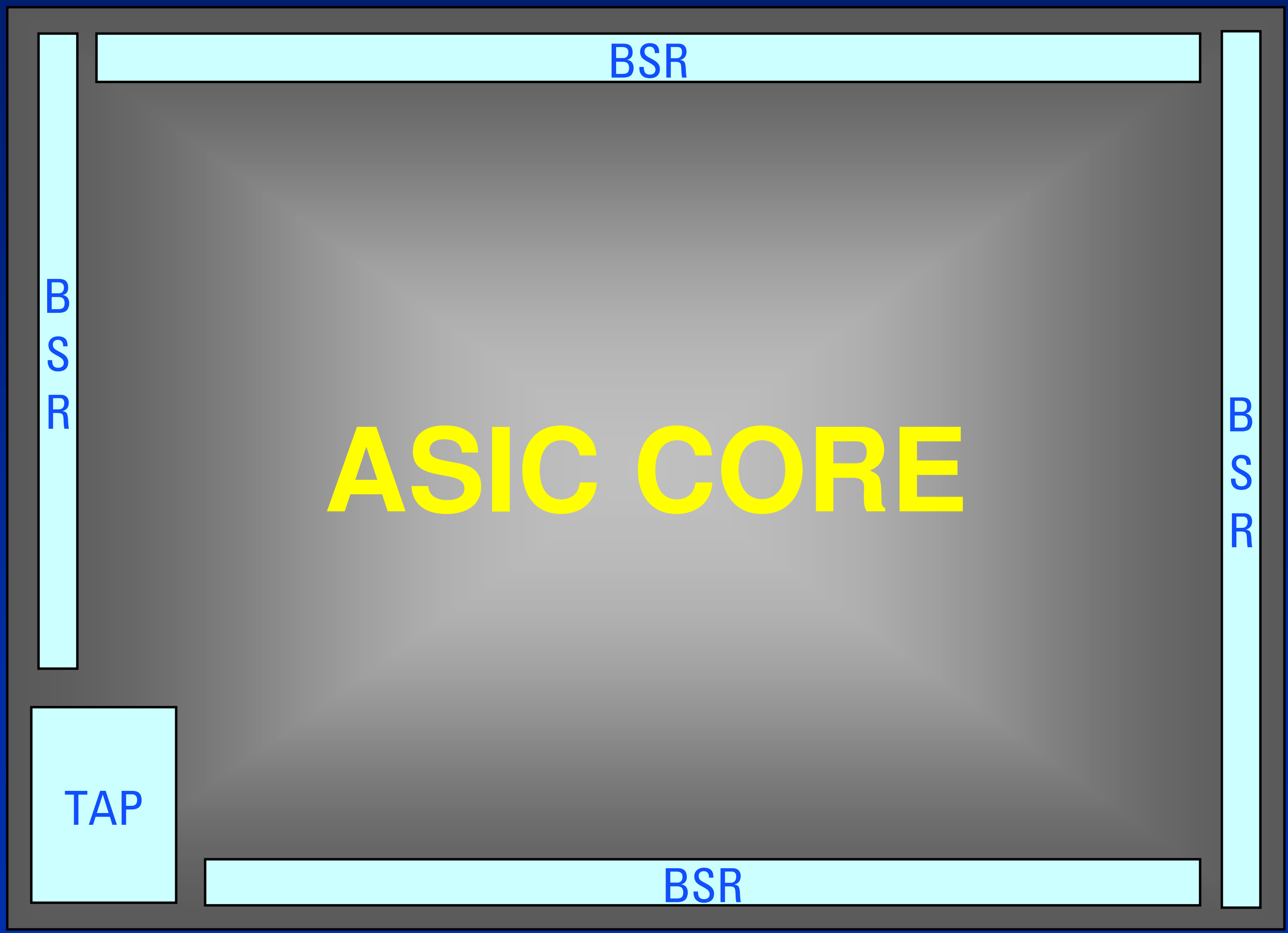
What is JTAG?

- Common term for:
  - Serial scan testing
  - Boundary scan in particular
  - Test Access Port interface pins
  - IEEE 1149.1
- Origin: Joint Test Action Group (late 1980s)
- Evolution: IEEE Standard 1149.1 (1990+)
- Boundary Scan and Test Access Port (TAP)

TAP and Boundary Scan



Leverage: 1149.4, .6; 1532; 1500

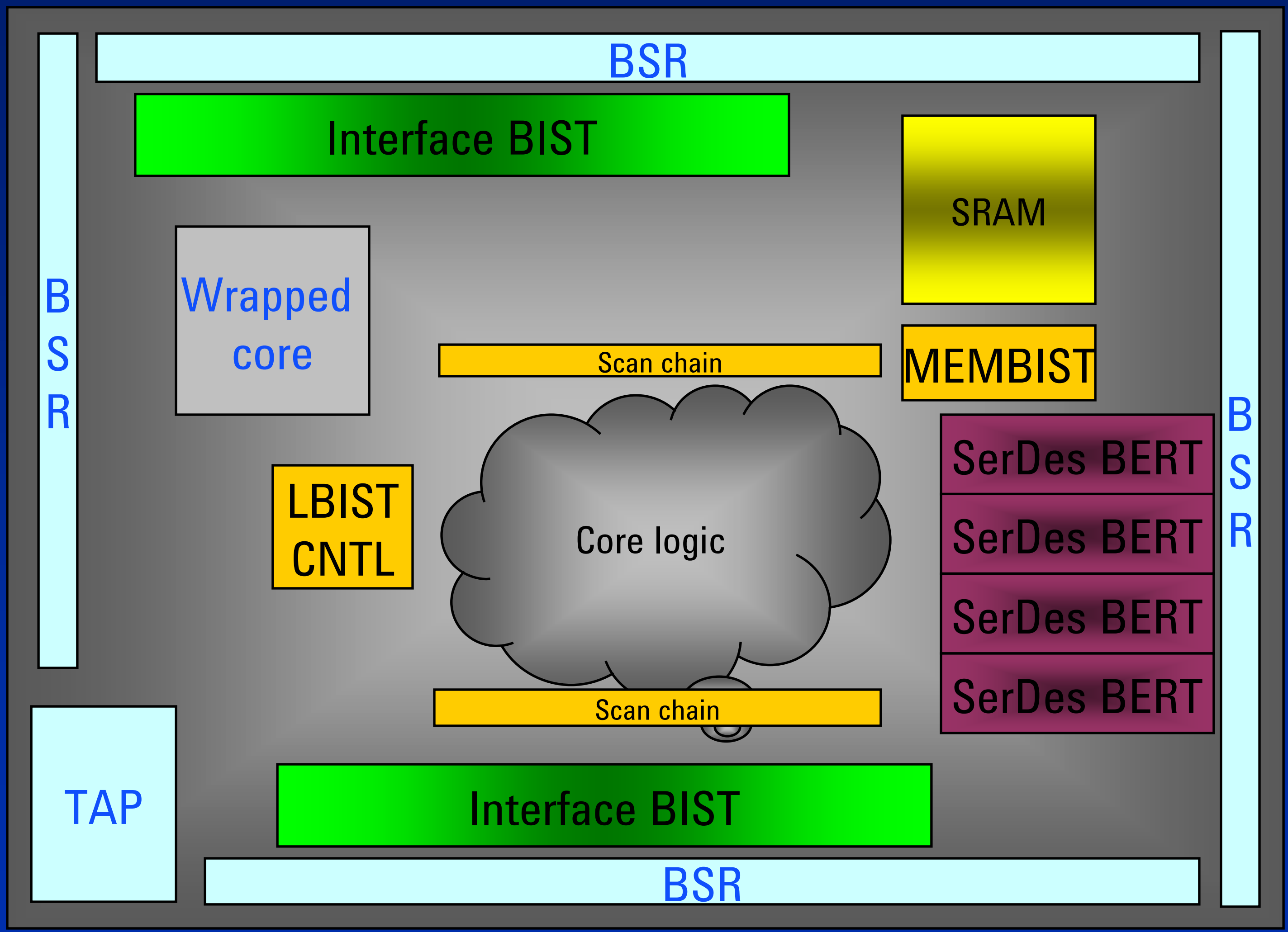
- Other IEEE standards using the TAP:
  - 1149.4 : Mixed-signal test bus
  - 1149.6 : Advance I/O test
  - 1532 : In-system programming
  - 1500 : Embedded core testing
- Non-IEEE standards using the TAP:
  - Nexus 5001
- Non-standard usages of the TAP:
  - A very long list…

Creative Uses of the IEEE 1149.1 TAP

- **Power management**
- **Clock control**
- **Chip configuration**
- **Memory test**
- **Scan test**
- **Logic BIST**
- **Debug/diagnosis**
- **PLL control**
- **Reduced pin count test**
- **Fault insertion**
- **Embedded instrument access**

Power management	Turn on/off input isolators (pass gates) [16]
	Turn on/off pullup/pulldown resistors
	Turn on/off entire clock domains
Clock control	Select chop-clock ratios for transition and path delay testing
	Select chop-clock ratios and dividers for functional operation
Chip configuration	Capture of alternate chip IDCode register (chip or mask version)
	Selecting Functional Units on the chip to be disabled/enabled
Memory test	Selection of Memory BISTs to be run in parallel (1-hot bit per BIST)
	Selection of memory BIST algorithm
	Selection of memory BIST background (e.g., 3-C, 5-A, 0-F, 9-6)
	Selection of Memory BISTs to be run in diagnostic mode
	Data collection from a memory BIST operating in diagnostic mode
	DMA (connecting BIST muxes to chip-level busses with access to pins)
	Enabling-Disabling memory lock for test and debug (OE and R/!W)
Scan test	Selection of chip-level scan mode or individual partition scan mode
	Enabling-disabling-configuring internal tristate busses
	Reconfiguration of scan chains
	Reconfiguration of scan wrappers around cores
	Selection of pins to be used as scan-ins and scan-outs
	Configuration of pins used as scan-ins and scan-outs
	Subsuming AC scan operation completely within JTAG
Logic BIST	Selection of STUMPs Logic BIST units
	Selection of polynomial of PRPG LFSRs
	Scanning in of seeds for re-seeding or debug
	Selection of 'final signature compare' vs. 'incremental signature extraction'
	Scanning in of signature to be compared
Debug & diagnosis	Loading an internal counter used as a breakpoint
	Shadow capturing key registers (with a SAMPLE-like function)
	Masking or overwriting key registers (with an EXTEST-like function)
	Replacing data in key registers (with and UPDATE-like function)
	Selection of scan dump mode (lock memory, enables scan-out)
PLL control	Access to control registers for gating Scan-Enable and Scan-Clock PLL outputs
Reduced pin count test	Access to low-frequency IOs
	Control PLL bypass for clock control
	Control of internal scan chain configurations (detect versus locate)
Fault insertion	Drive IO faults
	Drive internal faults
Control of embedded instrume ntation	Control of use of embedded instruments
	Access for embedded instrument outputs

TAP Access to Chip Test Features



Not a Laughing Matter…

- Internal test, debug, monitoring, repair, configuration, even reprogramming are all done via the TAP
- No common description language
- No common access method
- ⇨ Very difficult to re-use at higher levels

Moral: If left on their own, ~~guys~~ ***designers*** do silly things that don't conform with ~~societal~~ ***system-wise*** norms.

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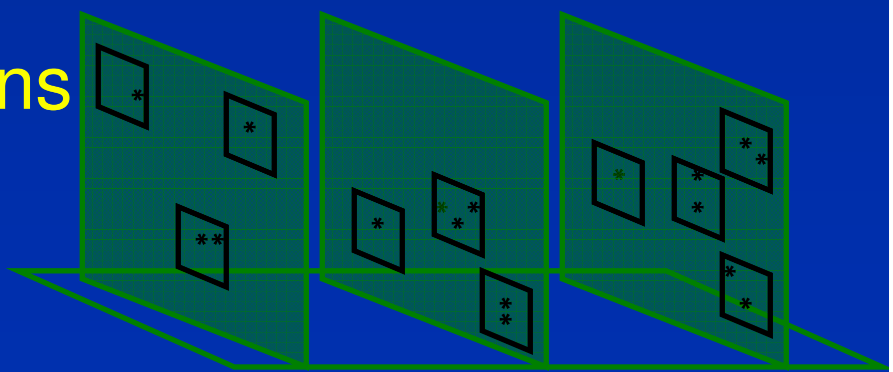
Example: Creating a Board/System Test

- Complex board/system
  - Multiple SOC ASICs
  - Microprocessors
  - Embedded and standalone memories
  - Programmable logic devices
- Complex features
  - High-speed I/O
  - Backplane connections
  - Reconfigurability



Goal: Re-use Component Test Features

- Re-run ASIC embedded memory tests
- Re-run ASIC logic BIST
- Run ASIC-based external memory tests
- Run chip-to-chip HSIO PRBS tests
- Monitor internal signal waveforms
- Capture internal chip state
- Use chip test features to test board

Daunting Task: Assembling ASIC Info

- BSDL (Boundary Scan Description Language)
- Initialization sequence(s) and clock control
- Logic BIST and external MBIST recipes
- For each embedded memory
  - Setup, launch, checking procedures
  - Diagnostic routines
- List of extra test features and access methods

More Information to Collect: Board/Sys

- For each high-speed link
  - Method to setup, launch, and check BER
  - Ability to apply different crosstalk, jitter, noise, data content conditions
- For each parallel bus
  - Method to setup, launch, and check SI
  - Patterns for crosstalk, glitches, etc.
- For each backplane configuration
  - …

Accessing Test Features is Painful

- Multiple ASIC vendors
- Multiple memory vendors
- Multiple test methodologies
- Multiple ATE platforms
- Multiple test languages
- Bottom line from example:
  - Chip test re-use at board/system: tough!

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The Brief History of IJTAG

- Early 2004: two independent (unaware) efforts
- Proposed to 1149.* and 1532 working groups at ITC 2004
  - Merged, approved, several sign-ons
- Proposed to IEEE TTSG at ITC 2004
  - Advised to proceed informally
- Working group meeting at VTS 2005
  - Officers elected; TTSG checkpoint
- Ongoing core team meetings

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  - Scope and focus
  - Technical challenges
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How to Fail at Standardization

- Too broad a scope
  - Fix every known problem with boundary scan standards; solve every test problem
- Too narrow a scope
  - Specify how to read results of MBIST
- Too fuzzy a focus
  - Invent new languages and interfaces
- Too sharp a focus
  - Use PCI-Express to access Mux-D scan

The Three IJTAG Components

- Description of on-chip "instruments"
  - Identify location, type, function
    - BSDL is not adequate for this; CTL may be
- Protocol for instrument communication
  - Specify instructions, timing, sequences
    - STIL or STAPL may suffice
- High-bandwidth interface to instruments
  - Define control vs. data, handshake, function
    - Goal is to always allow "today's best interface"

Defining "Instruments"

- Instrument, very broadly:
  - Any on-chip circuit for test, debug, diagnosis, monitoring, characterization, configuration, or functional use that can be accessed by, configured from, or communicate with a TAP controller.
- Examples:
  - Scan chains, BIST engines, CRC registers, packet counters, performance monitors, waveform ADCs, remapping registers, trace buffers, PLL controls, power managers, …

IJTAG Scope

- This standardization effort is intended to address the ***access*** to on-chip instrumentation, not the instruments themselves. The elements of standardized access include:
  - a description language for the characteristics of the instruments,
  - a protocol language for communication with the instruments, and
  - interface methods to the instruments.

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Four Technical Challenges

- Bandwidth
  - Bus sizing and data rates for instruments
- Sequencing
  - Temporal staging of instrument actions
- Synchronization
  - Coordination of chip resources and instruments
- Interoperation
  - Connectivity with external resources (e.g. ATE)

Bandwidth

- Communication bottlenecks:
  - Inside chip to outside world: state dump
  - Outside world to inside chip: memory preload
  - Inside chip to inside chip: BIST
- Control vs. Data bandwidth
  - Control precedence? Data interruptability?
- Scalability across instruments
  - Go/NoGo vs. massive data dump

Real estate vs. throughput

Sequencing

- Simplistic approach to instrument staging:
  - Initialize, launch, check
- Complications
  - Multiple launches
  - Interruptions
  - Destructive checking
  - Diagnostics
  - Power limitations
- Language requirements

Synchronization

- Coordination of chip activity with instruments
- Coordination of board/sys activity with instruments
- Coordination across multiple instruments
- Possible need for real-time interaction
- Time stamping with IEEE 1588
- Cross-clock domain data transfers
- Synchronization to TAP clock domain

Interoperation

- Connection to external resources (ATE, controllers, measurement devices, etc.)
- Control and data exchange protocol and language
- Access to instruments during mission mode
- Master/Slave relationships with multiple instruments
- Security

Technically, Non-trivial

- Despite clear scope and focus, there is still plenty of interesting work to do
- Striking a balance between ambition and practicality will be the key to progress

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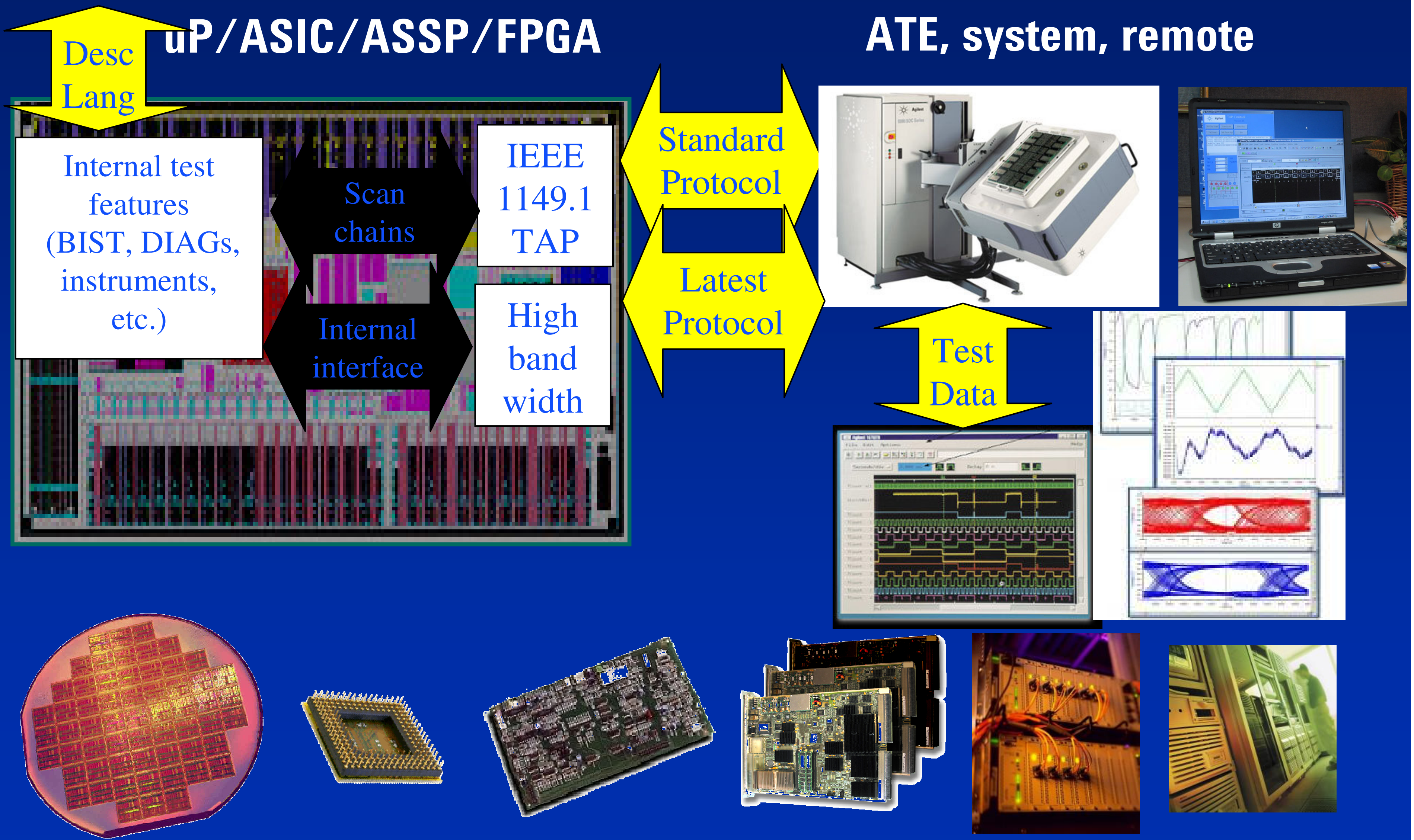
TAP-based Access to Test Features



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Next Steps

- IJTAG Working Group meeting at ITC
  - November 10, 2005
- Plan: request formal creation of standard working group
  - Preparation of IEEE PAR for TTSG submission
  - Synchronize with other related working groups
  - Start the IEEE clock ticking
- Solicit additional members and input

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- IJTAG fills a very real need
- IJTAG scope must be focused to succeed
  – Standard description of internal features
  – Standard protocol language for access
  – High bandwidth interface mechanism(s)
- IJTAG gaining momentum
- IJTAG needs your input!

A Background Joke…

Once upon a time, a guy asked a girl "Will you marry me?"

The girl said, ~~"NO!"~~ ***"YES!"***

~~And the guy lived happily ever after and went fishing and hunting and played golf a lot and drank beer and belched out loud whenever he wanted.~~

And they both lived happily ever after in the firm belief that standard is better than better.