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Strain for CMOS performance Improvement

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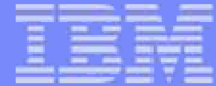
❖ Outline

* Introduction: Strain helps carriers to travel faster
* Substrate-induced strain
* Process-induced strain
  - Contact etch-stop nitride liner (DSL)
  - Stress Memorization Technique (SMT)
  - Embedded SiGe in S/D (e-SiGe)
* Stress and Device / Circuit Implication
* Mobility Improvement beyond Stress Engineering
  - Channel Orientation
  - Substrate Orientation (eg. HOT, DSB)
* Summary



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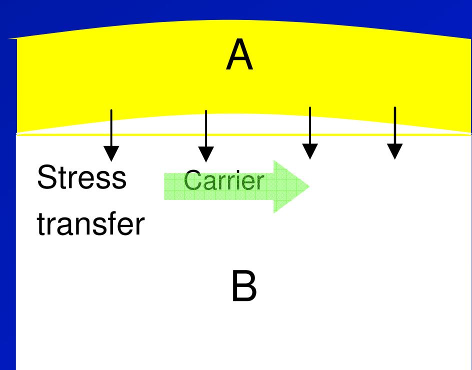
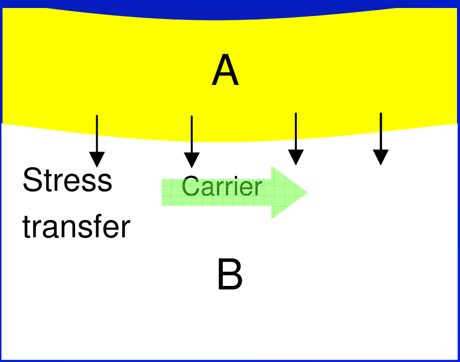
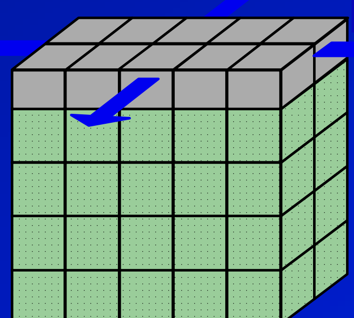
Mechanical Stress: basic

Material A (tens/comp) (eg. Nitride)
Material B (eg. Si)

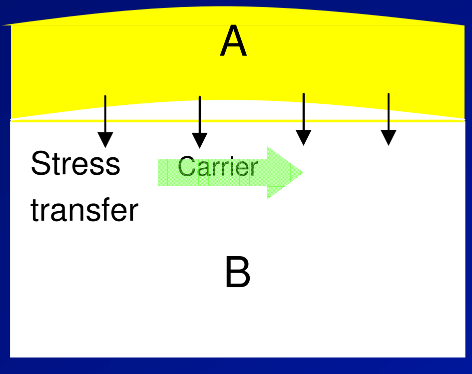
Due to material mismatch of A & B from material composition, element size / volume and thermal expansion rate, A will introduce mechanical stress to B.

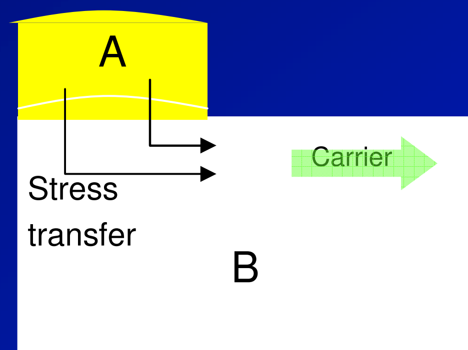


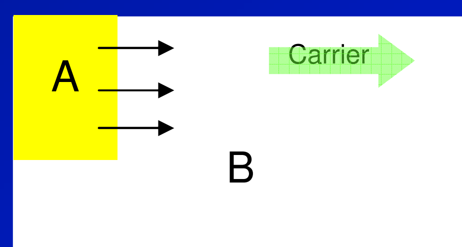




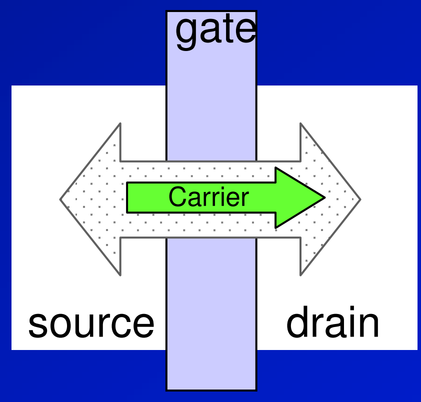
Mechanical Stress : many ways

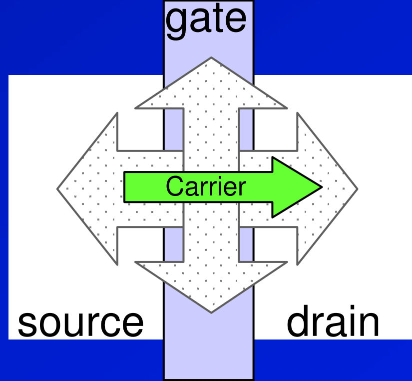






- Many different ways
- Stress transfer dependent on
  - material A deposition / growth condition (eg. process temp, material)
  - subsequent steps (eg. annealing, implantation)





Uniaxial stress: 1-direction **biaxial stress: 2-directions**

Electrons have higher mobility in Strained (biaxial tensile) Si

In Strained Si, i) m^* (effective mass) is smaller → higher mobility

ii) split energy band → less inter-valley scattering → higher mobility

$$\mu = \frac{q\tau}{m^*}$$

K. Rim, *VLSI Sym* 2002

Holes have higher mobility in Strained (biaxial tensile) Si

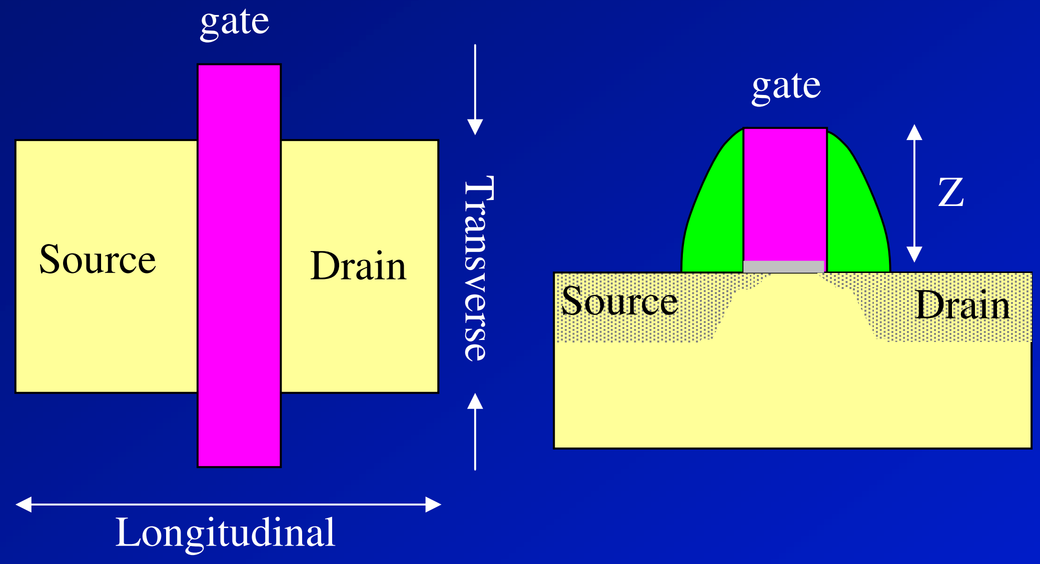
HH = heavy holes

LH = light holes

In Strained Si, i) *m** (effective mass) is smaller → higher mobility
ii) split energy band → less carrier scattering → higher mobility

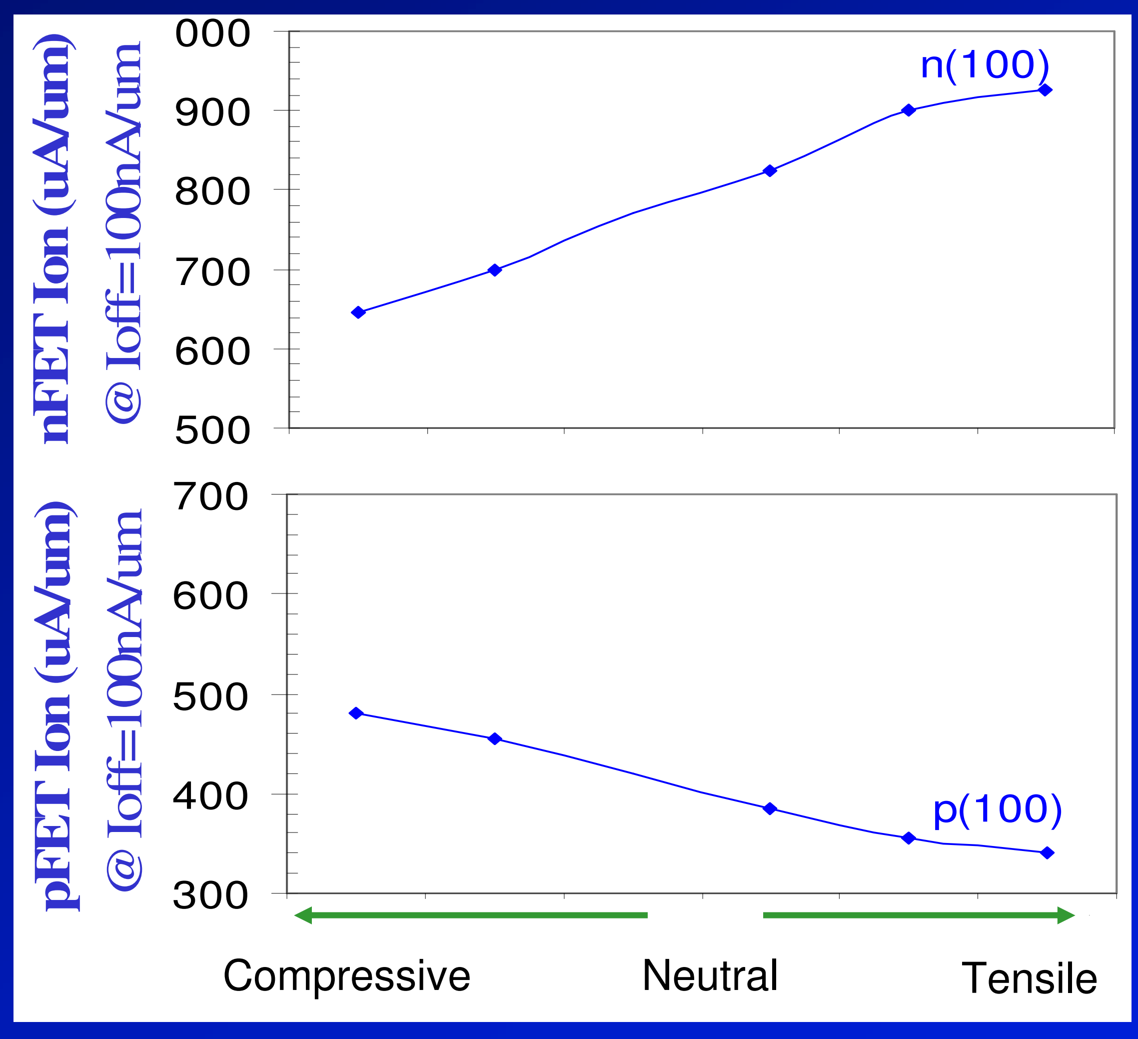
K. Rim, *VLSI Sym* 2002

Desired uni-axial stress on CMOS performance



		NMOS	PMOS
Longitudinal	X	Tensile	Compressive
Transverse	Y	Tensile	Tensile
Si Depth	Z	Compressive	Tensile

Longitudinal stress provides different drive current



Technology in this presentation

IBM 90 / 65nm CMOS technology

VCC (V)	1.0
Lpoly (nm)	45
Tox (nm)	1.2

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  - Substrate Orientation (eg. HOT)
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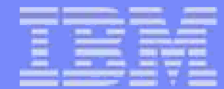
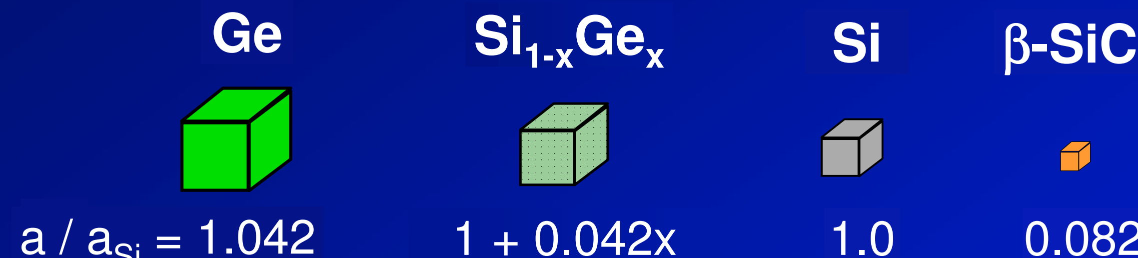
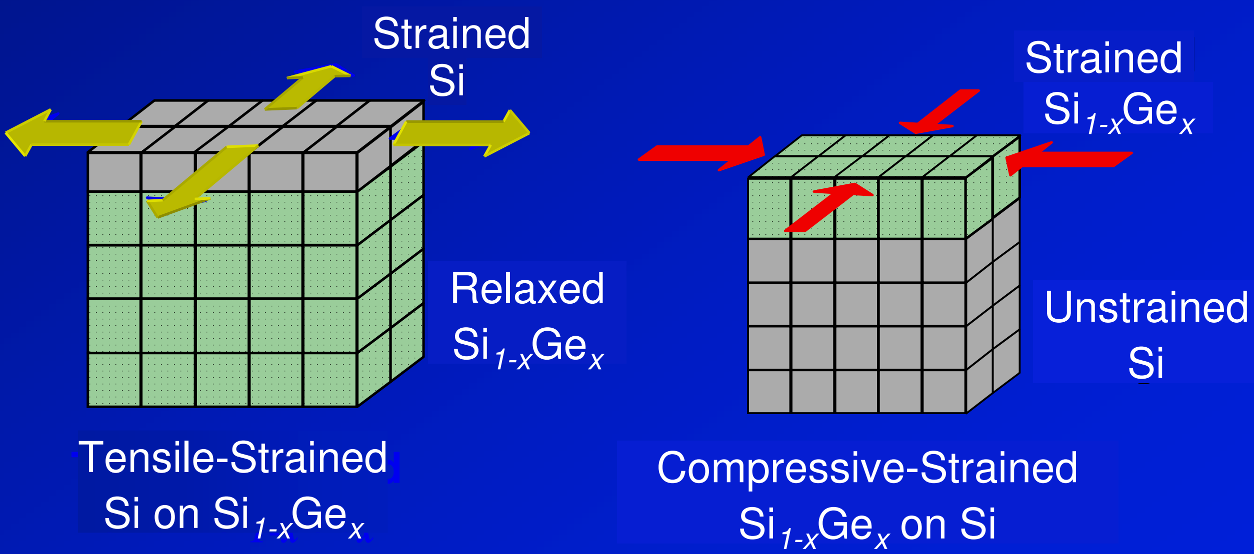
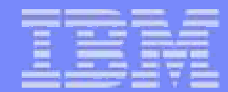


Strain in Si-based Heterostructures





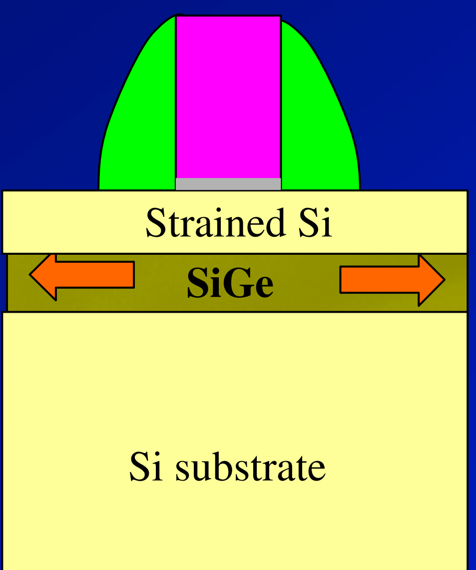


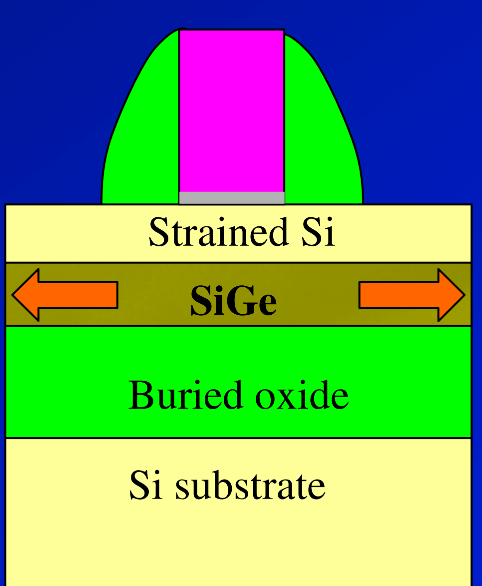
Schematic diagram to show three ways of formation of strained Si MOS devices

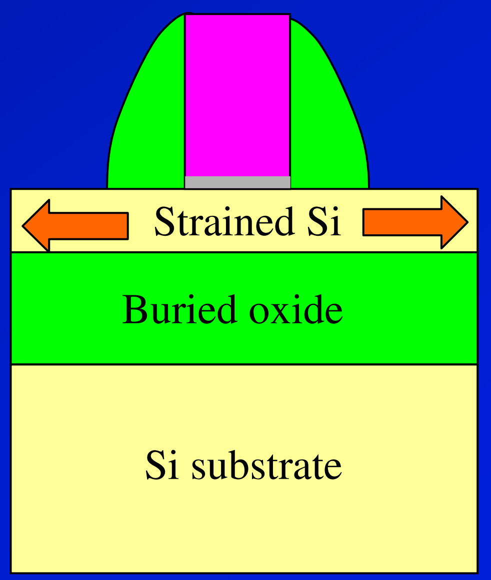
a) Strained Si/SiGe on bulk wafer

b) SiGe-on-Insulator (SGOI)

c) Strained-Si Directly On Insulator (SSDOI) MOSFET







K. Rim, *VLSI* 2002,
B. H. Lee *IEDM* 2002,
K. Rim *IEDM* 2003

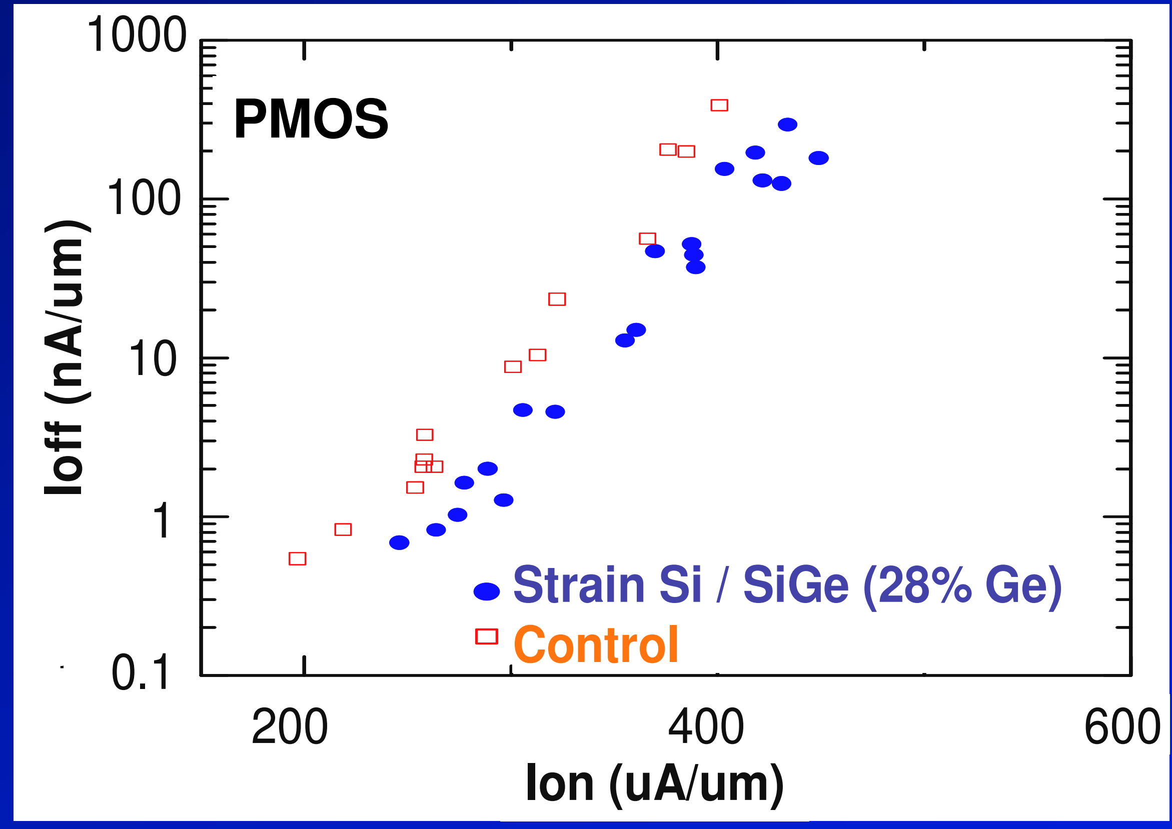
NMOS shows benefits with biaxial tensile strained Si with 13% & 28% Ge

- Higher NMOS Ion improvement with higher % Ge.

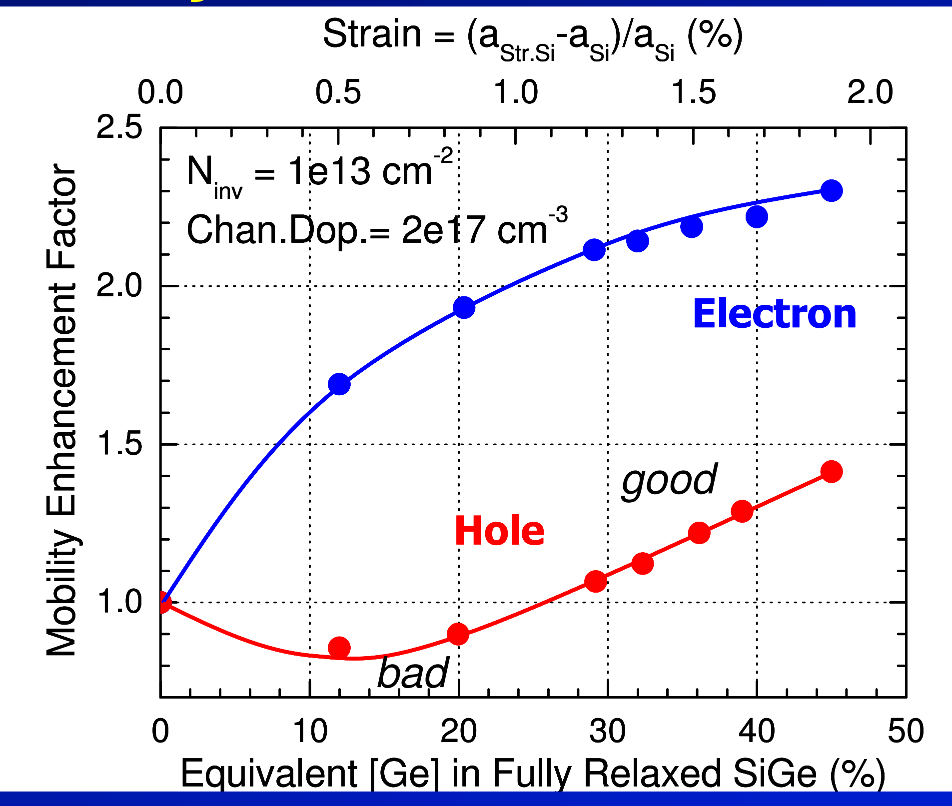
K. Rim, *VLSI Sym*, 2002

PMOS shows benefits with Biaxial Tensile Strained Si with 28% Ge

- pMOS Ion only improved with high % Ge in SiGe, eg. > 20%.



% Ge vs mobility



	nMOS (e^-)	pMOS (h^+)
Uniaxial longitudinal tensile stress	Good	Bad
Biaxial tensile stress	Good	Dependent on %Ge

K. Rim, *VLSI Sym,* 2002

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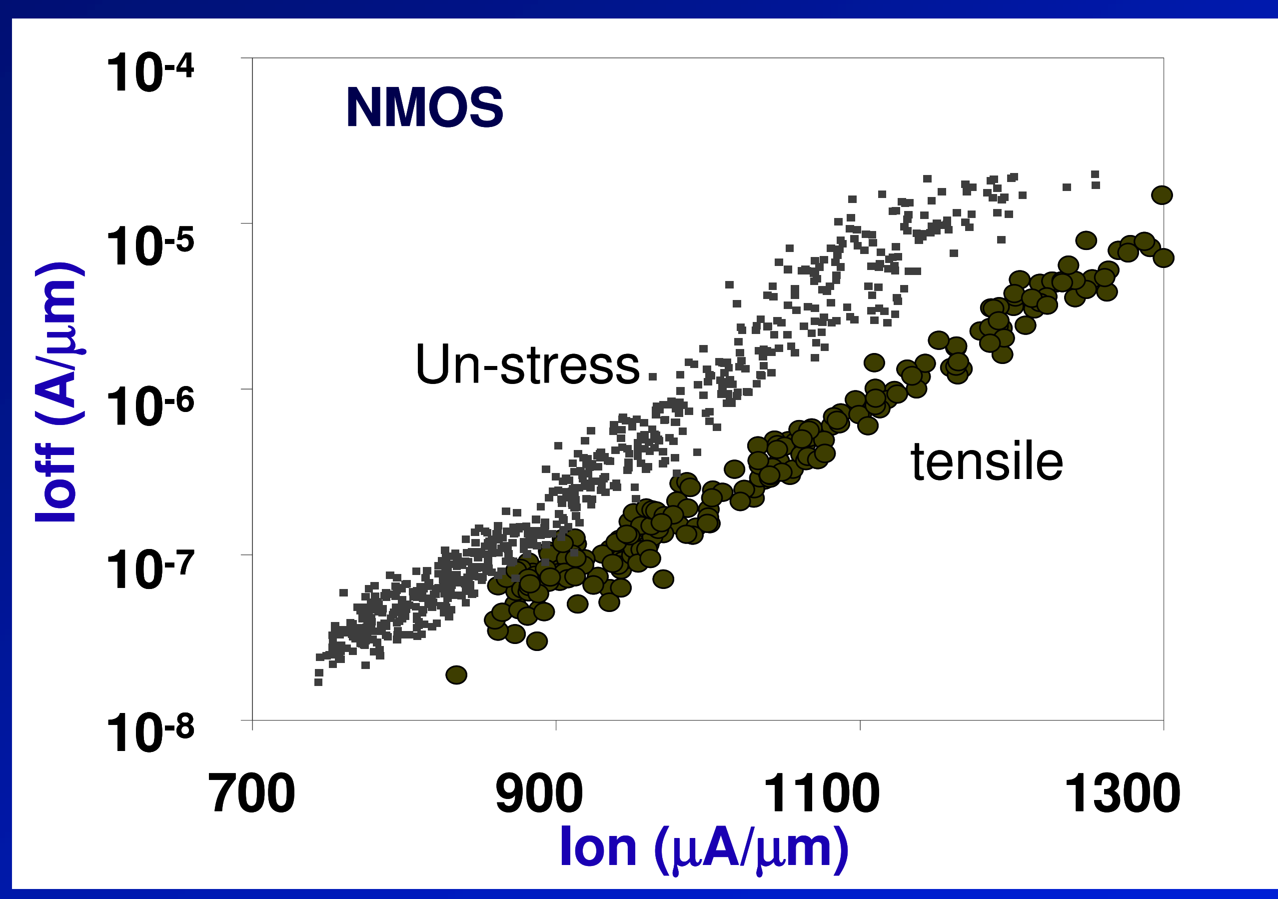
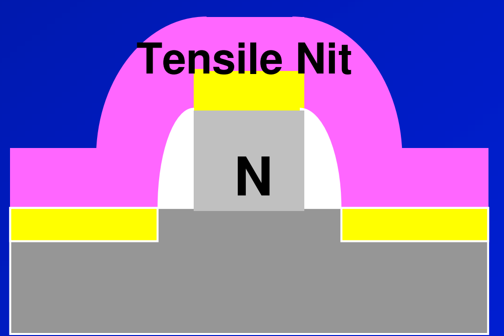
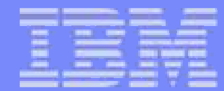
Ion enhancement using stress liner compared to neutral liner (non-stressed process) for nMOS

- nMOS Ion improves with higher Tensile nitride liner



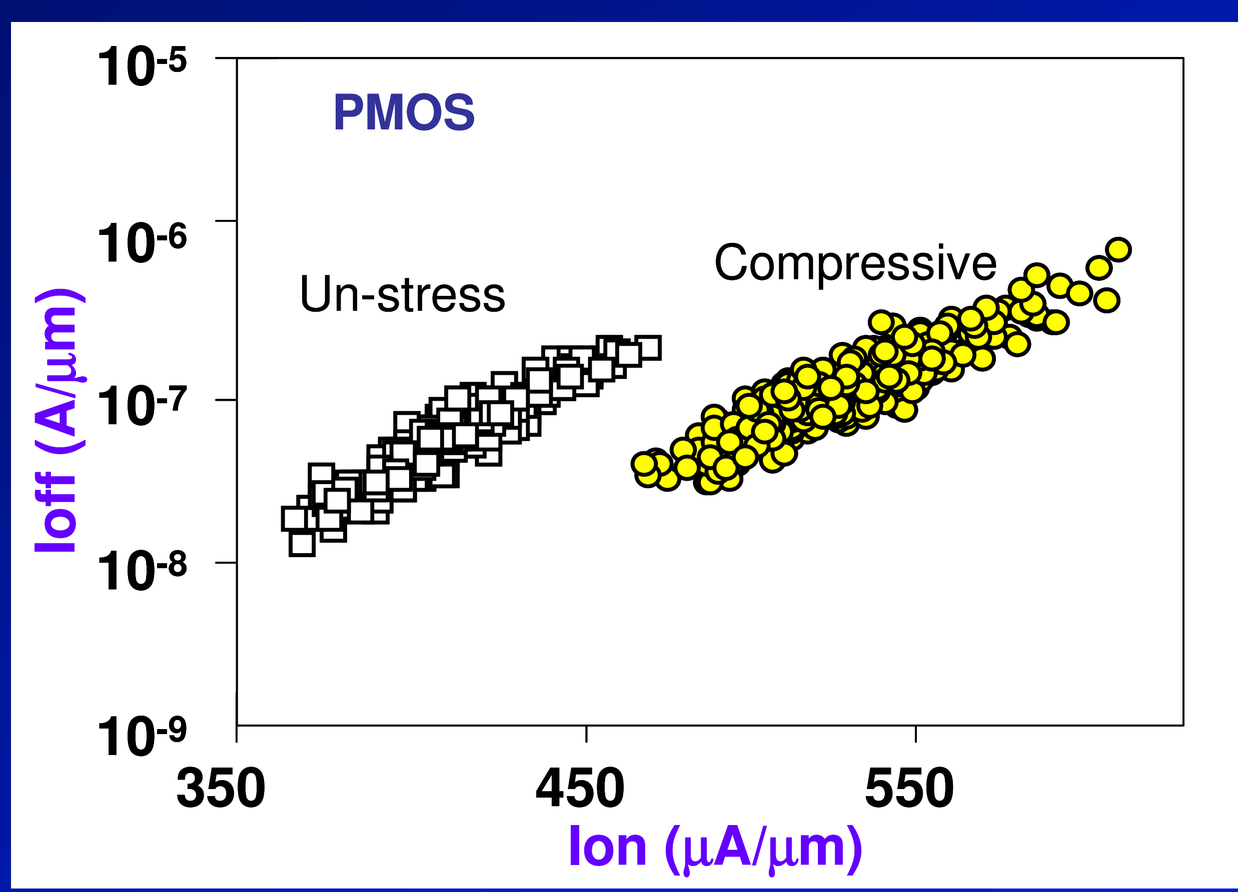


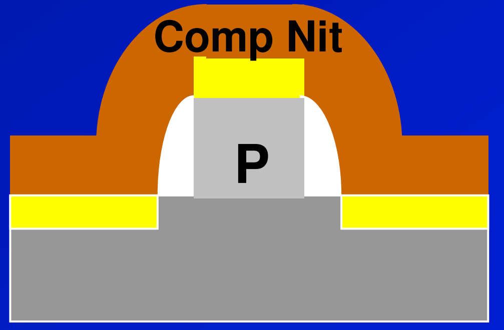
H. S. Yang, IEDM 2004



Ion enhancement using stress liner compared to neutral liner (non-stressed process) for pMOS

- pMOS Ion improves with higher Compressive nitride liner

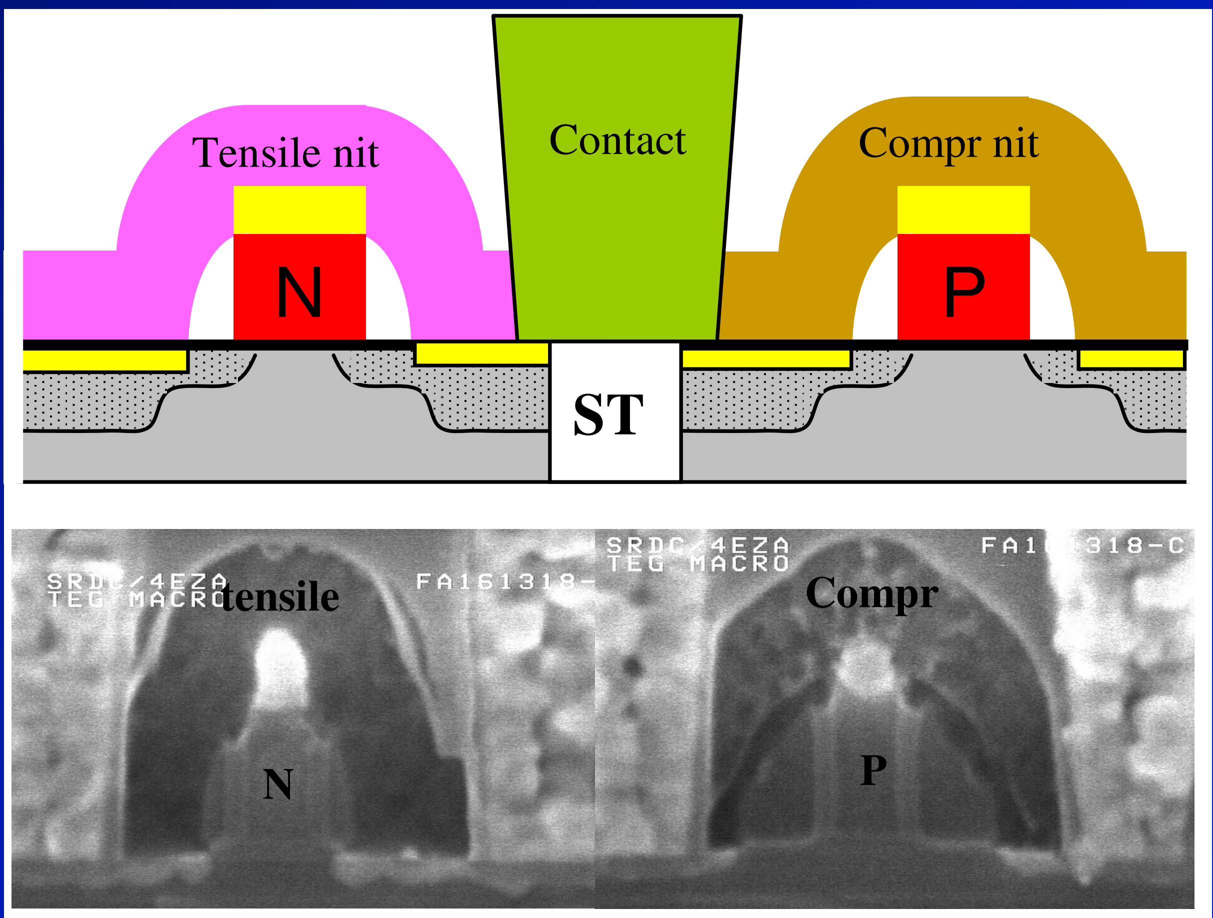




H. S. Yang, IEDM 2004

SEM cross-section of an SRAM cell features tensile and compressive liner in NMOS and PMOS respectively

- IBM powerPC ™ micro-processor Fmax vs power improves 7 % with DSL due to higher current.



Nitride film stress changes after annealing

- Nit film stress tends to be tensile after annealing
- Annealing temperature will affect hot-carrier reliability

Tensile

Neutral

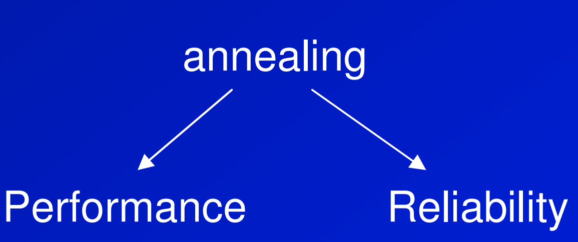
Compressive

Tensile liner A

Compressive liner B

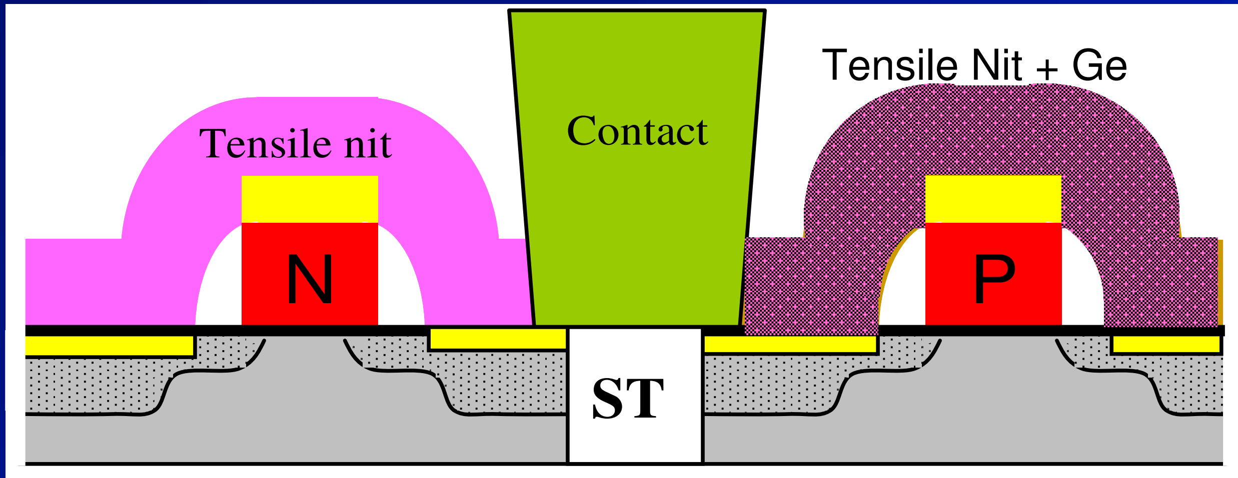
After nitride Liner deposition

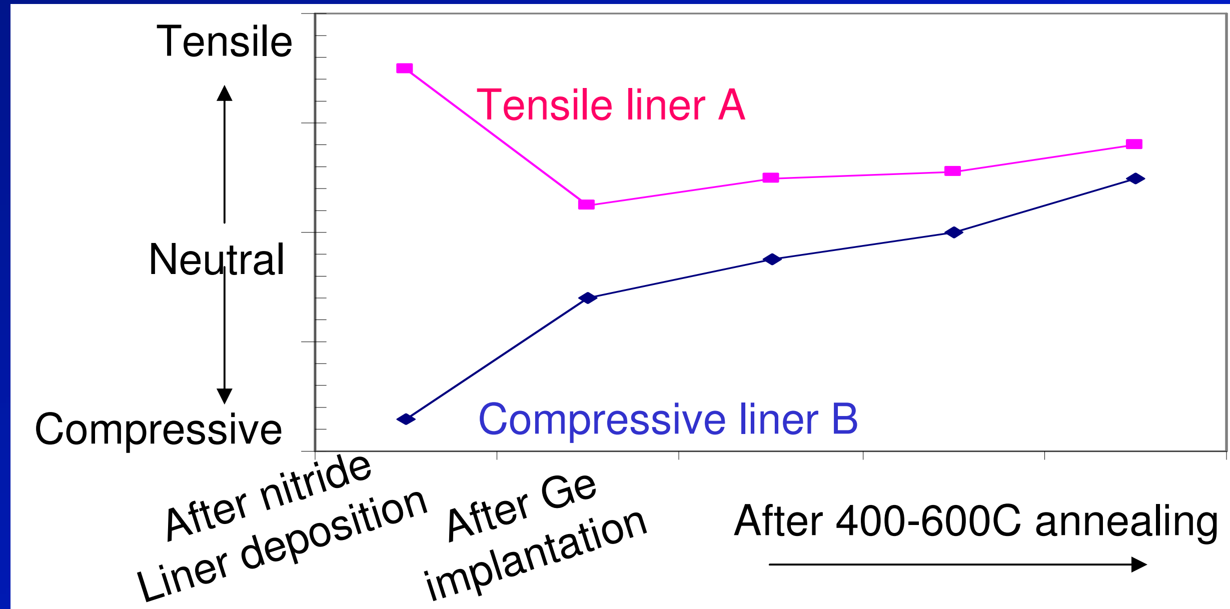
After 400-700C temperature annealing



K. Lim, EESDERC, 2005

Nitride film stress will be relaxed after Ge implant





- Ge implantation destroys and relaxes nit film
- Nit film stress tends to be tensile after annealing

H. S. Yang, IEDM 2004

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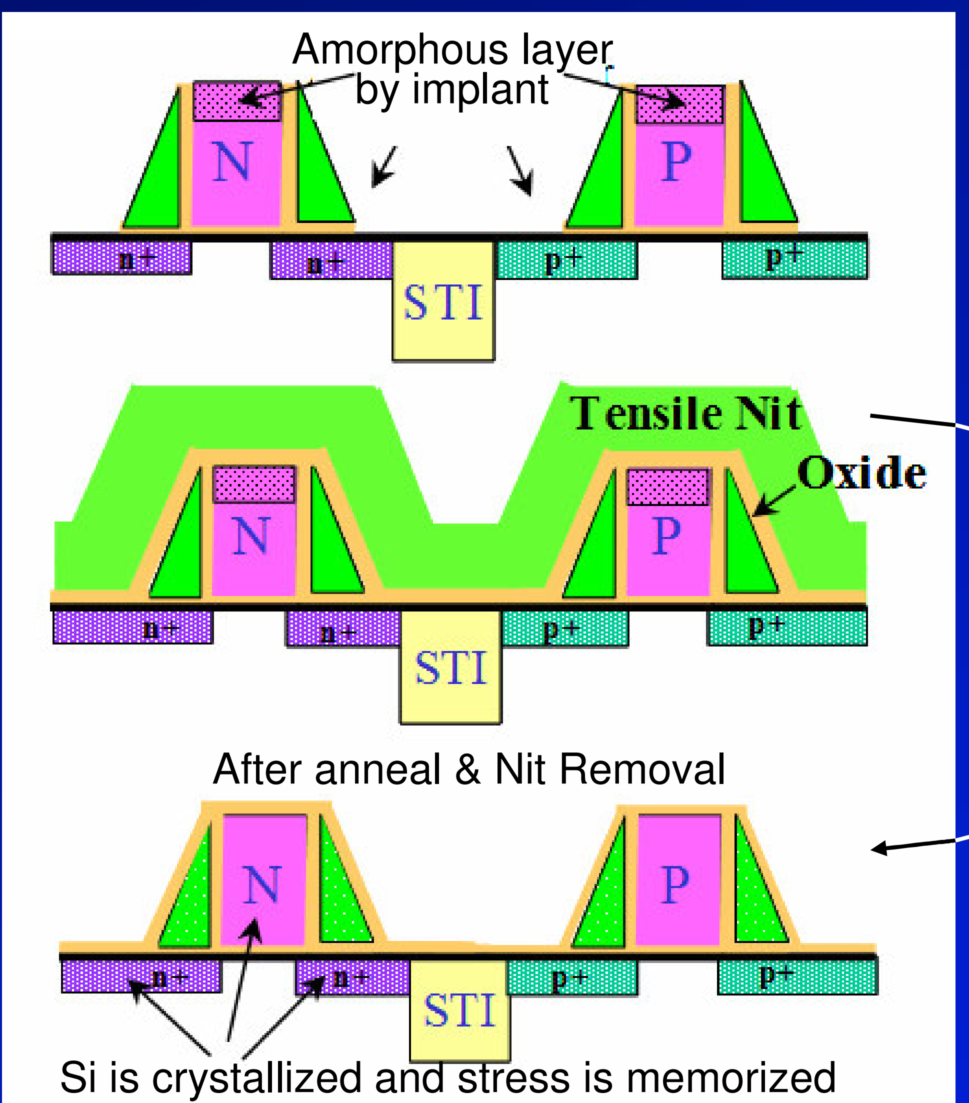
Integration process of SMT



- Stress will be transferred from the nitride film to the channel during annealing.

SMT vs DSL

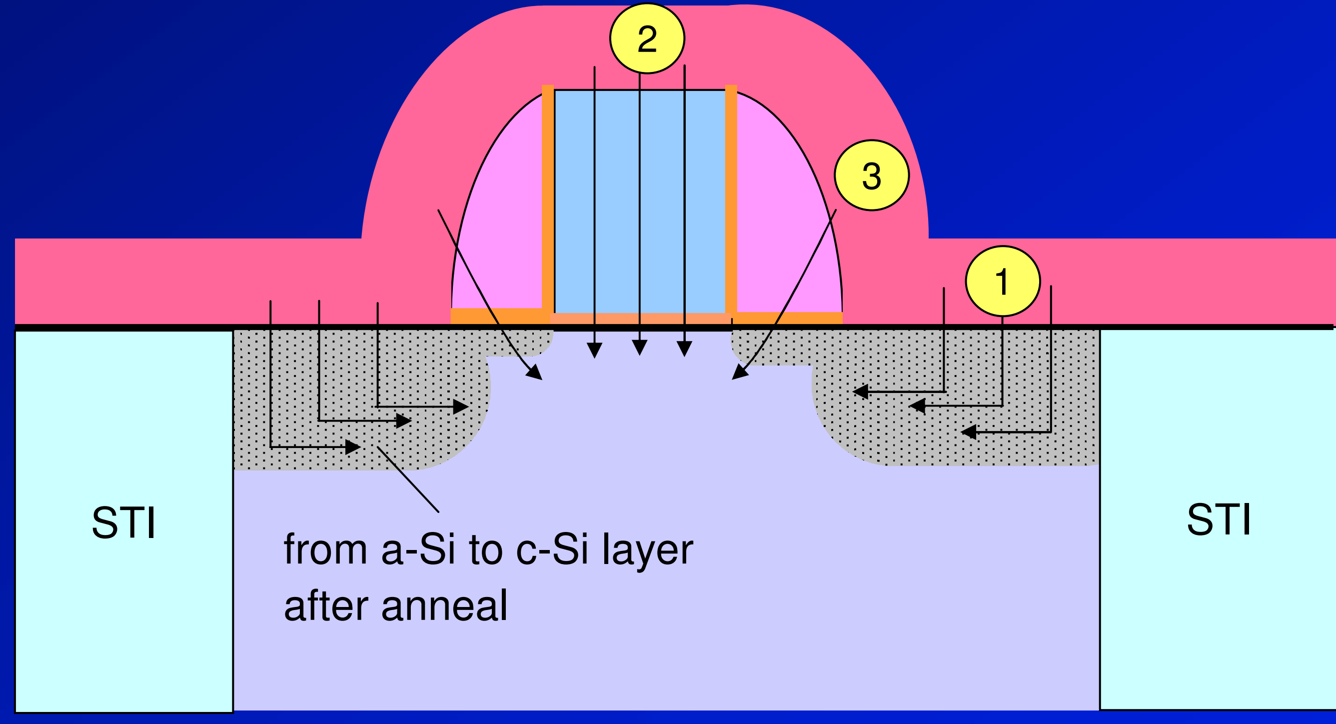
	SMT	contact end-stop liner
Sensitive to Nitride material (stress, thickness)	**yes**	**yes**
Require Annealing (dependent on annealing temperature and ramp rate)	yes	No
Sensitive to a-Si layer (from extension & S/D implant, dependent on implant species, dose, energy)	yes	some
Sensitive to transistor profile (eg. gate height, spacer shape and material)	yes	yes

SMT annealing

Purpose of annealing:

i) Tensile transfer from nitride to Si channel through amorphorization layer in S/D, extension and poly gate.

ii) a-Si crystallization



NMOS: 15% current improvement with Disposable Tensile Stressor

SMT benefit with different types of Nitiride stressor

- Stress properties of nitride material is changed after annealing

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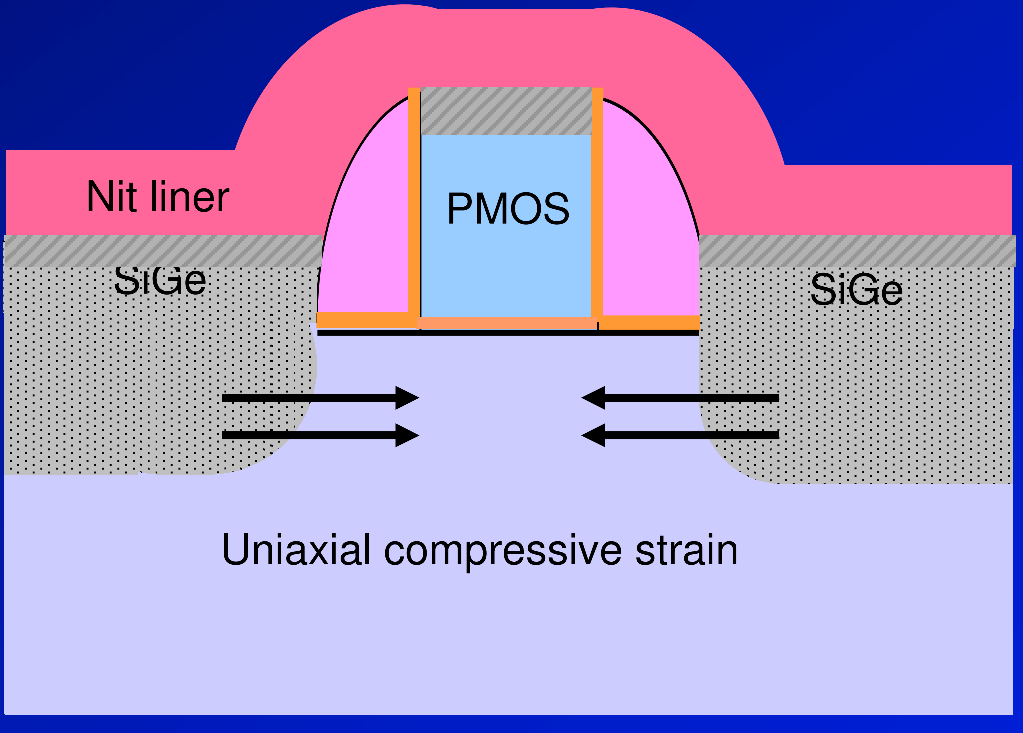
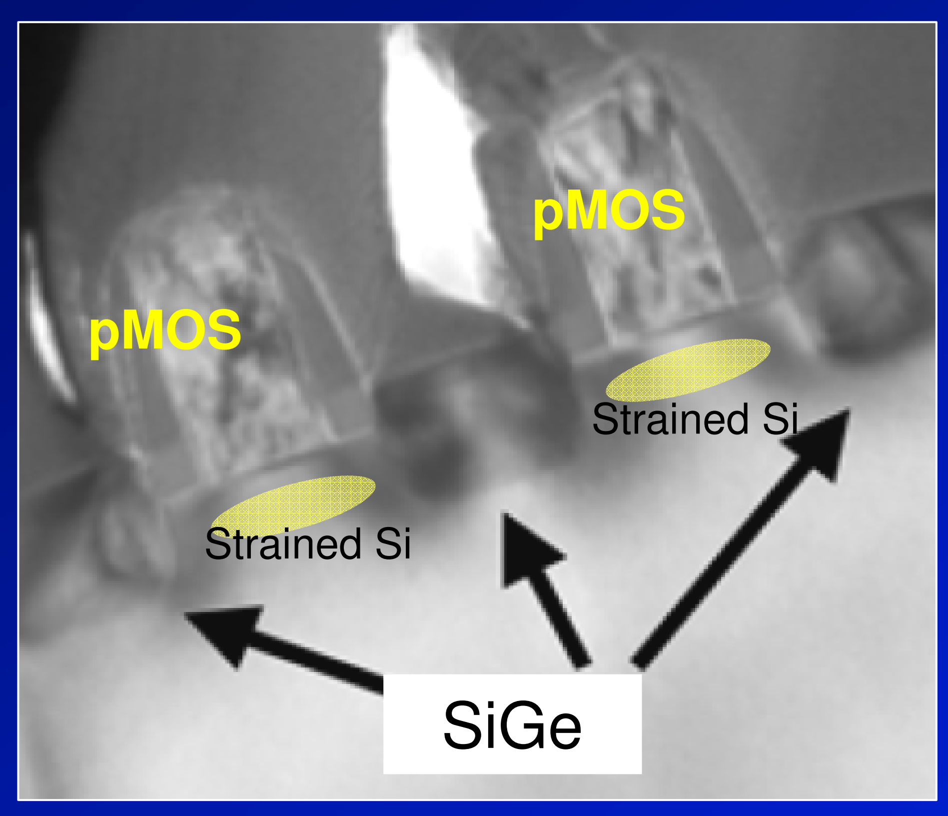
PMOS with e-SiGe structure in S/D

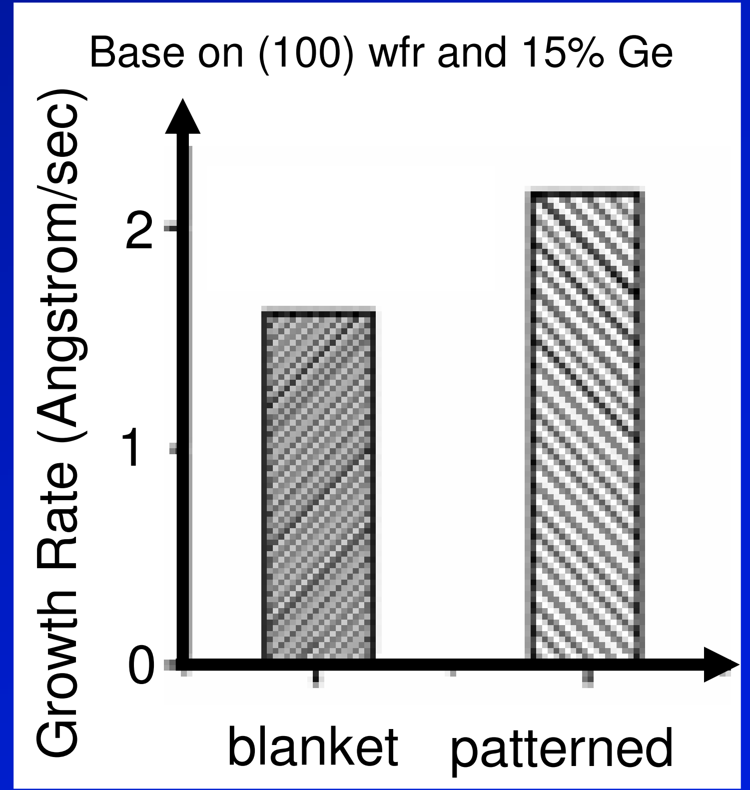
- Uniaxial stress in Si channel induced by SiGe S/D
- higher hole mobility to enhance drive current



SEM photo and SiGe grow rate

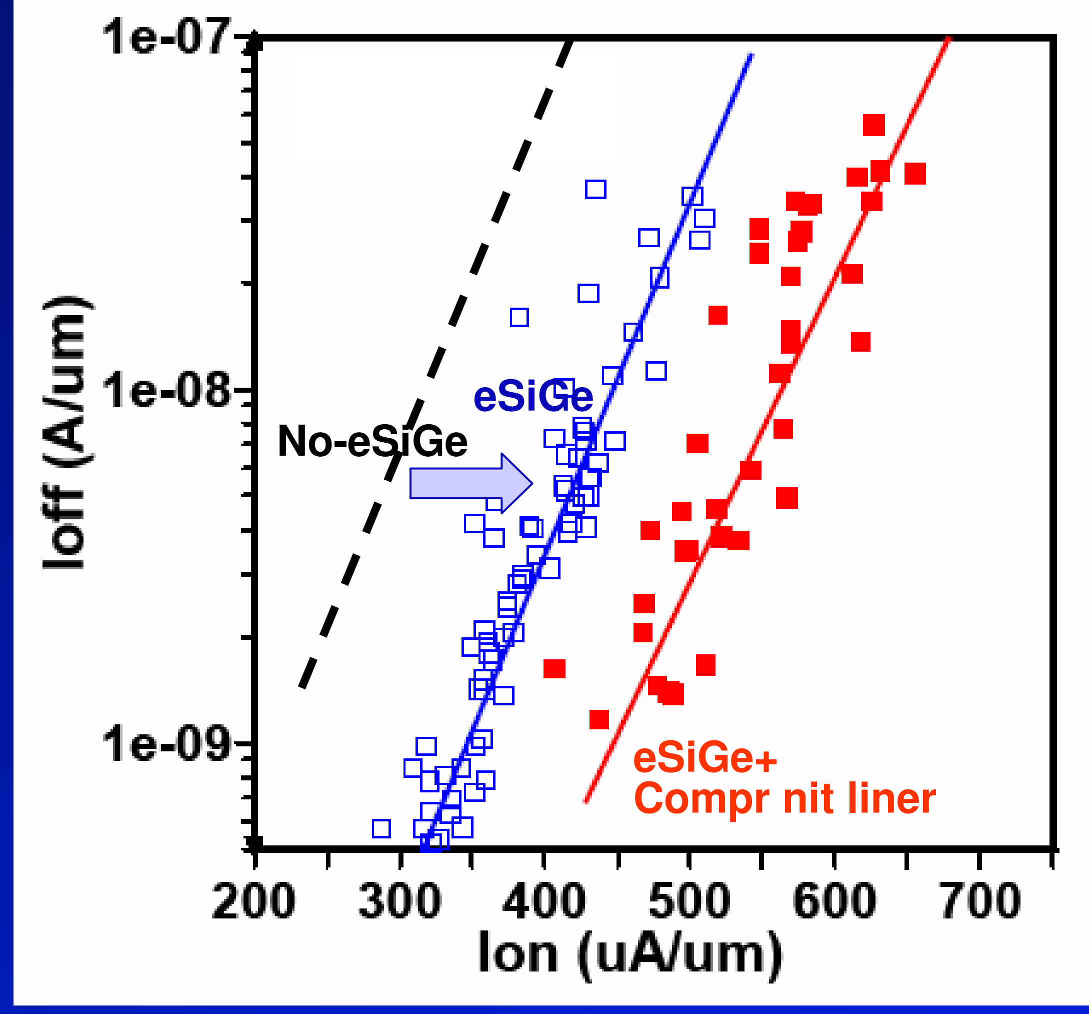
- SiGe epi growth rate in S/D is dependent on pattern density





C. Ouyang, *VLSI Sym*, 2005

PMOS Ion-Ioff for e-SiGe



From iedm 05, ibm, Luo

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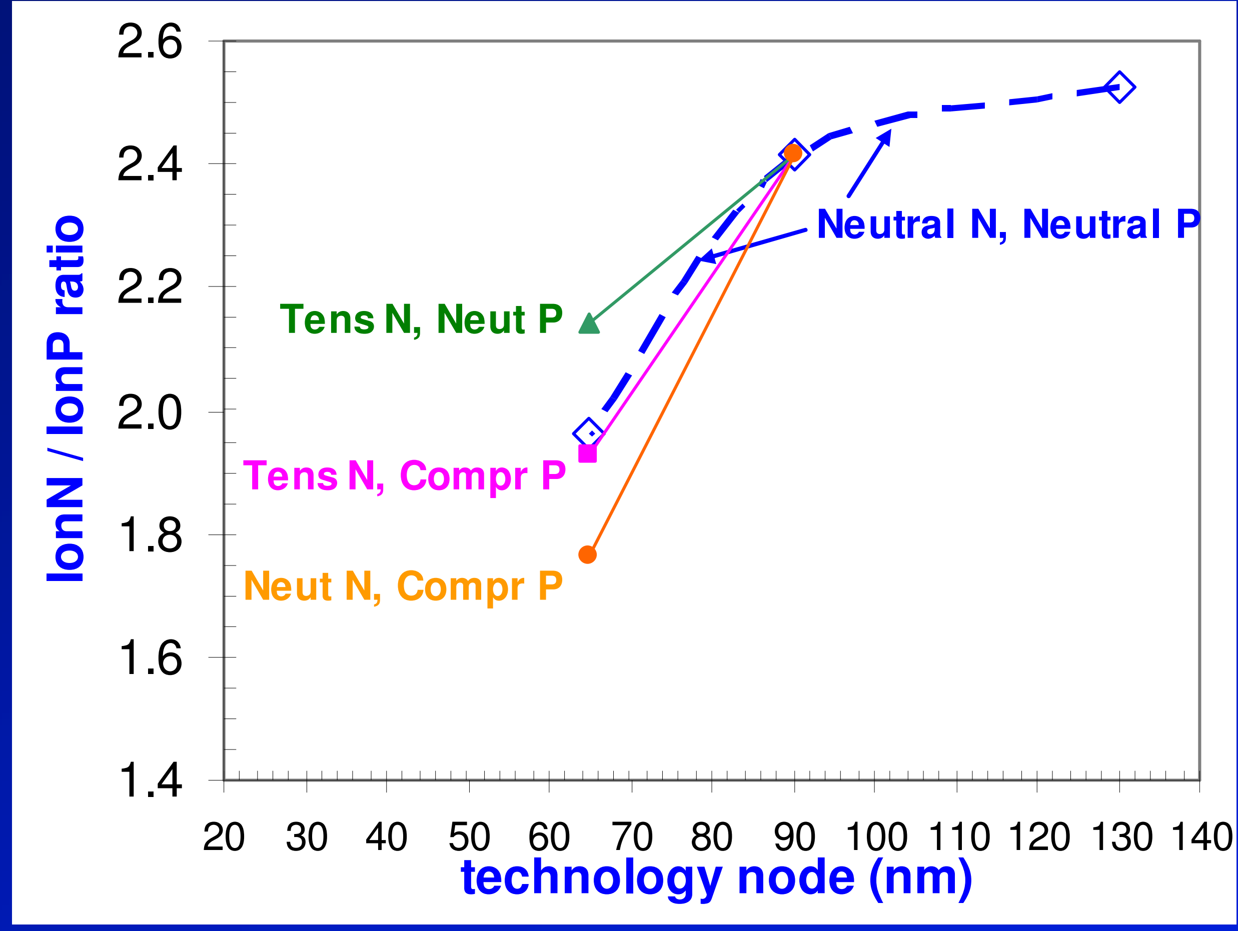
Ion_N / Ion_P ratio in the Recent Technology Nodes

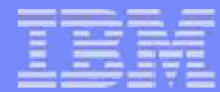
- Stress engineering → Ion changes → Ion_N / Ion_P (beta) ratio may change



Vt shift due to longitudinal tensile stress

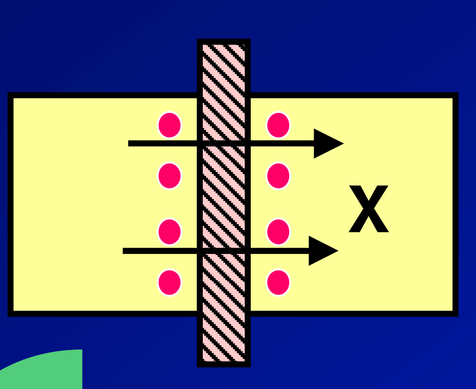
- Channel Stress can change the energy band gap of Si channel

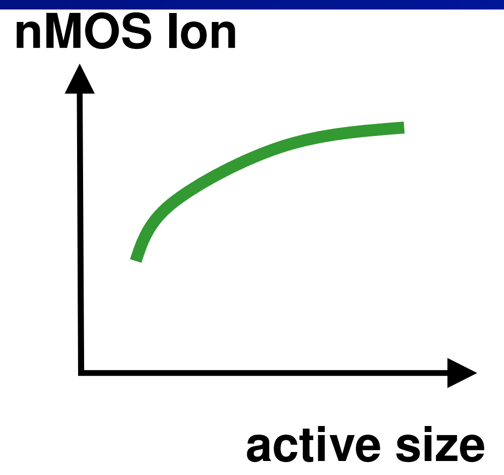
Un-stress
Tensile
Un-stress
Tensile
Vtlin (V)
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
0.01
0.1
Lpoly (um)

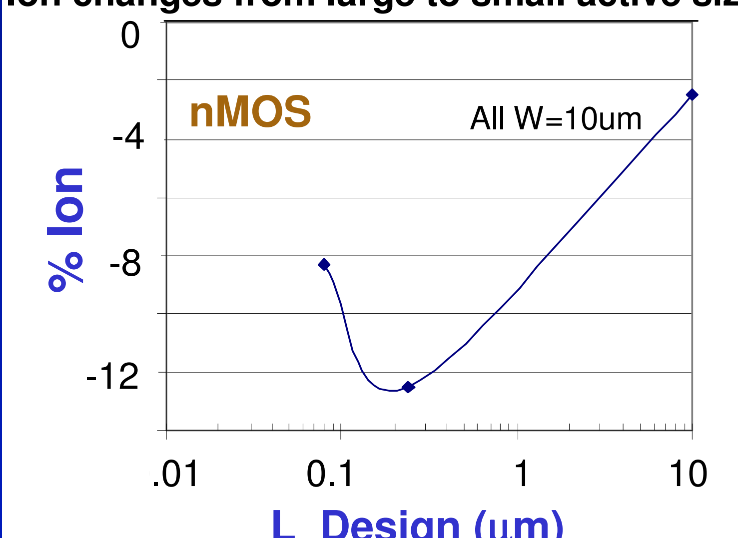


Different Active Sizes (along channel)

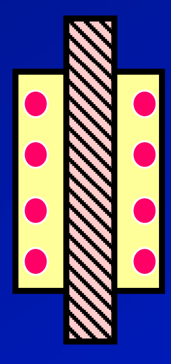
- STI provides longitudinal stress and affect N/P Ion.

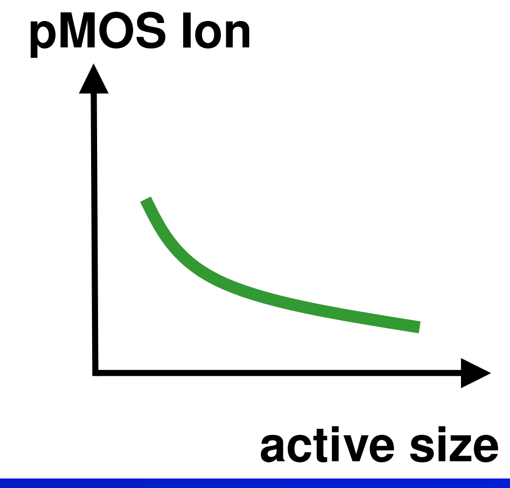


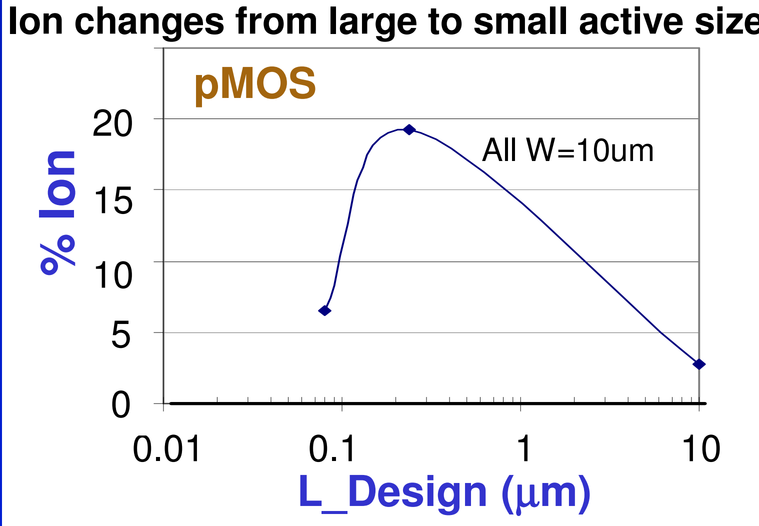




X-direction: more compressive
IonN decreases,
IonP increases







STI Stress Proximity Effect (Different Device Lengths)

Lgate (μm)

0.24

0.045

10

10

0.045

0.24

active size

pMOS

nMOS

n-10x0.045
n-10x0.24
n-10x10
p-10x0.045
p-10x0.24
p-10x10

Δ Drive current (%)

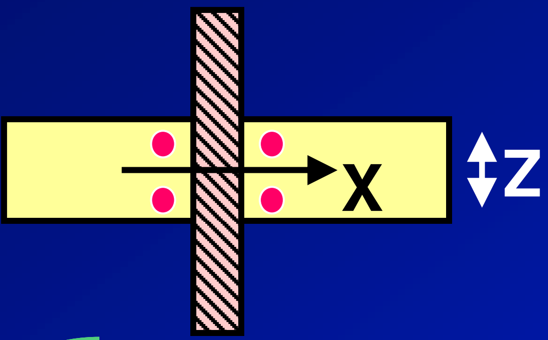
25
20
15
10
5
0
-5
10
-15

0
0.2
0.4
0.6
0.8
1
1.2
1.4

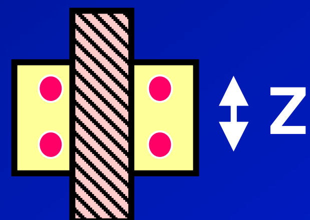
active size (symmetric) (μm)

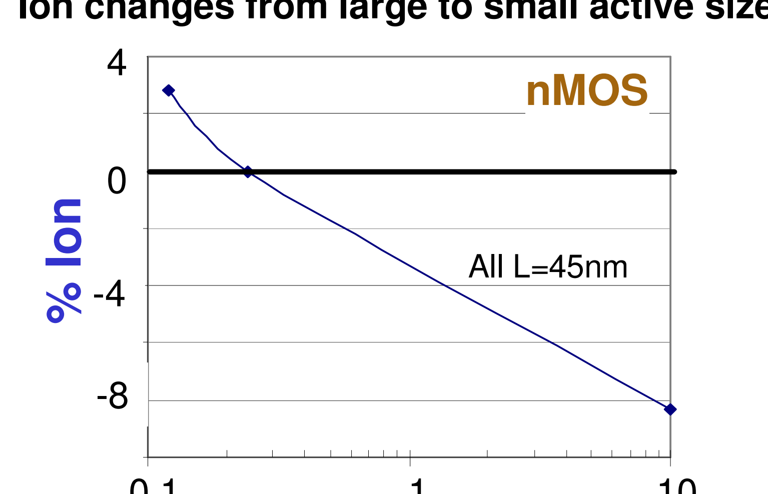
Different Active Sizes with different widths (bi-axial effect)

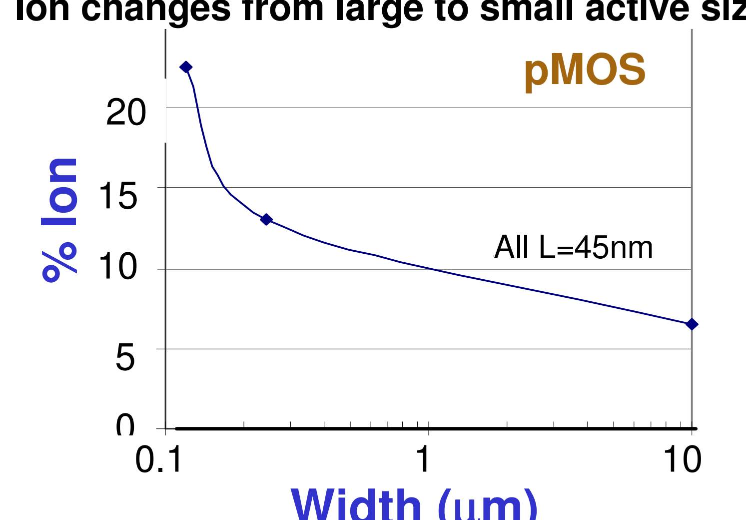
- STI provides both longitudinal and lateral stress and affect N/P Ion.



Z-direction: more compressive
IonN decreases,
IonP decreases







V. Chan, *IEDM*, 2003

STI Stress Proximity Effect (Different Device Widths)

V. Chan, *IEDM,* 2003

Technology development & Stress Engineering (1) [*Stress engineering is developed early*]

Base Line Development

Pre-manufacturing

Develop Strained Si

Fabrication Process

Modify Device model after mobility enhancement; include STI stress proximity model

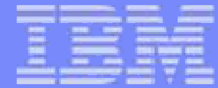
Mask tape-out (additional mask may be required)

Circuit adjustment

Stress Engineering Discovery

Circuit Design

Time



Technology development & Stress Engineering (2) [*Stress engineering is developed a little bit late*]

Base Line Development

Pre-manufacturing

Develop Strained Si Fabrication Process (late development)

Modify Device model after mobility enhancement: include STI stress proximity model

Not enough Time

*Mask tape-out (**additional mask** may be Required. logic vs array)*

Not Enough Time

Circuit adjustment

Stress Engineering Discovery

Circuit Design

Time

Technology development & Stress Engineering (3) [Device adjustment]

Stress engineering will change the devices:

1) Ion
2) Vt and Ioff

The change will be also dependent on

i) Active area dimension (longitudinal and lateral)
ii) Device length and width

Pre-manufacturing

a) Device re-centering

b) Additional mask
** different circuit region (eg. SRAM array) may have different device centering conditions*

c) SRAM stability & yield consideration
** Device centering to provide good read stability and writibility margin*

Time

Technology development & Stress Engineering (4) [Other consideration]

i) **Extra fabrication process**.

It may involve :

a) substrate preparation;

b) nitride deposition → process temperature, thickness, stress level, conformity

c) extra annealing → this may affect dopant activation / deactivation and device reliability (eg hot carrier);

d) lithography;

e) dry etch / wet etch;

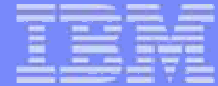
f) implantation.

ii) **Ground rule consideration**, especially in the SRAM cell.

iii) Critical path and circuit performance.

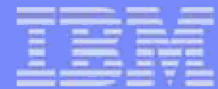
iv) **Stress Monitoring** by electrical device data and in-line stress monitoring procedure.

v) Fabrication process: cycle time, repeatability, uniformity, cost and yield.



❖ Outline

- Introduction: Strain helps carriers to travel faster
- Substrate-induced strain
- Process-induced strain
  - Contact etch-stop nitride liner (DSL)
  - Stress Memorization Technique (SMT)
  - Embedded SiGe in S/D (e-SiGe)
- Stress and Device / Circuit Implication
- **Mobility Improvement beyond Stress Engineering**
  - **Channel Orientation**
  - Substrate Orientation (eg. HOT)
- Summary



X (100)

<0$\bar{1}$1> channel

Z (001)

< 011> channel

0º notch

Y (010)

X (100)

<001>
channel

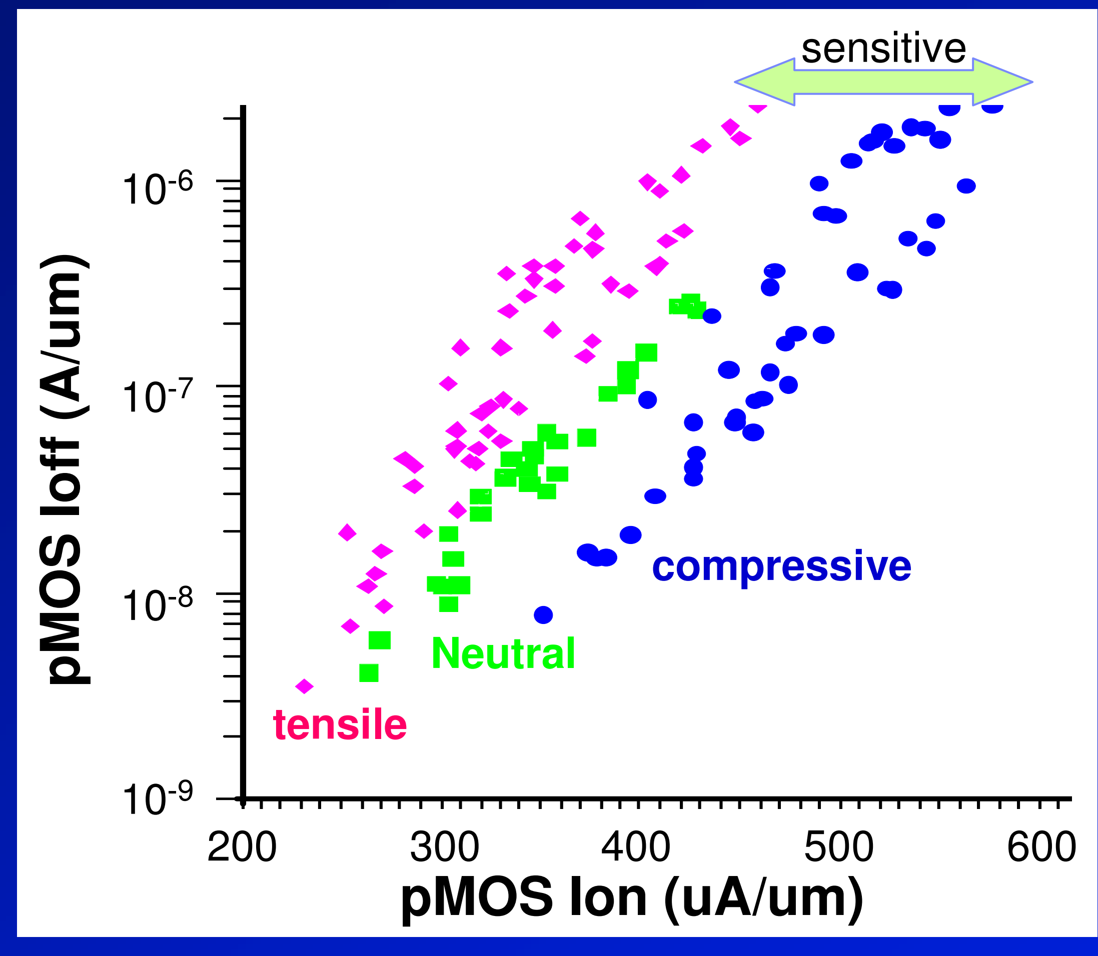
Z (001)

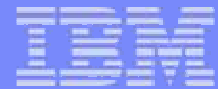
<010>
channel

45º notch

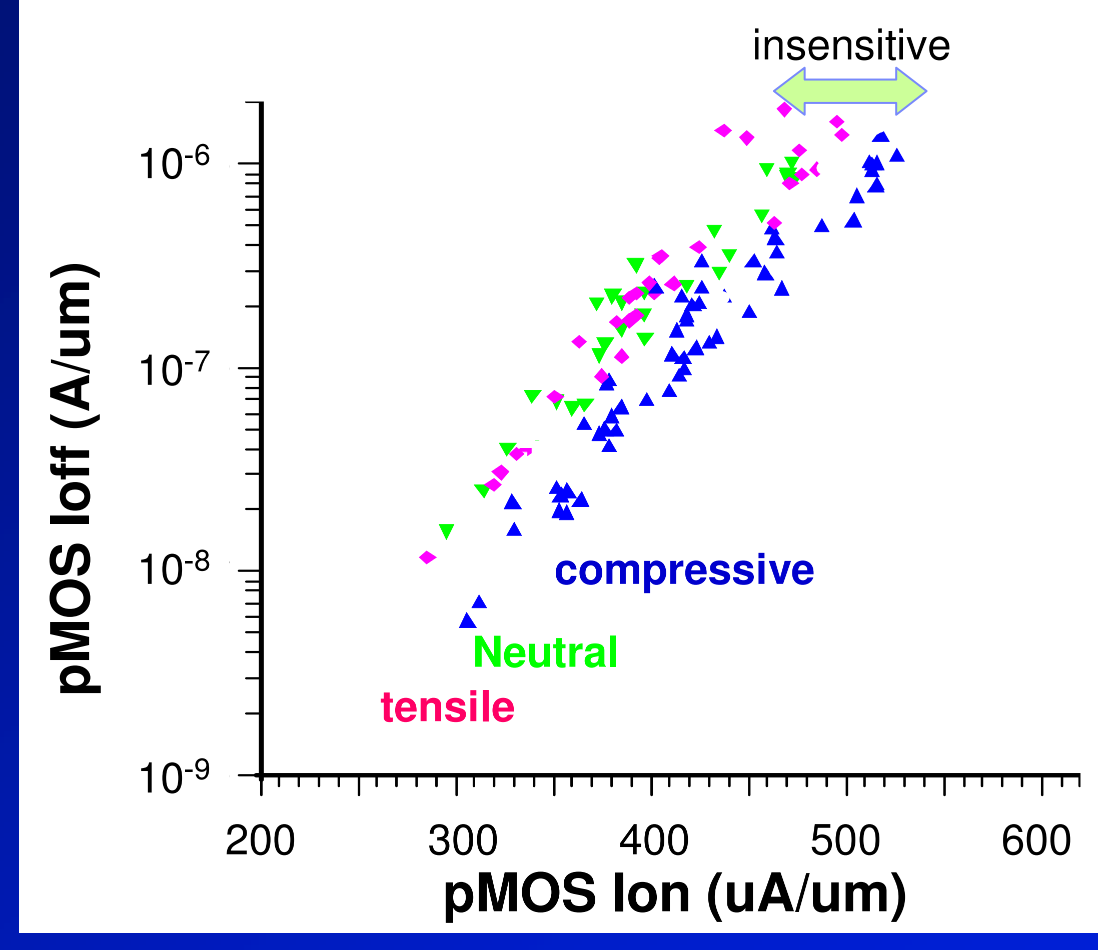
Y (010)

<110> (0deg notch) pMOS mobility is *very sensitive* to longitudinal stress





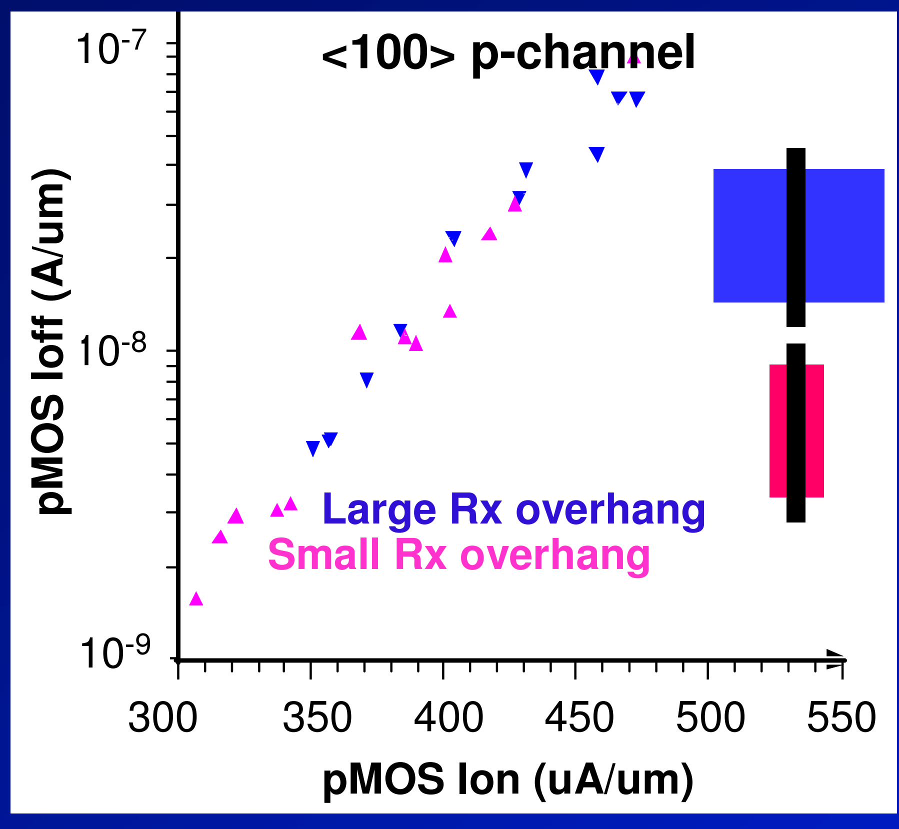
<100> (45deg notch) pMOS mobility is *insensitive* to longitudinal stress

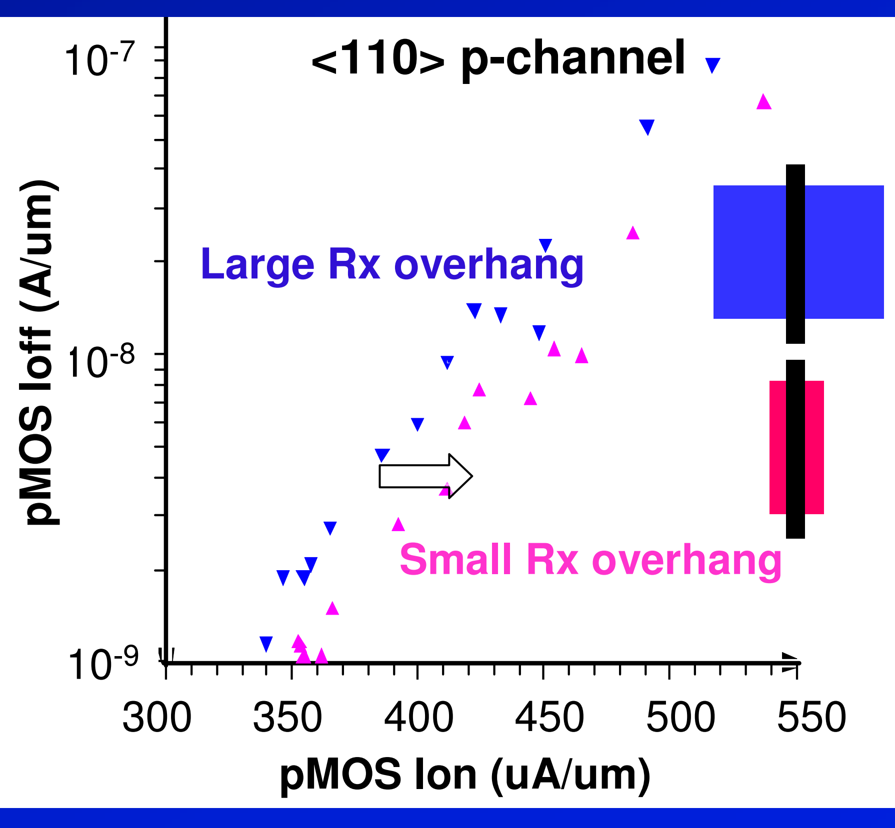


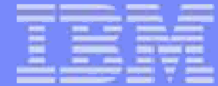
Both <110> (0 deg) and <100> (45deg notch) nMOS mobilities are *very sensitive* to longitudinal stress

nMOS Ioff (A/um)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
300 400 500 600 700 800 900 1000 1100
nMOS Ion (uA/um)
compressive
Neutral
tensile
Solid = <110> channel
Open = <100> channel
Tensile
45deg
0deg
Ioff (nMOS)
Ion (nMOS)

<100> pMOS is not sensitive to STI proximity stress







❖ Outline

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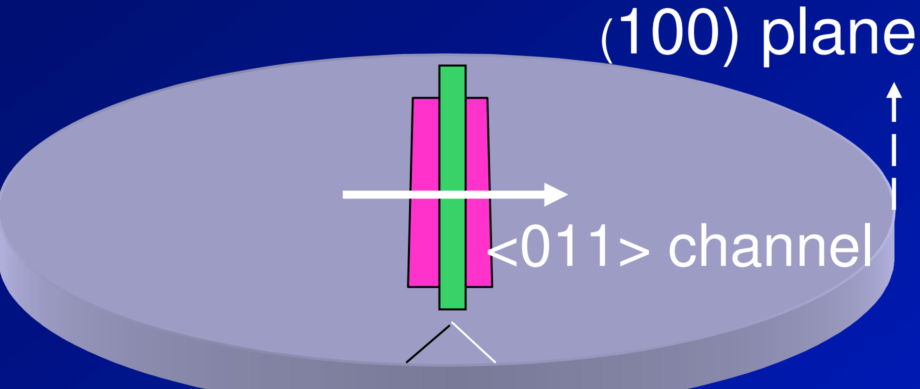
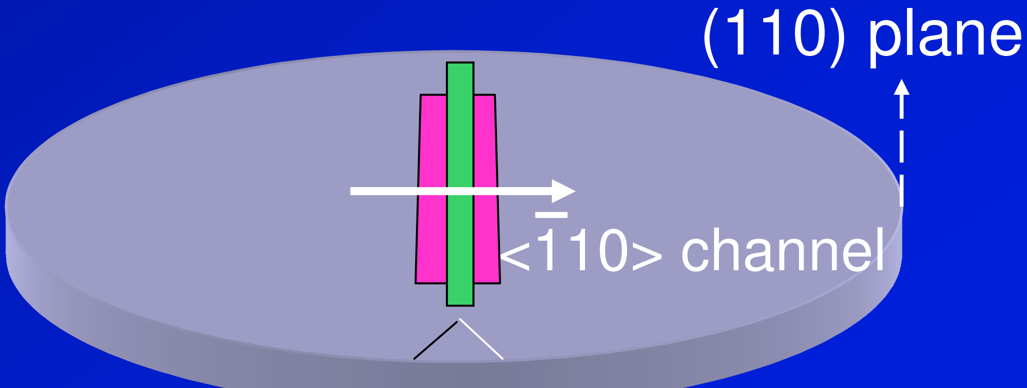
* Stress and Device / Circuit Implication
* **Mobility Improvement beyond Stress Engineering**
  - Channel Orientation
  - **Substrate Orientation (eg. HOT, DSB)**
* Summary

(100) and (110) wafers





Note: <110> and <001> channel in (110) substrate have different mobility enhancement.

Carrier Mobility Dependence on Surface Orientation

Holes

Hole Mobility ($cm^2V^{-1}s^{-1}$)

150

100

50

0.0

$5.0x10^{12}$

$1.0x10^{13}$

$1.5x10^{13}$

N_{inv} (cm^{-2})

(110)/<110>

> 2x

(111)/<112>

(100)/<110>

Electrons

Electron Mobility ($cm^2V^{-1}s^{-1}$)

300

200

100

0.0

$5.0x10^{12}$

$1.0x10^{13}$

$1.5x10^{13}$

N_{inv} (cm^{-2})

(100)/<110>

(111)/<112>

(110)/<110>

Electron mobility is highest on (100) surface

Hole mobility is highest on (110) surface

→ Combine the (100) and (110) surfaces to obtain the highest mobility for electrons and holes

M. Yang, *IEDM* 2003, M. Yang, *VLSI* 2004

CMOS fabrication on Substrates with Hybrid Orientation (1)

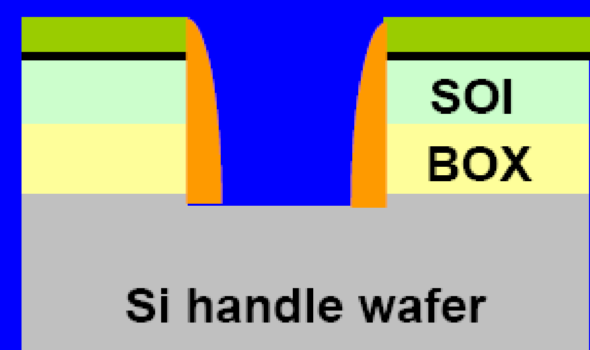
Nitride

(100) SOI

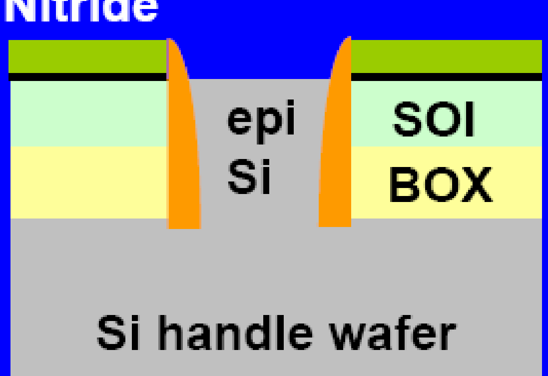
BOX

(110) Si handle wafer

Step 1: Thin oxide & nitride deposition

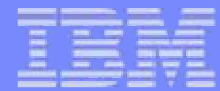


Step 2: SOI/BOX stack etching and spacer formation

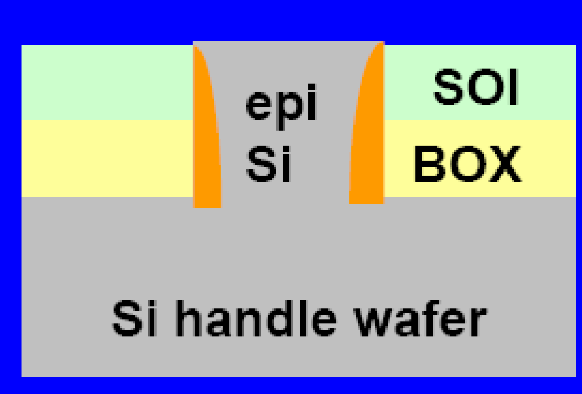


Step 3: Si epitaxy, CMP and recess

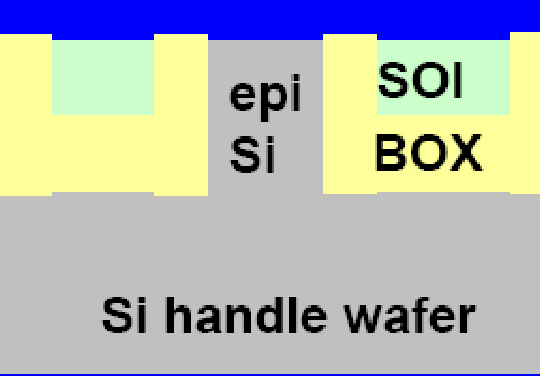
M. Yang, *IEDM* 2003, M. Yang, *VLSI* 2004



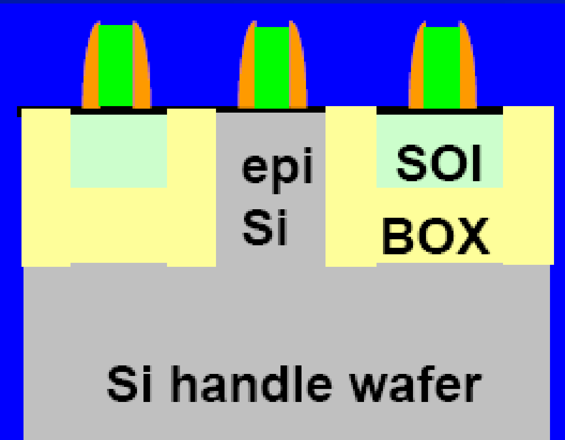
CMOS fabrication on Substrates with Hybrid Orientation (2)



Step 4: Thin nitride & oxide strip

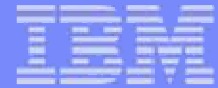


Step 5: Shallow trench isolation



Step 6: Continue CMOS fabrication

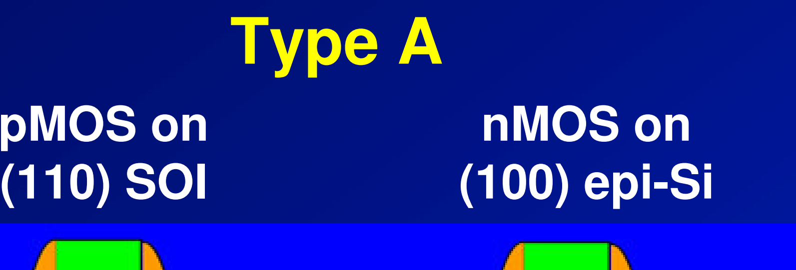
M. Yang, *IEDM* 2003, M. Yang, *VLSI* 2004



CMOS Structure Using HOT

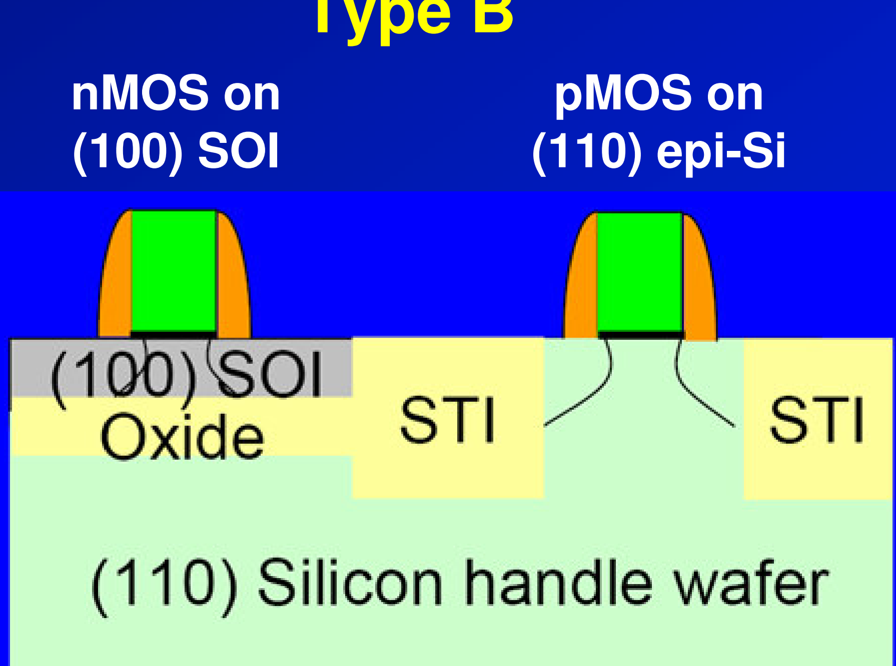
Type A

pMOS on (110) SOI | **nMOS on (100) epi-Si**



Type B

nMOS on (100) SOI | **pMOS on (110) epi-Si**



Key Process Step	Type A	Type B
Selective Epitaxy	grow (100) Si	grow (110) Si
layer transfer @ bonding	in (110) Si	in (100) Si

M. Yang, *IEDM* 2003, M. Yang, *VLSI* 2004

Carrier Mobility Dependence on Surface Orientation

PMOS

NMOS

STI

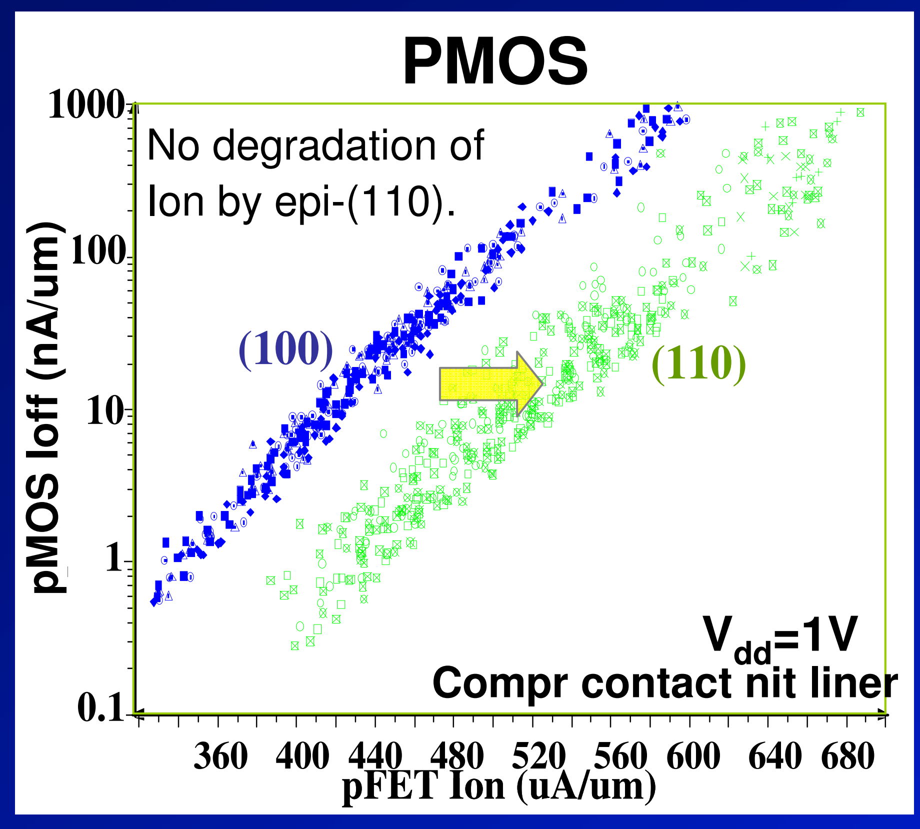
buried oxide

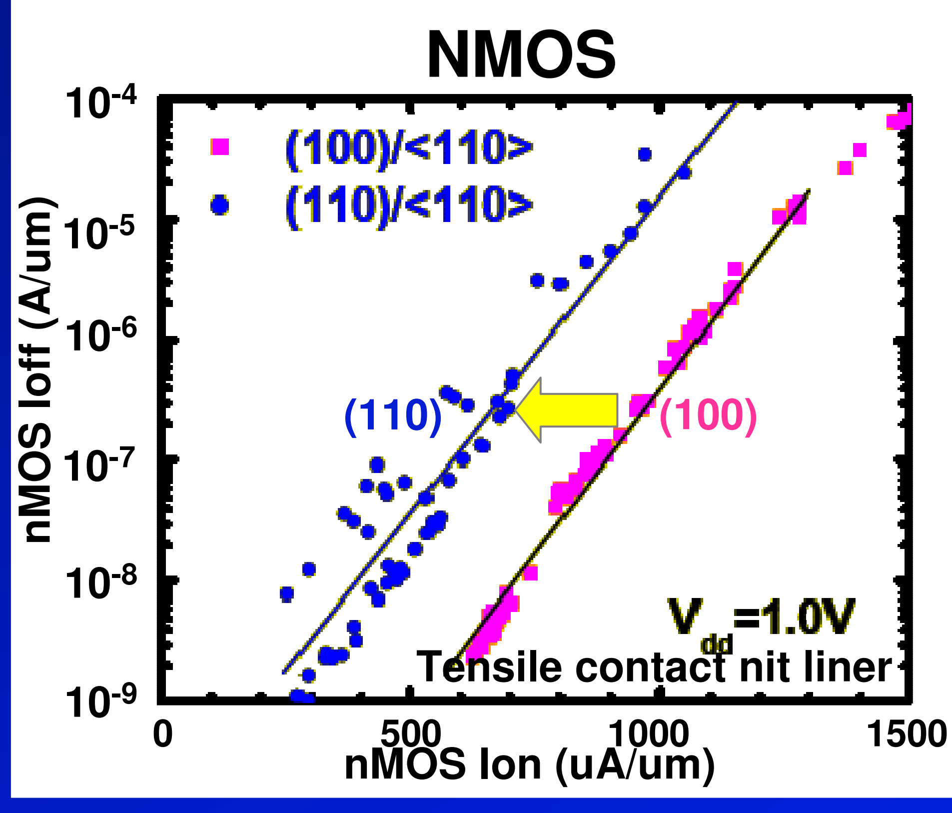
(110) Si handle wafer

- pMOS on (110) surface and nMOS on (100) surface
- Forming hybrid substrate using wafer bonding and Si epitaxy – One additional litho level
- Planar structure, fully compatible with standard CMOS processes

M. Yang, *IEDM* 2003, M. Yang, *VLSI* 2004

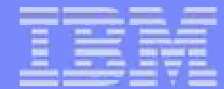
Performance of CMOS on Bulk Silicon Substrates



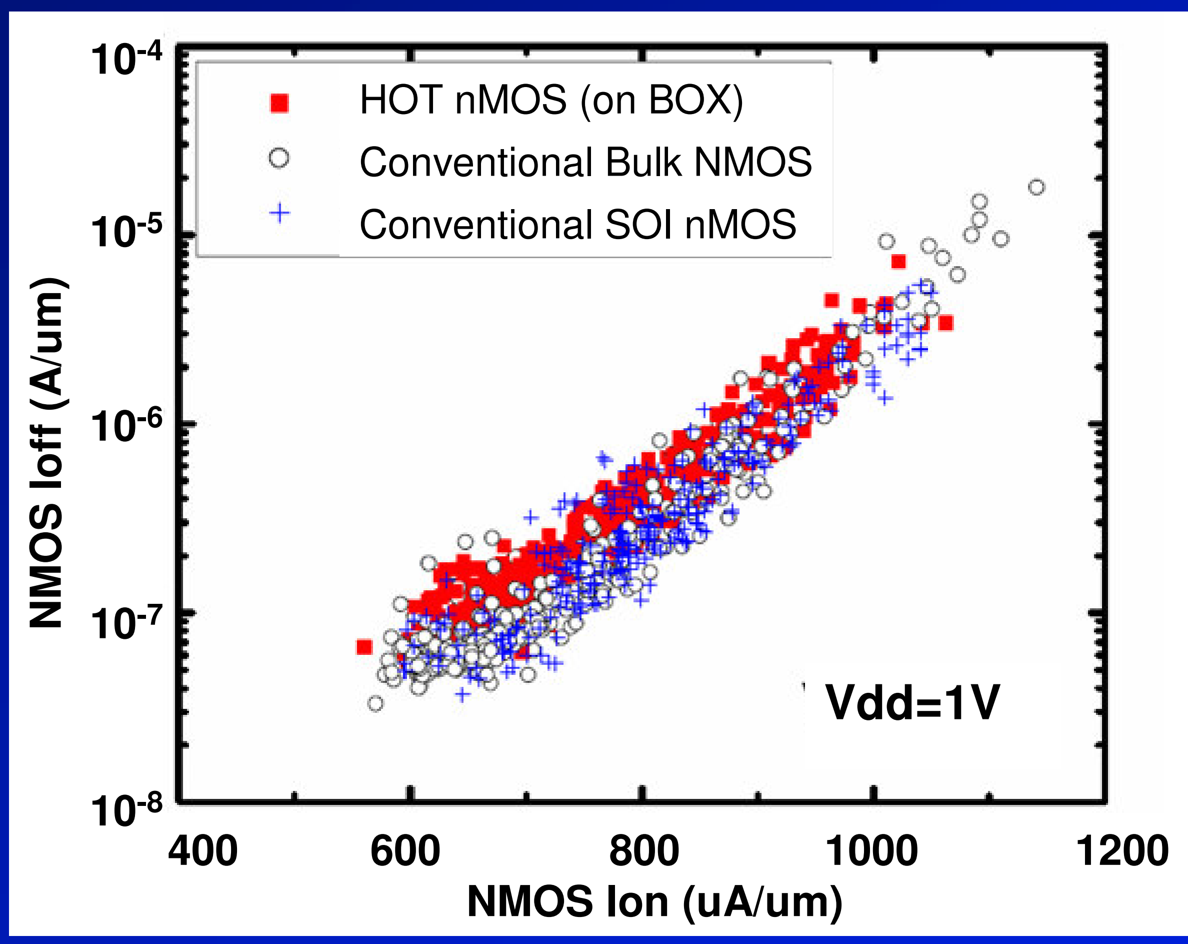


	PMOS Δ Ion	NMOS Δ Ion
Ioff = 100uA/um	+20%	**-35%**
Ioff = 10nA/um	+26%	-50%

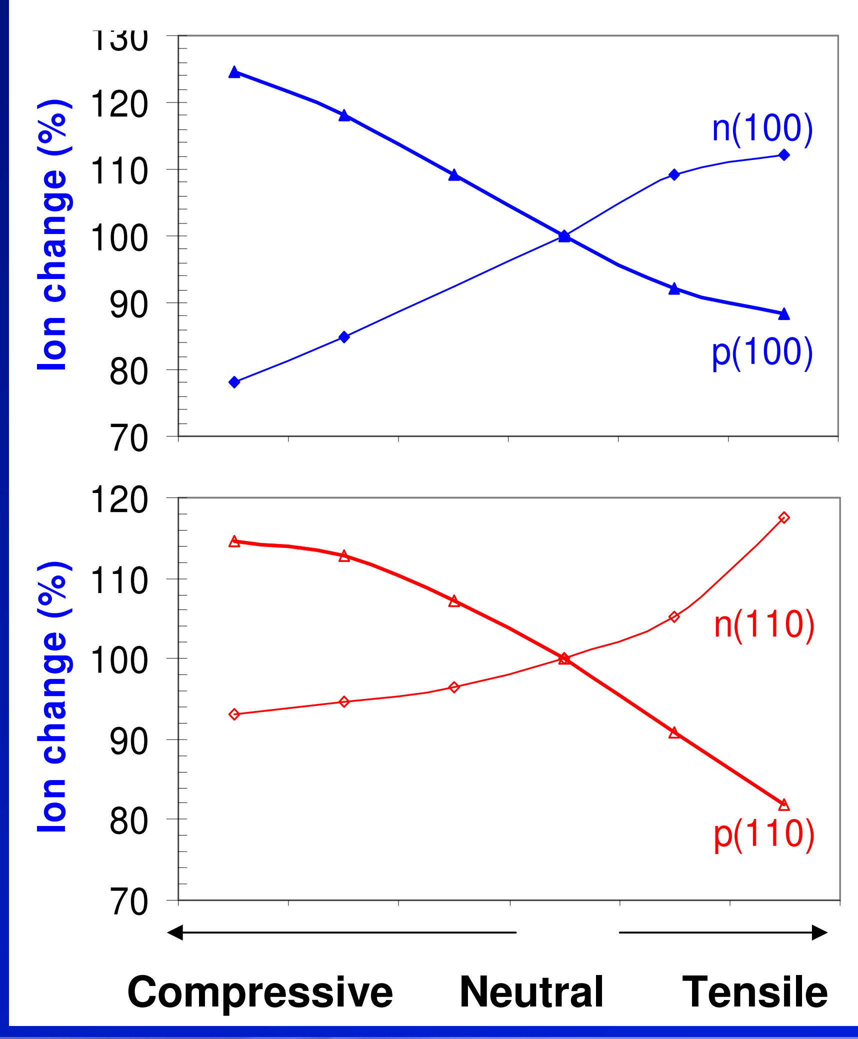
M. Yang, *IEDM* 2003, M. Yang, *VLSI* 2004



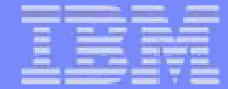
HOT NMOS has same Ion as conventional bulk NMOS and bulk SOI.



Carrier mobilities in (100) and (110) substrates are both sensitive to longitudinal stress in channel.



PMOS on (110) substrate performance is further enhanced by stress engineering



Mobility Enhancement is dependent on device orientation

(110)-Y (compressive)

(100), X,Y

(110)-X (compres)

(110)-Y

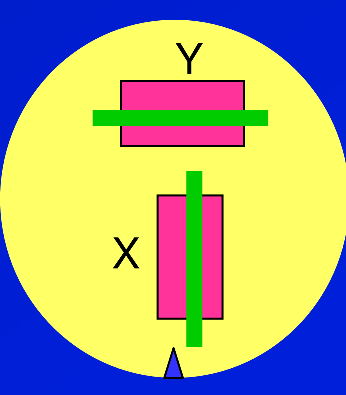
(110)-X

Solid symbol = X = [1$\bar{1}$0] direction

Open symbol = Y = [001] direction

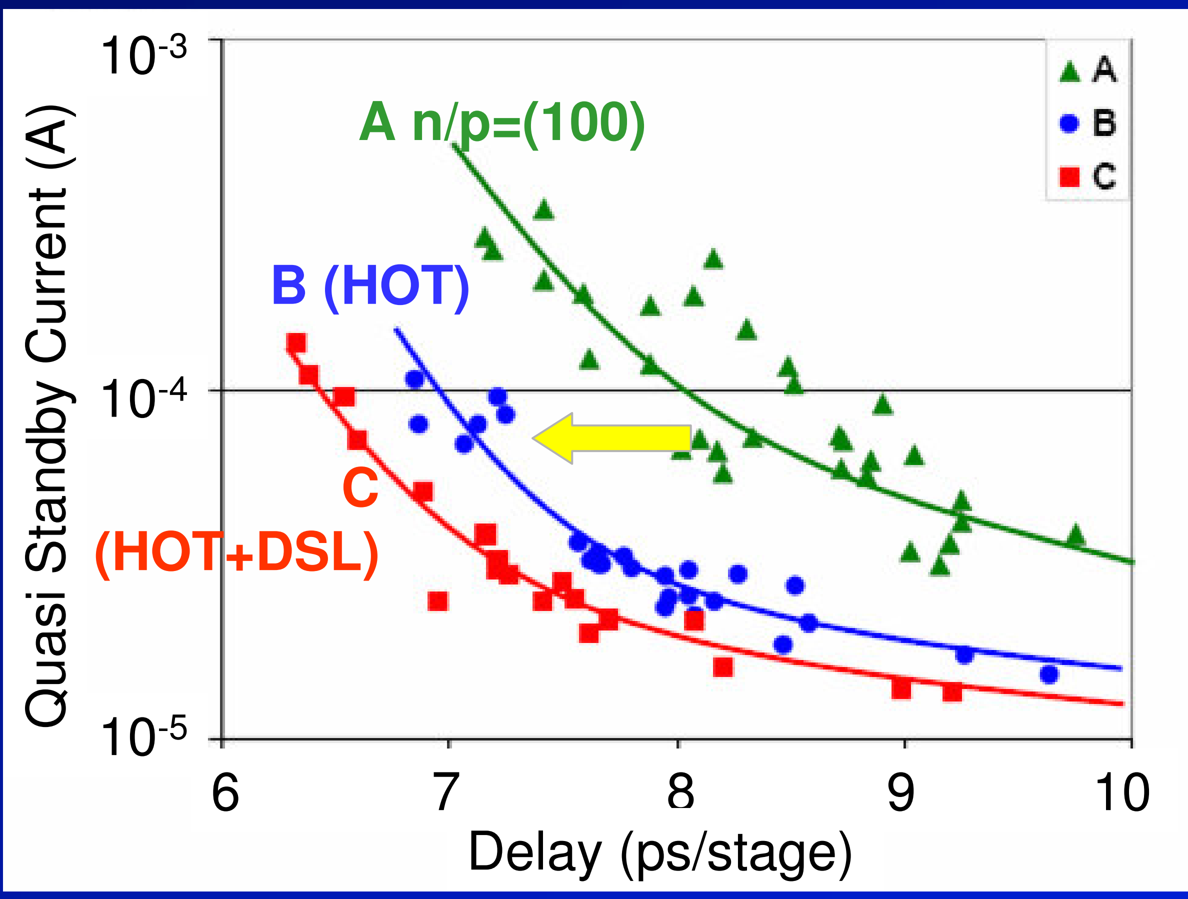
PMOS Ioff (nA/um): 1000, 100, 10, 1

PMOS Ion (uA/um): 350, 400, 450, 500, 550, 600, 650



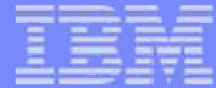
C. D. Sheraw, VLSI 2005

Ring Oscillator Delay is improved by higher PMOS Ion with HOT process



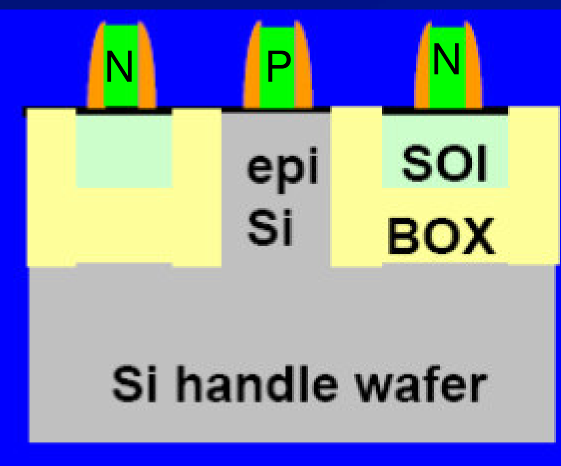
	NMOS	PMOS
A	(100) SOI Tens liner	(100) SOI Neutral liner
B	(100) SOI Tens liner	(110) bulk Neutral liner
C	(100) SOI Tens liner	(110) bulk Comp liner

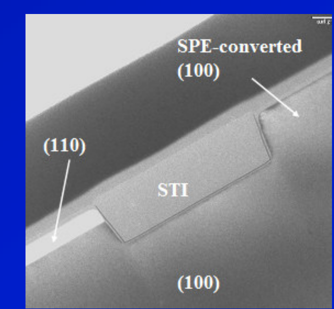
C. D. Sheraw, VLSI 2005



DSB – Direct silicon Bonding

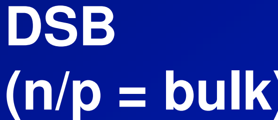
HOT
(p=bulk, n = SOI)

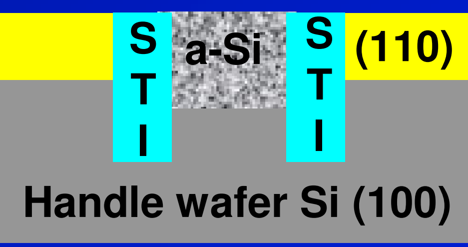


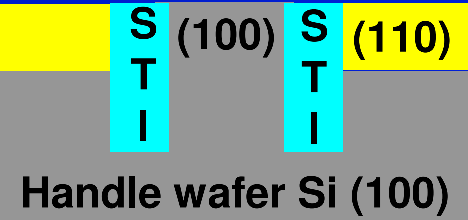


Ox free interface

DSB
(n/p = bulk)







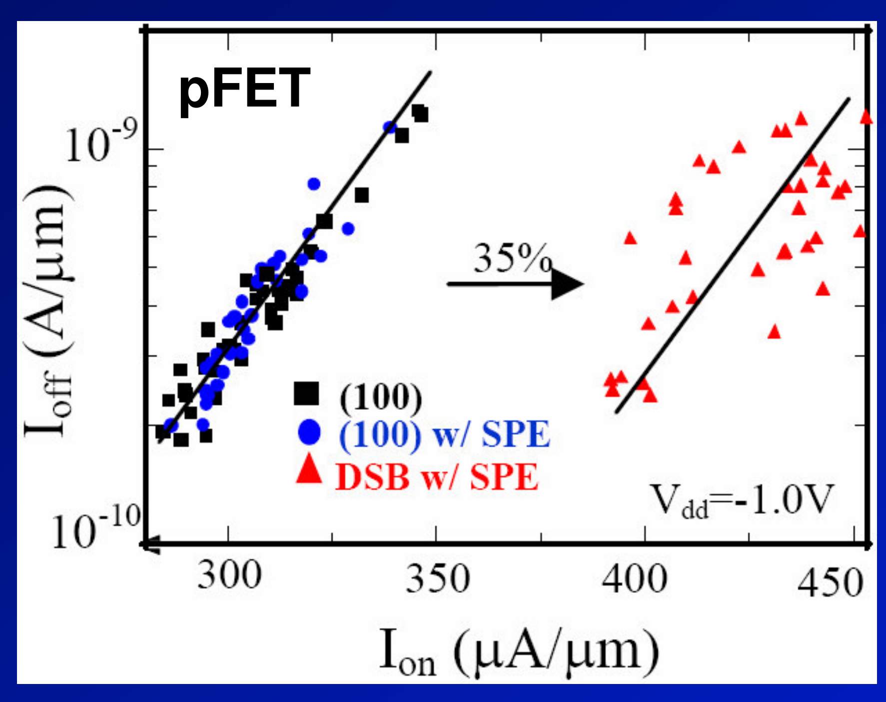
Step 1: (110)/(100) DSB

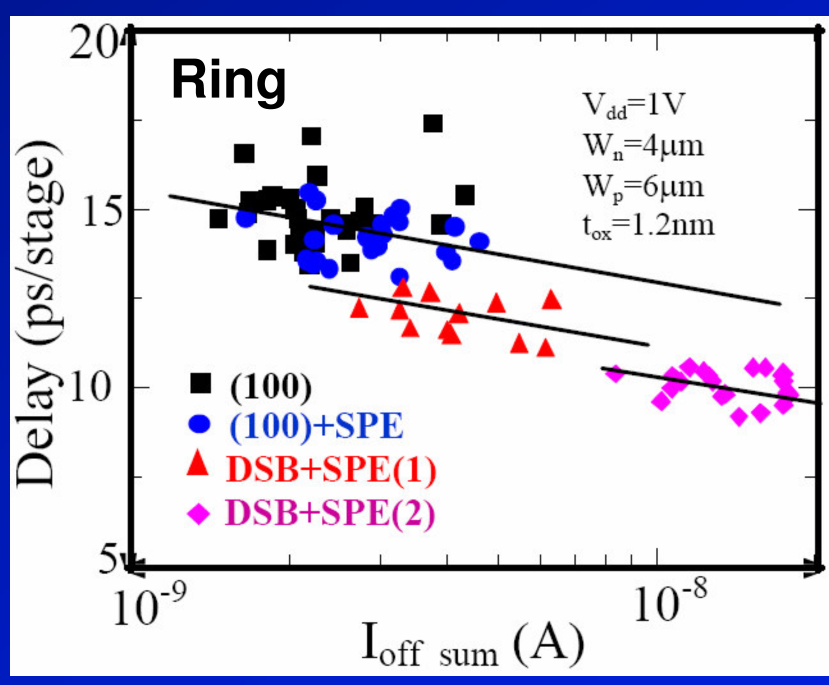
Step 2: selective implant

Step 3: SPE & CMOS

SPE=solidd phase epitaxy

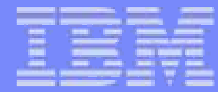
pFET performance comparison





- **pFETs on DSB shows 35% enhancement compared to (100)**
- **Ring oscillator speed is improved by higher pFET Ion in DSB.**

DSB=direct silicon bonding
SPE=soild phase epitaxy



(100) vs (110) substrates: vector notation

- don't be confused by **<110> channel** in (100) Substrate and **(110) substrate**

(100) substrate

X

<0$\bar{1}$1> channel

Z (001)

< 011> channel

Y (010)

(110) substrate

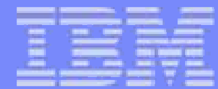
X (100)

Z (001)

Y (010)

<001> channel (bad)

<1$\bar{1}$0> channel (good)



0 deg vs 45 deg on (100) wafer: vector notation

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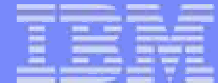

Summary

	NMOS	PMOS	Disadvantage & limitation
Biaxial Tensile Strain	↑	↑	Extra cost on substrate, difficulty in substrate preparation, integration, & device design.
Contact etch-stop liner (DSL)	↑	↑	Extra steps in integration, ground rule considera tion
SMT	↑	o	Extra steps in integration
e-SiGe	o	↑	High process complexity, difficulty in epi-growth, yield
Substrate Orientation (HOT, DSB)	o	↑	Extra Cost on hybrid substrate, extra steps eg. Epi to prepare isolation
Channel Orientation (<100>, 45deg)	o	↑	No further improvement in PMOS current

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IBM Yorktown Research,

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ASTA alliance (IBM, AMD, Sony, Toshiba)