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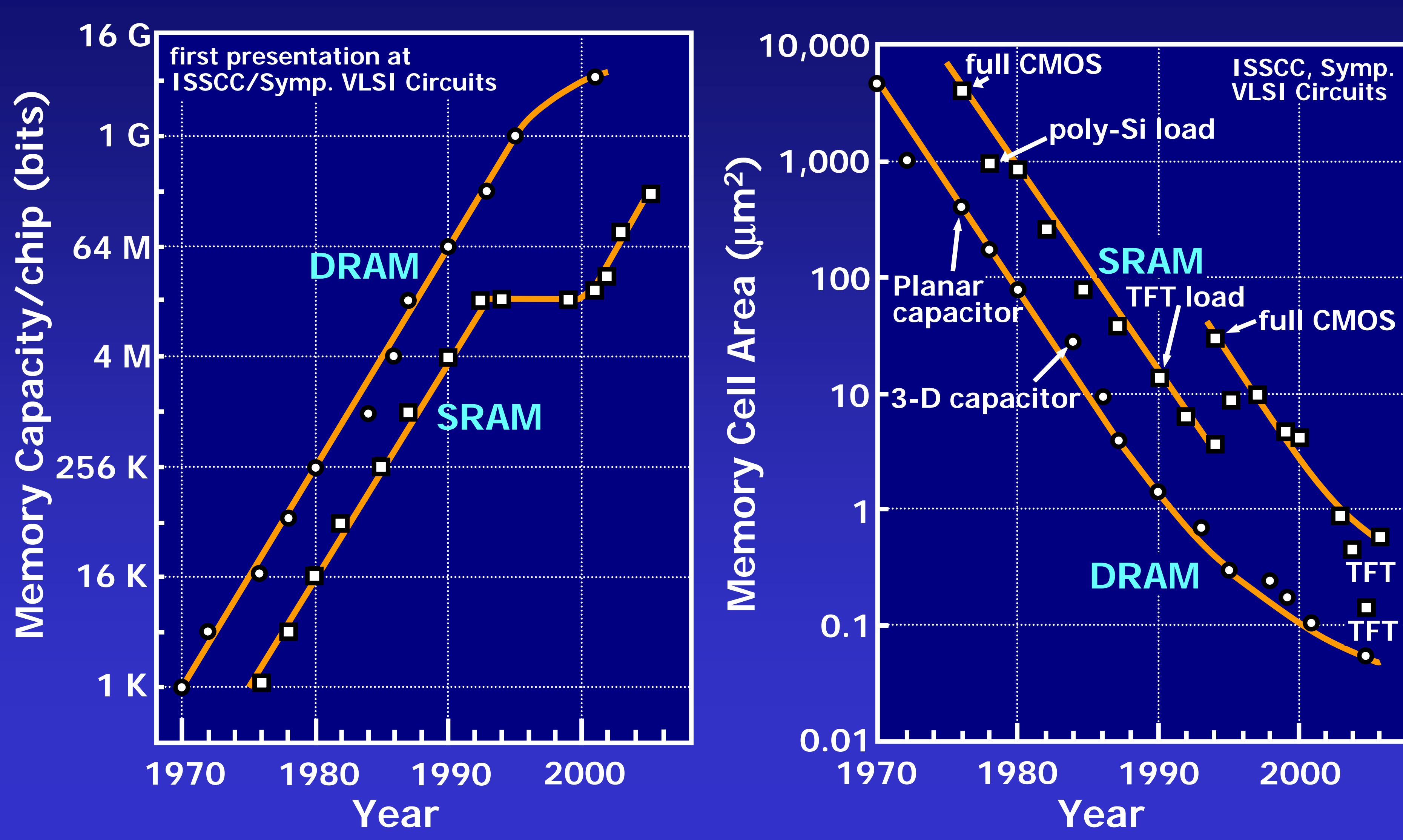
Ultra-Low Voltage Nano-Scale Embedded RAMs

Kiyoo Itoh, Hitachi Ltd.

OUTLINE

1. Introduction
2. Trends & Challenges
3. Low-Voltage Limitation of RAMs
4. Leakage & Speed Variation of Peripheral Logic Circuits
5. Memory Cell Size
6. Future Prospects
7. Conclusion

Trends in RAM Developments (R&D)



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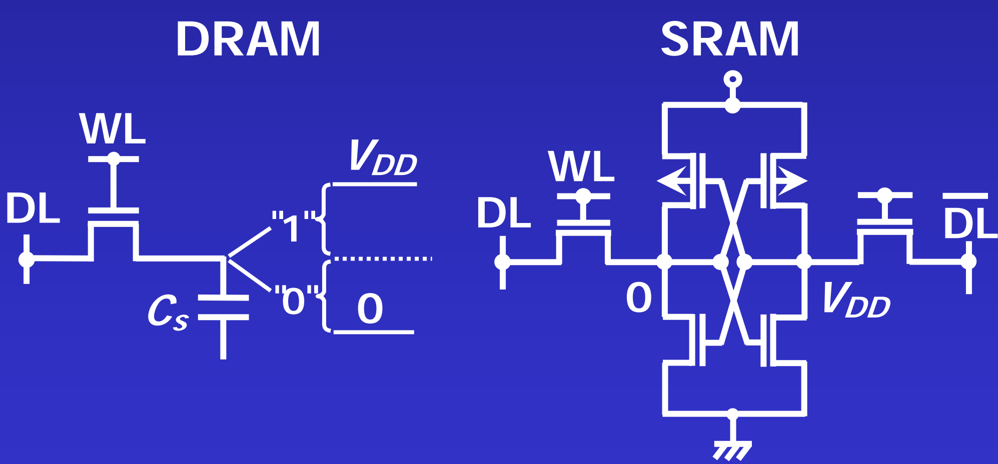
Challenges to LV e-RAMs

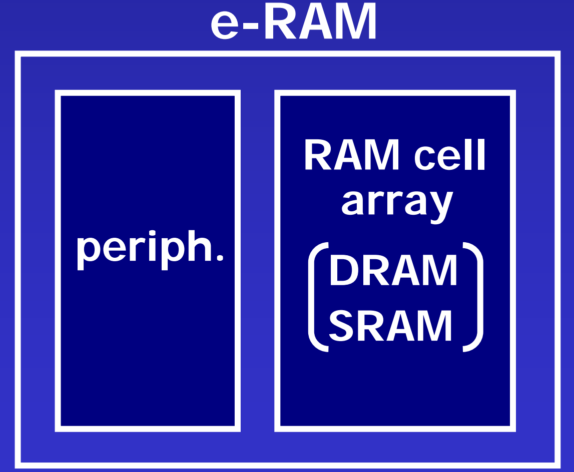
RAM Cells

- Extend low-voltage limitation to sub-1 V
  - -Degraded S/N
  - -Increased leakage
- Reduce cell size

Peripheral Circuits

- Reduce leakage
  - -Increased I_{STB} & I_{ACT}
- Reduce speed variation
  - -Unreliable operations





K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

Low-Voltage Limitation of RAMs

1. It is governed by soft-error of cells, or S/N of cells and cell-relevant circuits.
2. As long as ECC is used, it is governed by S/N.

   ECC: Error Checking and Correcting circuit

3. S/N is determined by
   - Signal charge & signal voltage of cells,
   - Flip-flop circuits that DRAMs use for sense amps, while SRAMs use for cells themselves.

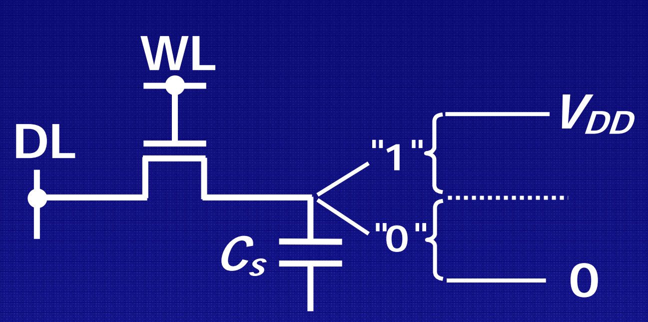
Comparisons of Flip-Flop Circuits

	DRAM SA	SRAM Cell
Circuit	SP $V_{DD}/2$, V_{DD}, DL, $\overline{DL}$, $V_{DD}/2$ $-v_S$, $V_{DD}/2$, M_1, M_2, SN $V_{DD}/2$, STB, ACT, 0	V_{DD}, M_5, DL, $\overline{DL}$, i, M_1, V_{DD}
Standby	**Off** with all nodes at $V_{DD}/2$	**On** with static of all MOSTs
Active	**Dynamic** sensing of v_S (SN on, then SP on)	i by **ratio** of M_1 & M_5 **Static** of other MOSTs
Margin	Sensitive to V_T & ΔV_T of **only two MOSTs, M_1 & M_2**	Sensitive to V_T & ΔV_T of **all MOSTs** → **Narrow margin**

Signal Charge Q_S of RAM Cells

$Q_S \cong$ Soft-Error Q_{crt}. The larger the Q_S, the smaller the SER.
Q_S decreases with device and voltage scaling.

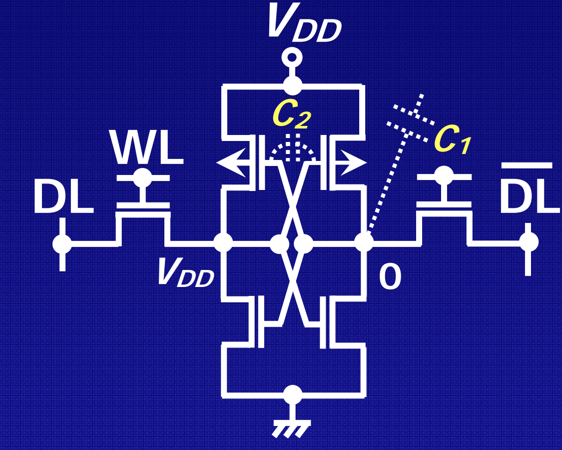
DRAM



$$Q_S = C_S V_{DD}/2$$

C_S; Intentionally added, large, and needs to be gradually decreased with device scaling for maintaining large v_{SIG}.

SRAM



$$Q_S = C_S V_{DD},\ C_S = (C_1 + 2C_2)$$

C_1, C_2; parasitic, small, and rapidly decrease with device scaling.
SER is always larger than for DRAM.

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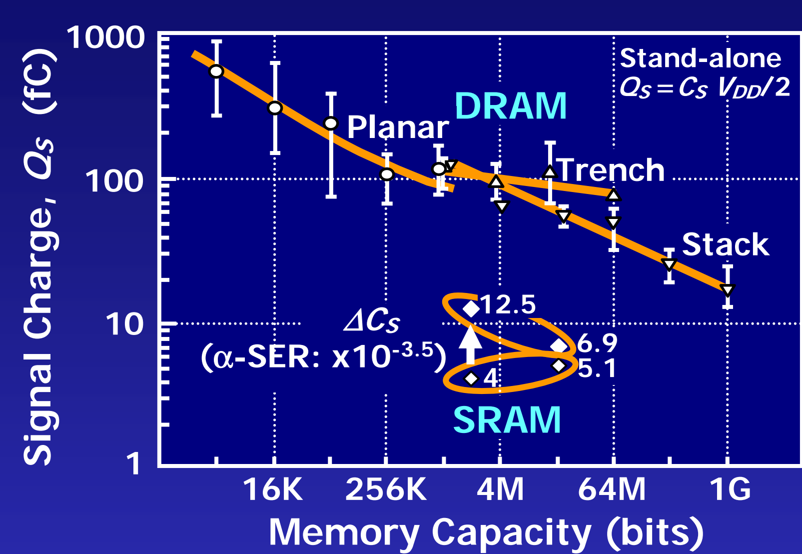
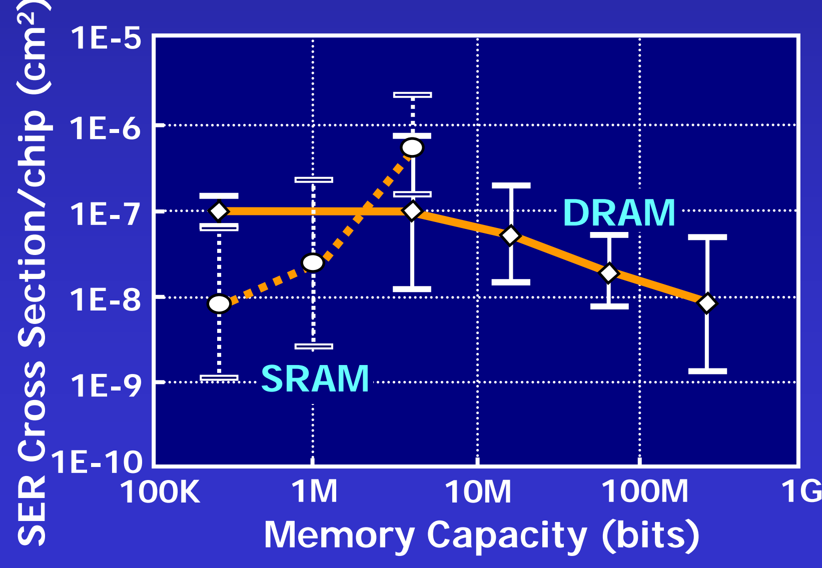
Signal Charge (Q_S) of RAM Cells

- Q_S reduced with capacity due to V_{DD} & device scaling
  Smaller Q_S of SRAM cell
- SER depends on Q_S
  DRAM; *decreases* with memory capacity due to large intentionally-added C_S & spatial scaling that reduces charge collection.
  SRAM; *increases* with memory capacity due to rapidly-decreasing parasitic C_S despite spatial scaling.

Solutions:

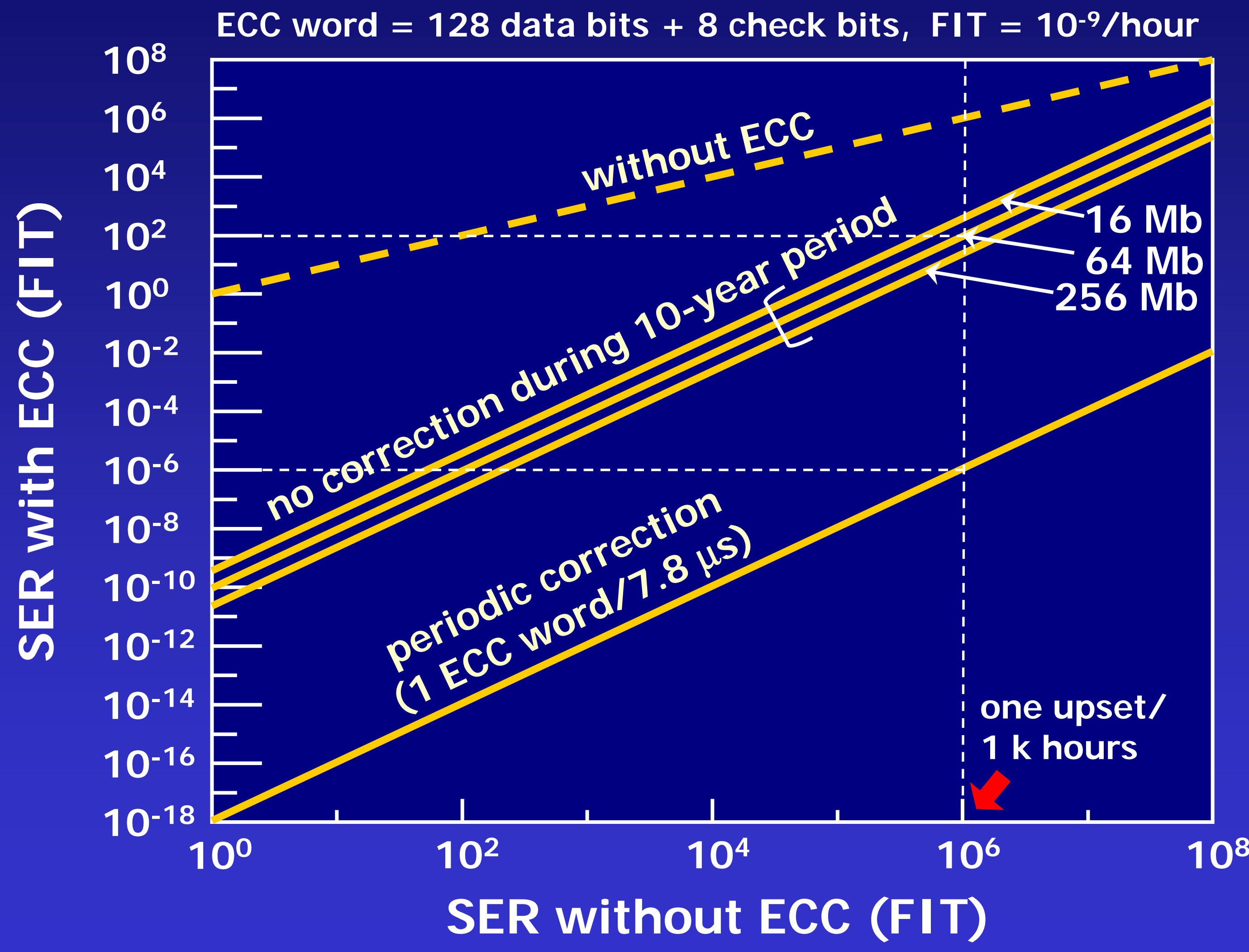
- Increase in C_S (SRAM cells)
- Uses of triple well, redundancy, ECC etc.





Y. Nakagome et al., IBM J. R&D, Vol.47, No.5/6, Sep./Nov. 2003
E. Ibe, The Svedberg Laboratory Workshop on Applied Physics, Uppsala, May 3, 2001

Error Checking & Correcting (ECC)

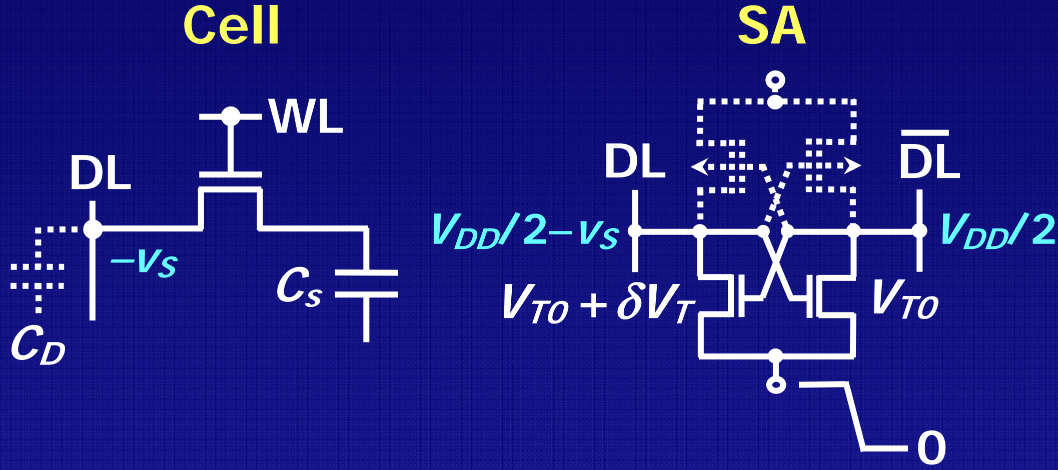


K. Itoh, Hitachi

M. Horiguchi et al., IEEE J. SSC, 23, p. 27, Feb. 1988

Minimum V_{DD} (V_{min}) of RAMs

DRAM



$v_S > \delta V_T,$

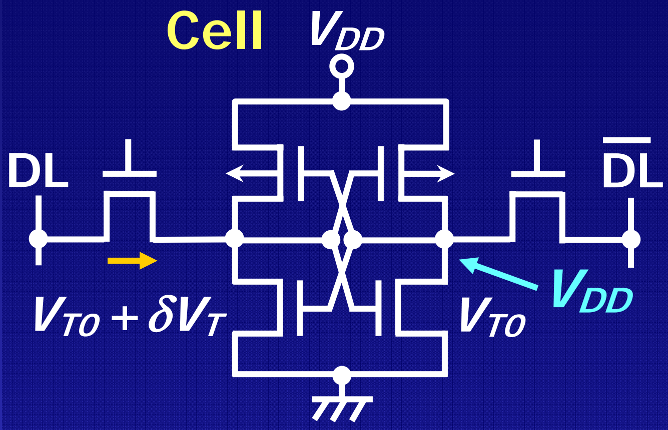
$v_S \cong (V_{DD}/2)\, C_S/C_D$

$\therefore V_{min} = 2\delta V_T\, C_D/C_S = 10\delta V_T \;(C_D/C_S \cong 5)$

$V_G = V_{DD}/2 - (V_{T0} + \delta V_T) > 0$

$\therefore V_{min} = 2\,(V_{T0} + \delta V_T)$

SRAM



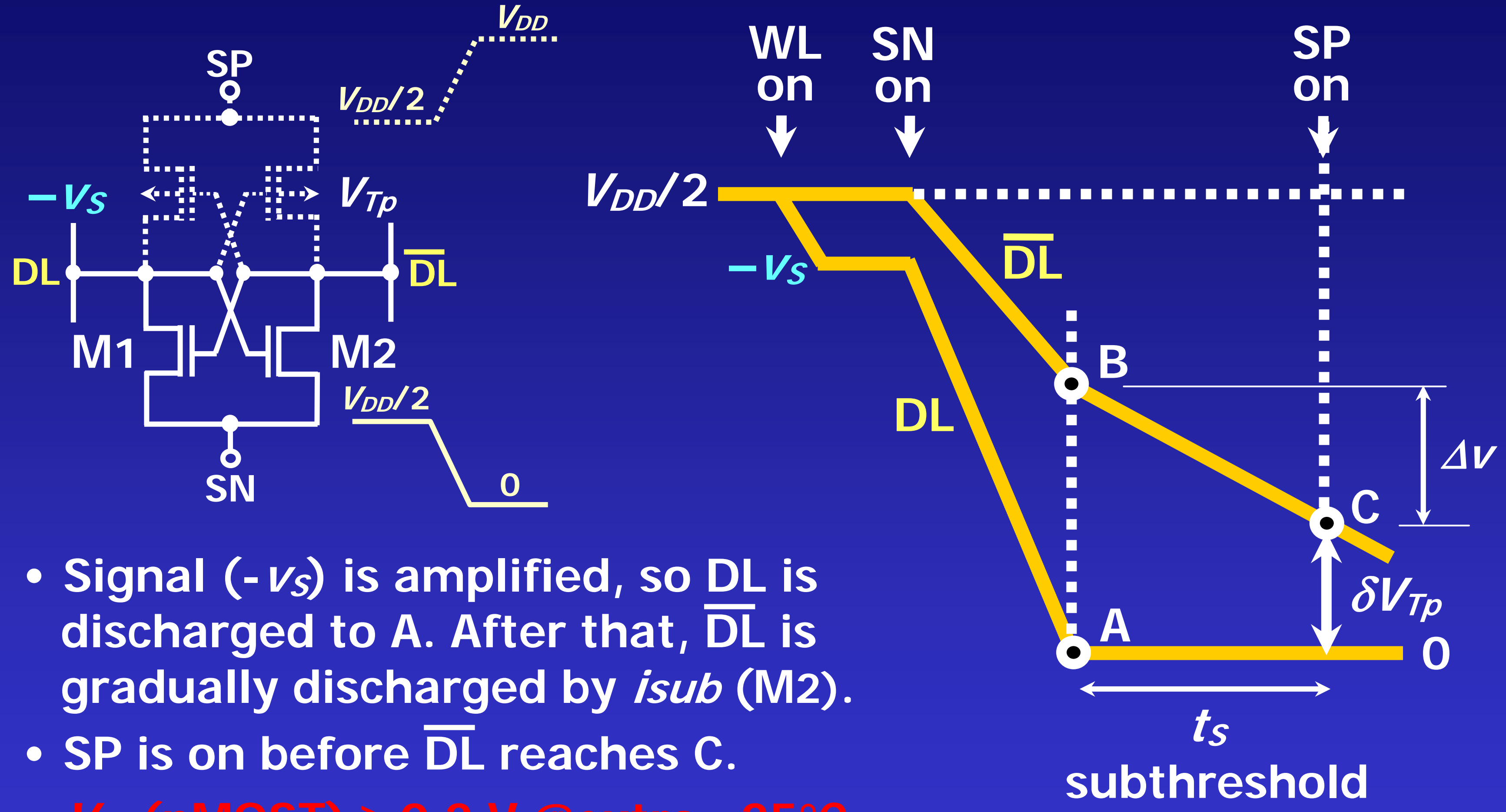
If only cross-coupled nMOSTs determine the voltage margin during read,

$V_G = V_{DD} - V_{T0} - \delta V_T \geq 0,$

$\therefore V_{min} = V_{T0} + \delta V_T$

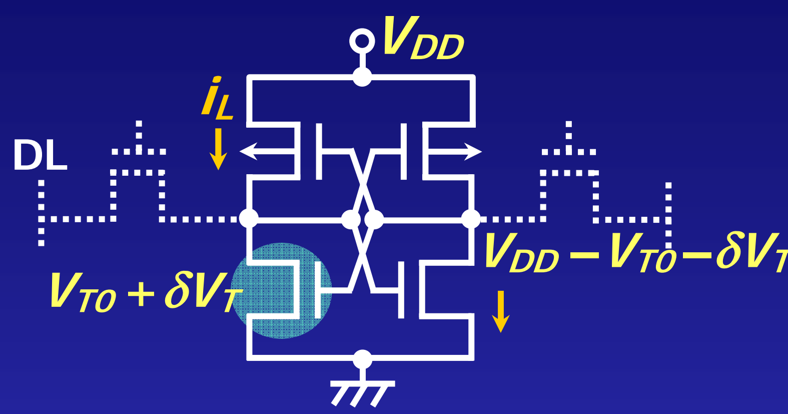
δV_T: V_T-mismatch between paired MOSTs, V_{T0}: Average V_T

Lowest Necessary V_{T0} for SA



- Signal ($-v_S$) is amplified, so DL is discharged to A. After that, $\overline{DL}$ is gradually discharged by *isub* (M2).
- SP is on before $\overline{DL}$ reaches C.
- V_{T0} (nMOST) ≥ 0.2 V @extra., 25°C, if t_S = 5 ns, Δv = 50 mV, C_D = 100 fF @ 120°C

Lowest Necessary V_{TO} for SRAM Cell



- Cross-coupled MOSTs need a high V_T to ensure a small retention current through reducing i_L.
- V_{TO} is the average in a chip, because it is the average that determines retention current of the chip.
- V_{TO} must be quite high and unscalable.

Extrapolated $V_T = V_T$ (nA/µm) + 0.3 V
T_j = 125 °C
100 °C
75 °C
50 °C
25 °C
L_g = 0.1 µm
W (Q_T) = 0.20 µm
W (Q_D) = 0.28 µm
W (Q_L) = 0.18 µm
high speed (0.49)
low power (0.71)
10 µA
0.1 µA
1-Mb array retention current (A)
10^0
10^{-2}
10^{-4}
10^{-6}
10^{-8}
-0.2 0 0.2 0.4 0.6 0.8 1.0
Extrapolated V_{TO} (V) at 25 ºC

K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

V_T-Mismatch (δV_T)

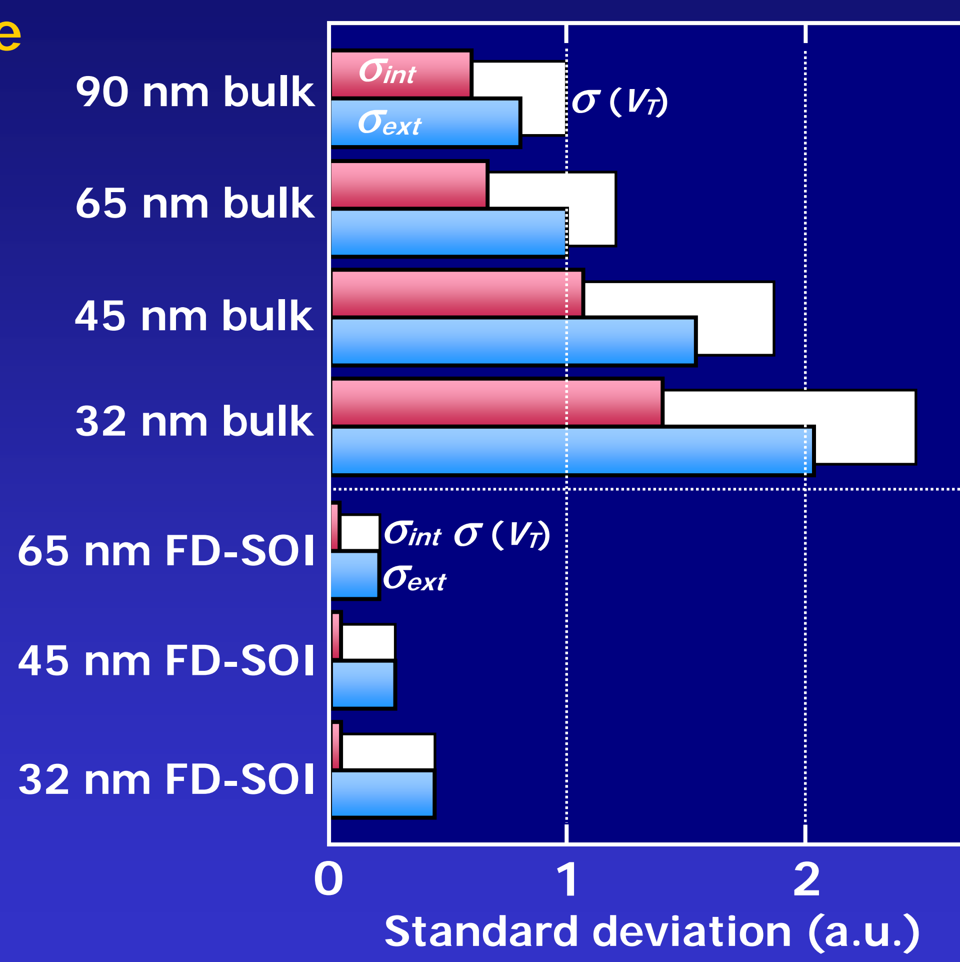
1. V_T Variation (ΔV_T) as source of δV_T
   - Extrinsic ΔV_T due to implant non-uniformities & $\Delta (L, W)$
   - Intrinsic ΔV_T due to random microscopic fluctuations of dopant atoms in the channel area.
2. ΔV_T & δV_T increase with reducing MOST size even for a fixed generation.

$$\sigma_{int} \propto 1/\sqrt{LW}$$

$$\sigma(\delta V_T) \cong \sqrt{2}\ \sigma_{int}$$

3. ΔV_T & δV_T increase with device scaling.

ΔV_T in a chip has no room in time & area to be compensated for.



M. Yamaoka et al., Symp. VLSI Circuits 2004

Larger δV_T of SRAM cell

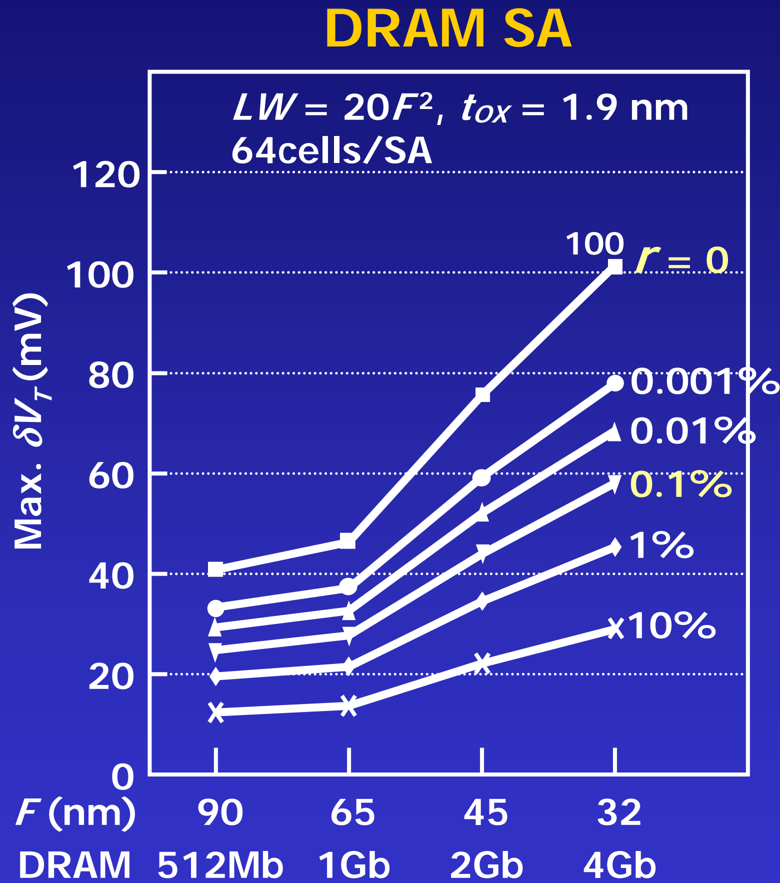
	DRAM SA	SRAM Cell
Circuit	DL, $\overline{DL}$	DL, $\overline{DL}$
MOS Size	10 – 20 F^2	1.8 – 2.8 F^2
Circuit Count in a chip	M/(64 -1024) 64-1024 Relaxed SA layout	M Array M
δV_T	Small	Large

M : memory capacity

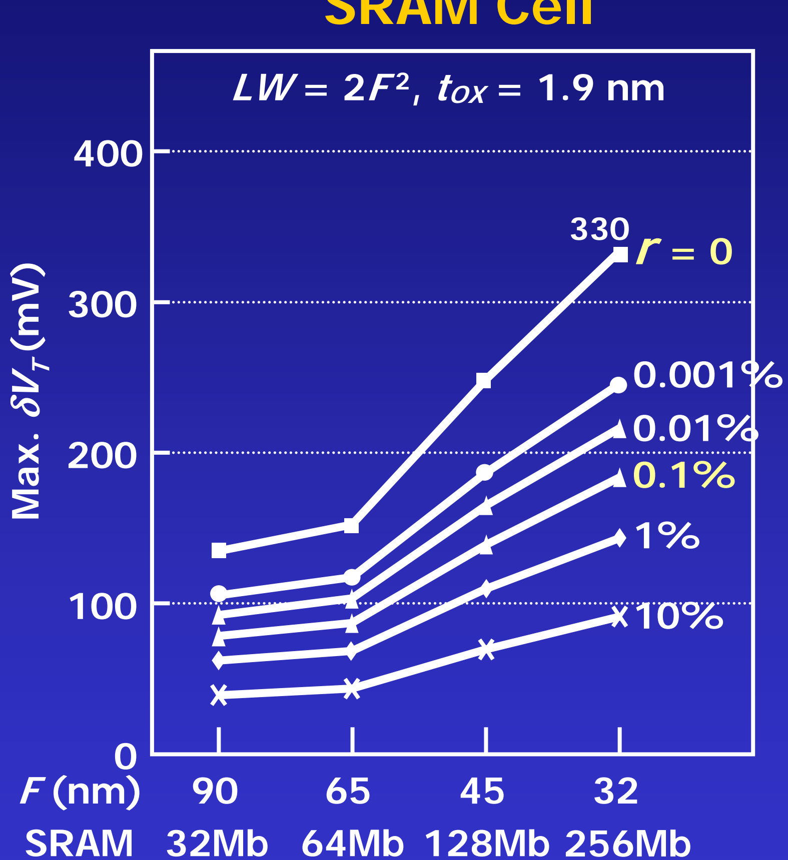
Maximum δV_T in a chip

r : repairable percentage

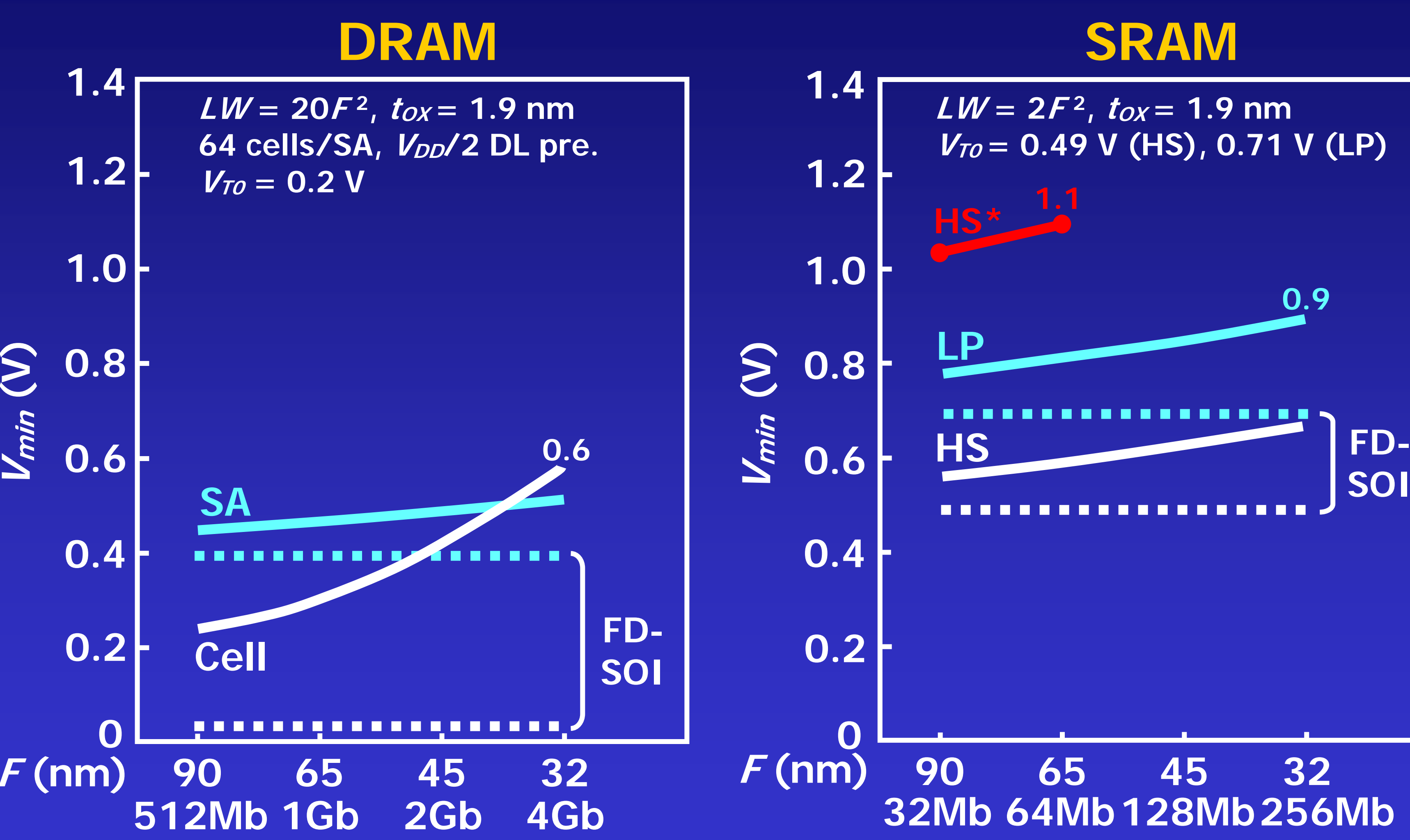
DRAM SA



SRAM Cell



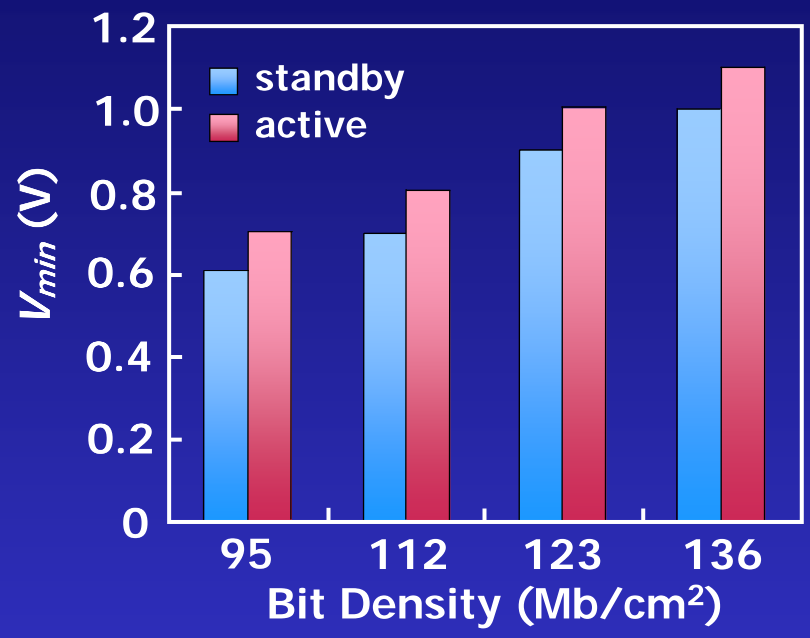
V_{min} (r = 0.1 %)



*Actual V_{min} determined by all MOSTs in a cell.

Approaches to LV SRAMs

1. Use ECC & Redundancy.
2. Minimize ΔV_T & δV_T.
   - Large cells with large MOSTs despite losing bit density
   - Symmetric cell layout
3. Stay at a high V_{DD} (≥1 V) due to its still large ΔV_T & δV_T of bulk CMOS. Even so, power-supply control cells needed for small subthreshold current.
4. Extend low-V_{DD} limitation to sub-1-V with FD-SOI.



M. Khellah, et al., ISSCC Dig., pp. 624-625, 2006

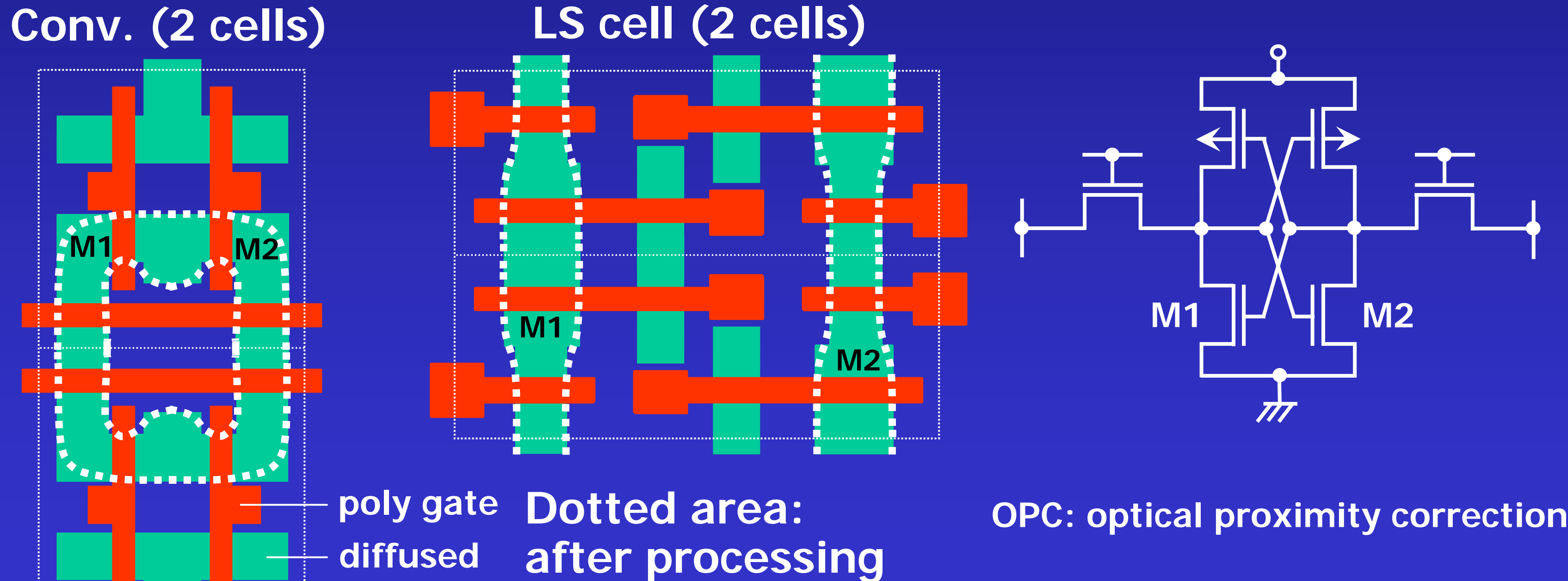
Symmetric Layout for Small δV_T

Sources of extrinsic δV_T in the conventional cell:

- Pattern deformation after processing
- Mask misalignment
- Local size fluctuation

Solution: Lithographical symmetric cell ("Thin" Cell)

- Reduced δV_T by simple patterns suitable for OPC
- DLs shielded by power lines

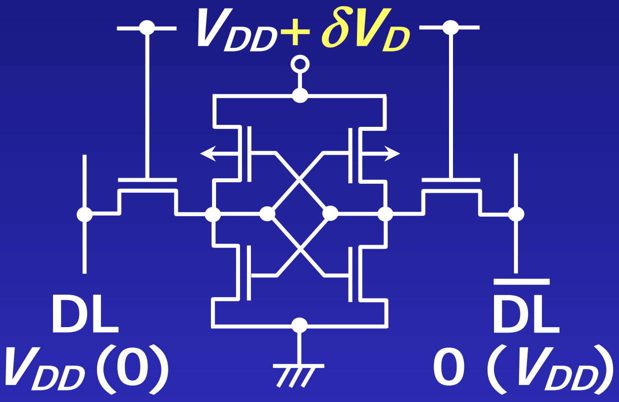


K. Osada et al., IEEE J. SSC, vol. 36, No. 11, pp. 1738-1744, Nov. 2001.
M. Kanda et al., Symp. VLSI Tech. Dig. Tech. Papers, pp. 13-14, June 2003.
F. Arnaud et al., Symp. VLSI Tech. Dig. Tech. Papers, pp. 65-66, June 2003.

Power-Supply Control Cells

for small subthreshold currents

Boosted Power Supply

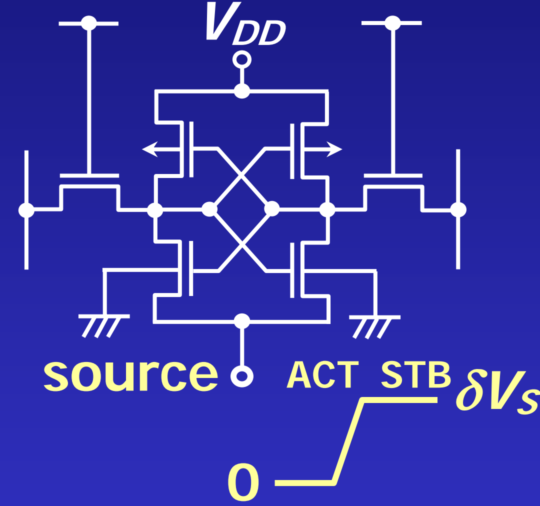


- High V_T to reduce i_L
- δV_D to offset a high V_T & δV_T

Low leak, wide margin & low power with low-V_{DD} DL.

Unscalable MOSTs needed.

Source-Line Driving

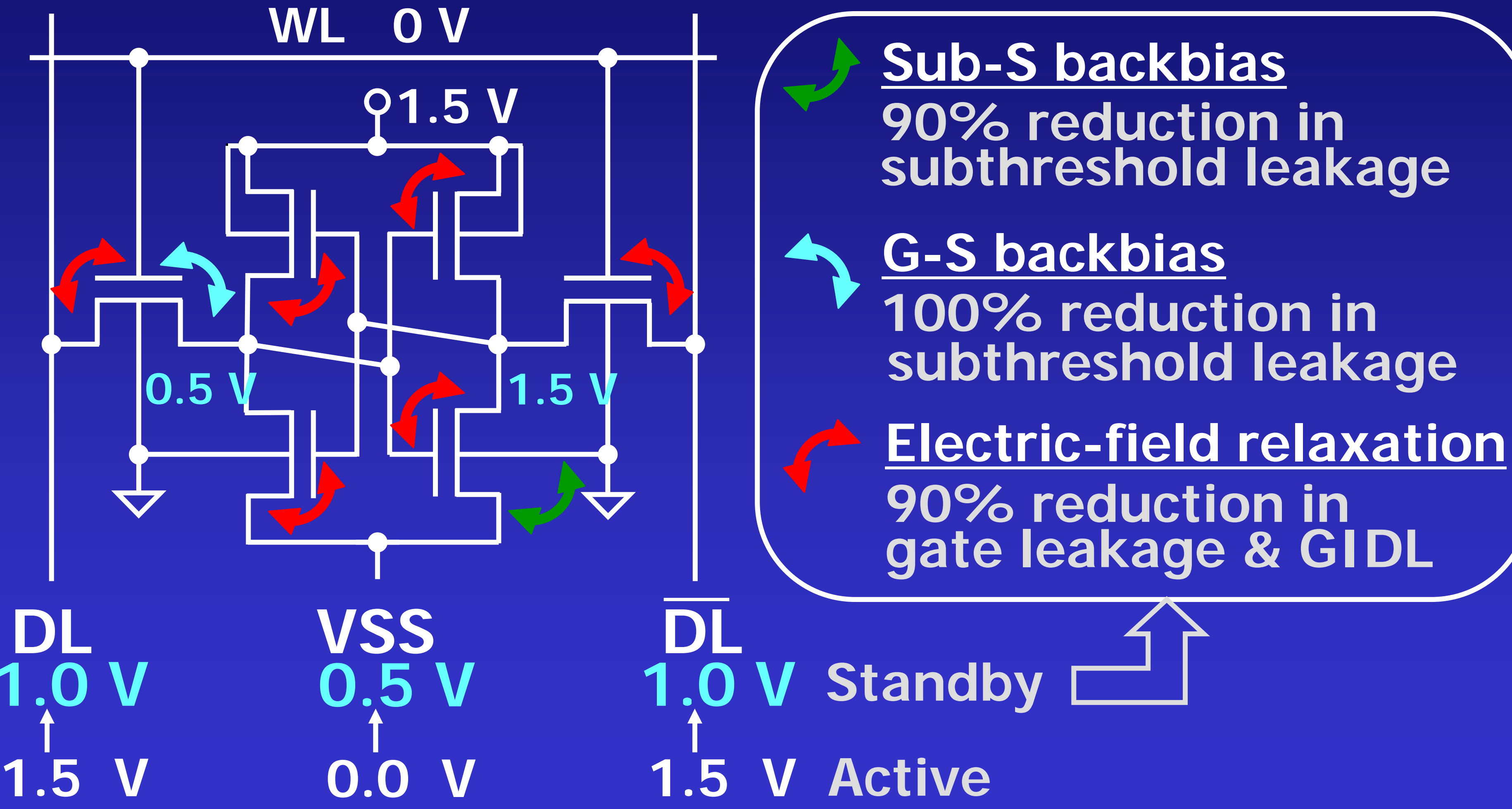


- Raised source during STB to reduce i_L with increased V_T of off-MOST

Reduced margin during STB by δV_S (>0.3 V)

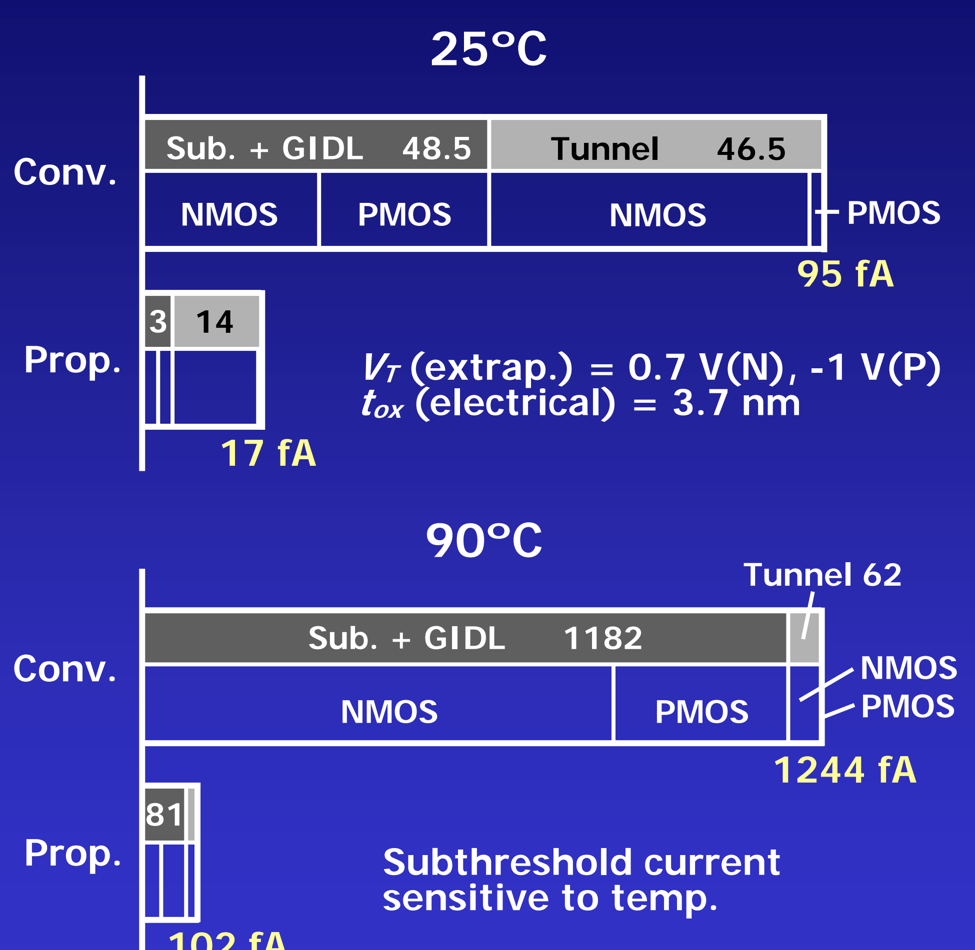
Source-Line Driving

Along with reduced DL voltage at active-standby transition



K. Osada et al. ISSCC2003 Dig. pp. 302-303

Measured Retention Current of Cell



- **Successful Application**

  1.5-V 27-ns 6.42 x 8.76 mm² 16-Mb using ECC with 3.2-ns/9.7% speed /area penalties.

- **Limitations and Challenges**

  (1) Leakage still large

  1.6 µA for 16 Mb despite high V_T, thick t_{ox}, and S-driving.

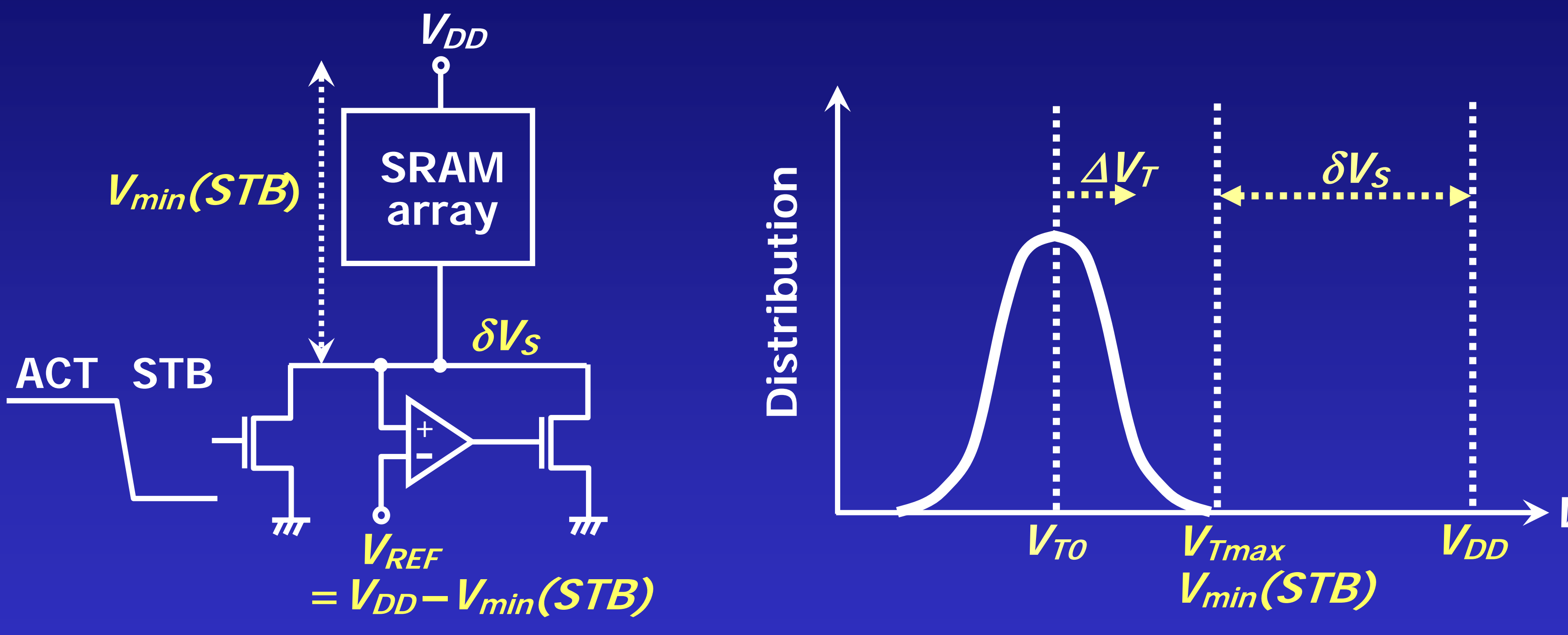
  (2) Reduced Q_S in standby mode

  The cell power-supply decreases by the raised source voltage. Further low-V_{DD} operation may be hazardous, even if ECC is used.

K. Osada et al. ISSCC2003 Dig. pp. 302-303

Source-Line Driving

to reduce leakage & its variation while retaining the data



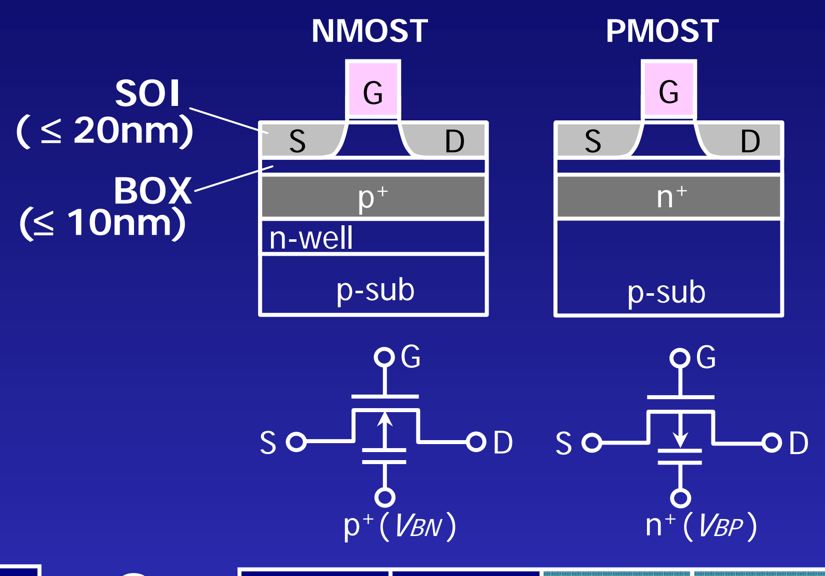
$V_{min}(STB)$: Min. V_{DD} to retain the data of all cells in the array.

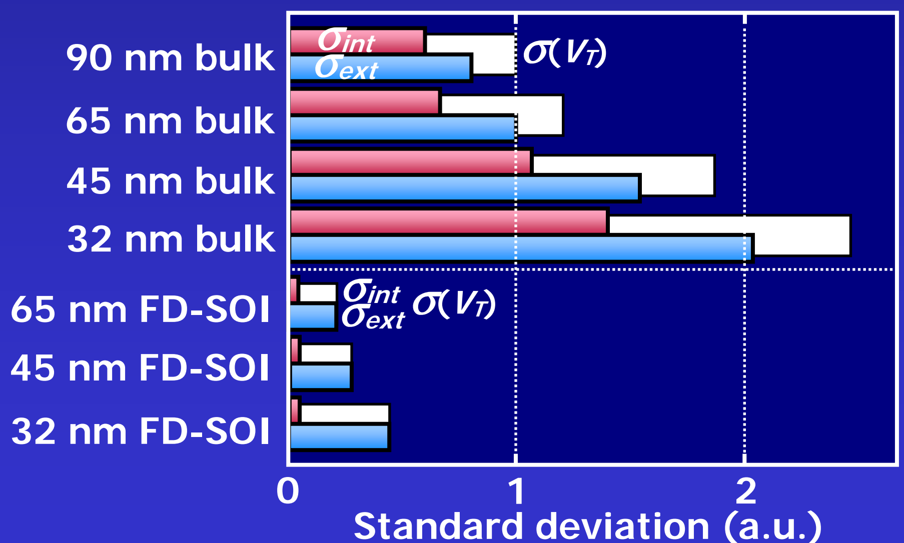
Lower $V_{T0} \rightarrow$ Larger δV_S $\rightarrow$ Higher V_{T0} with deeper body bias (ΔV_T) $\rightarrow$ Lower i_L

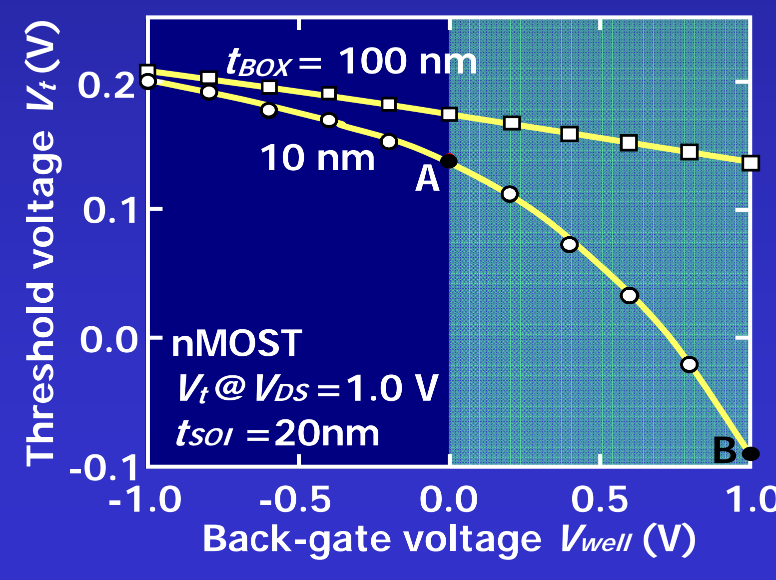
M. Khellah, et al.,ISSCC Dig. pp. 624-625, 2006

Double-Gate FD-SOI

- **Small ΔV_T & negligible δV_T** (ultra-thin & lightly-doped channel)
- **Adjustable $V_T \rightarrow$ multi-V_T**
- **Large V_T change** (wide-range well-bias control)
- **Reduced SER & small i_{pn}**
- **Dynamic V_T MOST** (e.g., G-well connection)



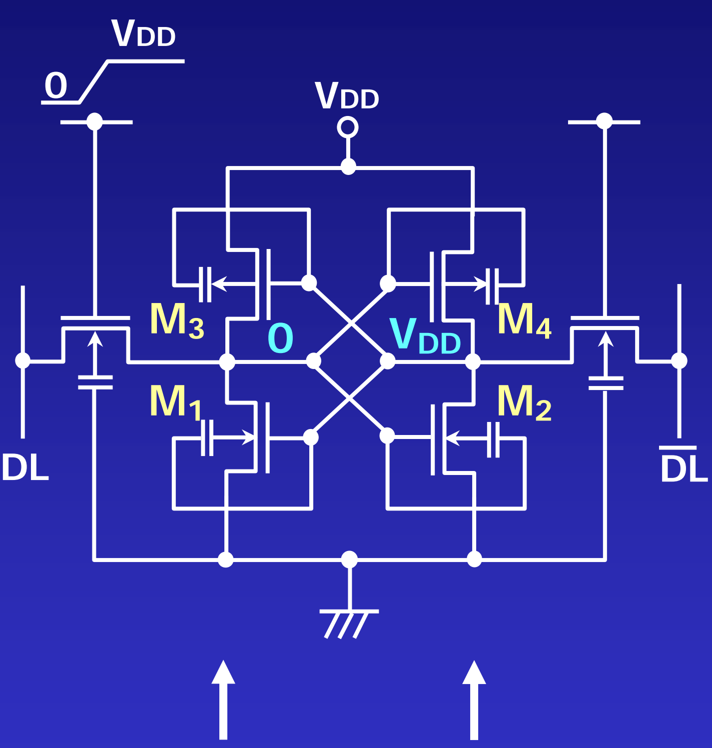


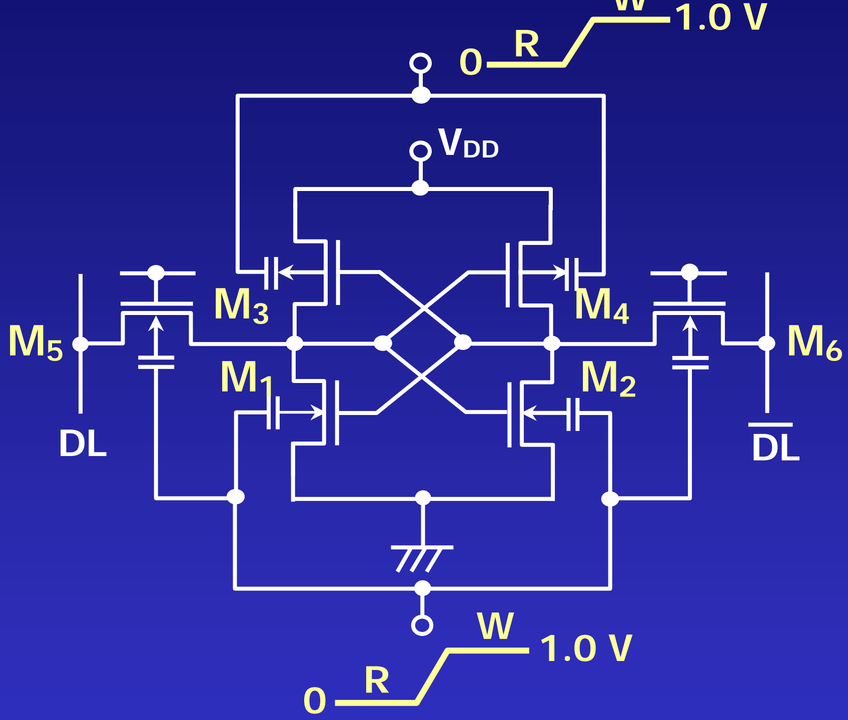


M. Yamaoka et al., Symp. VLSI Circuits 2004, R. Tsuchiya et al., IEDM2004 Dig. pp. 631-634

SRAM Cells with Dynamic-V_T MOSTs

to widen the voltage margin





M_1: decreased V_T M_2: increased V_T
M_3: increased V_T M_4: decreased V_T

Write margin improved with decreased V_T for driver/transfer MOSTs & increased V_T for load MOSTs.

M. Yamaoka et al., SOI Conf. Dig. pp. 109-111, Oct. 2004

M. Yamaoka et al., A-SSCC Dig. pp. 109-112, Nov. 2005

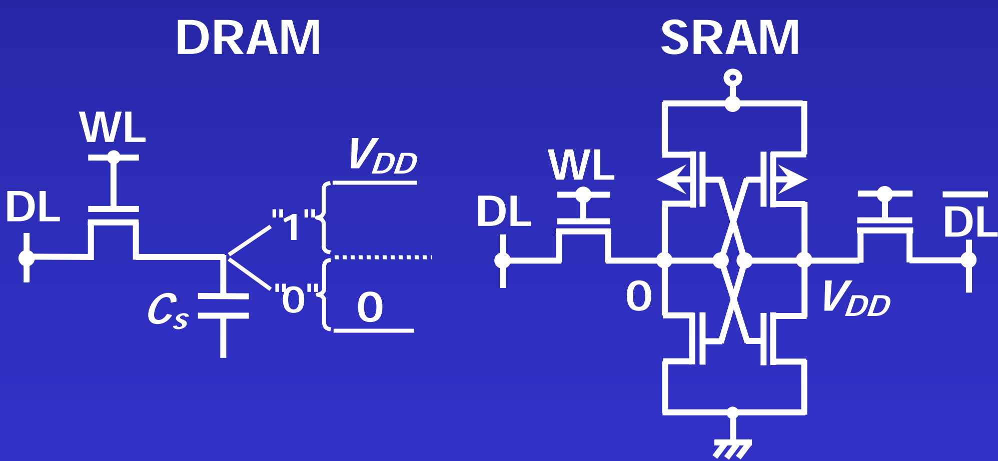
Challenges to LV e-RAMs

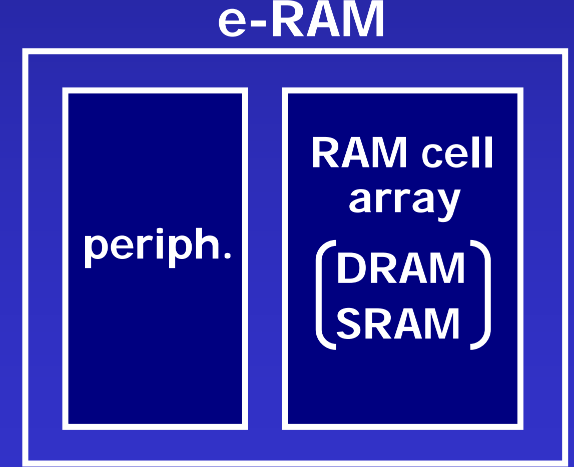
RAM Cells

- Extend low-voltage limitation to sub-1 V
  - -Degraded S/N
  - -Increased leakage
- Reduce cell size

Peripheral Circuits

- Reduce leakage
  - -Increased I_{STB} & I_{ACT}
- Reduce speed variation
  - -Unreliable operations





K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

Leakage Currents of Periphery

■ Gate tunneling current (i_G)

- Insensitive to V_G & temp.
- Sensitive to t_{ox}

1/10 i_G-reduction with t_{ox}-increment of only 2-3 Å for S_iO_2, while the same reduction with V_G-decrement of as much as 0.5 V. Such a large V_G control in low-V_{DD} region is risky.

→ Device designers are responsible for the reduction. (High-k)

■ Subthreshold current (i_L)

- Insensitive to device structures
- Sensitive to V_G, V_T & temp that can be controlled by circuits.

1/10 i_L-reduction with V_T-increment, or V_G-decrement of only 100 mV.

→ Circuit designers are responsible for the reduction.

$$i_L \propto W\,10^{(V_G - V_T)/S}$$

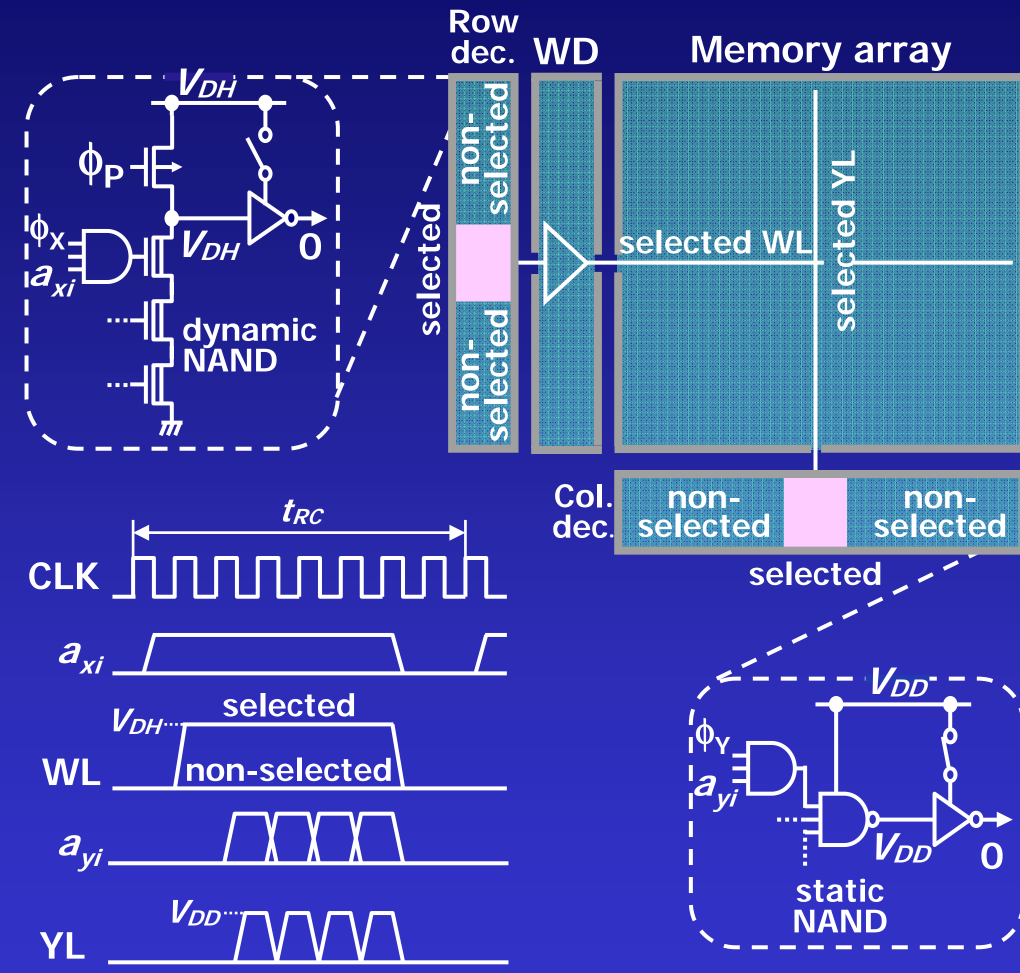
S ~ 100mV/dec.@100°C

1/10 with ΔV_T = 100mV
or ΔV_G = -100mV

Subthreshold Current (i_L) of Periphery

Features of RAM Periphery

1. **Input-Predictable Logic**
   Designers can prepare the schemes in advance.
2. **Slow Cycle (t_{RC} = 25, 60 ns)**
   Each circuit is active for only a short period within "long" cycle, enabling additional time for i_L-control.
3. **Iterative-Circuit Blocks**
   Major i_L sources.
   All circuits in each block are inactive, except selected one.
4. **Robust Circuits**
   i_L-immune NAND dec.
   (w/o i_L-sensitive NOR dec.)
5. **On-Chip Power Supplies**
   V_{DH} & V_{BB} utilized for dual-static V_T.

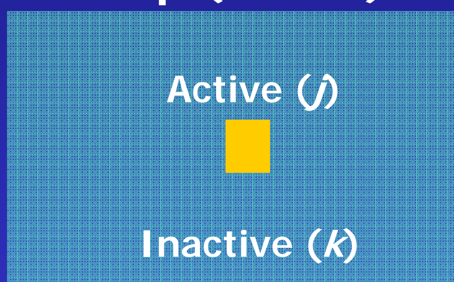


K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001
Y. Nakagome et al., IBM J. R&D, Vol.47, No.5/6, Sep./Nov. 2003

i_L-Increase in Periphery

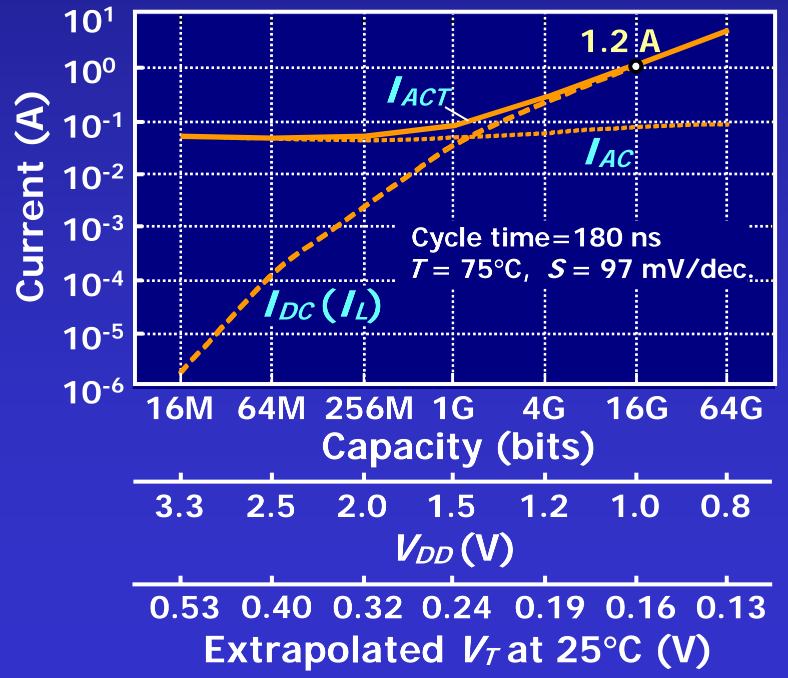
- At present, V_T is still so high that i_L is small in active mode, though i_L dominates in standby mode.
- In the future, with further reducing V_T, i_L will dominate even in active mode. Leakage reduction for active mode is the key.

chip (active)



$$I_{ACT} = I_{AC} + I_{DC}$$
$$I_{AC} = \Sigma C_j V_{DD} f$$
$$I_{DC} = \Sigma i_{Lk} \propto \Sigma W_k 10^{-V_T/S}$$
$$V_T = aV_{DD}$$
$$k >> j$$

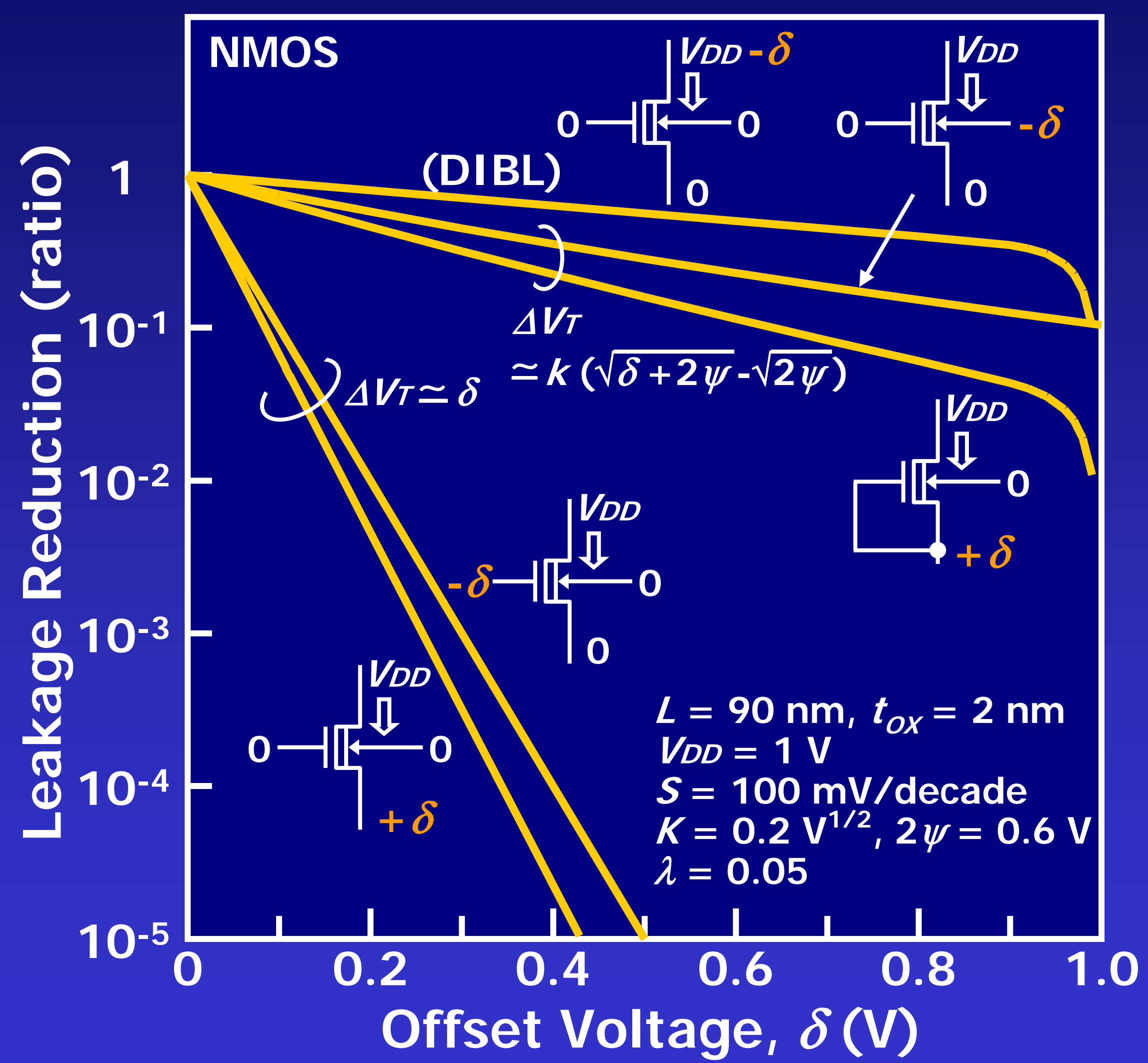
Trends in DRAM Peripheral Current



 K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

Basic Concept of i_L-Reduction

- Use high-V_T MOST achieved statically or dynamically with $V_{Th} = V_{Tl} + \Delta V_T$
- For static high-V_T ΔV_T by ion impla. or static-V_{BB} application.
- For dynamic high-V_T ΔV_T by dynamic back-biasing schemes
  G-S back-bias is best due to large $\Delta i_L / \Delta\delta$, applicable even to active mode.



Y. Nakagome et al., IBM J. R&D, Vol.47, No.5/6, Sep./Nov. 2003

Three Practical Reduction Circuits

Applicable even to Active Mode

Circuit	Examples
Switched-**S**ource **I**mp. (G-S Self-Backbiasing)	V_{DD}, IN (0), OUT (V_{DD}), δ, SSI / V_{DD}, SSI, V_{DD} - δ, IN (V_{DD}), OUT (0)
Power Switch utilizing internal power supply (G-S Offset Driving)	V_{DD}, low-V_T core, V_{DD}, $-V_{BB}$, low V_T / V_{DH} (>V_{DD}), V_{DD}, 0, low V_T, low-V_T core
Dual-Static V_T utilizing internal power supply	$-V_{BB}$ / V_{DD}, V_{DD}, V_{DH} (>V_{DD})

SSI (G-S Self-Backbias)

for fast i_L-control of input predictable logic

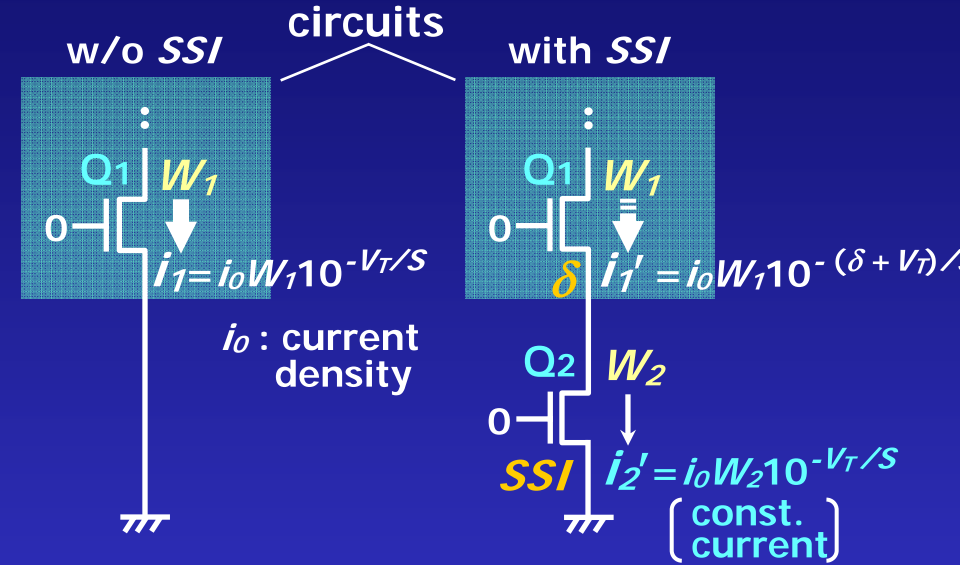
No matter how large i_1 is, it is confined to const. current i_2' with self-adjusting δ.

Stacking effects (δ = 0.2 V)

- G-S backbias of Q1 (1/100)
- Sub-S backbias of Q1 (1/1.5)
- DIBL effect of Q2 (1/2)

Applicable even to active mode

- Fast i_L-control capability with small δ & C_L and self-reduction
- Small area penalty if applied to iterative circuit blocks
- Capability of confining to min. active circuitry



$i_1' = i_2'$

$\therefore \delta = (S/\ln 10) \ln(W_1/W_2)$

Reduction Ratio $\gamma = i_1'/i_1 = 10^{-\delta/S} = W_2/W_1$

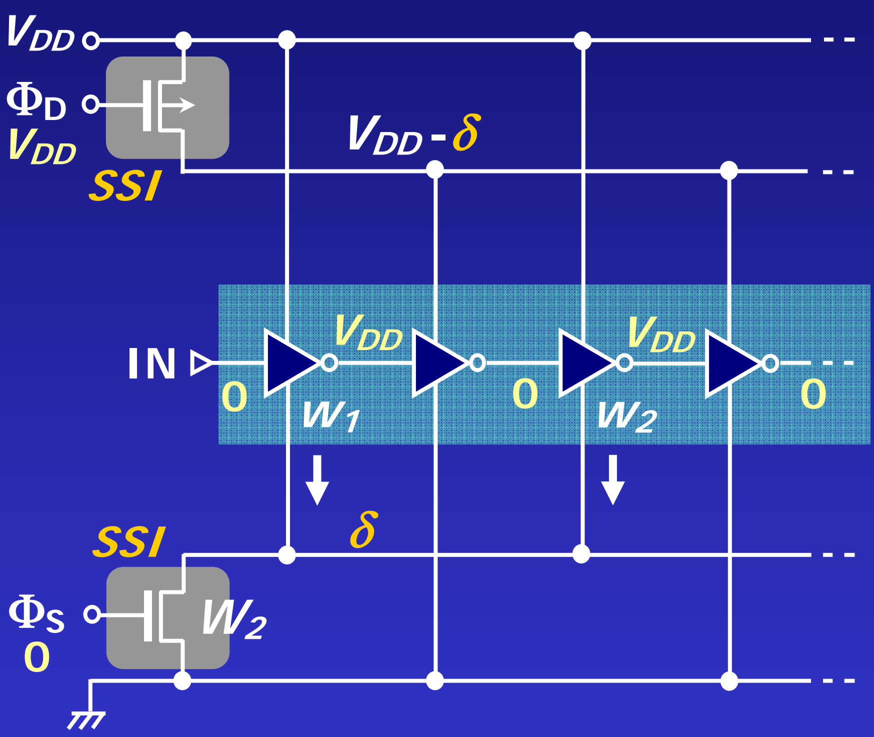
- Smaller i_L ($= i_2'$) & larger δ with smaller W_2
- γ = 1 (no reduction) for $W_2 = W_1$

Other secondary effects reduce i_L. (Sub-S backbias & DIBL)

 M. Horiguchi *et al.*, Symp. VLSI Circuits Dig., p. 47, 1993.

Small Area Penalty with *SSI* Sharing

Inverter Chain



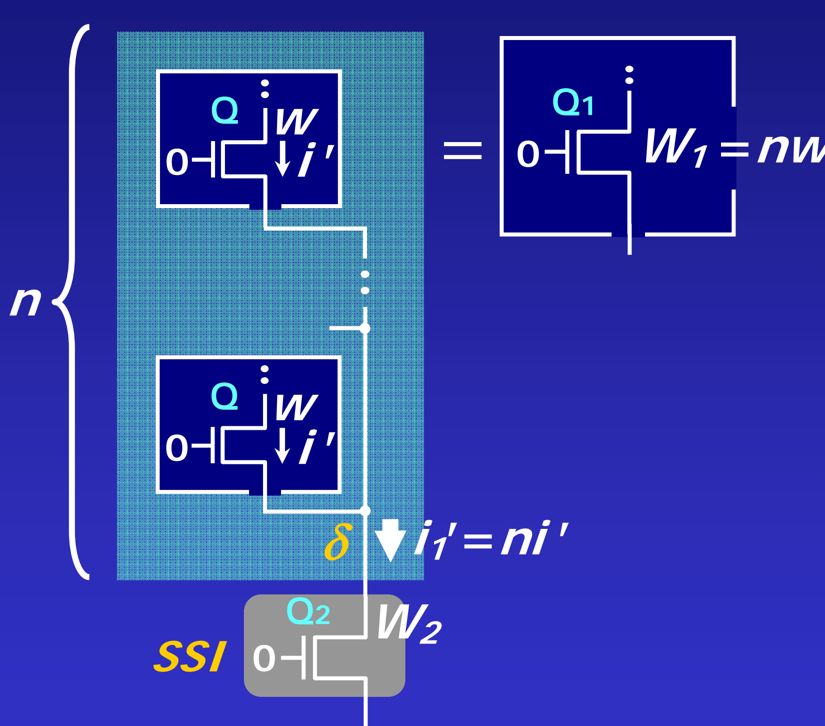
- For 0-V input, i_L flows from an n-MOST in each 0-V input inverter, and accumulates into *SSI*.
- *SSI* confines to its constant current ($= i_0 W_2 10^{-V_T/S}$).
- $W_2 \cong w_1 \cong \ldots \cong w_n$ without speed penalty because each inverter switches at different timing.
- Area penalty is negligible with increasing the number of inverters because $W_2 \ll \Sigma w_i$.

  Such is the case for p-MOST *SSI*.

M. Horiguchi *et al.*, IEEE J. Solid-State Circuits, vol. 28, no. 11, pp. 1131-1135, Nov. 1993.

Small Area Penalty with *SSI* Sharing

Iterative Circuit Block (non-selected/standby)

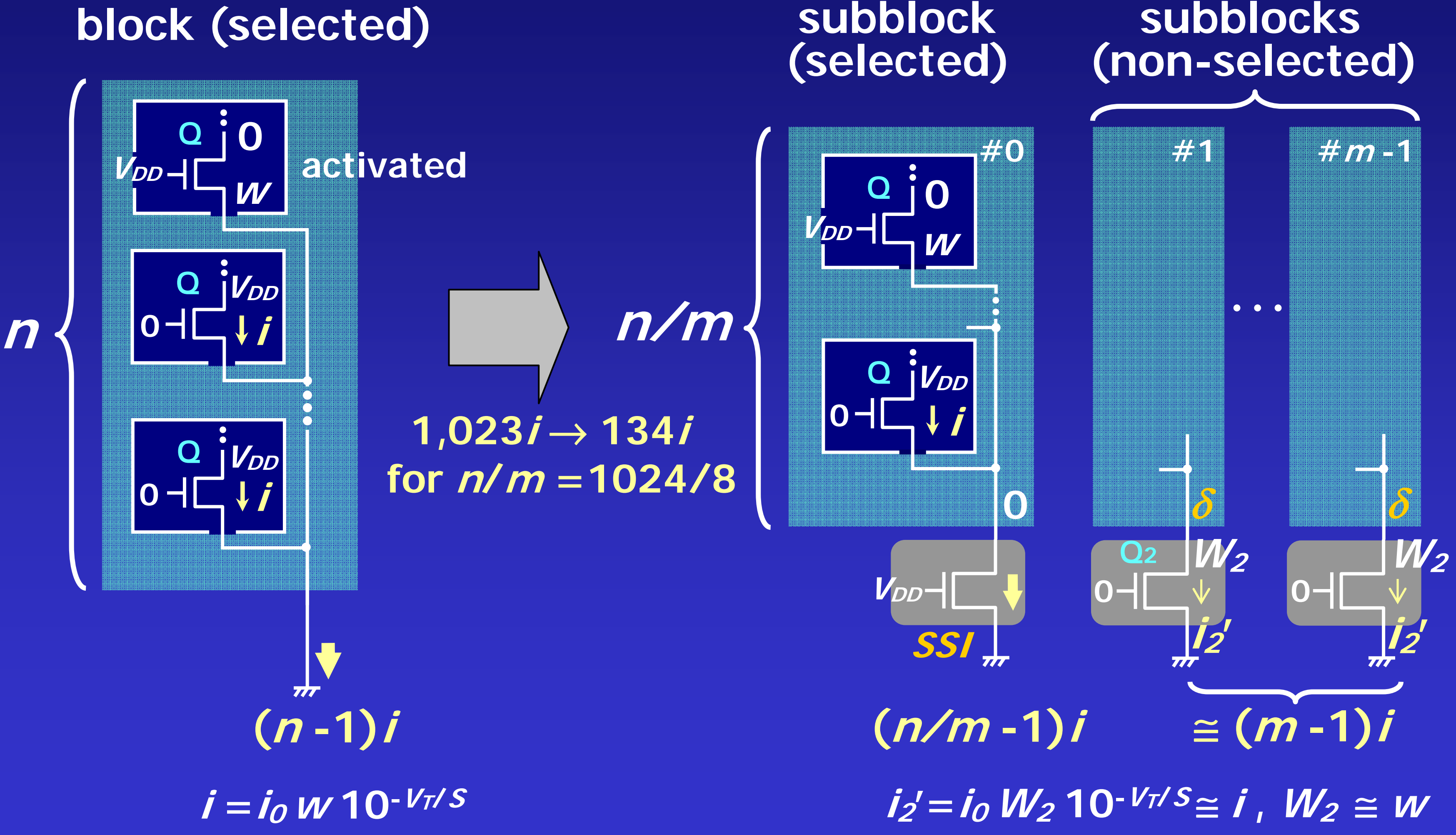


- During non-selected periods i_L (= i') flows from each circuit, and accumulates into *SSI*.
- *SSI* confines to its constant current (= $i_0 W_2 10^{-V_T/S}$).
- $W_2 \cong w$ without speed penalty because only one MOST is activated with *SSI* on.
- Area penalty is negligible with $n \gg 1$ because $W_2 \ll nw$.

M. Horiguchi *et al.*, IEEE J. Solid-State Circuits, vol. 28, no. 11, pp. 1131-1135, Nov. 1993.

Confining to Minimum Active Circuitry

Partial activation of multi-divided block



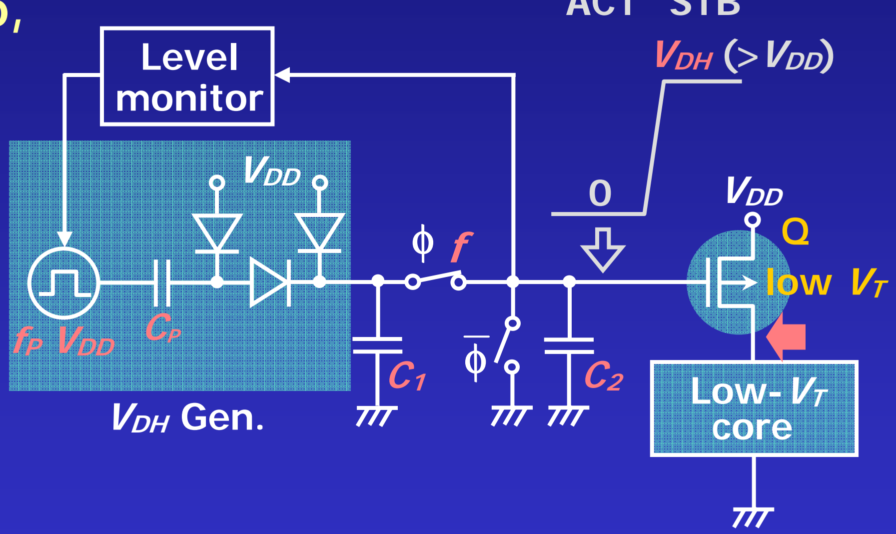
 K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

Power Switch (G-S Offset Drive)

Low-V_T switch (Q) shuts off the supply of low-V_T core during standby. A raised V_{DH} needed to cut off Q with G-S backbias.

Problems:

1. If V_{DH} generated by charge pump,
   - Unregulated floating V_{DH}
     For well-regulated V_{DH}, $C_2 V_{DH} f < C_P V_{DD} f_P$, $C_1 \gg C_P$, $C_1 \gg C_2$, level monitor.
   - Increased pump power
     For low pump power with keeping the V_{DH} level, $C_P V_{DD} f_P$ & $C_2 V_{DH} f$ reduced.
     -> Smaller C_2 & slower f



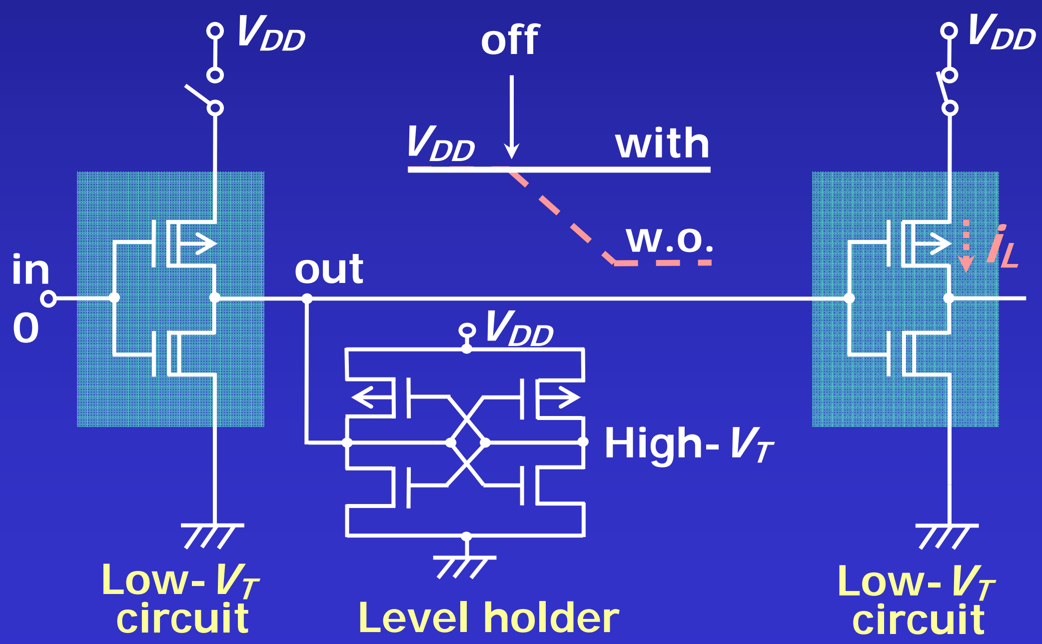
2. Area penalty by large Q
3. Slow recovery of internal power node (⇐)

K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

Power Switch with Level Holder

Applicable even to active mode, if the switch itself operates fast enough.
After evaluating the input, the output level continues to be held by high-V_T holder without leakage. Otherwise

- Floating output discharges, causing a large i_L at pMOST in the succeeding circuit, in which the switch is still on.
- Unnecessary discharging prevents the output from quick recovery.



 K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

Dual Static V_T

Useful for active & standby modes

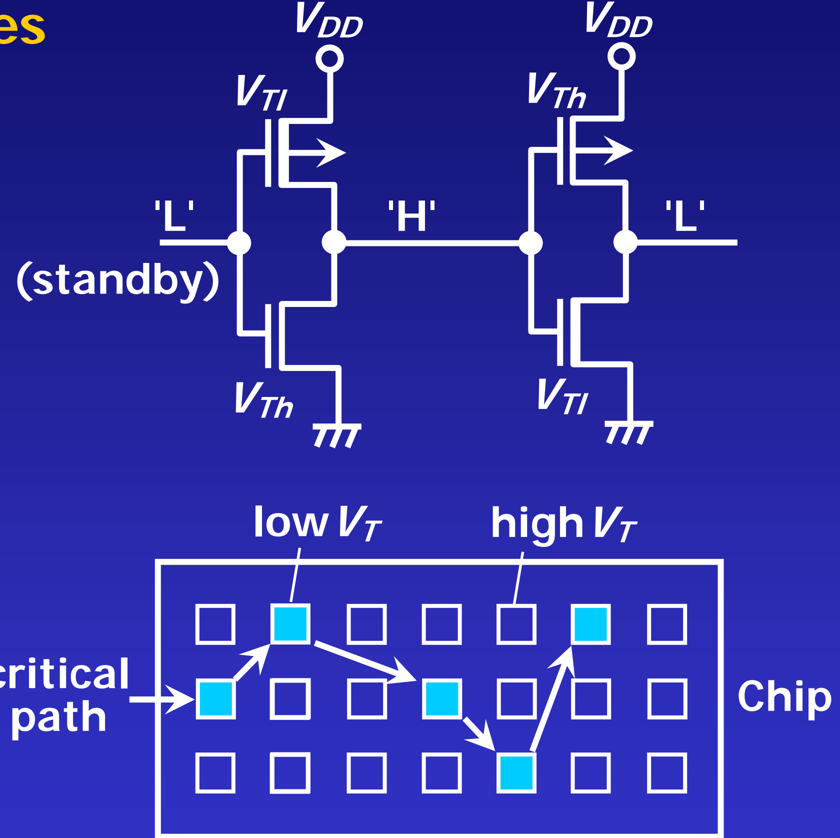
Selective use of a high V_T to

- Off-MOSTs during standby
- Non-critical path, while using low V_T to critical path.

-> Low i_L & high speed chip

The reduction is not remarkable because V_T difference must be small.

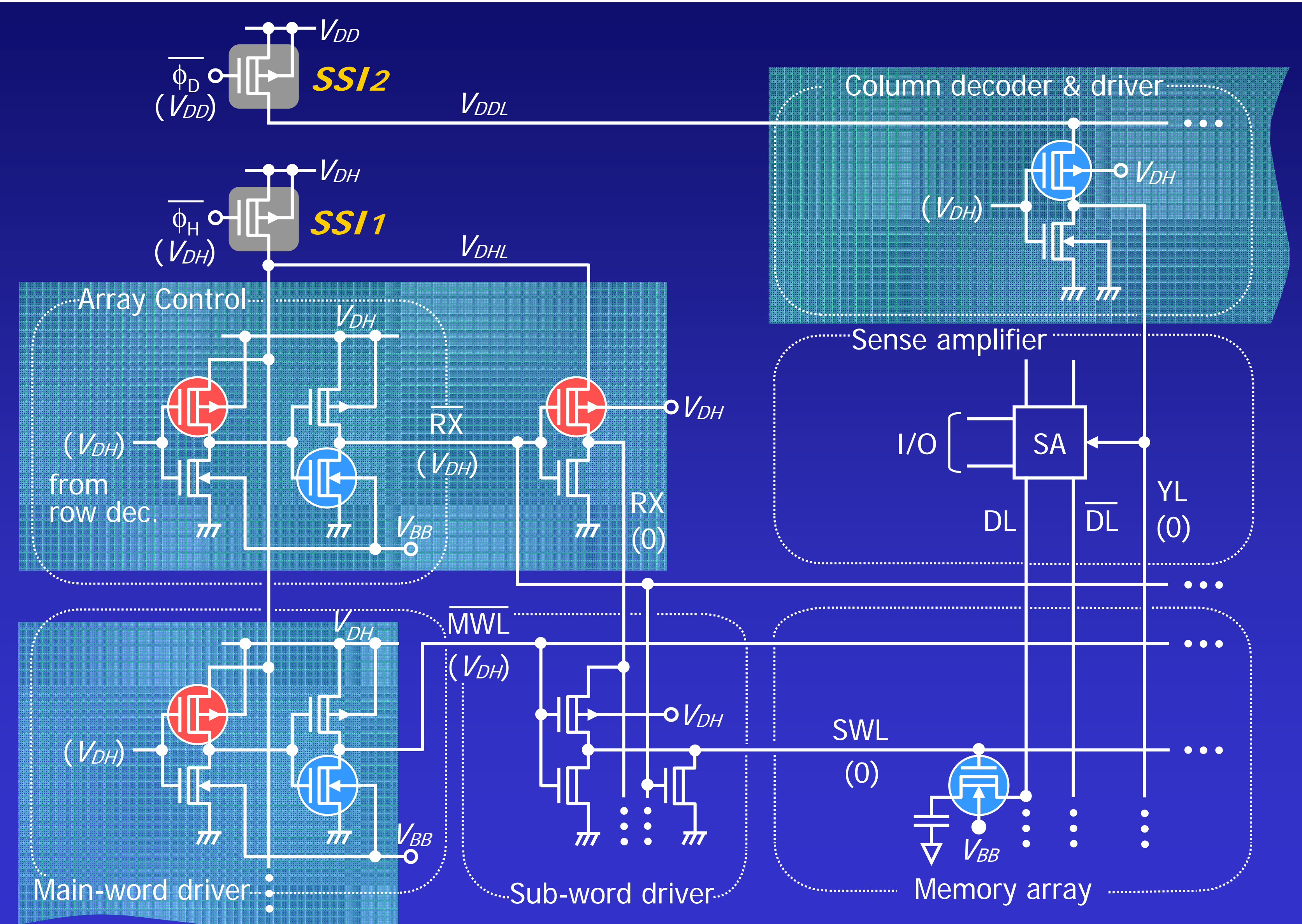
A large V_T difference may cause a racing problem: a pulse-timing imbalance between V_{Tl} -& V_{Th}-circuits.



i_L reduced to 1/5 for uniform use of V_{Tl} with assumptions:
W_{total}(critical path) = 10% of W_{total}(chip), V_{Tl} = 0.21 V, V_{Th} = 0.31 V, S = 0.1 V/dec.

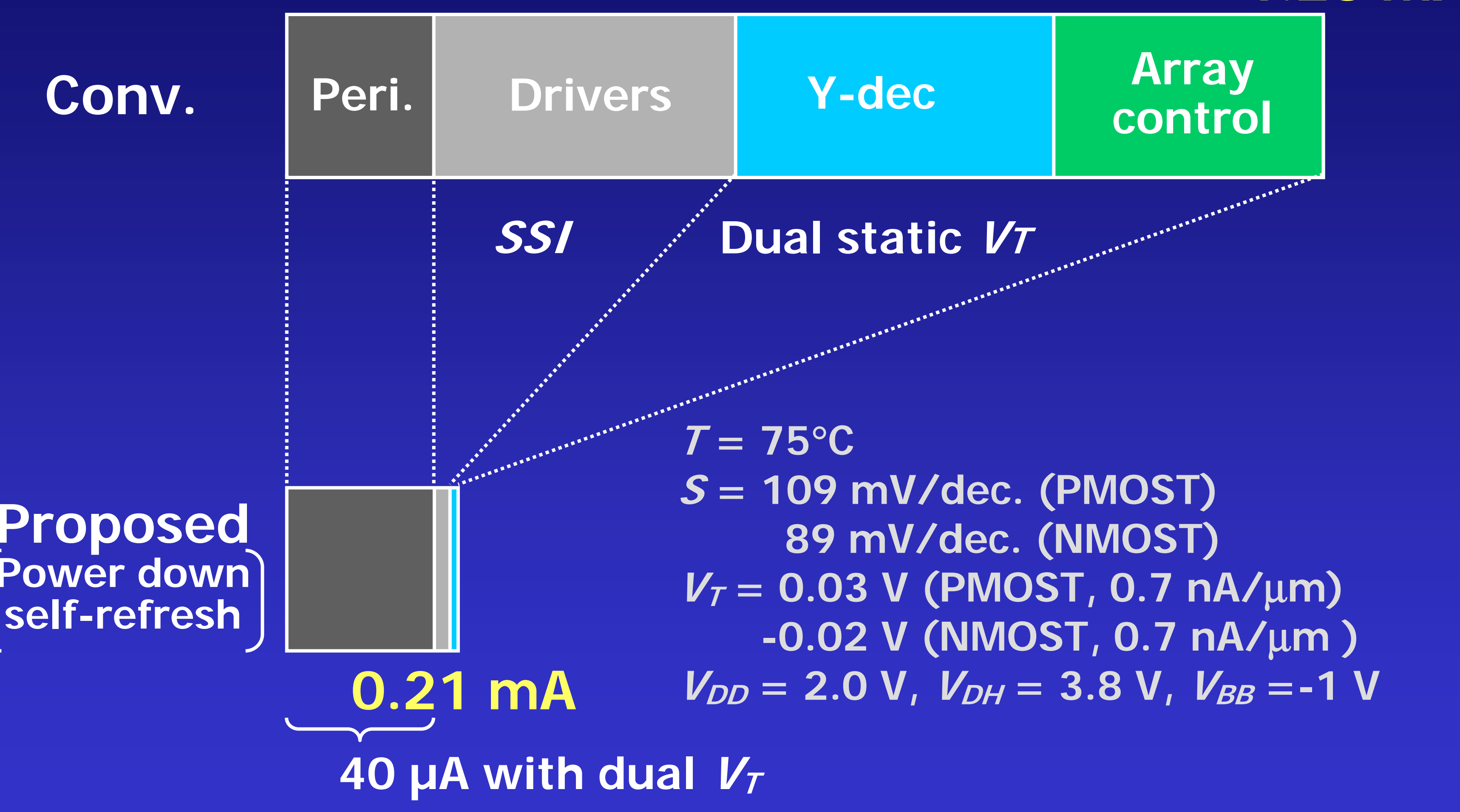
 K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

256-Mb DRAM (Standby)



M. Hasegawa et al., ISSCC Dig. pp. 80-81, 1998.

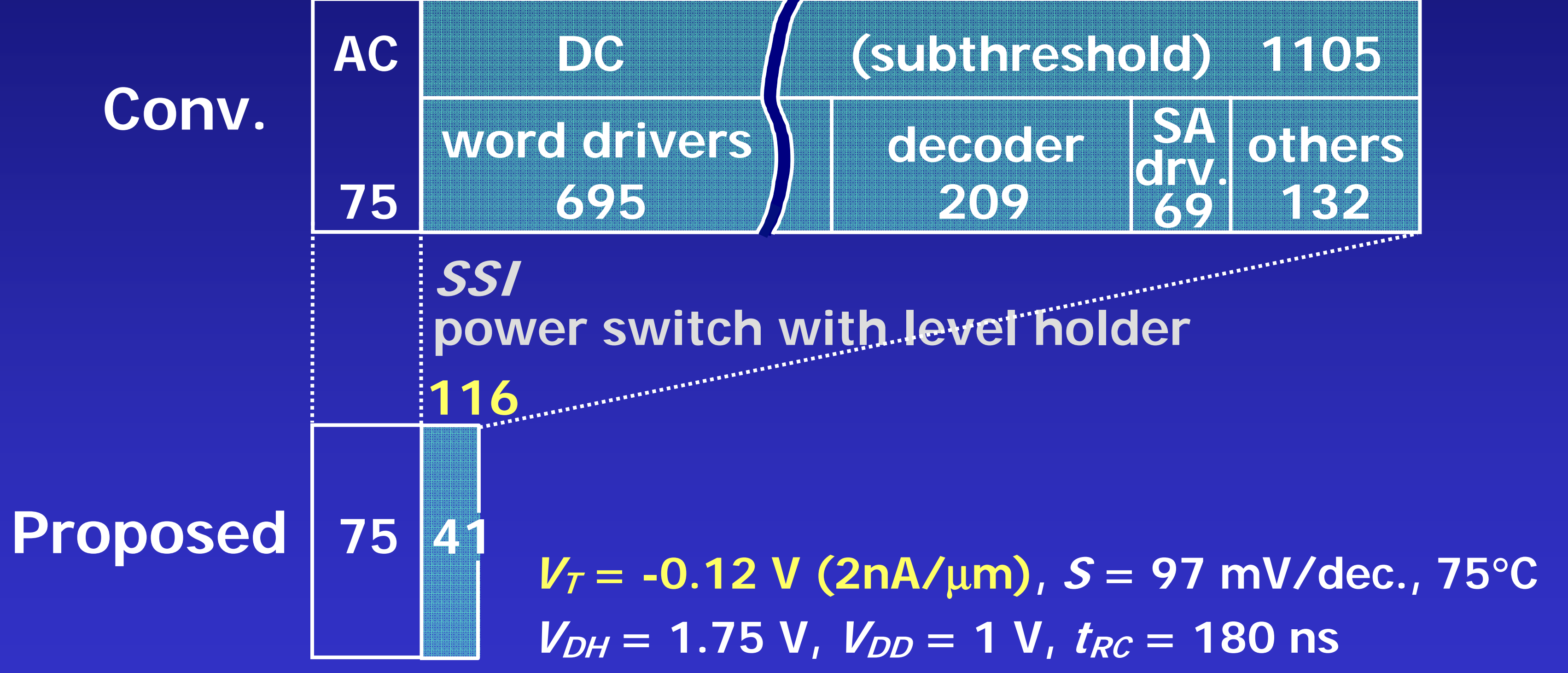
Standby Current Reduction (256 Mb)



M. Hasegawa et al., ISSCC Dig. pp. 80-81, 1998.

1-V 16-Gb DRAM

Active Current Reduction

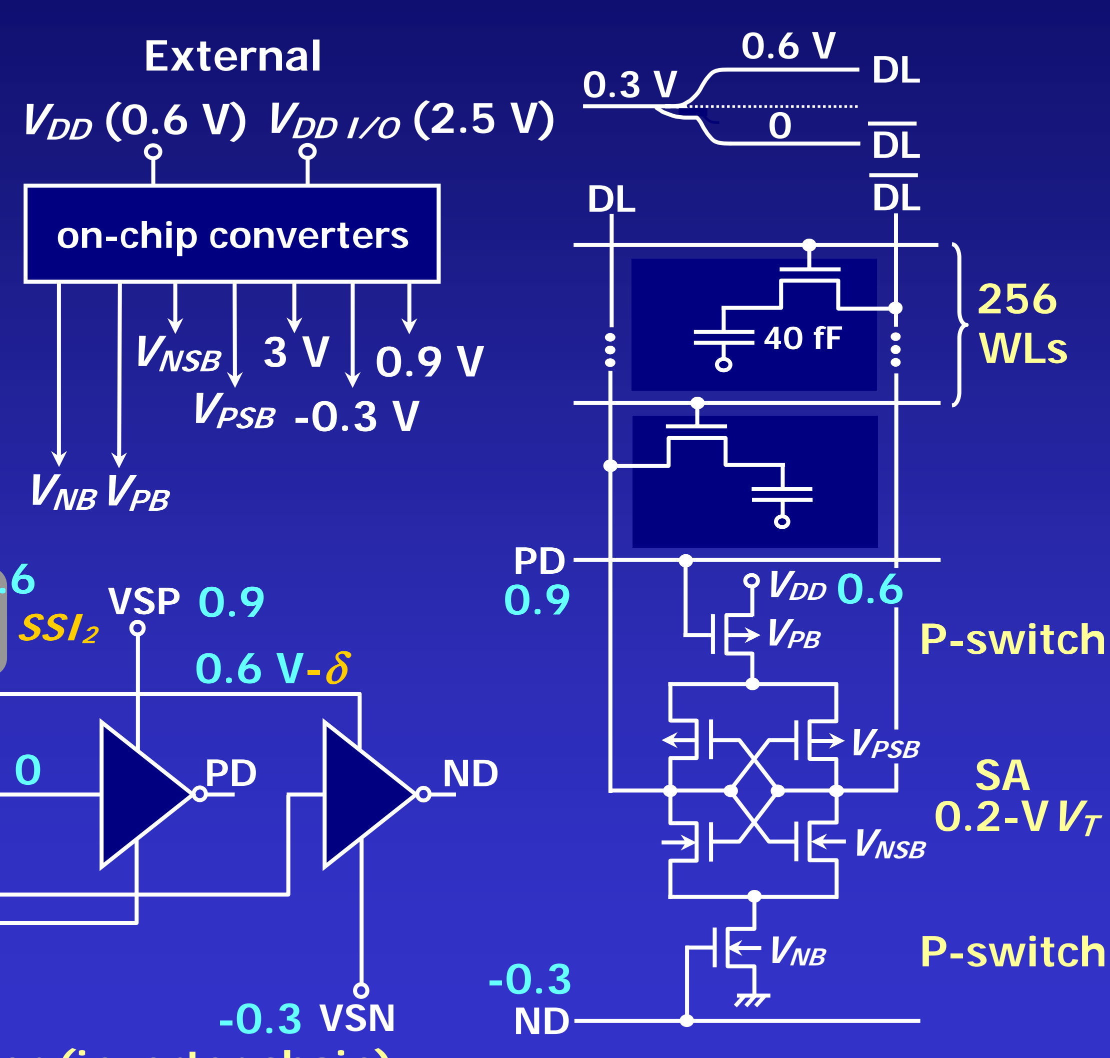


T. Sakata *et al.*, 1993 Symp. VLSI Circuits.

0.6-V 16-Mb e-DRAM

Y Circuits

- Some int. voltages are controlled to compensate for Δ (i_L, τ) caused by Δ (V_T, T, V_{DD}).
- In sleep mode, 0.3-V G-S b.b. reduces SA's i_L.

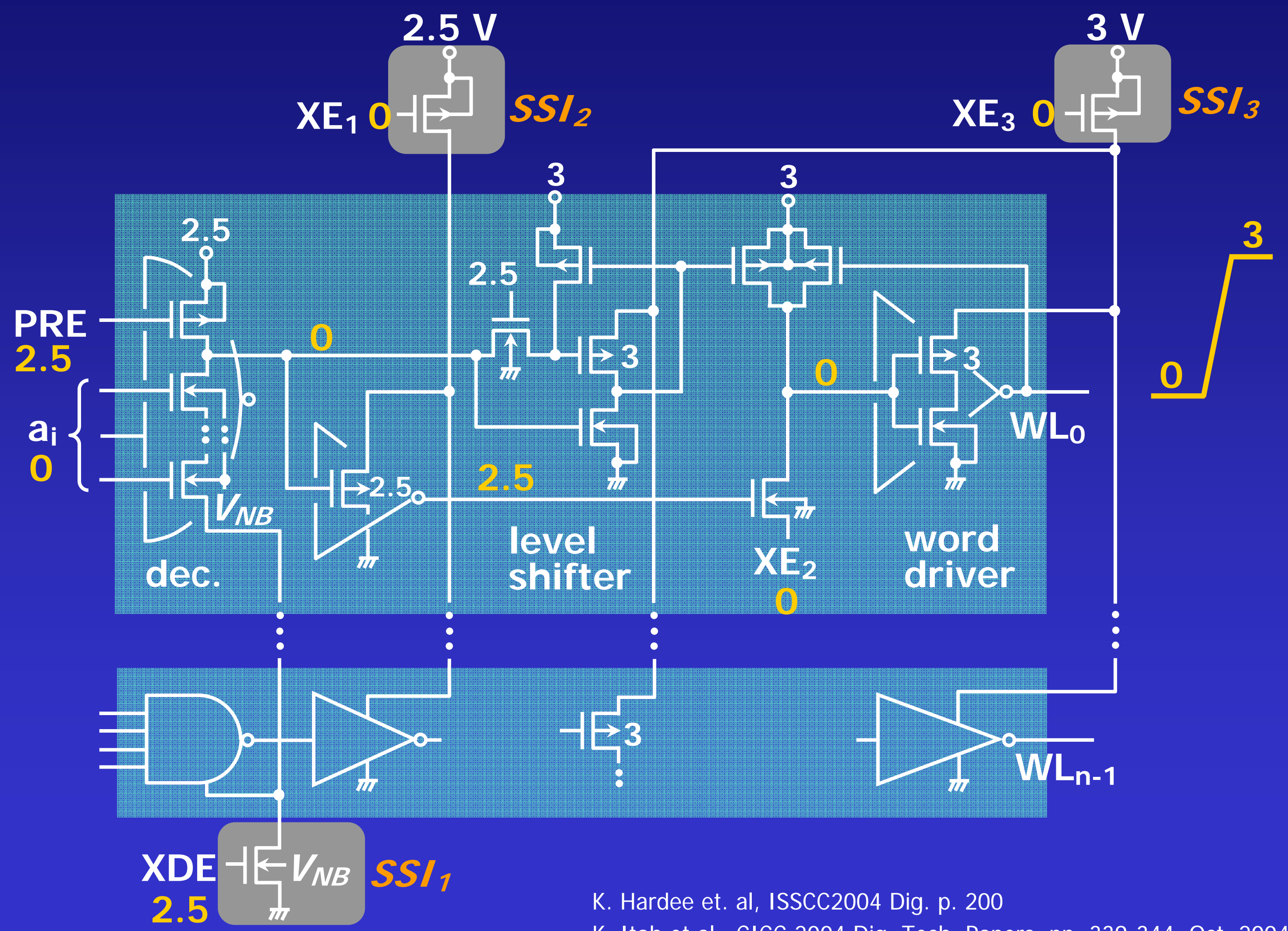


P-switch driver (inverter chain)

K. Hardee et. al, ISSCC2004 Dig. p. 200 K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

0.6-V 16-Mb e-DRAM

X Circuits (Active)

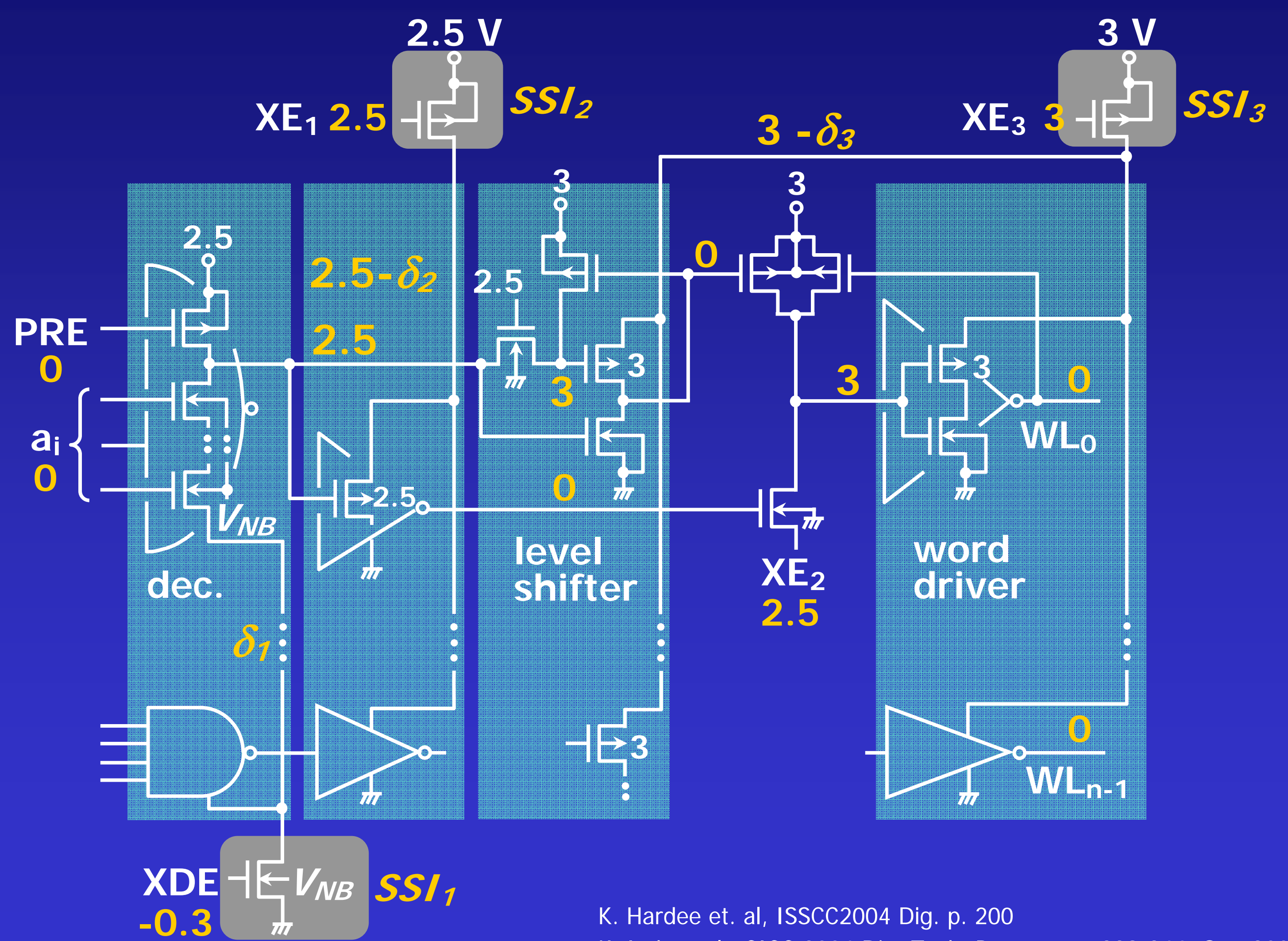


K. Hardee et. al, ISSCC2004 Dig. p. 200

K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

0.6-V 16-Mb e-DRAM

X Circuits (Sleep)



K. Hardee et. al, ISSCC2004 Dig. p. 200

K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

1.2-V 1-Mb e-SRAM

Multi-Bank Architecture

Active Mode

4-bank arch. with one-bank activation confines active circuitry to 1/4, and reduces

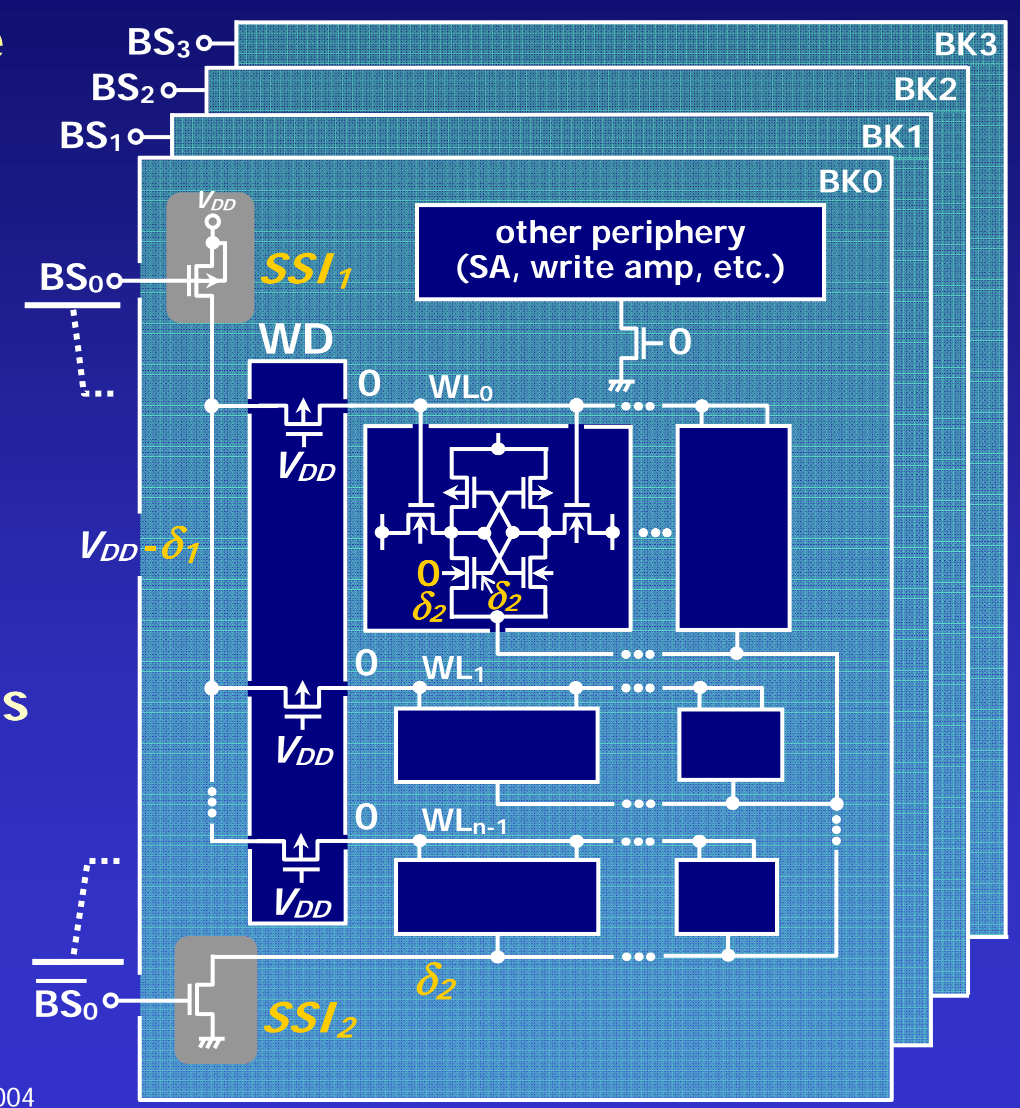
- AC power of cont. signals
- i_L in inactive banks if *SSI* is applied to WD & cells.

SSI₁ : Small δ_1 & $C_L \rightarrow$ 0.3 ns

SSI₂ : Drawbacks;
Large δ_2 (0.4 V) & $C_L \rightarrow$ 3 ns
Cell-supply reduced by δ_2

Sleep Mode

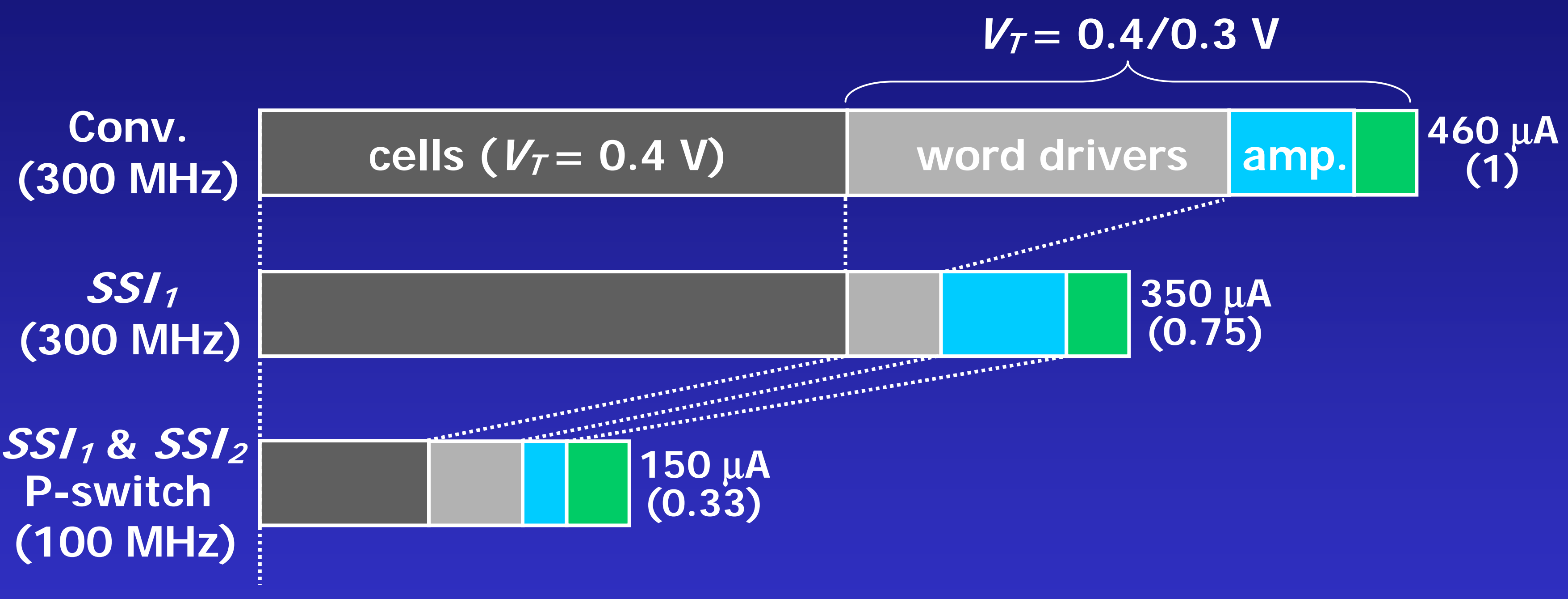
Periphery off with power switch off → 3ns



M. Yamaoka et. al., ISSCC2004 Dig. p. 494
K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

Leakage of 1-Mb e-SRAM (Active)

1.2 V, room temp.



M. Yamaoka et. al., ISSCC2004 Dig. p. 494

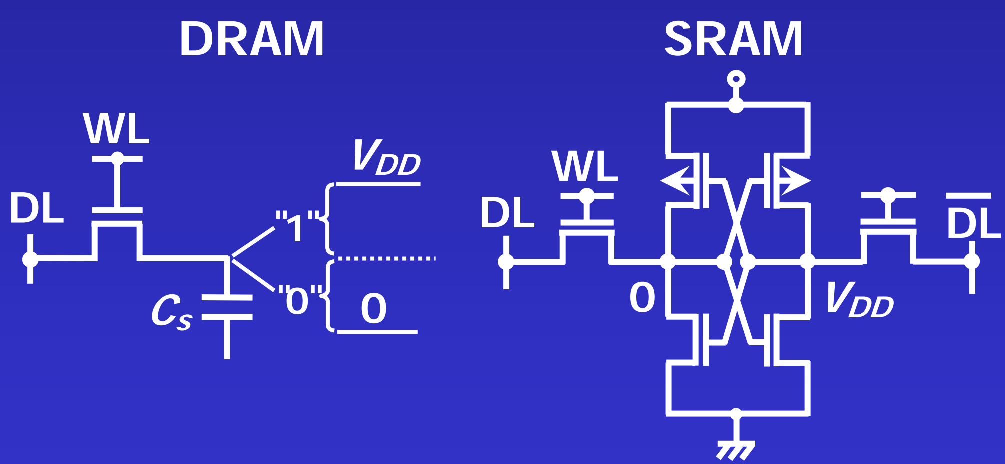
Challenges to LV e-RAMs

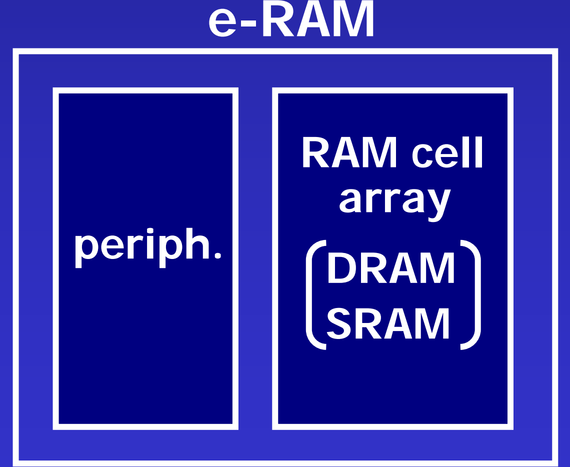
RAM Cells

- Extend low-voltage limitation to sub-1 V
  - -Degraded S/N
  - -Increased leakage
- Reduce cell size

Peripheral Circuits

- Reduce leakage
  - -Increased I_{STB} & I_{ACT}
- Reduce speed variation
  - -Unreliable operations

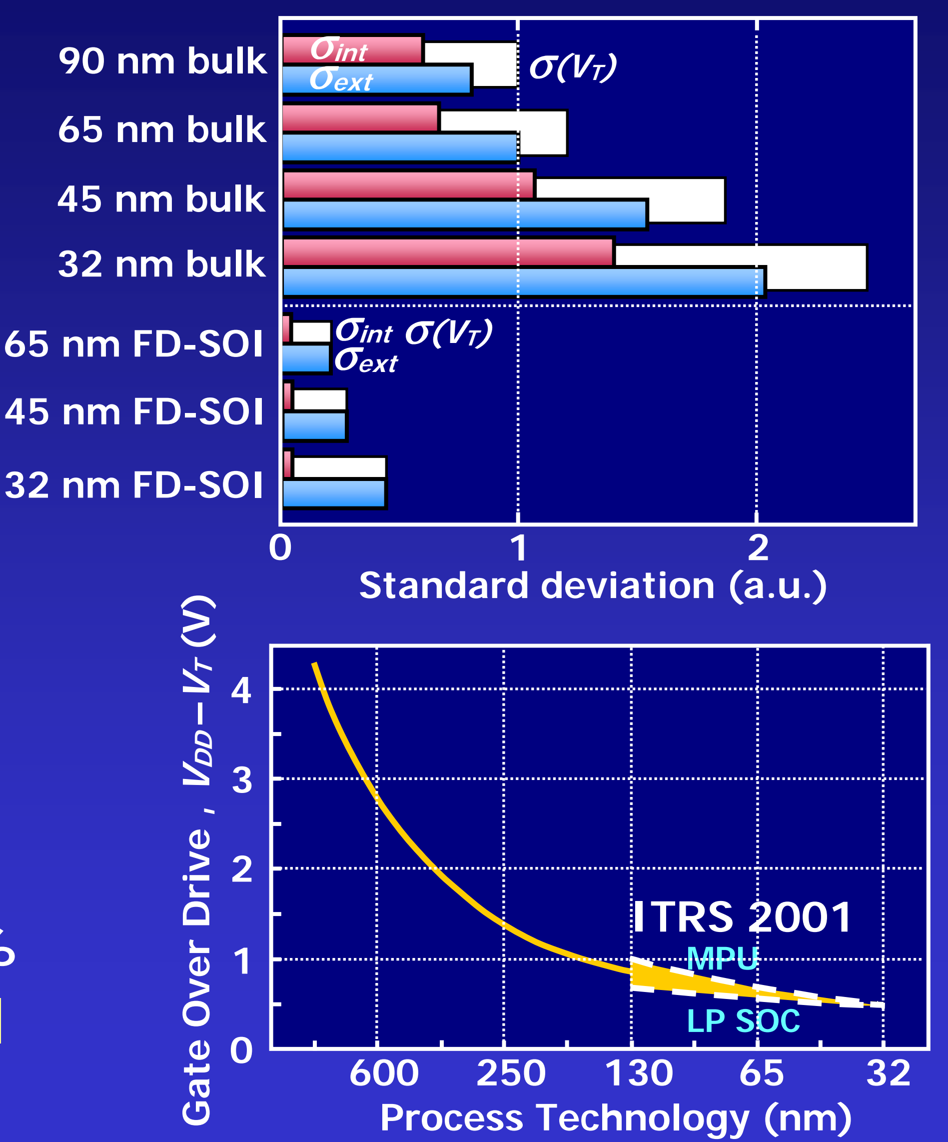




K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

Speed Variation

- Ever-increasing ΔV_T, and rapidly-lowering gate-over drive with device scaling.
- They enhance speed variation of periphery
  $\Delta\tau/\tau \propto \Delta V_T/(V_{DD}-V_T)$
- Solutions
  - For inter-die $\Delta\tau$, Compensation with V_{BB} generator. e.g., Speed improvement by 63%
  - For intra-die $\Delta\tau$, FD-SOI



M. Yamaoka et al., Symp. VLSI Circuits 2004

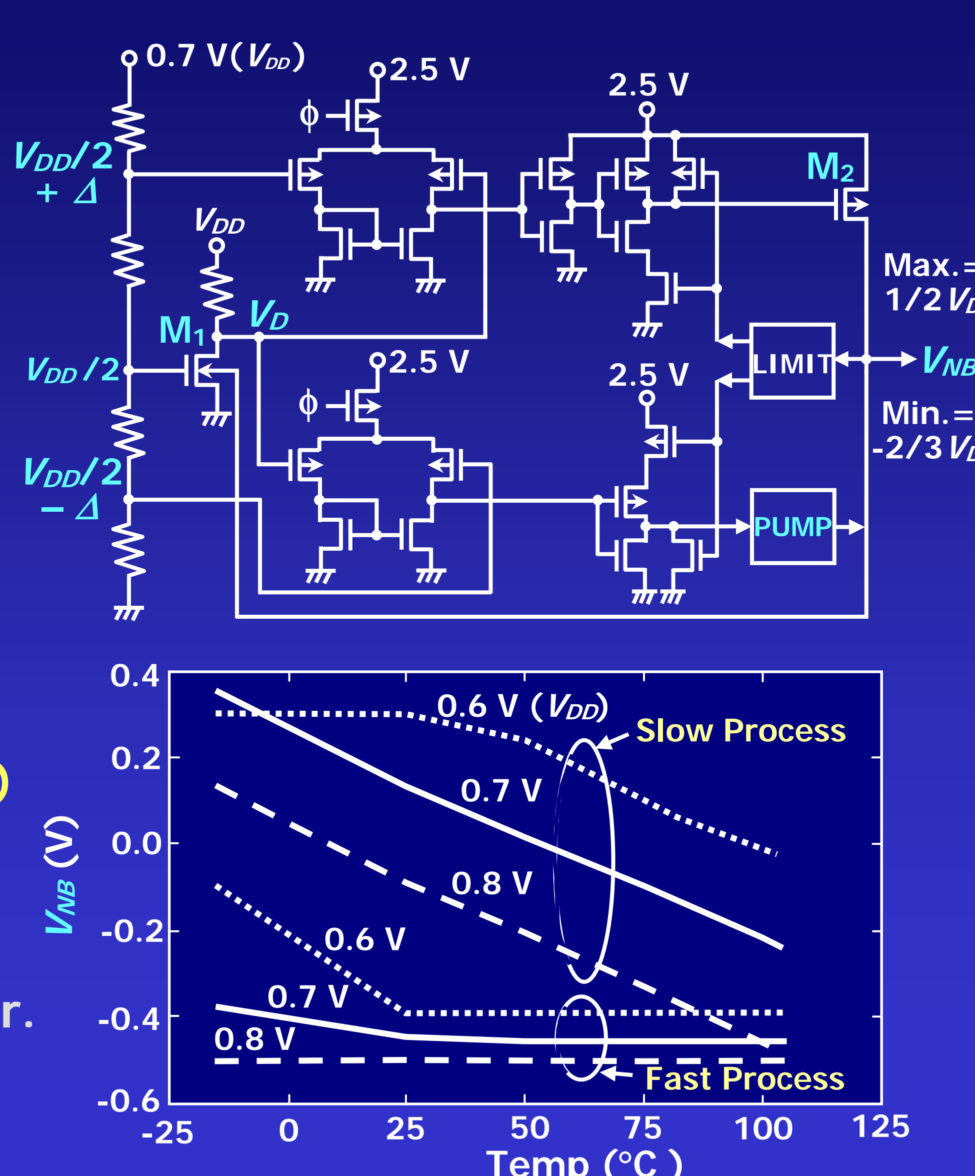
V_{BB} Generator for NMOS Body

I_{DS} (M1) is a good indicator of i_L & speed. V_{GS} (M1) = $V_{DD}/2 \cong V_T$. V_D is compared to $V_{DD}/2 + \Delta$ and $V_{DD}/2 - \Delta$ to determine if V_{NB} should be increased or decreased.

e.g.,
For low V_T (fast process or high T_j)
$V_D < V_{DD}/2 - \Delta$.
The lower OP activates PUMP, so V_{NB} starts to decrease and V_T is increased to compensate.

For high V_T (slow process or low T_j)
$V_D > V_{DD}/2 + \Delta$.
The upper OP discharges M2-gate for driving the body, allowing V_T to be reduced and compensated for.

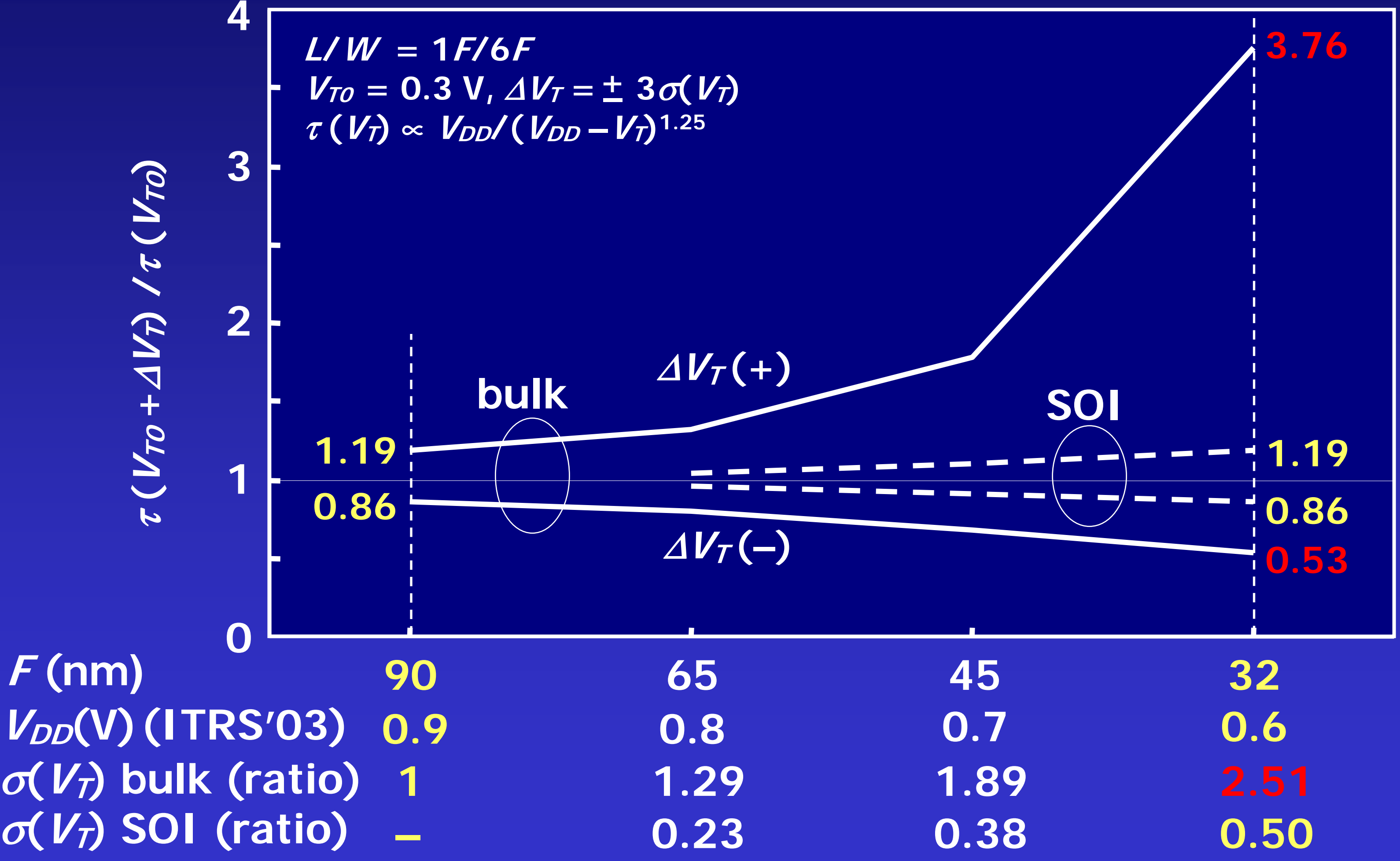
Such is the case for V_{DD}.



K. Hardee et. al, ISSCC2004 Dig. p. 200

Intra-Die Speed Variation

Low-Power CMOS LSIs



K. Itoh, Hitachi

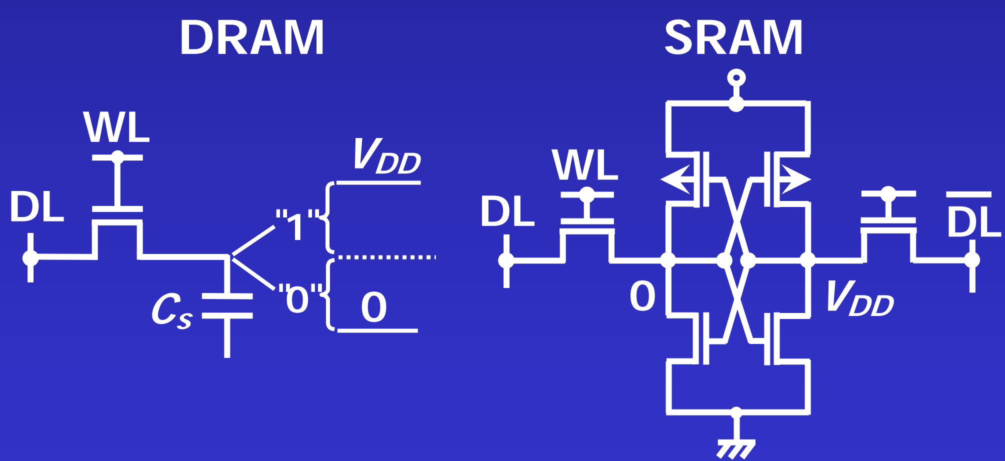
Challenges to LV e-RAMs

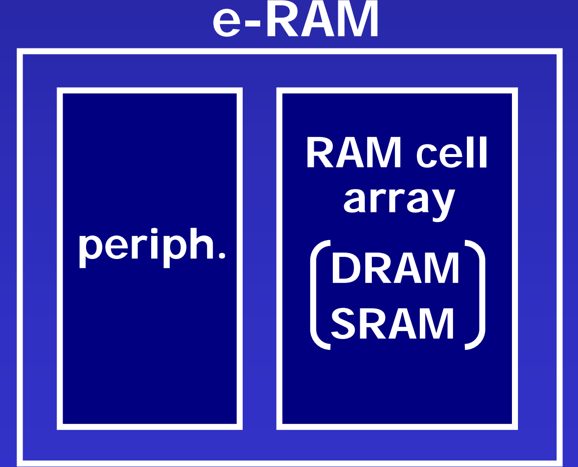
RAM Cells

- Extend low-voltage limitation to sub-1 V
  - -Degraded S/N
  - -Increased leakage
- Reduce cell size

Peripheral Circuits

- Reduce leakage
  - -Increased I_{STB} & I_{ACT}
- Reduce speed variation
  - -Unreliable operations

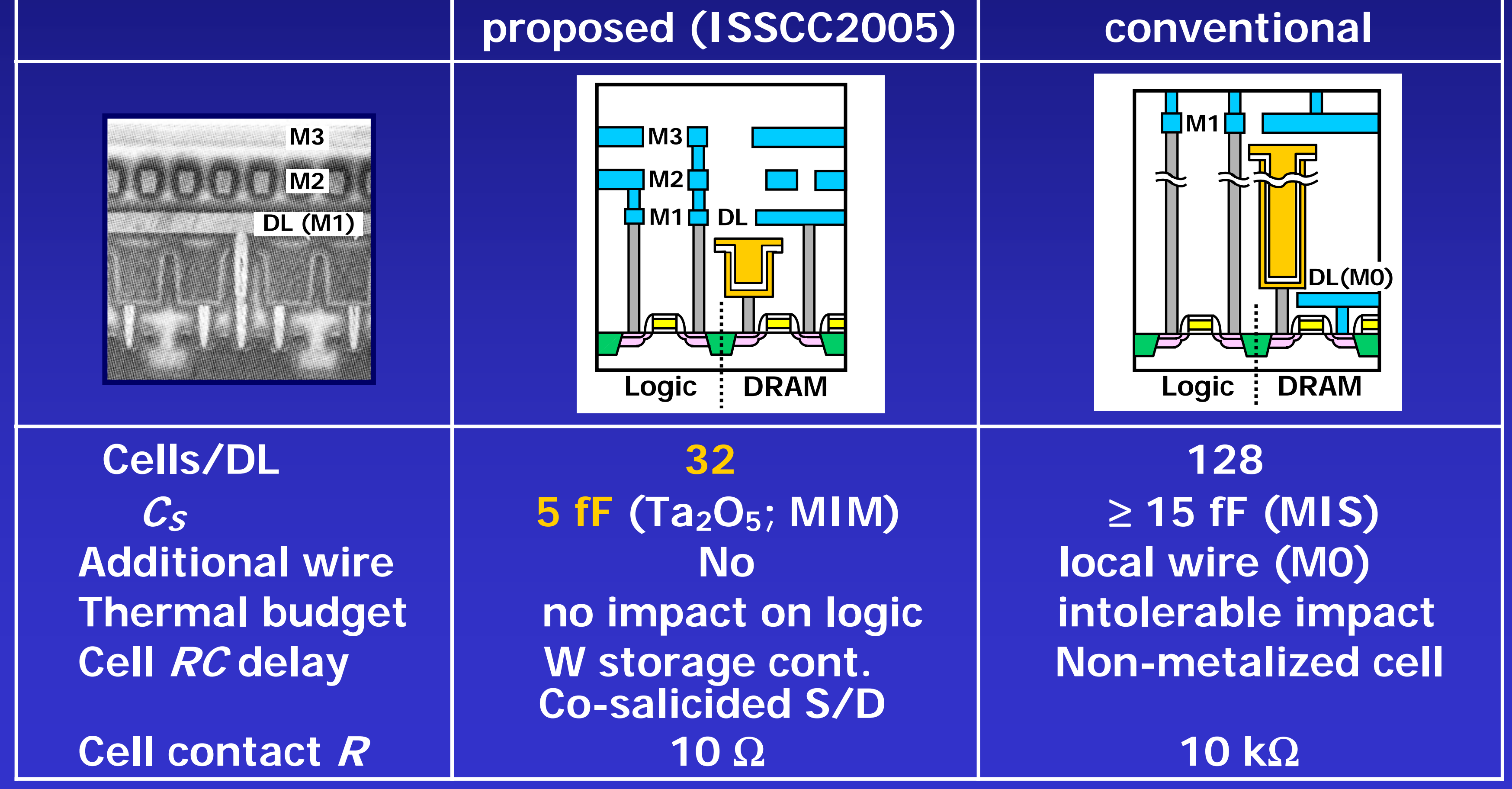




K. Itoh, VLSI Memory Chip Design, Springer-Verlag, March 2001

RAM Cells (DRAM)

Short DL allows a small C_S & simple C_S-structure with small C_D.
Planar-C_S cell might replace e-SRAM cells. $v_{sig} \cong C_S / C_D \cdot V_{DD} / 2$.
In addition, short DL enables low-V_{DD} fast operation.



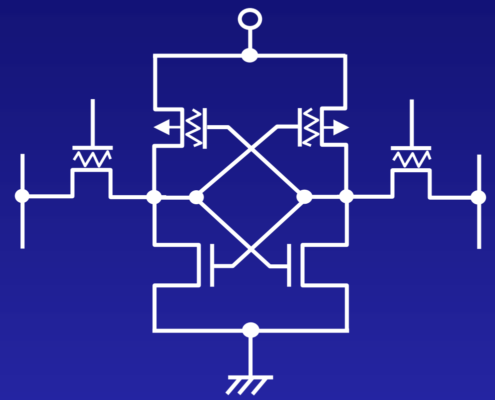
	proposed (ISSCC2005)	conventional
Cells/DL	32	128
C_S	5 fF (Ta_2O_5; MIM)	≥ 15 fF (MIS)
Additional wire	No	local wire (M0)
Thermal budget	no impact on logic	intolerable impact
Cell *RC* delay	W storage cont. Co-salicided S/D	Non-metalized cell
Cell contact *R*	10 Ω	10 kΩ

M. Iida et al., ISSCC2005 Dig. p. 460, M. Shirahata et al., ISSCC2005 Dig. p. 462

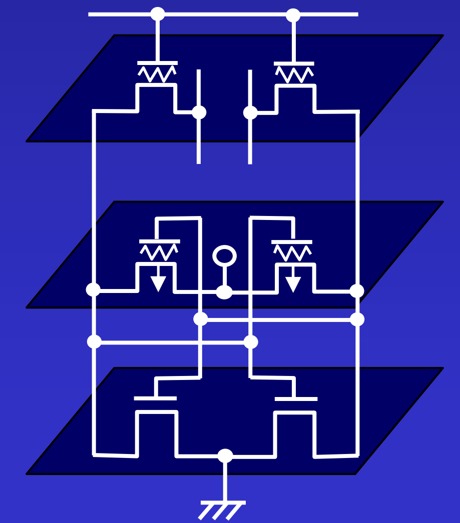
Cell Size Reduction (6-T SRAM Cell)

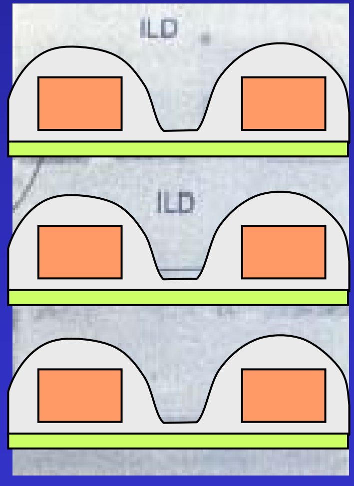
Stacked TFT SRAM Cells

- **Single-crystal TFT**
  The highest density cell ($25F^2$) comparable to DRAM cells.
  1.8-V 61.1-mm² 144-MHz 256-Mb SRAM.
- **Drawbacks as e-SRAMs**
  Sophisticated process,
  High-V_{DD} operation due to TFT PMOST of $S = 140$ mV/dec.,
  I_{DS} = 2/3 of the bulk.



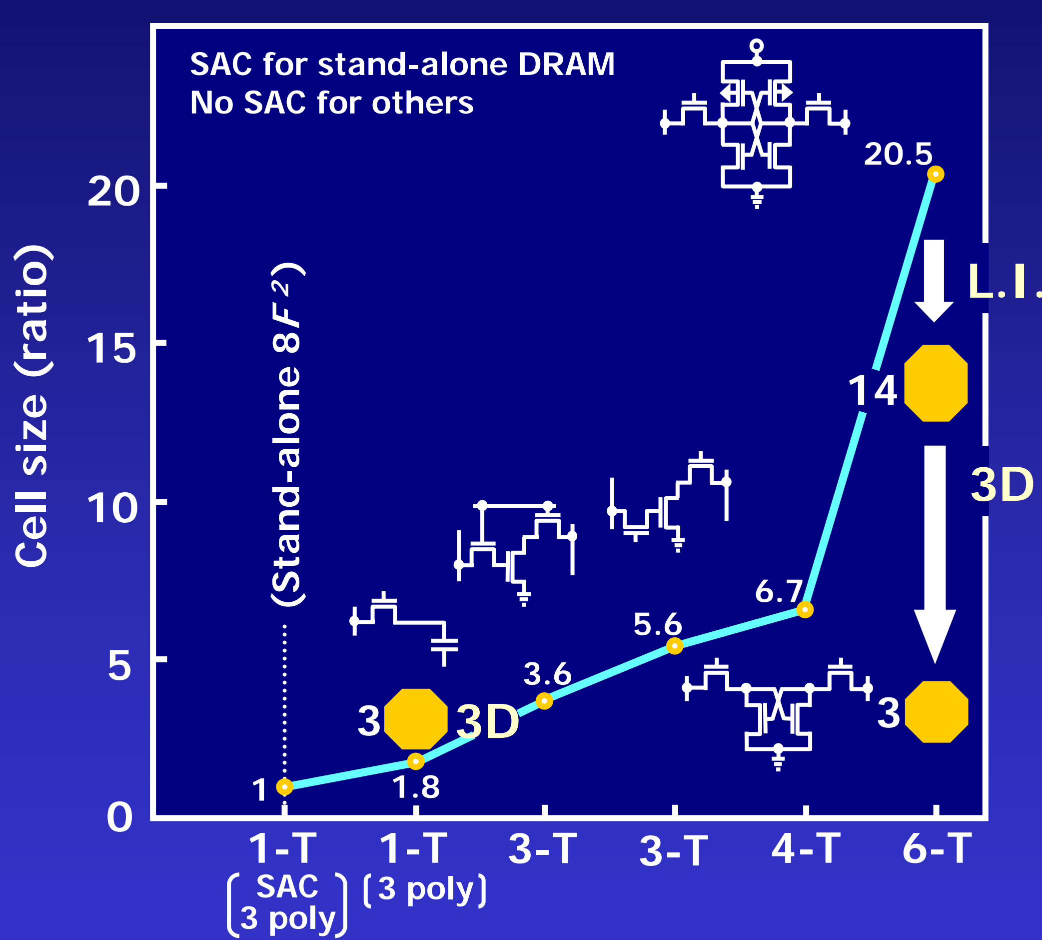
Load p-TFTs & transfer n-TFTs double-stacked over bulk driver n-MOSTs in different levels of layers.





S.-M. Jung, et al., Symp. VLSI Tech. June 2004, Y.H.Suh et al., ISSCC2005 Dig. p. 476.

Cell-Size Comparisons



Future Prospects for RAMs

6-T SRAM Cell: Due to high necessary V_T & large ΔV_T

- Not suitable for sub-1-V V_{DD},
- Continue to be used for a high V_{DD} (≥ 1 V).

Challenge; Small-ΔV_T MOSTs. TFT cells for stand-alone SRAMs.

1-T DRAM Cell: • Suitable even for sub-1-V V_{DD}.

Challenges; Planar capacitors, Small-ΔV_T MOSTs.

Peripheral Circuits:

- Subthreshold-currents will be reduced sufficiently with existing techniques even for active mode.
- Speed variations will continue to be serious.

Challenges; V_{BB} control, Small-ΔV_T MOSTs.

Two Approaches:

High-V_{DD} bulk-CMOS for low-cost RAMs,
Low-V_{DD} FD-SOI for high-speed low-power RAMs.

Conclusion

1. I discussed challenges and trends in LV RAMs.
2. I reviewed state-of-the-art LV RAM circuits.
3. I gave prospects of RAMs with emphasis on further needs for
   - Ultra-low voltage RAM cells,
   - Advanced devices & circuits to reduce speed variations.