
Analog Design in Sub-100nm Technologies

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History



Pederson/Wooley, ca. 1970



Boser/Murmann, ca. 2003



Pederson, ca. 1951



Wooley/Boser, ca. 1988



?

?

Outline

- Impact of scaling on analog performance metrics
- How to improve analog performance using digital gates
 - Digitally assisted A/D converters

Quotes

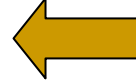
- [Vertregt, *ESSCIRC 2004*]
 - "Significant power efficiency improvements are predicted as a result of scaling to deep sub-micron technology nodes."

- [Annema, *IEEE J. Solid-State Circuits*, 12/2005]
 - "In summary: unlike digital designs, analog circuits can benefit from technology scaling if the supply voltages are not scaled down."

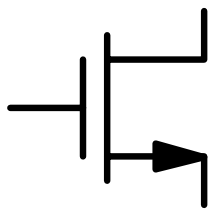
- [Nauta, *ESSCIRC 2005*]
 - "The evolution of CMOS technology will continue for many years to come, which is beneficial for digital circuits but which is not so for analog."

List of Concerns

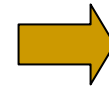
- Reduced supply voltage
- Low intrinsic gain
- Variability
- Distortion
- Gate leakage
- Isolation
- ...
- Cost (mask & wafer)
- Model accuracy
- ...



Technology Benchmarking

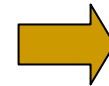


■ Transit frequency



$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs}}$$

■ Transconductor efficiency



$$\frac{g_m}{I_D}$$

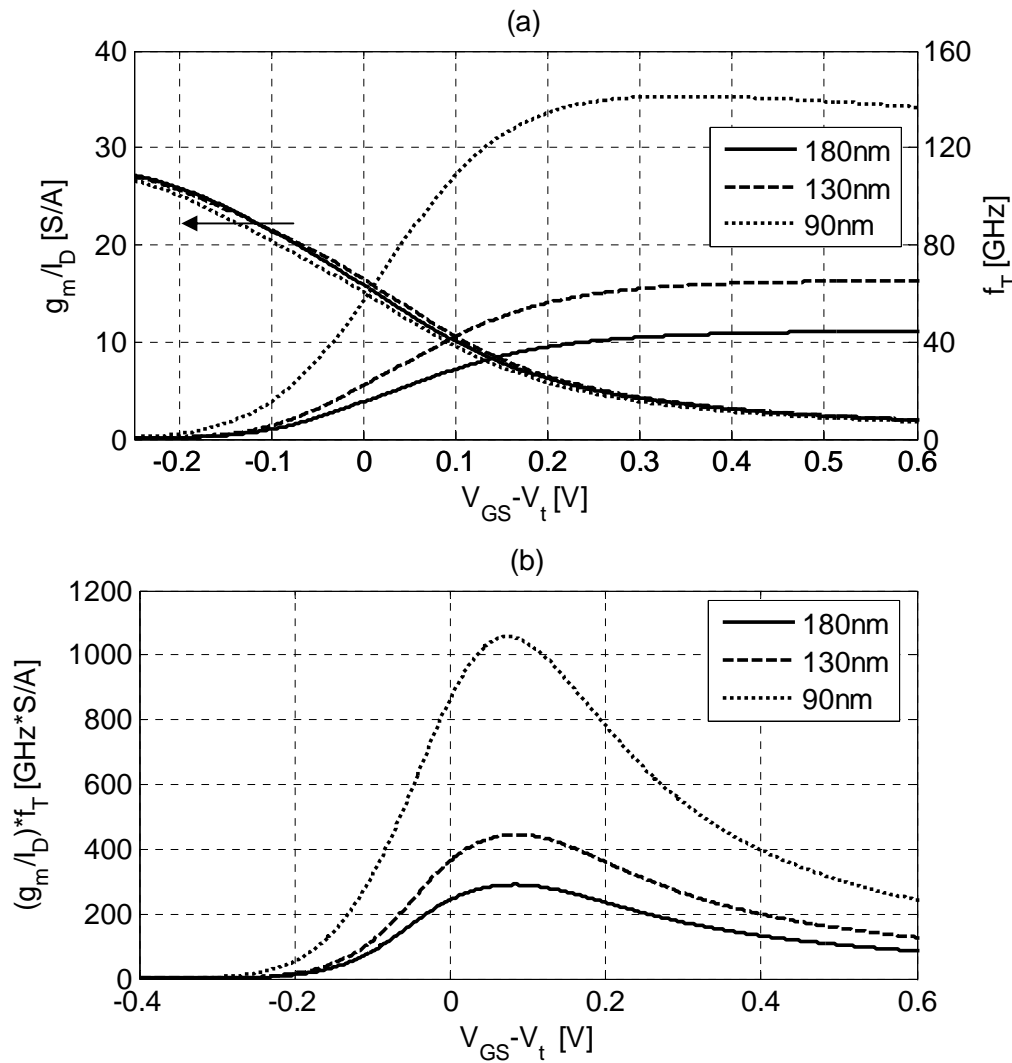
■ Available signal swing

■ Intrinsic gain



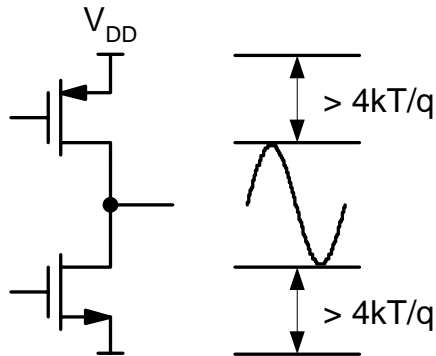
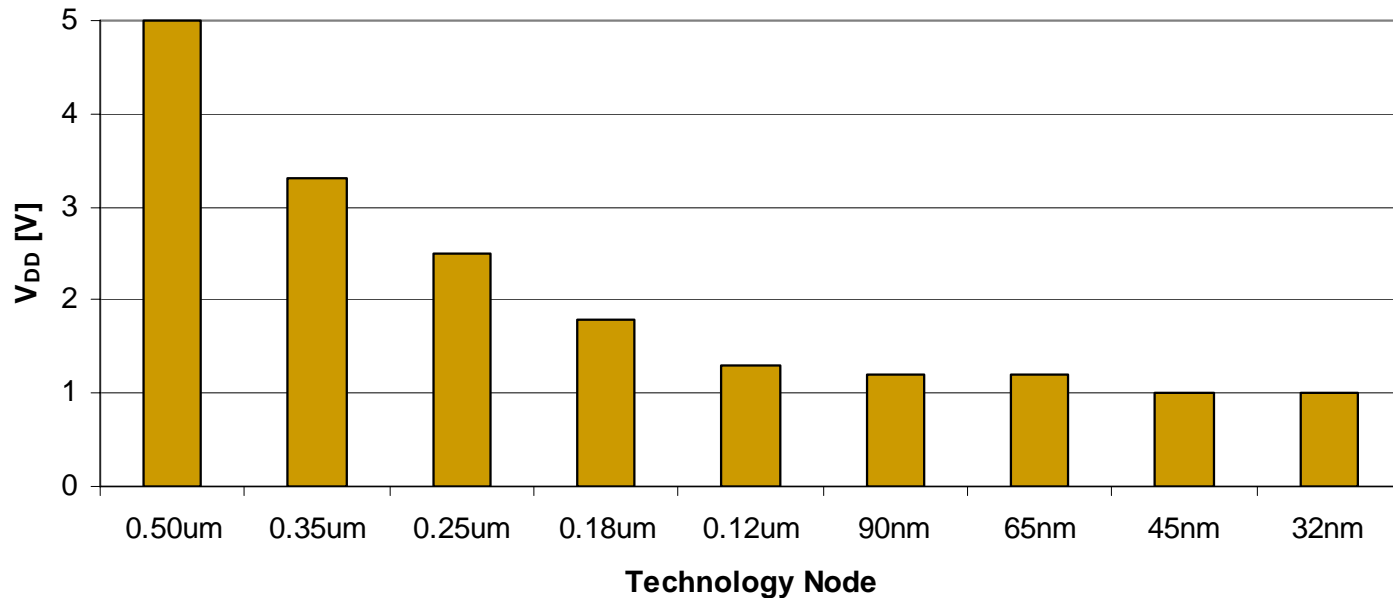
$$\frac{g_m}{g_{ds}}$$

g_m/I_D and f_T trends



- g_m/I_D essentially unaffected by scaling
- Very high f_T in recent technologies
- Enables RF CMOS

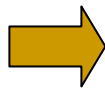
Available Signal Swing



$$\text{Available Swing} < V_{DD} - 8 \frac{kT}{q}$$

Noise Limited Circuit Performance

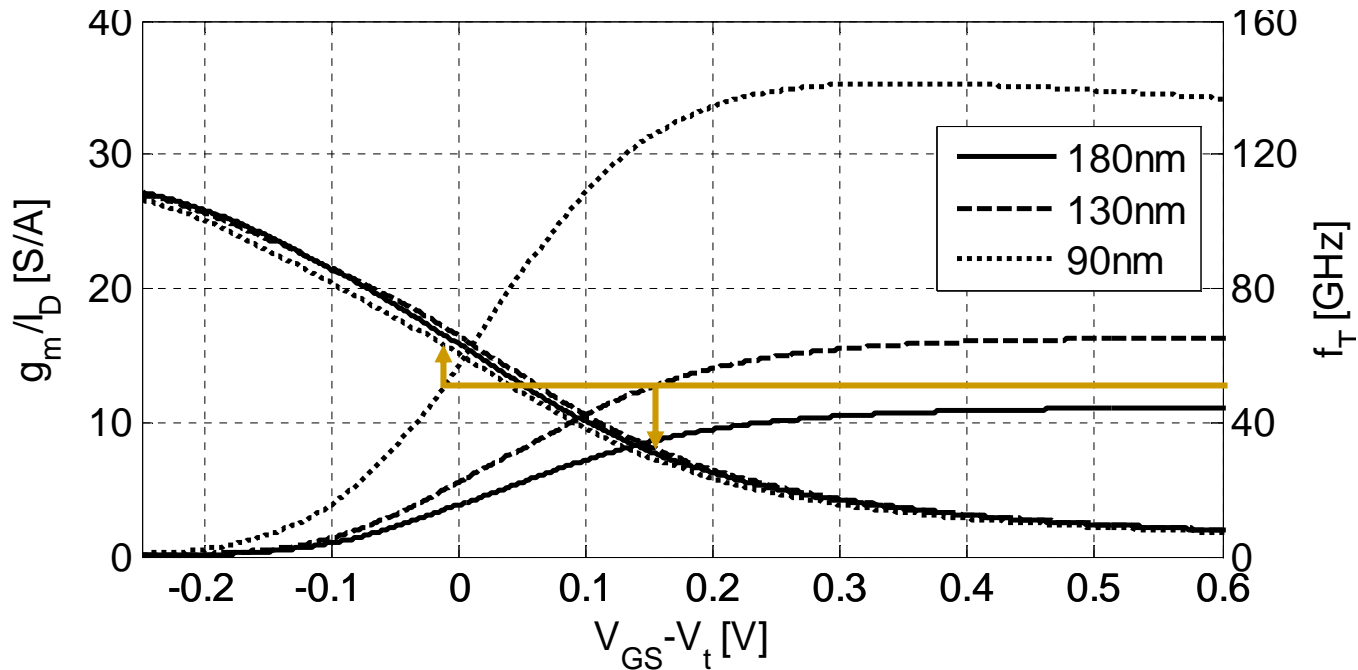
$$P \propto V_{DD} \cdot I_D \quad BW \propto \frac{g_m}{C} \quad DR \propto \frac{Swing^2}{kT/C}$$



$$\frac{BW \cdot DR}{P} \propto V_{DD} \cdot \left(\frac{Swing}{V_{DD}} \right)^2 \cdot \frac{g_m}{I_D}$$

- Low V_{DD} is generally bad news, but
 - Analog designers have worked hard to maintain or even improve $Swing/V_{DD}$
 - Typical ADC in 0.5 μ m: $Swing/V_{DD}=2/5$
 - Typical ADC in 90nm: $Swing/V_{DD}=0.5/1$
 - How about g_m/I_D ?

Leveraging f_T



- Example

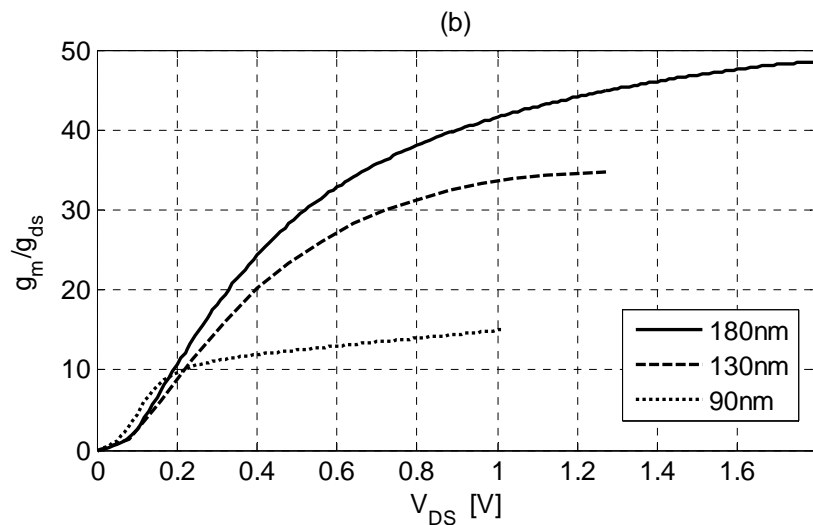
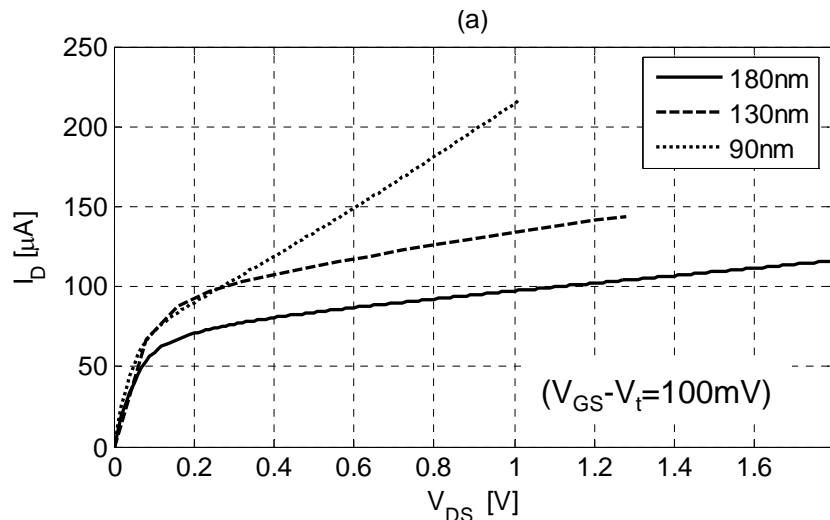
- $f_T = 50\text{GHz}$, 130nm: $g_m/I_D = 8\text{S/A}$, 90nm: $g_m/I_D = 16\text{S/A}$

- For "fixed-speed" applications, high f_T can be leveraged to mitigate low V_{DD} penalty

Further Considerations

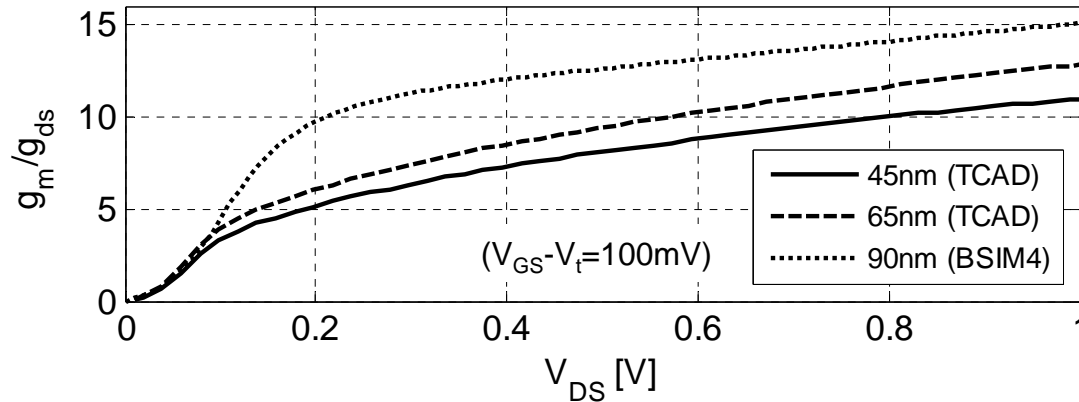
- Analog building blocks are never completely limited by thermal noise
 - Not uncommon to have ~50% dynamic power
 - Decreases with scaling
- Designers are continuing to develop/refine low-voltage design techniques
 - Recent publications show very good analog building block performance at 1V
- Bottom line
 - Analog design is challenging at 1V, but it's neither impossible nor detrimental

Intrinsic Gain



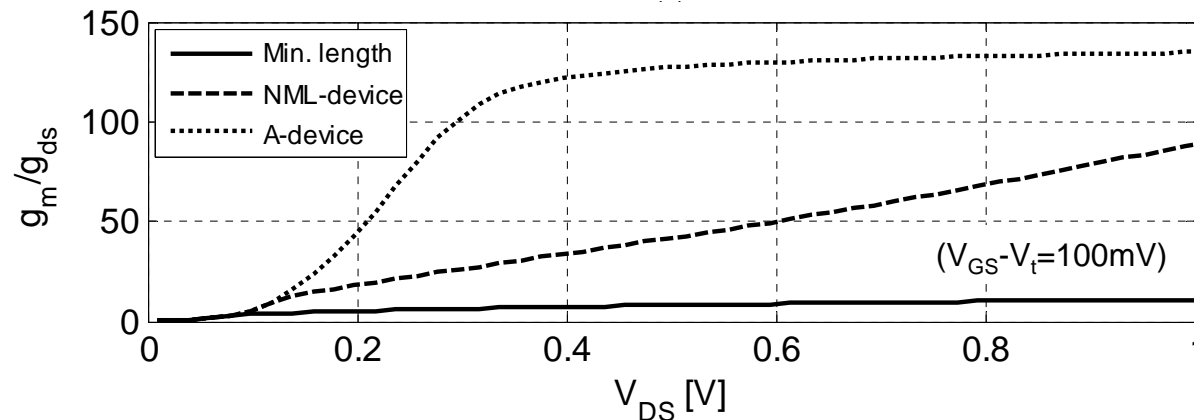
- A real issue
 - How to design a high-gain op-amp with devices that have intrinsic gain of ~ 10 ?
- How much worse does this get at 45nm/65nm?

Intrinsic Gain in the Near Future



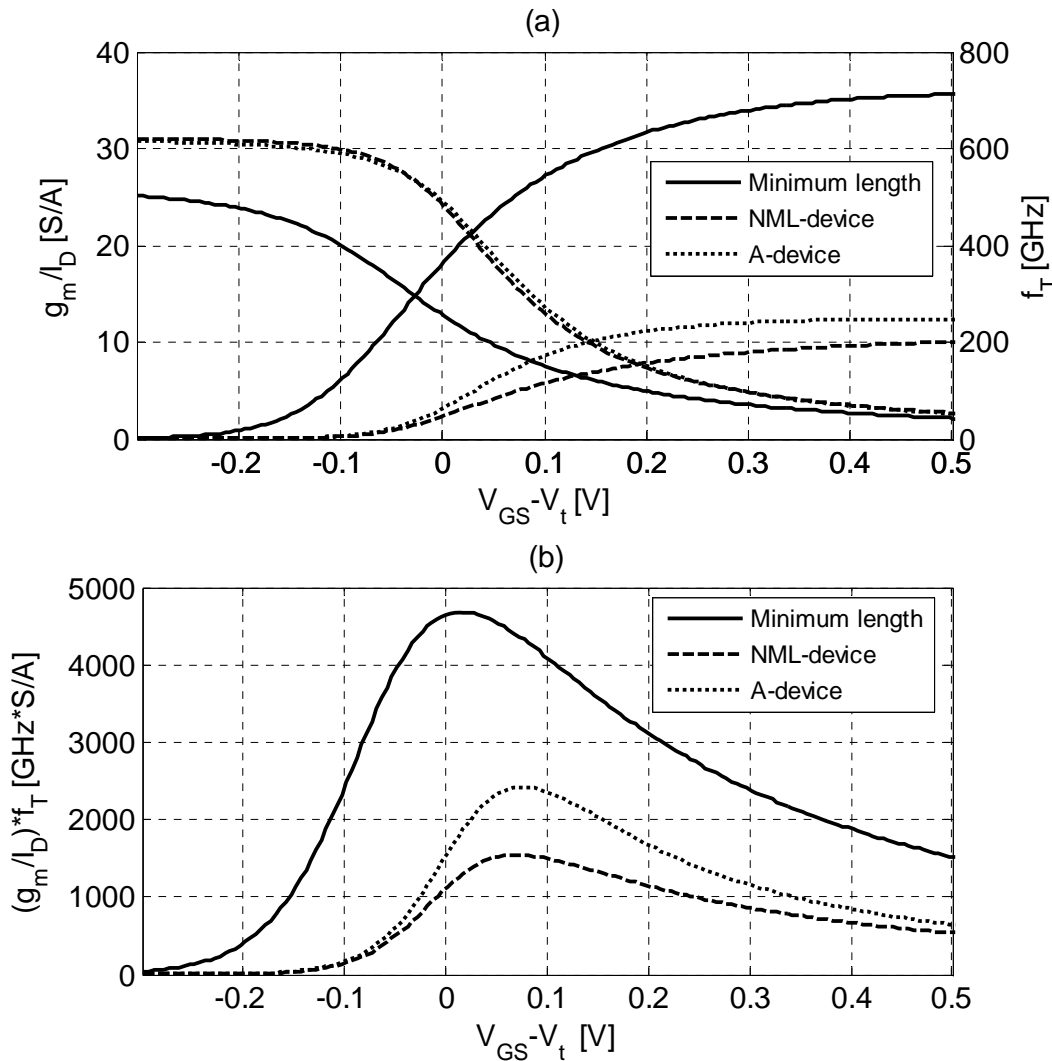
- Pretty bad...
- Solutions
 - Use non-minimum length device (NML-device)
 - Use asymmetric device without drain-side pocket implant (A-device)
 - Or, don't try to build op-amps in these technologies...
 - More later

Intrinsic Gain of Alternate Devices (45nm)



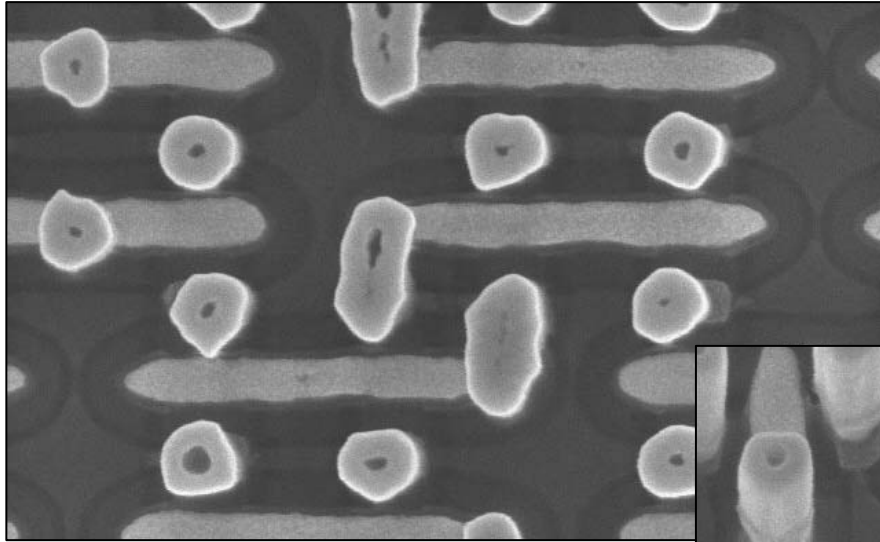
- For both NML and A-device $L_{\text{physical}}=80\text{nm}$ ($L_{\text{physical}}=24\text{nm}$ for minimum length device)
- Great, lots of gain!
 - But how about f_T ?

g_m/I_D and f_T for Alternate Devices (45nm)

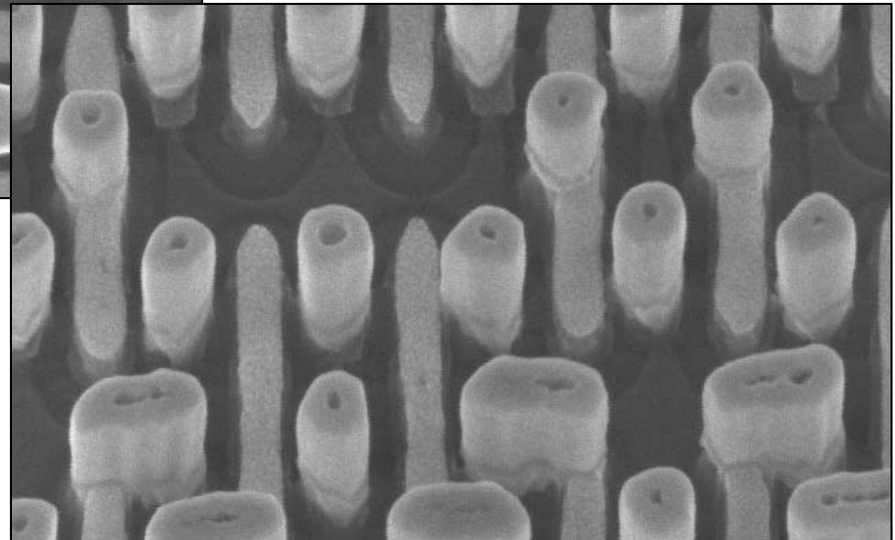


- f_T much lower than for minimum length 45-nm device
- But still better than minimum length device in 90nm...
- Who needs $f_T > 200\text{GHz}$ in an op-amp...?

Variability (1)

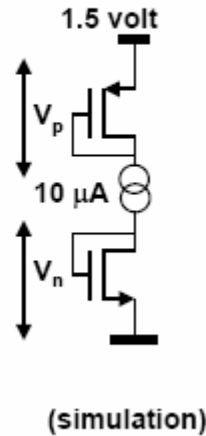
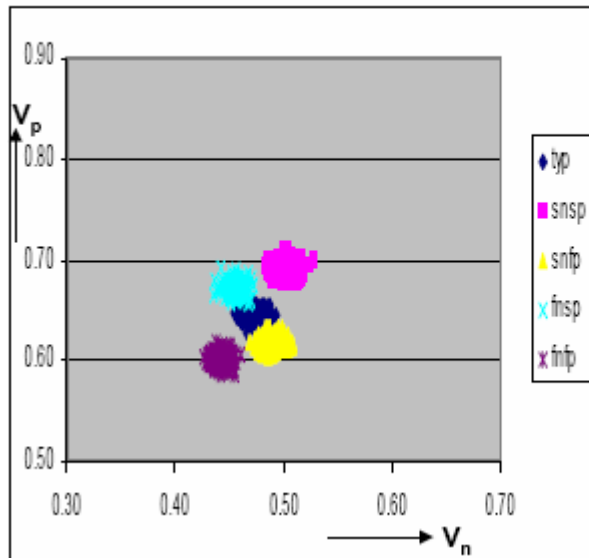


[Courtesy A. Bowling,
Texas Instruments]

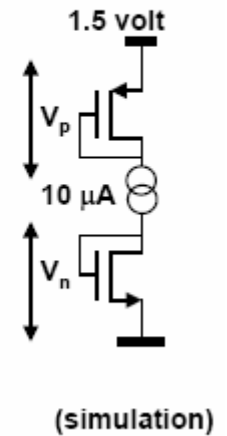
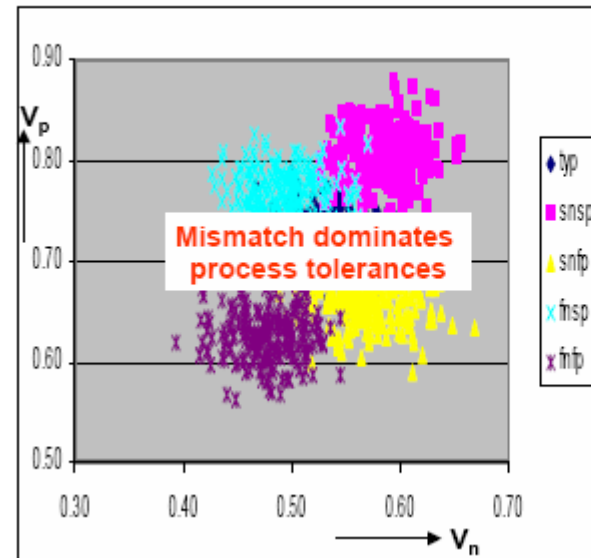


Variability (2)

Matching: CMOS 90nm, W/L=1/0.5



Matching: CMOS 90nm, W/L=0.2/0.1



[Marcel Pelgrom, Philips]

- Device mismatch larger than process corner variations!
 - For small "digital" transistors...

Variability (3)

Digital

- A "new" problem
 - Significant impact on achievable performance, yield, design methodology, EDA, ...
- Big difference compared to analog
 - Care about millions if not billions of devices!

Analog

- A well known problem
 - Designers are used to "caring" about mismatch
- Lots of options and potential solutions
 - Layout techniques, analog or digital calibration, dynamic element matching, larger device area, ...
- Usually care about matching for a few up to a few hundred transistors

Outline

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- How to improve analog performance using digital gates
 - Digitally assisted A/D converters

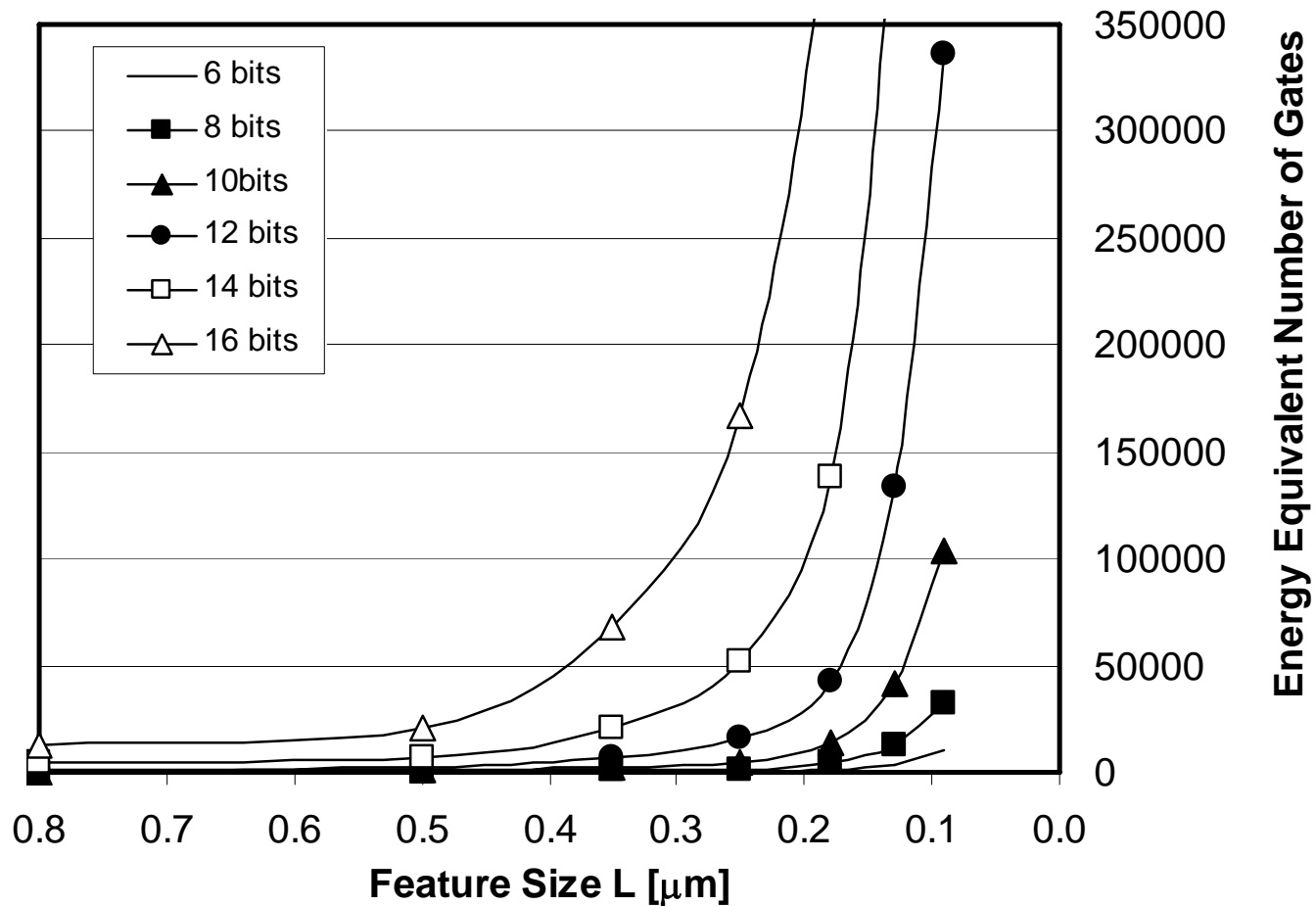
"Mostly Digital" or "Digitally Assisted" Analog

- Based on minimalistic analog circuits
- Achieve precision/performance by means of added digital processing
- Examples
 - Mostly digital PLLs
 - Power amplifiers with digital pre-distortion
 - Digital radio processor architecture (TI)
 - Digitally corrected ADCs
 - ...

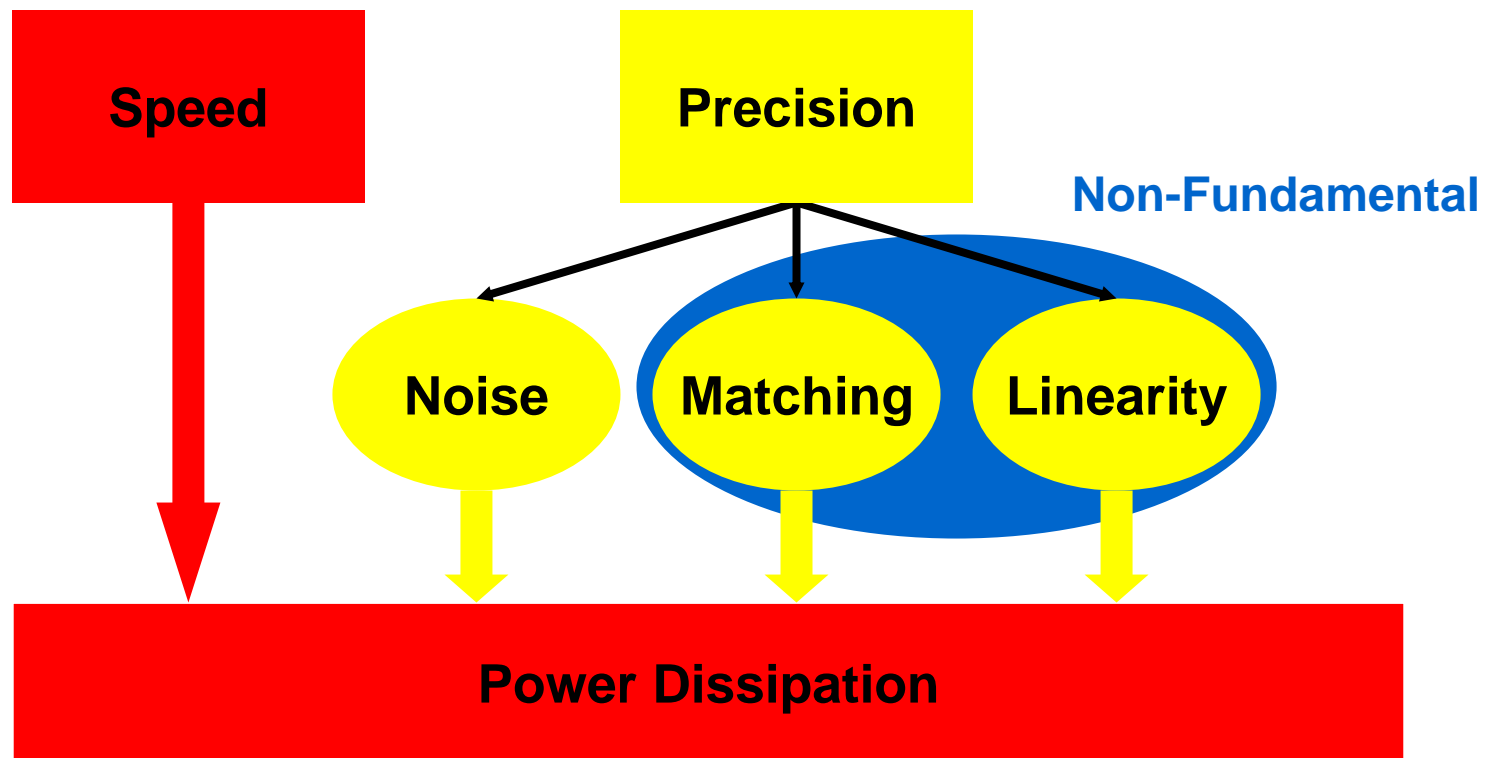
Motivation from Energy Perspective

- Does "digital assistance" make sense?
- Interesting metric to look at
 - How many digital gates can you toggle for the energy needed in one A/D conversion?
- Example
 - Two-input NAND gate in 90nm CMOS consumes 2.5 fJ/operation
 - 10-bit ADC consumes 0.25 nJ/conversion
 - Energy equivalent number of gates
 - $0.25\text{nJ}/2.5\text{fJ} = 100,000$

Impact of Technology Scaling



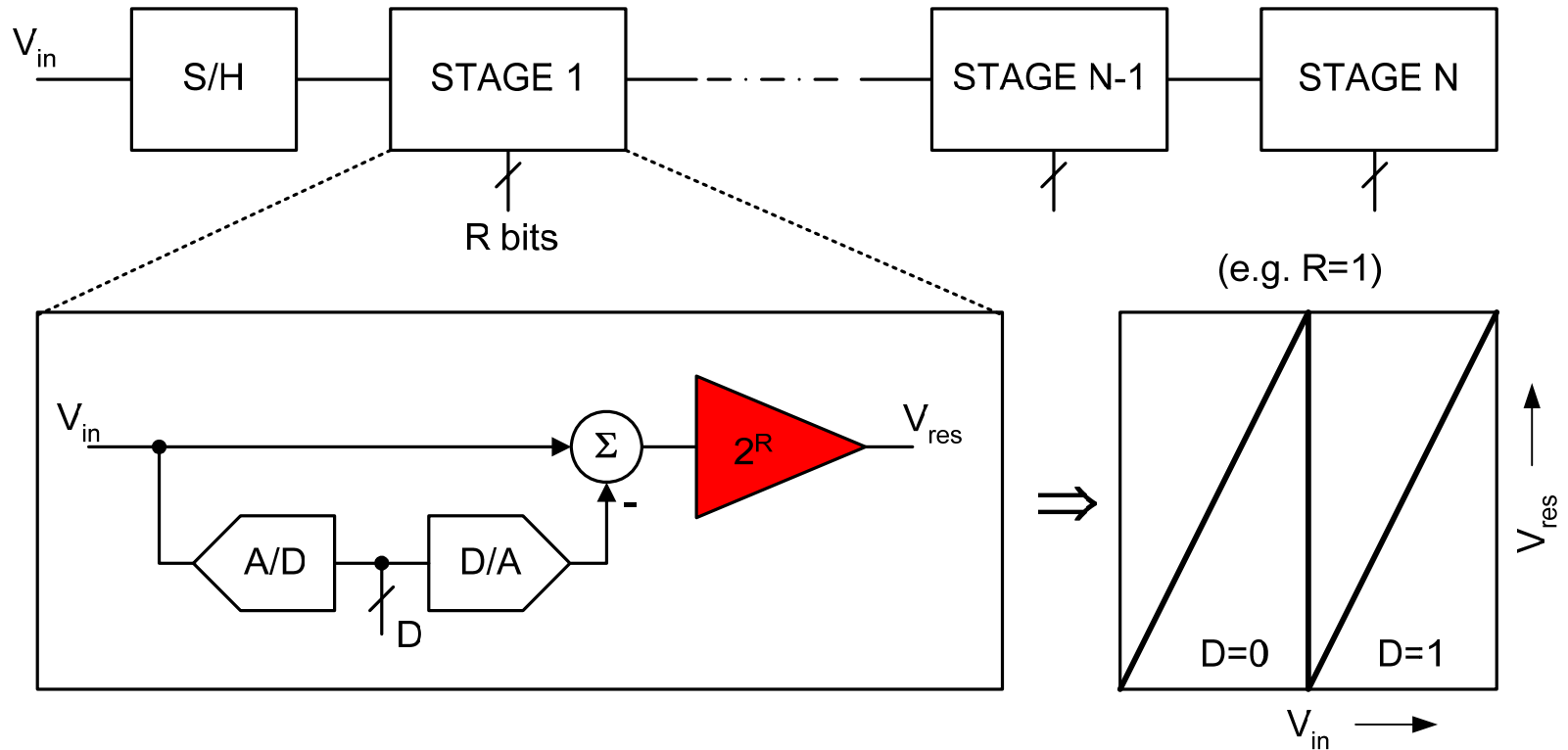
Leveraging Digital Assistance (1)



Leveraging Digital Assistance (2)

- Can correct deterministic, repeatable error using digital processor
- Important considerations
 - Impractical to correct for arbitrary errors
 - Must limit "sloppiness" through judicious analog design
 - Must be able to adjust correction functions over time
 - Errors will depend on operating conditions, circuit age, etc.

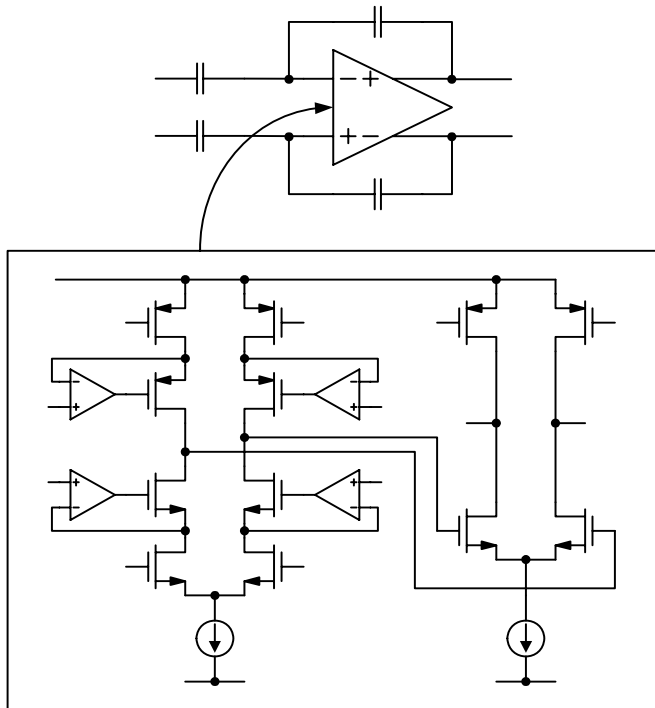
Example: Pipeline ADC



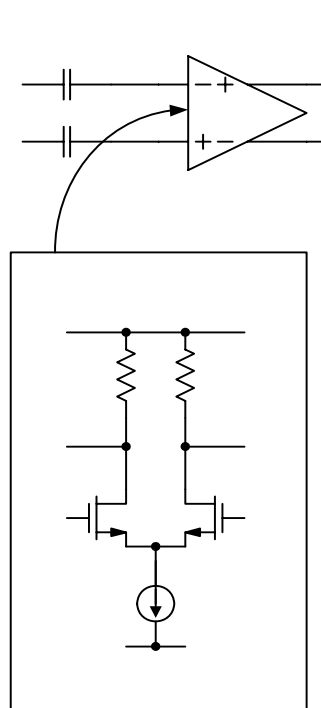
- Bottleneck: Highly linear gain element

Open-Loop Gain Element

Conventional Precision Amplifier

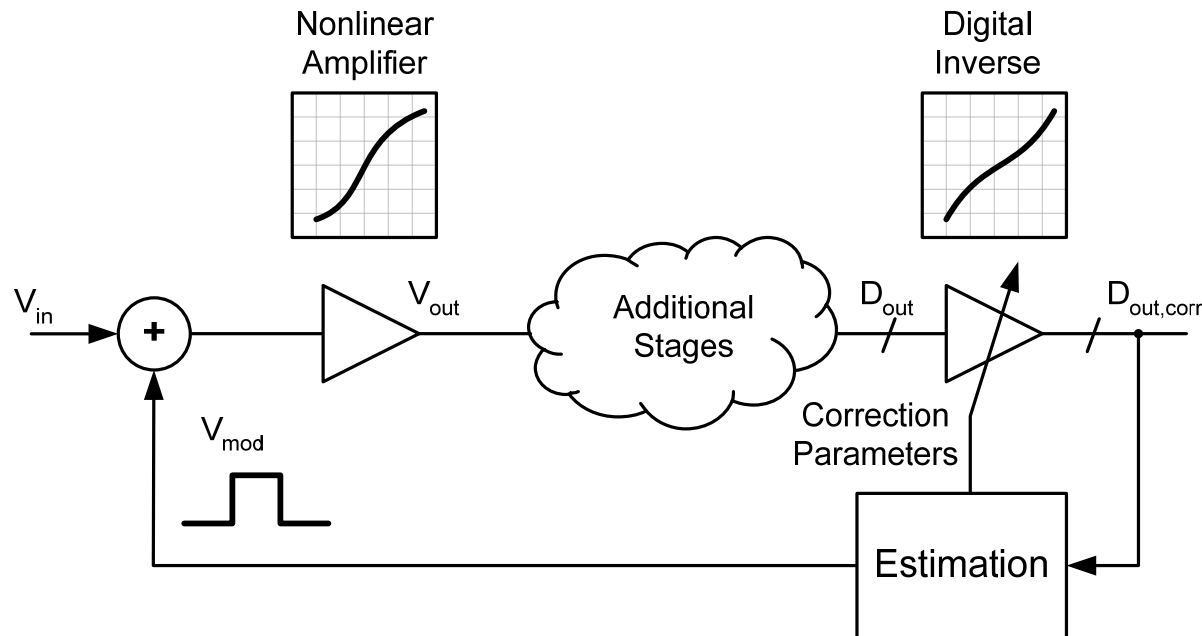


Open-Loop Amplifier



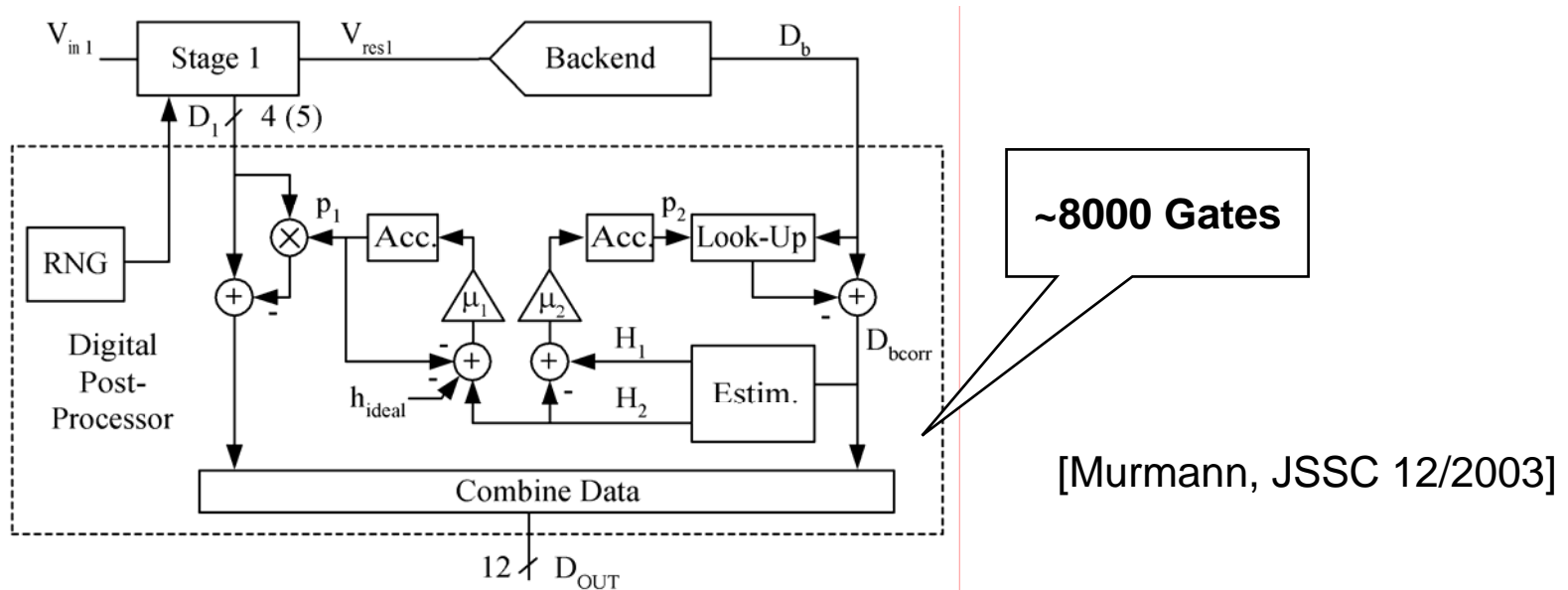
- + Lower noise
- + Increased signal range
- + Lower power
- + Faster
- Nonlinear
 - Use post-processor to linearize!

Digital Nonlinearity Correction



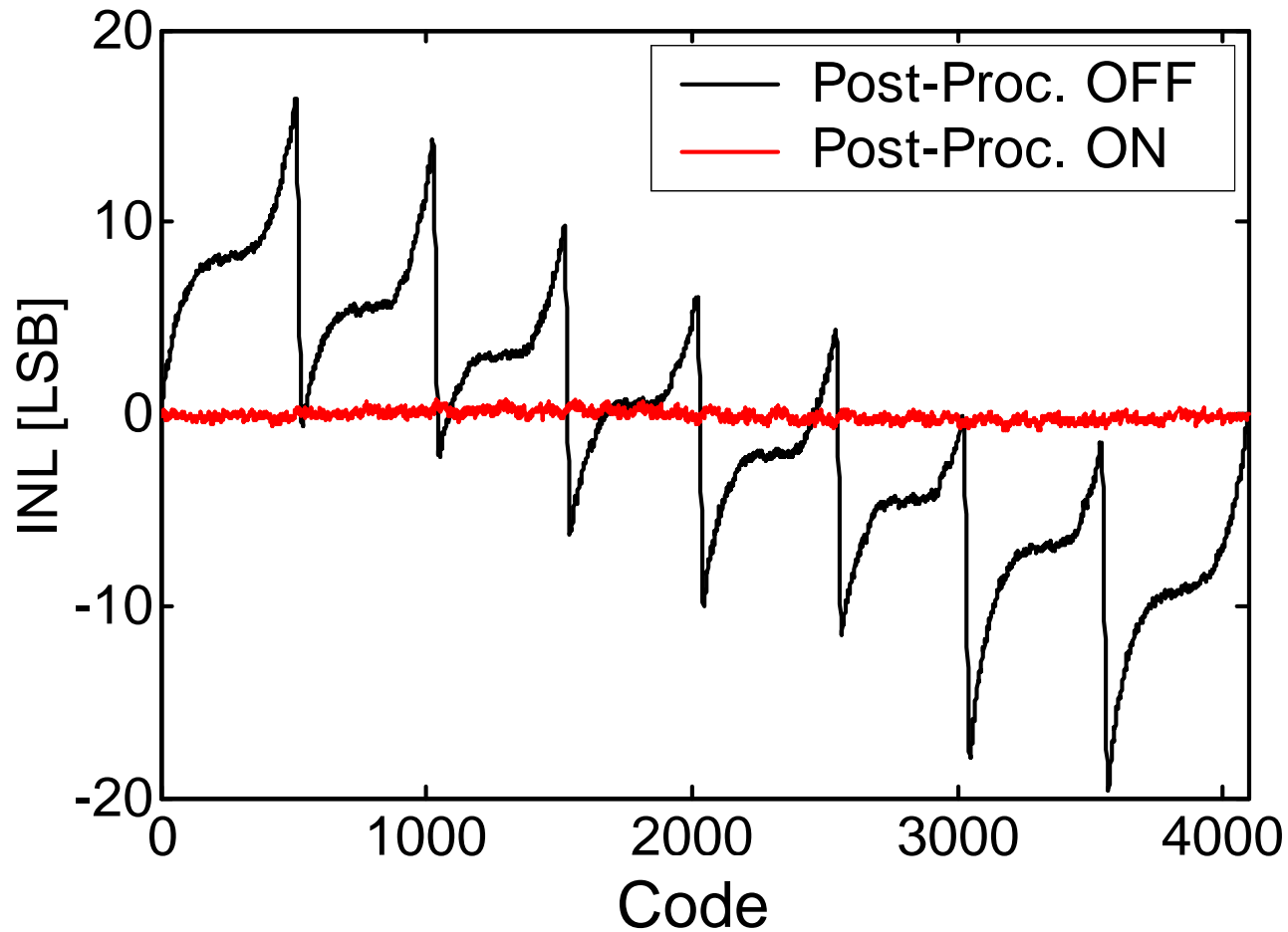
- Calibration of digital inverse is accomplished by adjusting parameters such that signal statistics at output are independent of V_{mod}
 - Algorithm continuously tracks variations in amplifier polynomial

Proof of Concept Prototype

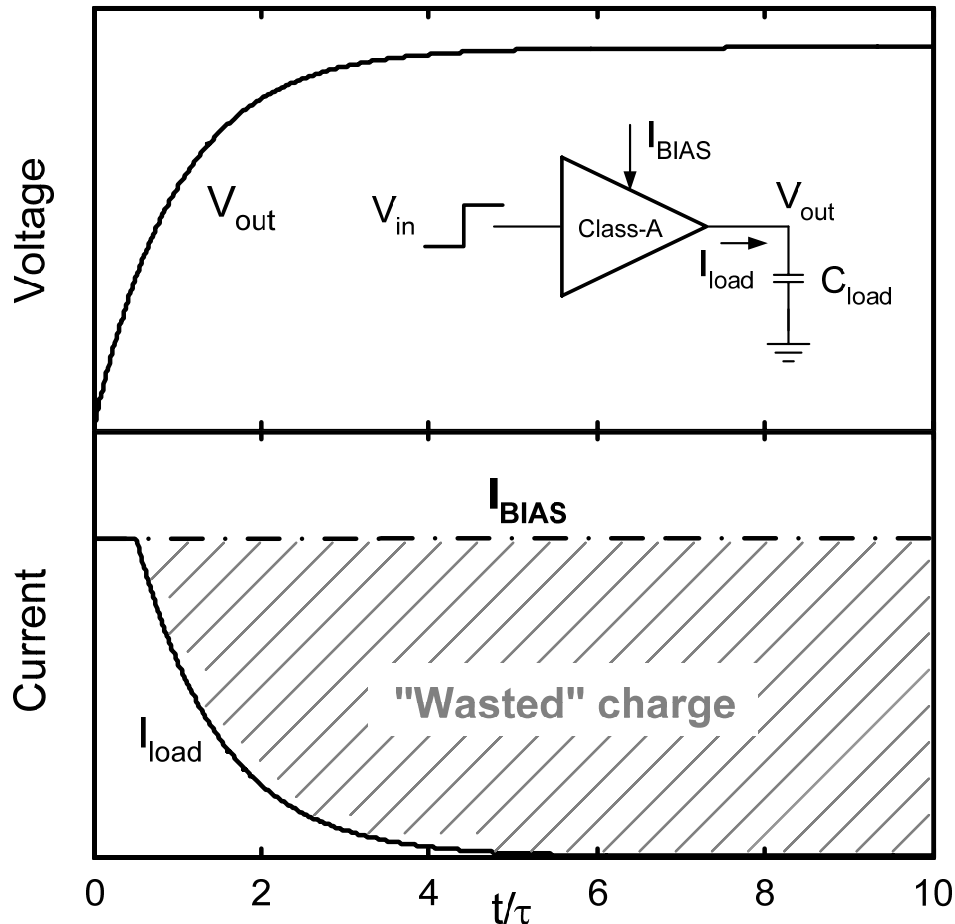


- Open-loop amplifier only in first, most critical stage
 - Amplifier power savings $\sim 4x$
- Judicious analog/digital co-design
 - Only two correction parameters (linear and cubic amplifier error)

Digital Linearity Correction

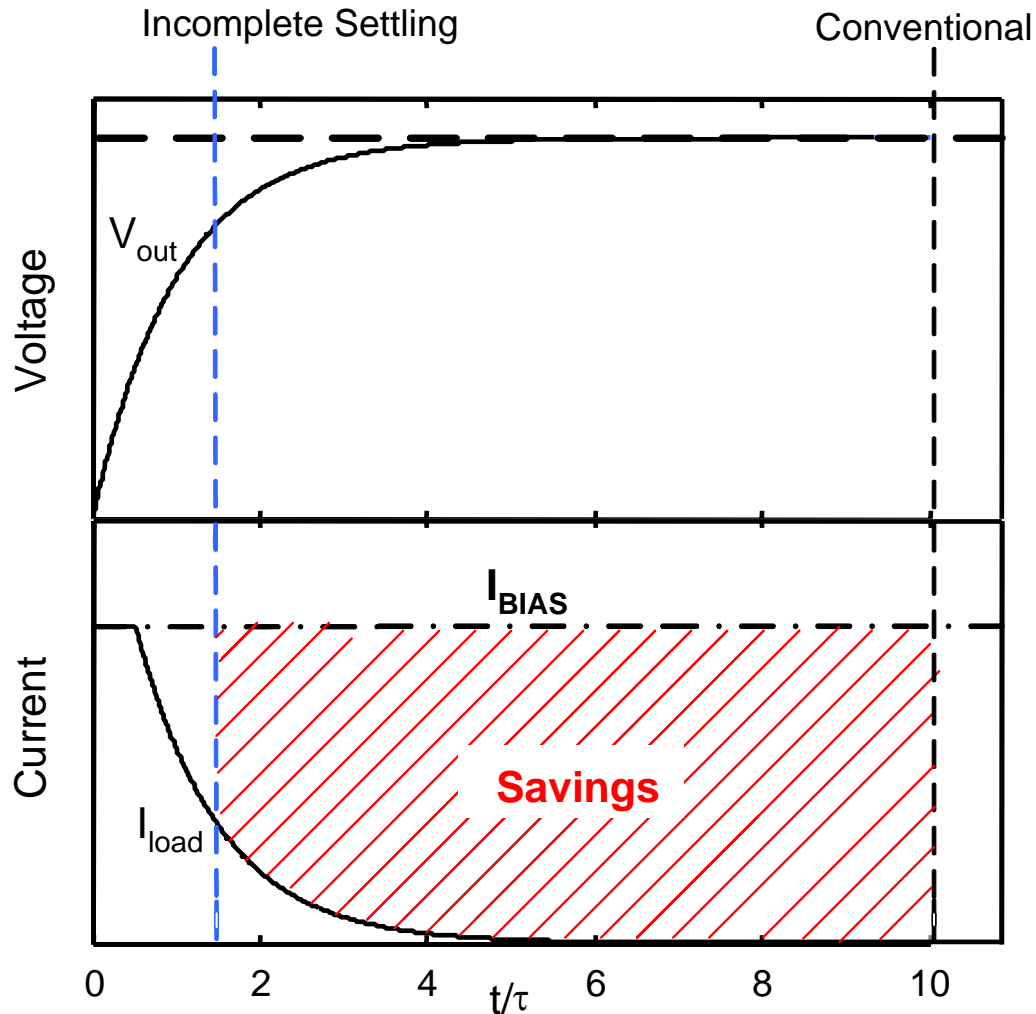


Amplifier Waveforms



- Typically settle to within small % error of final value
- Most of I_{BIAS} is shunted to ground through the amplifier for $t > 2\tau$

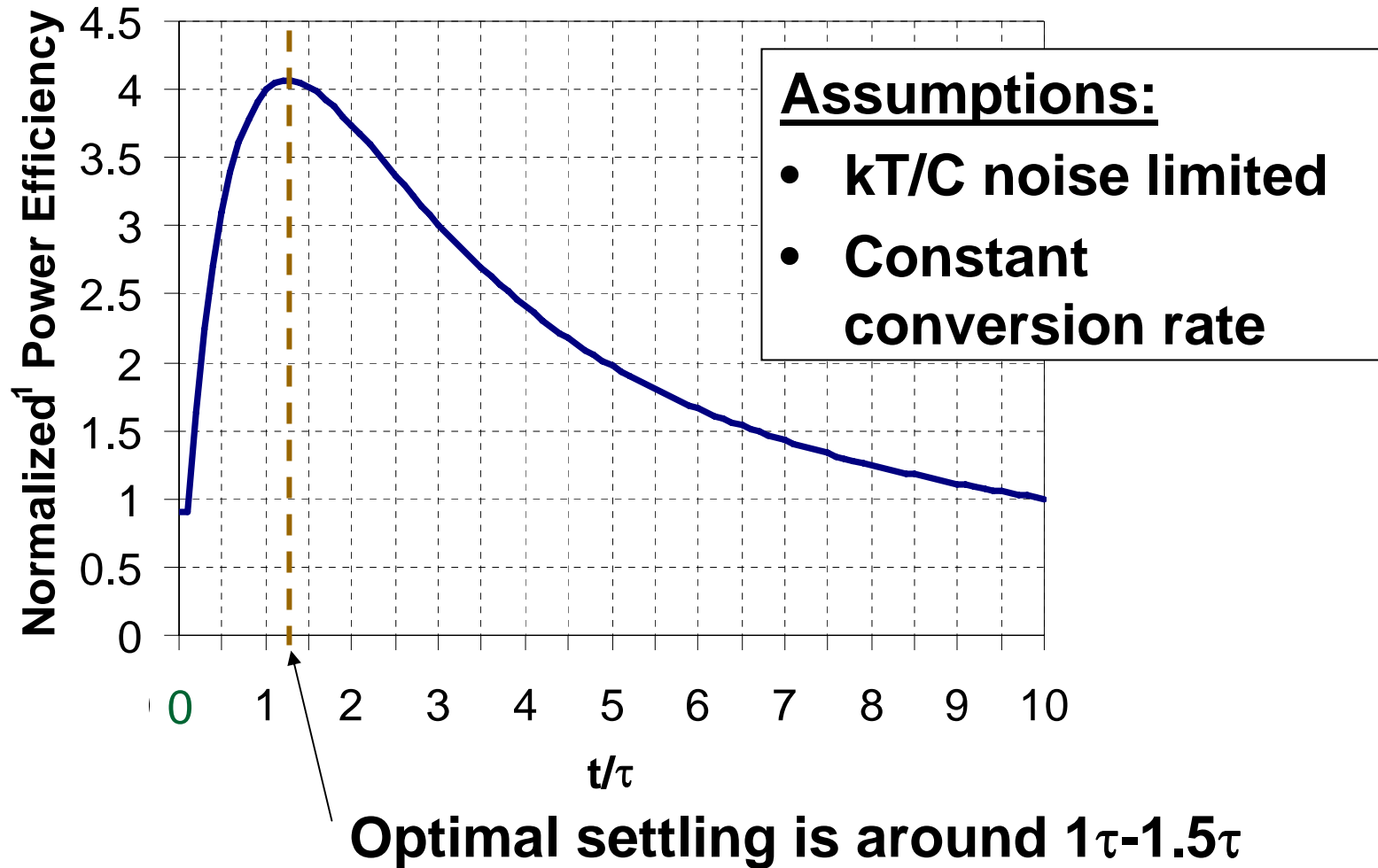
Exploiting Incomplete Settling



- Idea

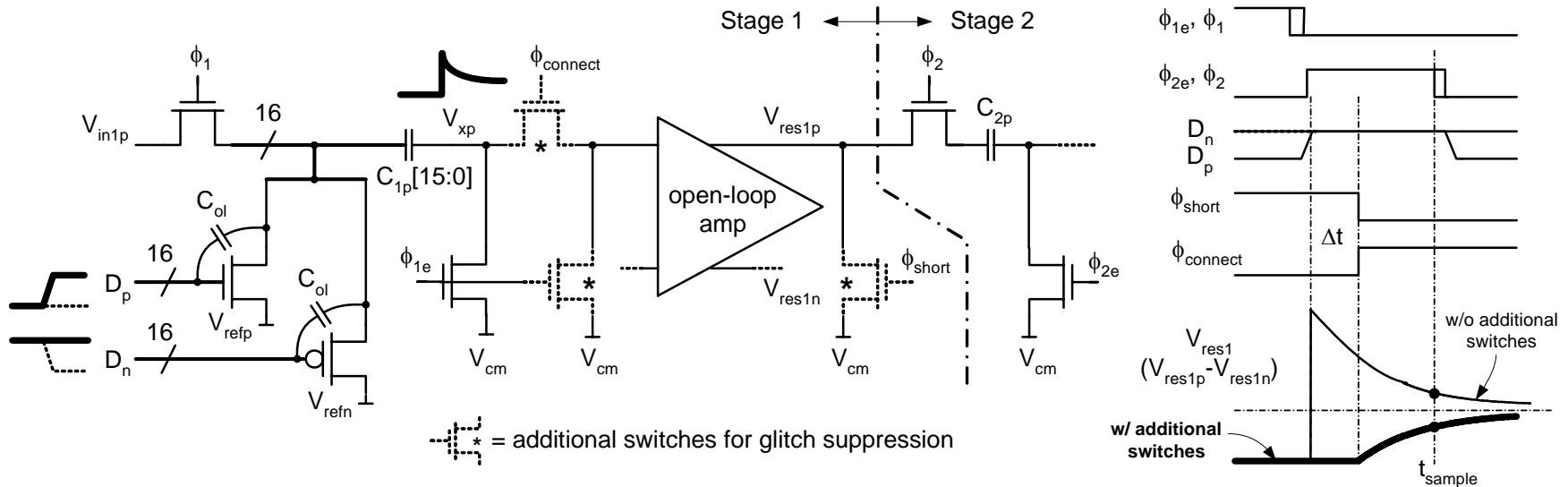
- Settle for only 1.5τ to improve power efficiency (or speed)
- Use digital processing to correct for settling error (in addition to nonlinearity)

Power Efficiency versus Settling



¹Normalized to power at 10τ settling.

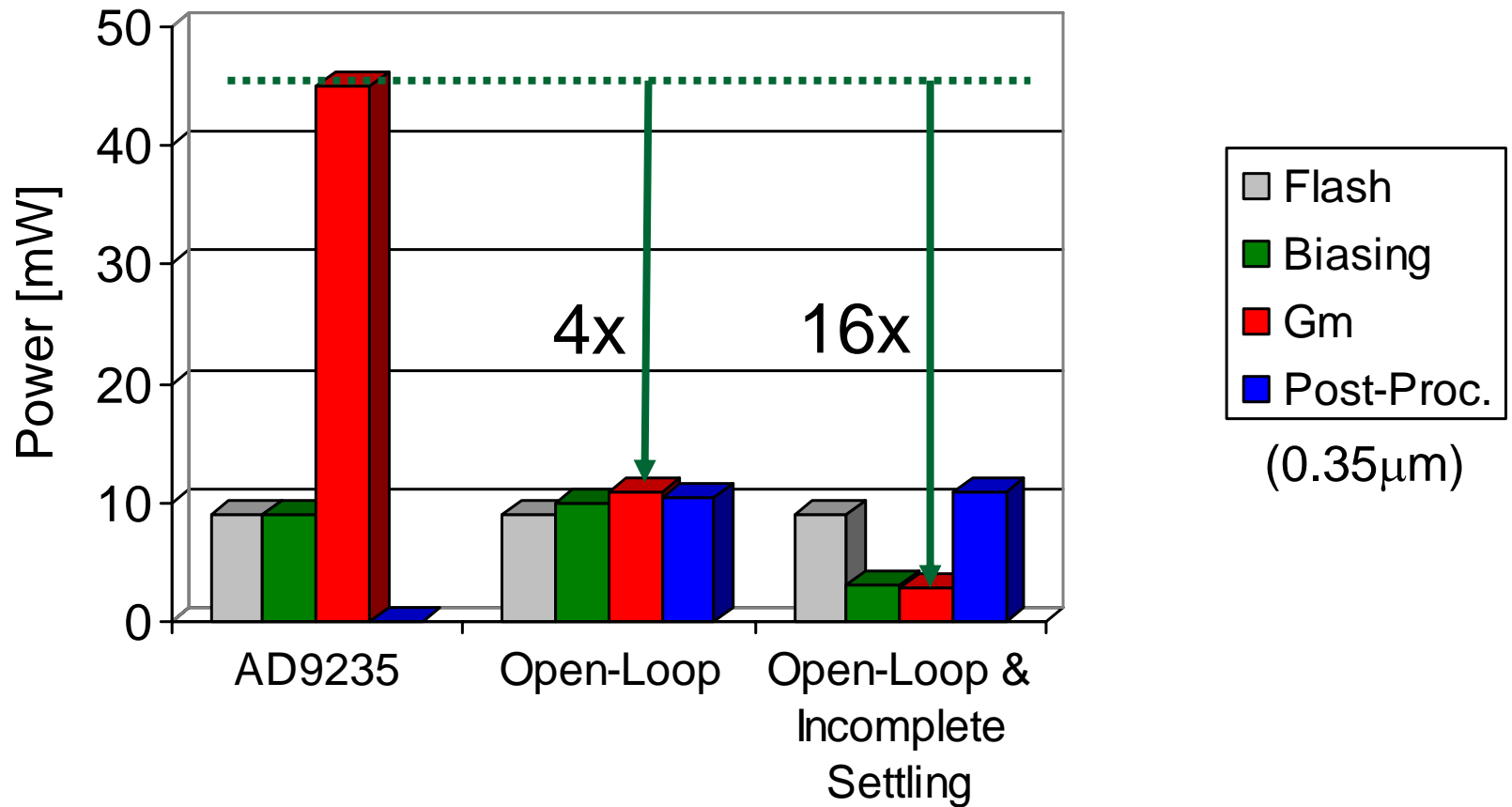
Proof of Concept Circuit



[Iroaga & Murmann, VLSI 2006]

- Judicious analog design ensures that incomplete settling error is linear (or only weakly nonlinear)
 - Very easy to correct!

Pipeline Stage Power Breakdown

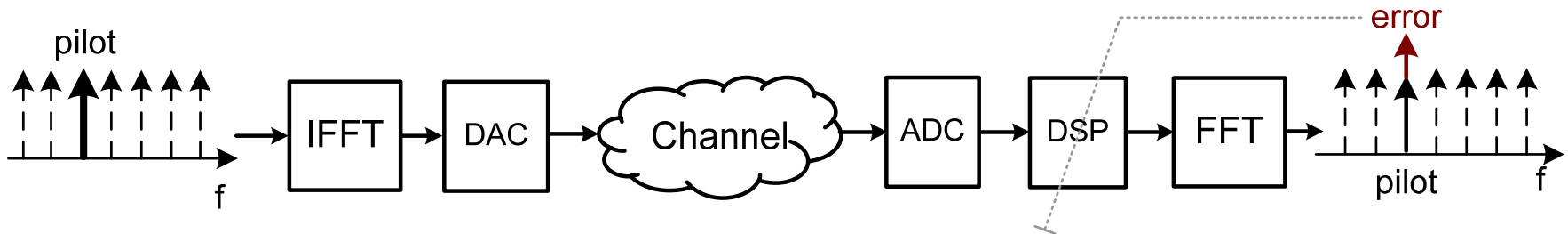


Calibration Problem Revisited

- The "sloppier" we make the analog portion of the ADC, the more parameters we need to estimate and track
 - Can become quite complex or even impossible without disturbing normal ADC operation
- Idea: "System Embedded" postprocessing and calibration of ADC
 - Leverage redundancy and knowledge of certain input signal properties to estimate ADC errors
 - Re-use existing system resources for ADC calibration

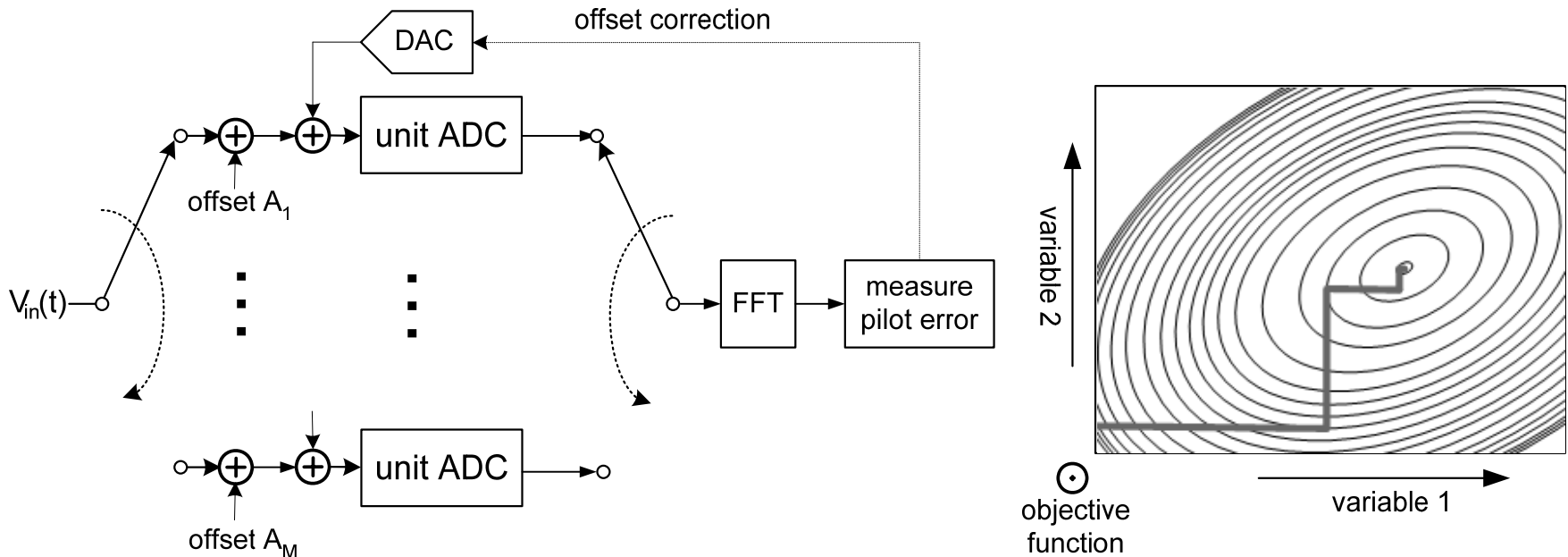
Embedded ADC Calibration for OFDM

[Oh and Murmann, to appear, IEEE TCAS1]



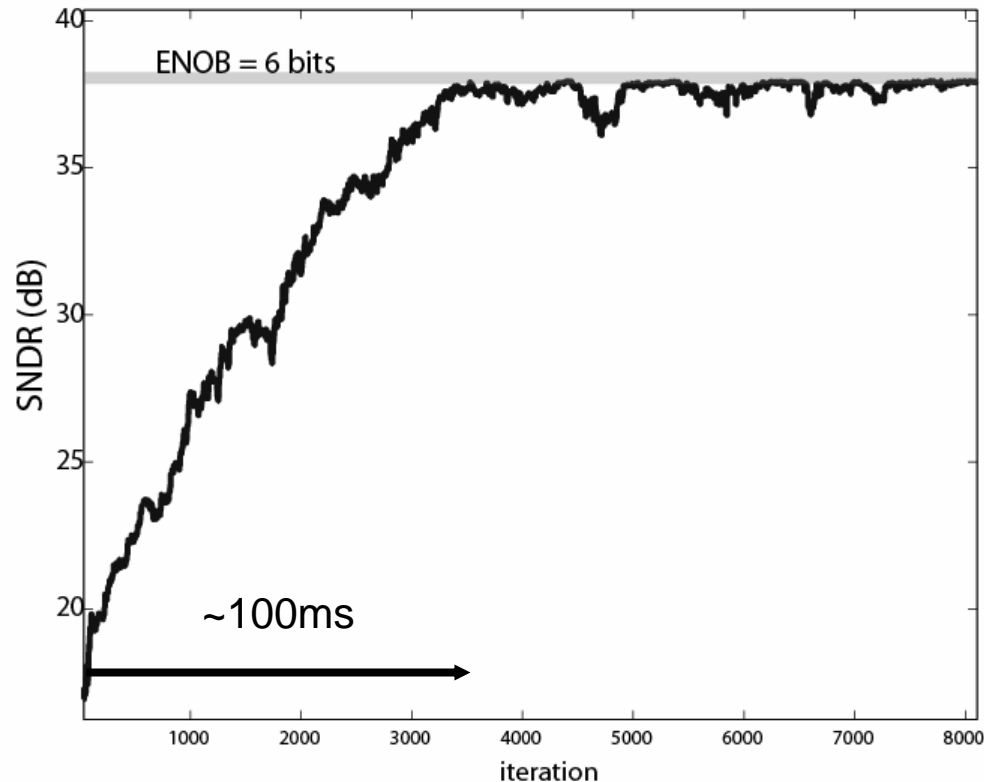
- Communications protocol uses "pilot tones" to measure and equalize RF channel nonidealities
- Why not use these pilots to "equalize" ADC?
 - Errors in pilot signals can be used to estimate correction parameters for sloppy ADC
- Example: Offset correction in time interleaved ADC

Offset correction in Time Interleaved ADC



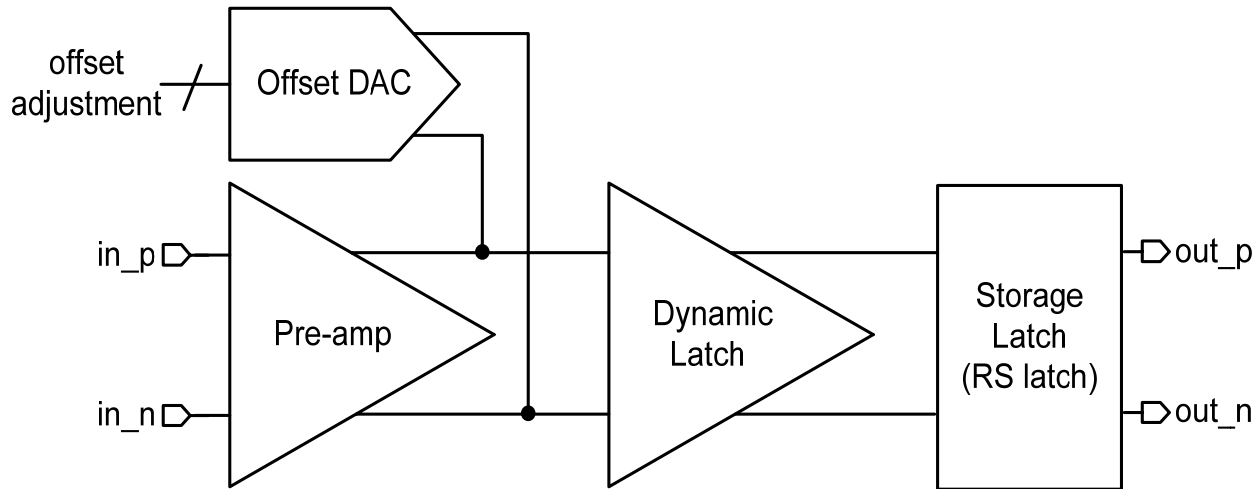
- Offset corrections are adjusted sequentially to minimize errors seen in pilot tones
 - Coordinate descend algorithm

Typical Learning Curve



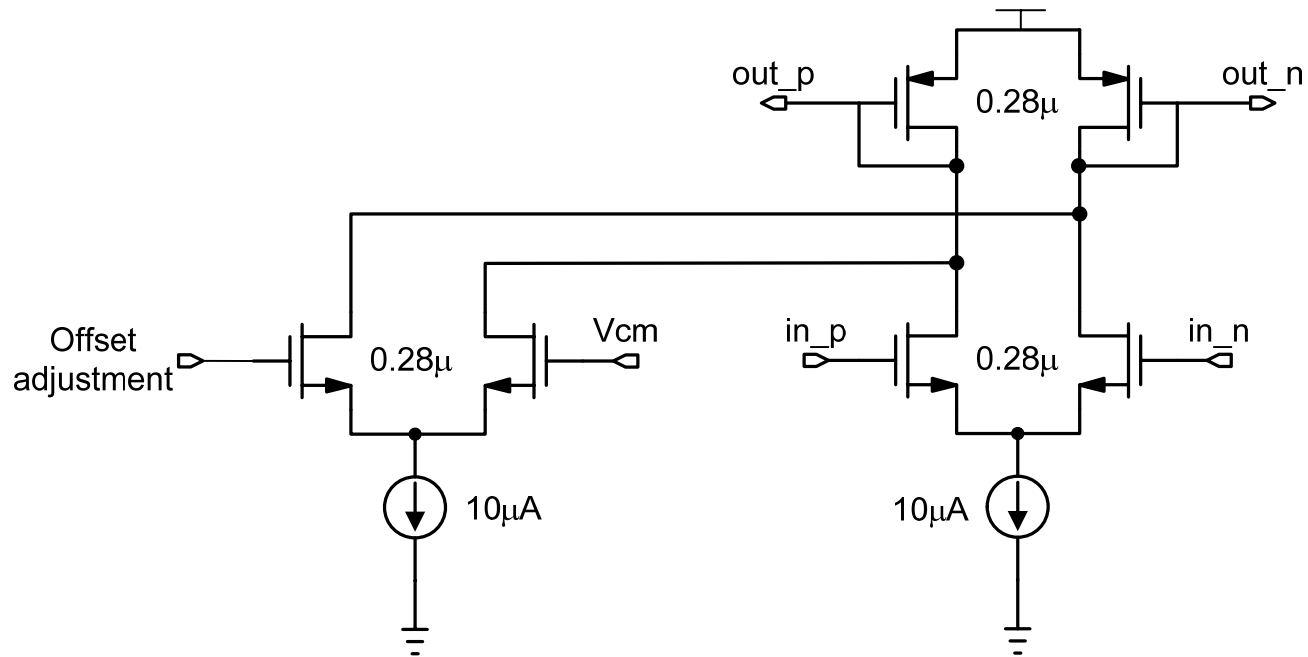
- Steady state ripple due to communication channel noise
 - Tradeoff: Ripple versus convergence rate
- $\text{ENOB} \cong 5.8\text{bits}$ in AWGN channel with $\text{SNR} = 20\text{dB}$

Comparator Circuit



- Fully differential architecture
- Low gain/low power pre-amp, primarily for common mode rejection
- Dynamic latch with positive feedback for fast comparison

Pre-amp with Offset Adjustment



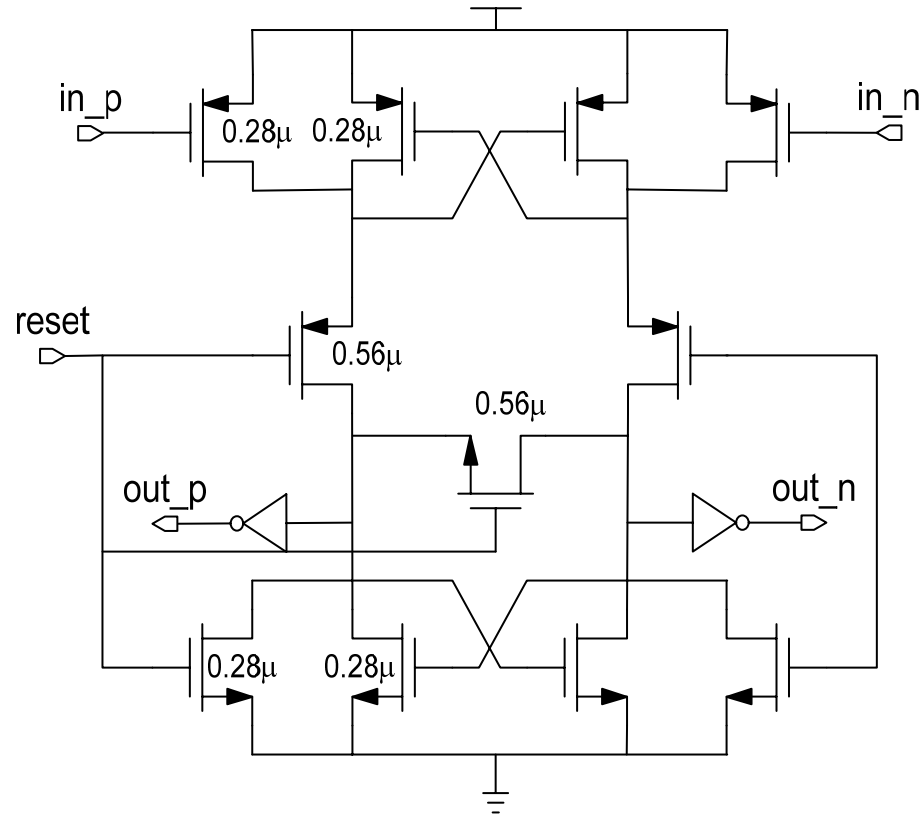
- Offset DAC

- Current mode
- Offset correction range ± 8 LSB

- Pre-amp

- Low gain (~ 2)
- CMRR > 20

Dynamic Latch

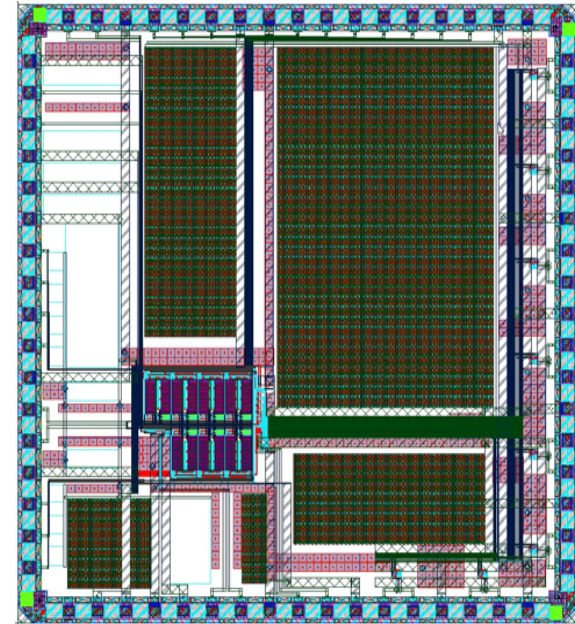


- Calibration allows use of near minimum width devices for low power

Layout



(a) ADC Core



(b) full chip

- Core area: $640\mu\text{m} \times 550\mu\text{m}$ ($0.18\mu\text{m}$ CMOS)

Estimated Power (Post-Layout)

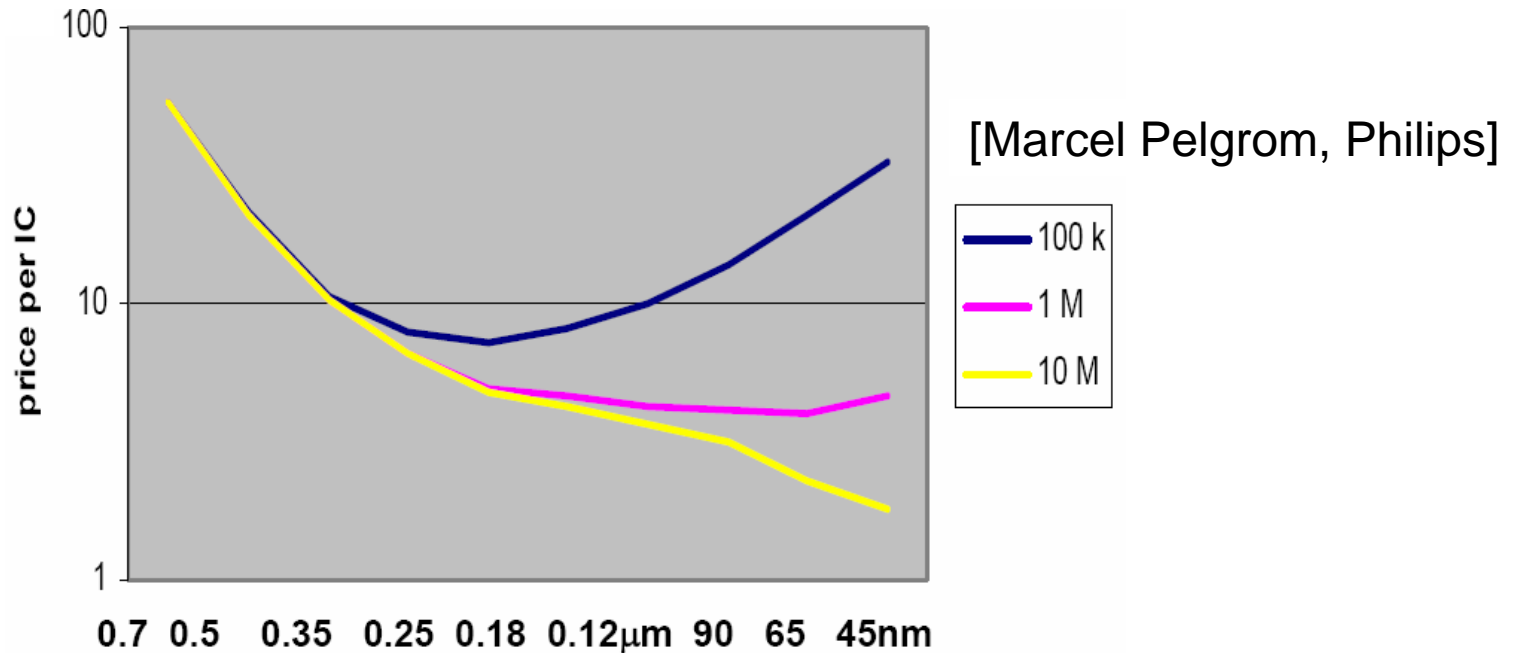
- 500MS/s, 6-bit ADC

	Power (mW)
Digital	9.0
Analog	3.6
Clock	3.6
Calibration (estimated)	0.4
Total	16.6

An Interesting Hike Lies Ahead...



Cost – The "Real" End of The Roadmap?



- Reference point: 30 mm² die in 0.12μm CMOS

Conclusions

- Analog design in modern IC technologies is and always will be challenging
 - This is what keeps our job interesting...
- New technologies means new solutions
 - Must continue to develop low voltage design techniques
 - Must continue to leverage digital capabilities for analog performance enhancements
- Based on current roadmap, there is no fundamental reason why analog couldn't be implemented in "digital" technologies of the near future
- Interesting questions
 - Will high performance digital circuits survive scaling?
 - Can the IC industry continue to benefit from scaling despite the large anticipated wafer & mask costs?

Acknowledgements

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