60-GHz CMOS Transceivers: Why and How?

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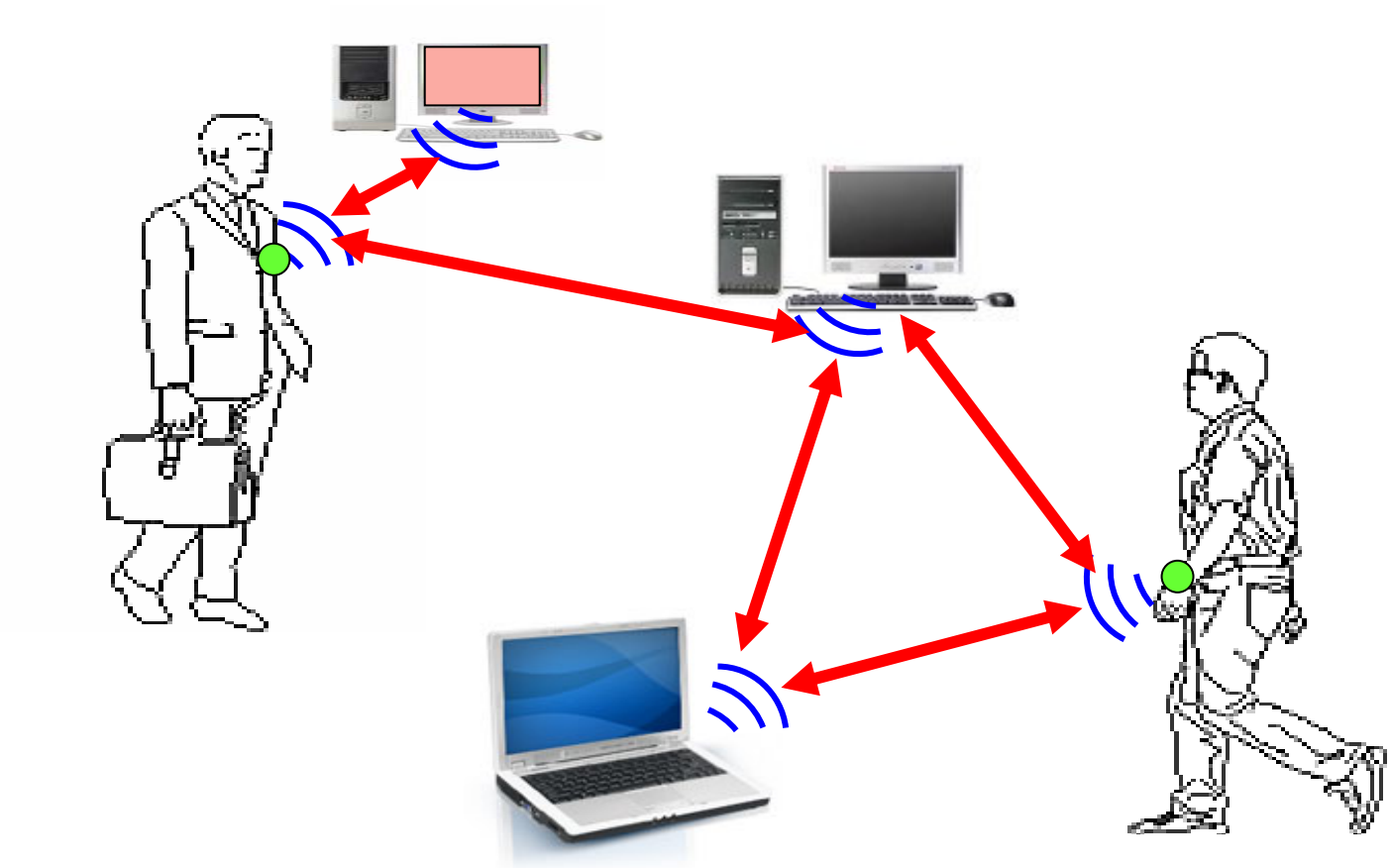
Outline

- Introduction
- Receiver Front End
- Transmitter Front End
- Frequency Divider
- Reflections
- Conclusion

Why 60 GHz?

- 7 GHz of Unlicensed Band
- Possibility of Realizing (Multiple) On-Chip Antennas:
  - Low-Cost Packaging
  - Differential Operation → Higher Output Power
  - No Need for T/R Switch
  - No Need for AC Coupling
  - No Need for High-Frequency ESD Devices
- Possible Applications:
  - Gb/s Networks, e.g., Video Streaming
  - Highly-Interconnected Networks

Highly-Interconnected Networks



Why CMOS?

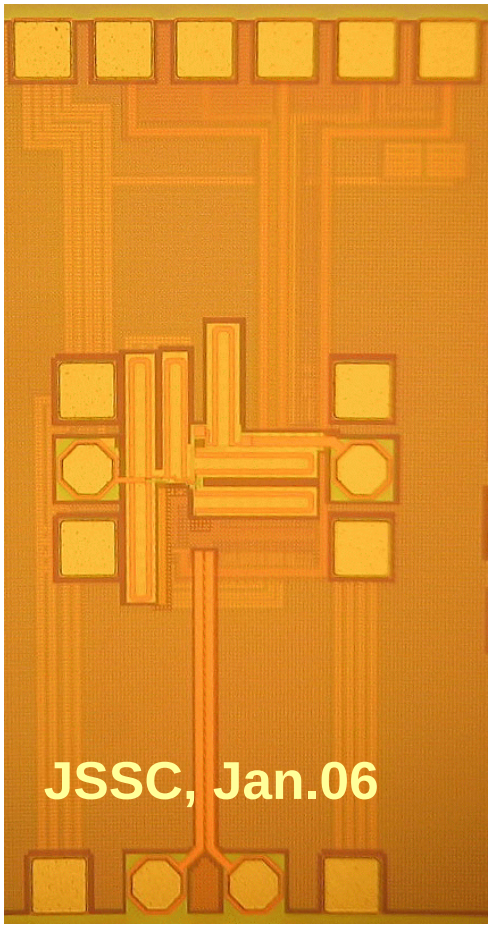
- **Need Complex Modulation Techniques:**
  - **OFDM**
  - **QAM**
  - **Frequency Hopping?**
- **Need Sophisticated Analog Calibration:**
  - **I/Q Matching at 60 GHz?!**
  - **Wideband Analog Baseband Filters**
  - **Multitude of High-Speed ADCs**
- **Large Fractional Bandwidth (>10%):**
  - **Several Staggered High-Q Signal Paths**
  - **Multiple VCOs and Tuned Dividers**

Challenges

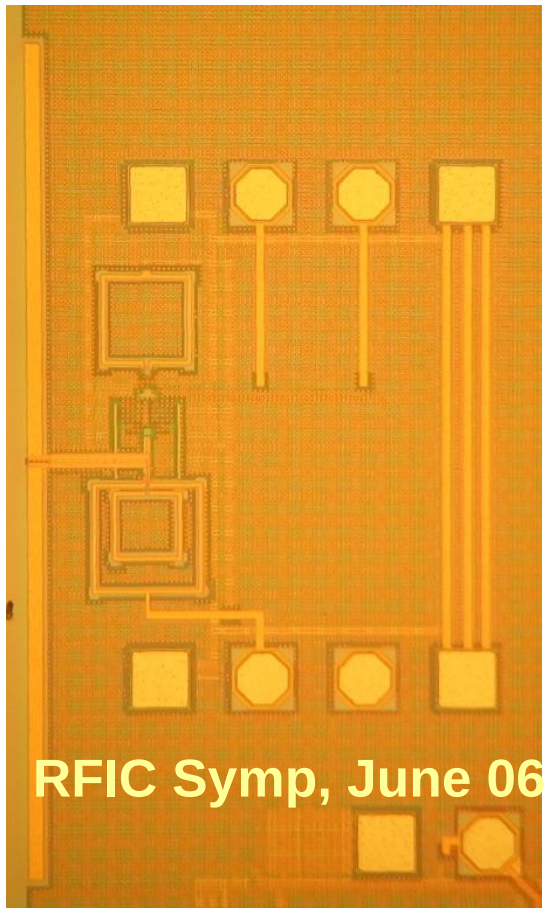
- **Limited transistor speed → Need for inductors and transmission lines.**
- **Inductor footprints → Long interconnects**
- **Inductor Q's tend to saturate around 25.**
- **Varactor Q's likely to be lower than inductor Q's.**
- **Lossy on-chip antennas → Beamforming**
- **Passive and active device modeling**
- **Gain and phase mismatches, etc.**

Transceiver Building Blocks

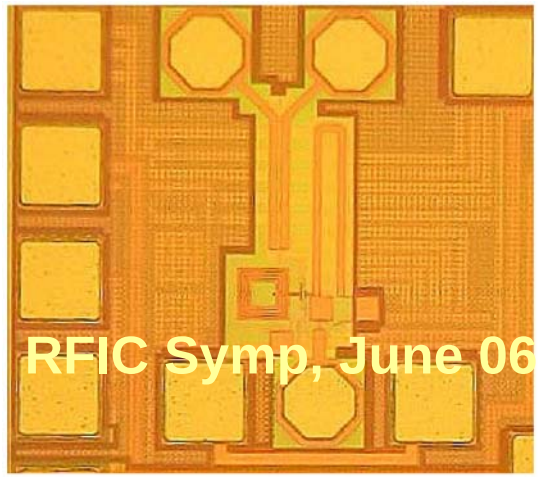
Receiver Front End



Transmitter Front End

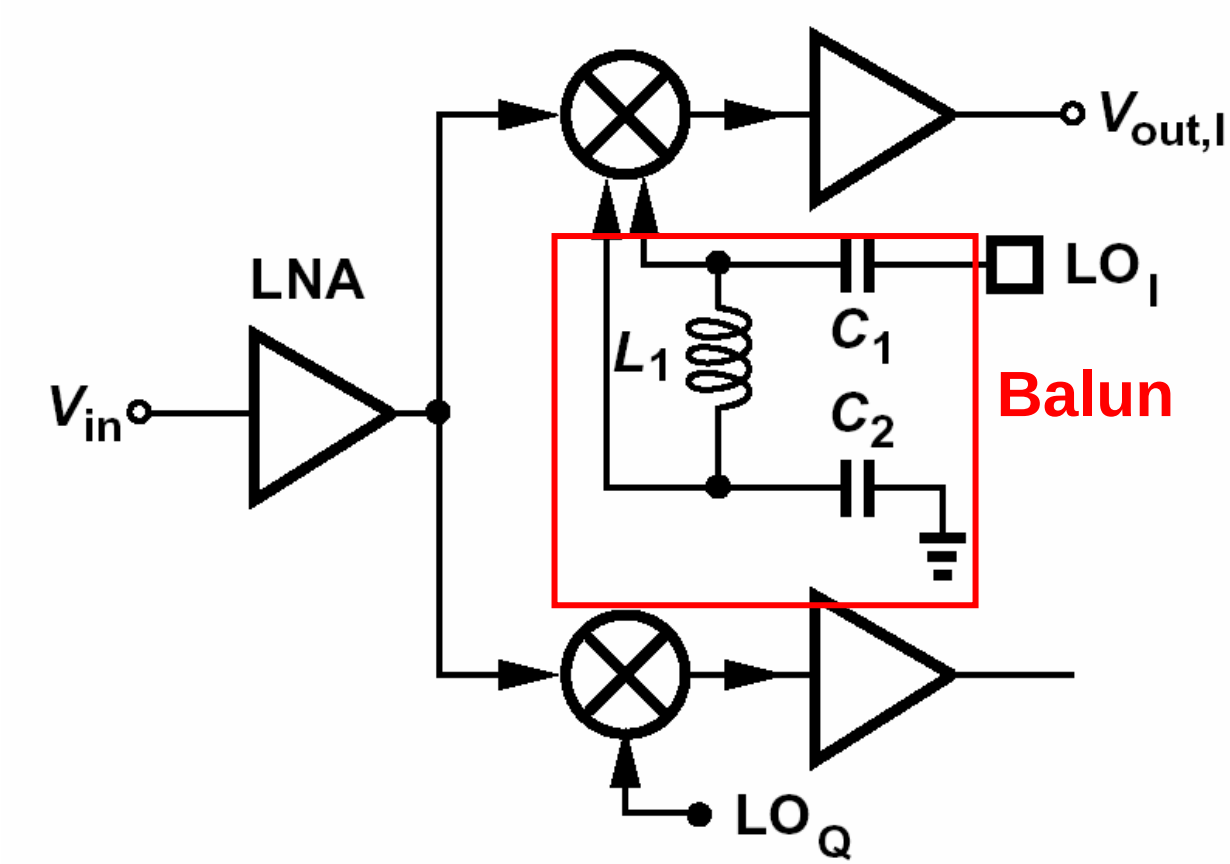


Frequency Divider

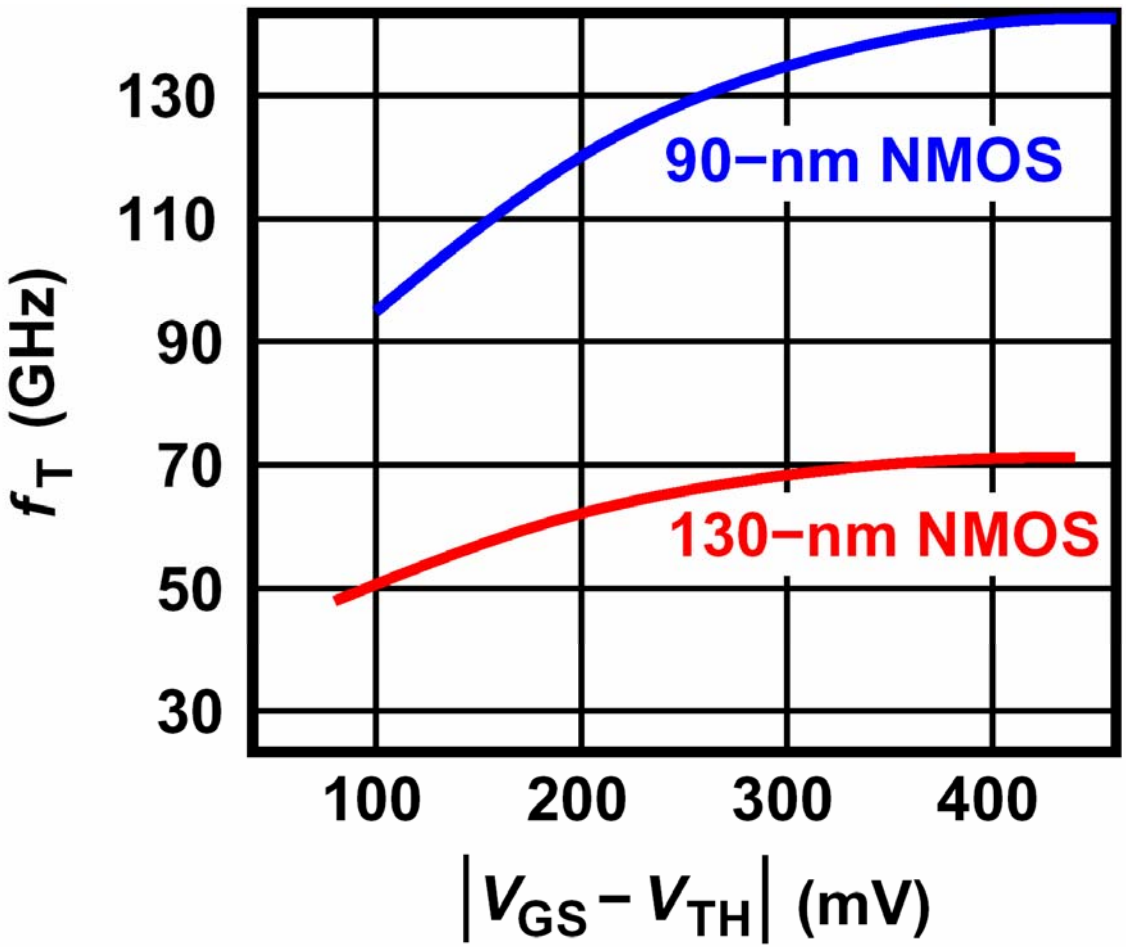


Designed in 0.13-μm CMOS; migrating to 90-nm process.

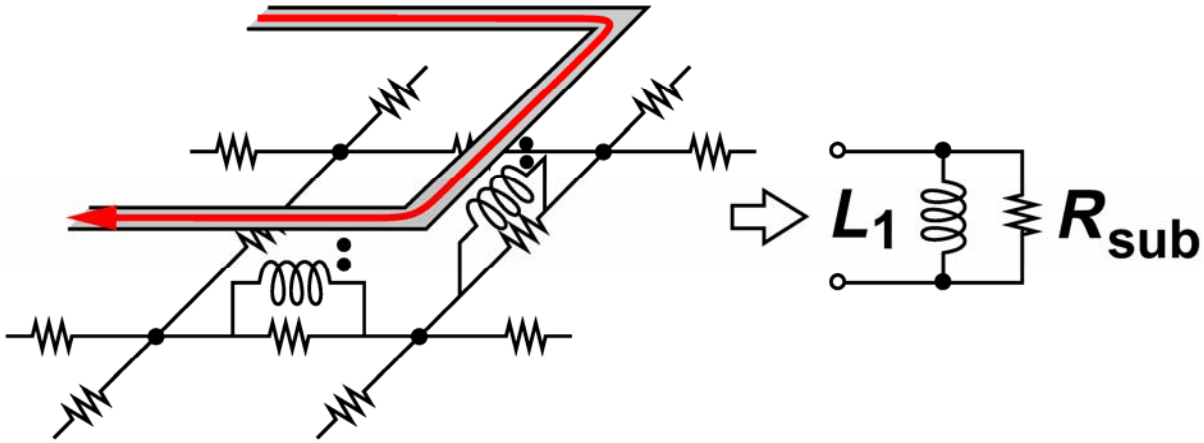
Receiver Architecture



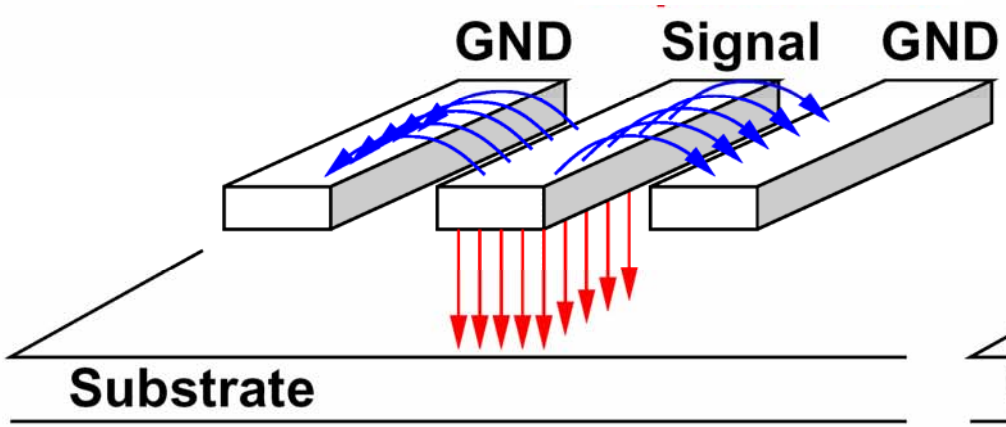
Raw Speed of MOS Devices



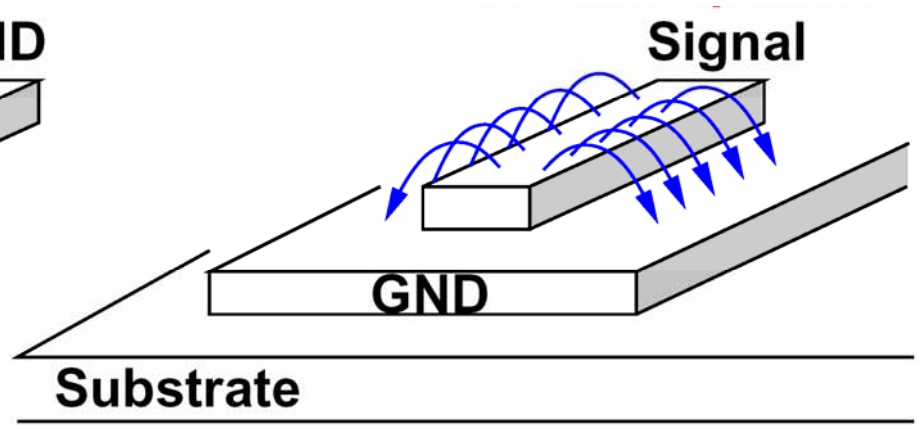
Spiral Inductors vs. Transmission Lines



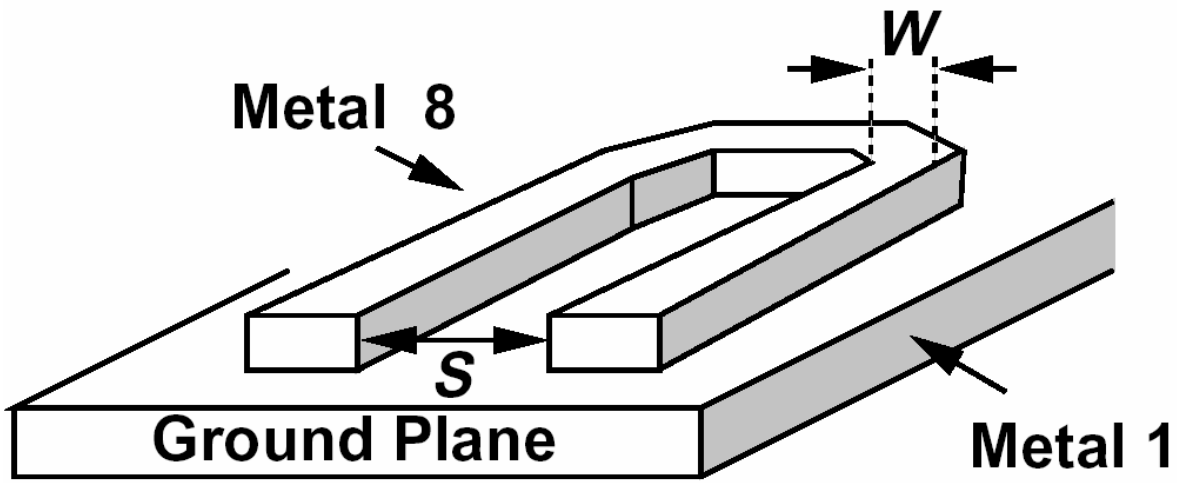
Coplanar Line

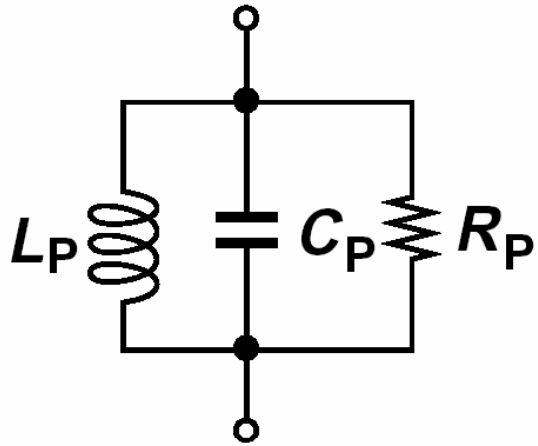


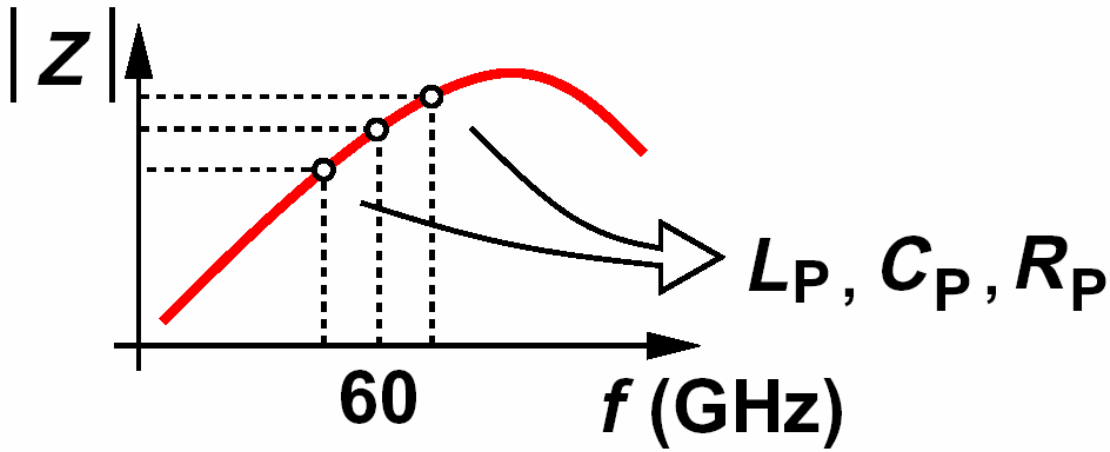
Microstrip Line



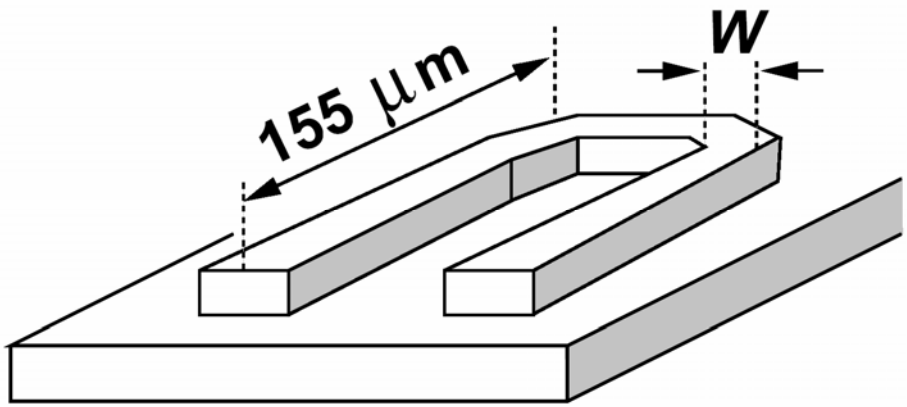
Folded Microstrip

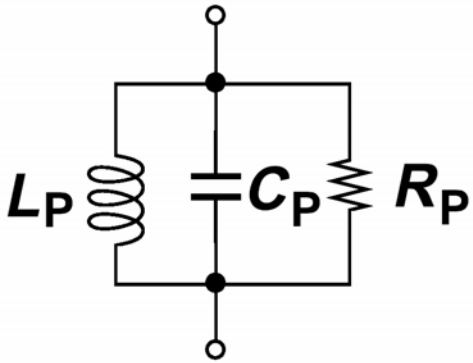


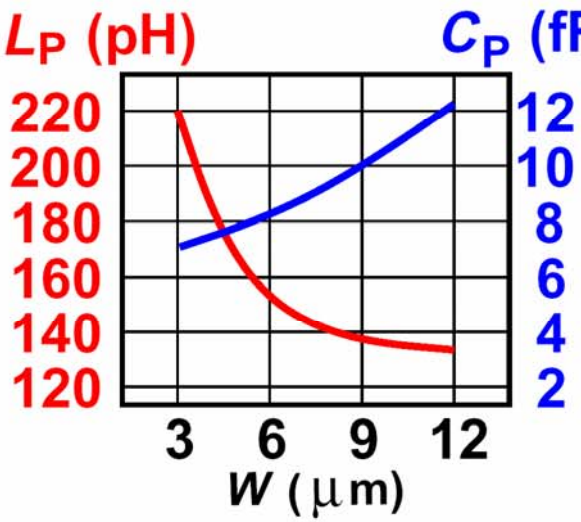


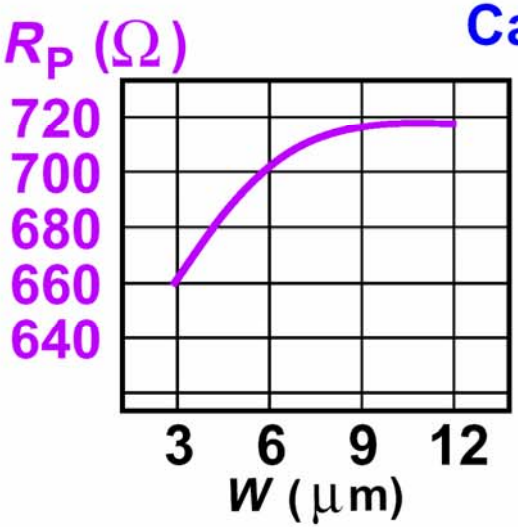


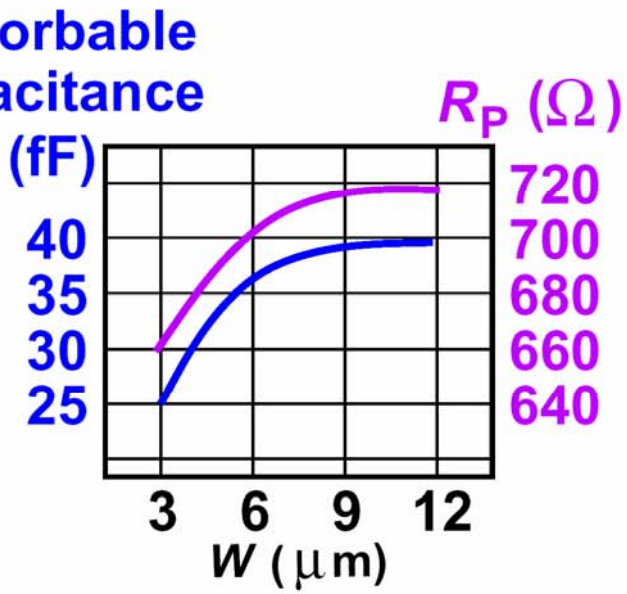
Choice of Linewidth



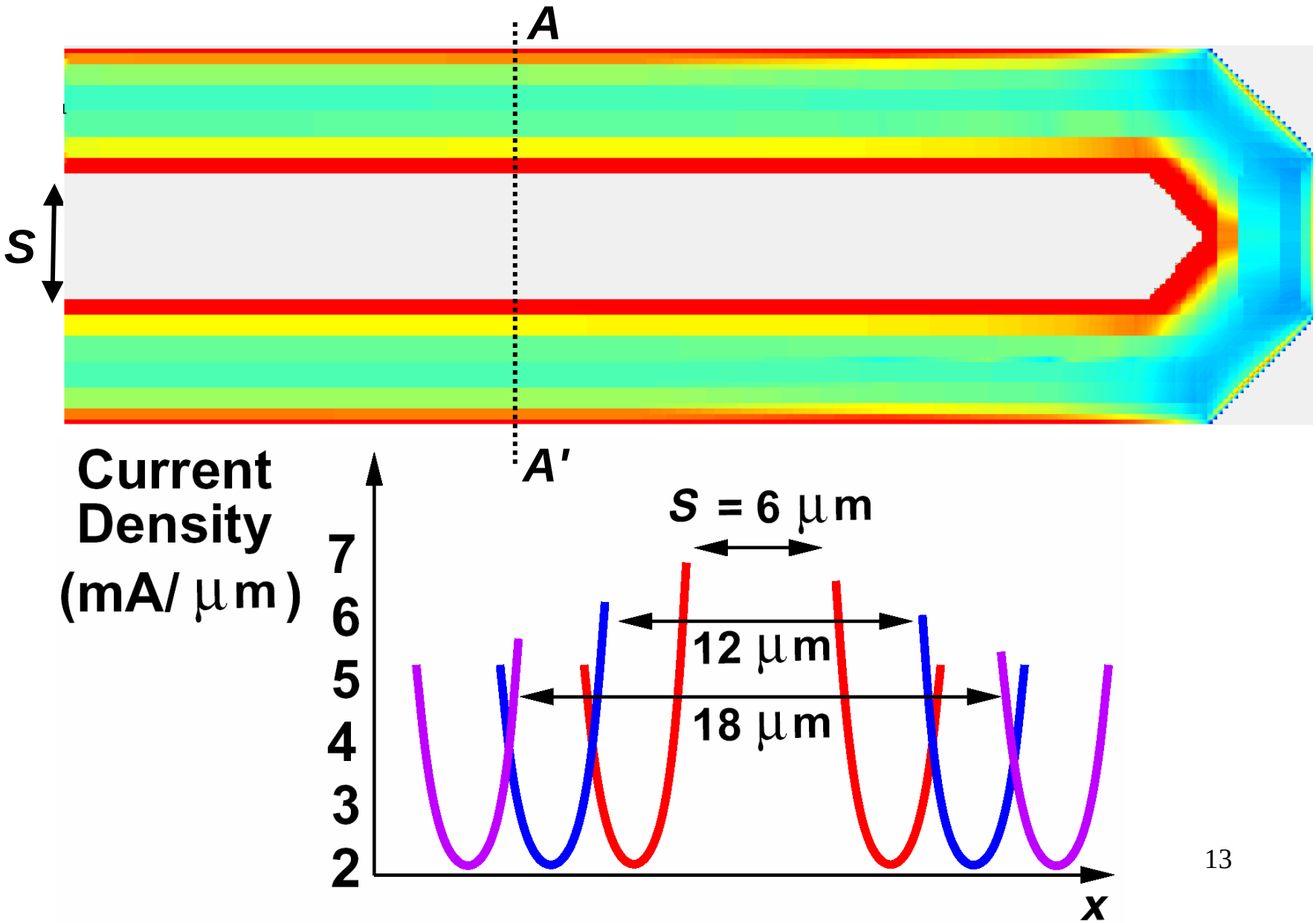








Choice of Line Spacing



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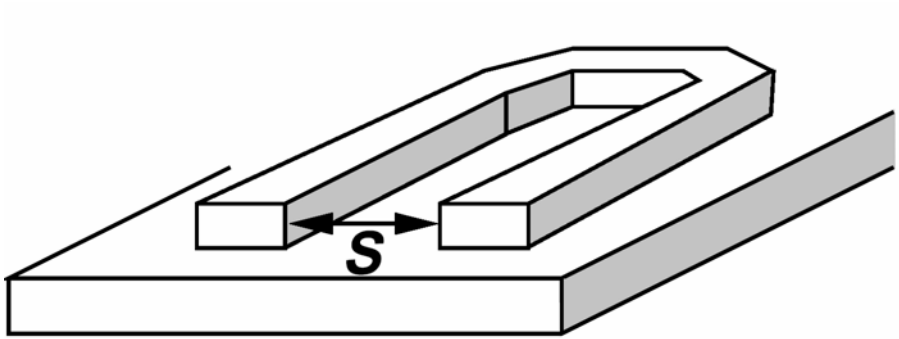
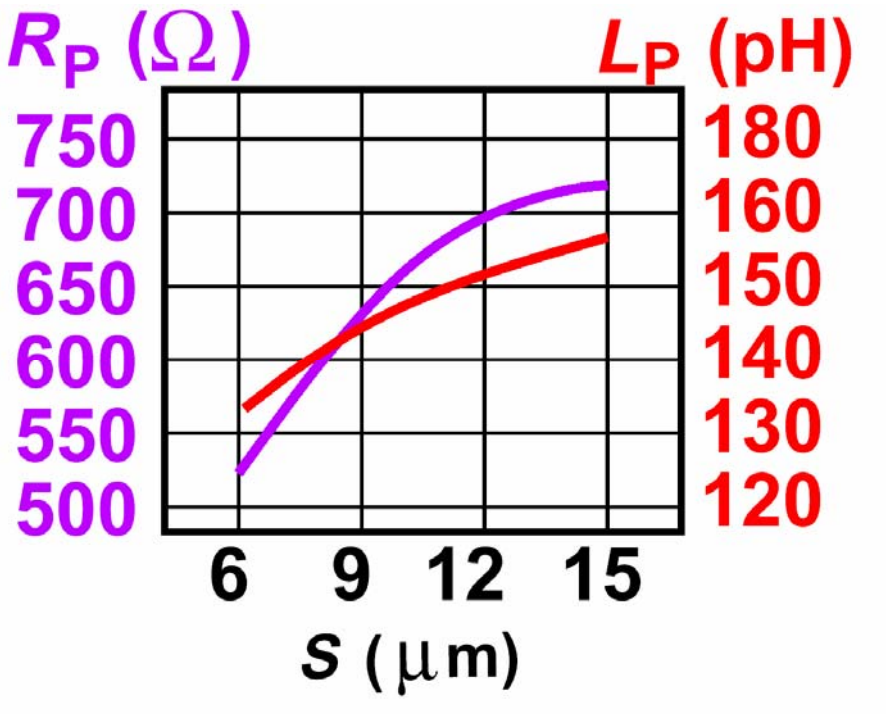
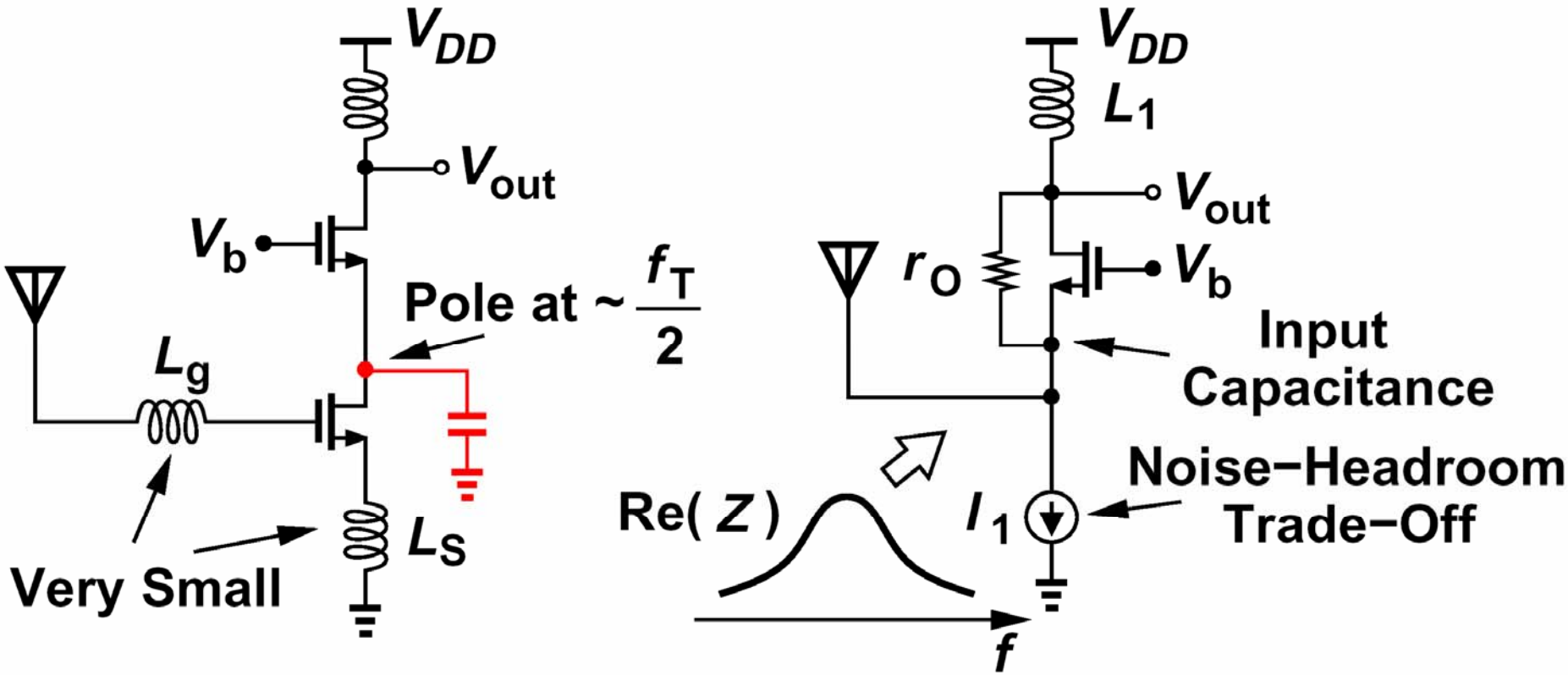
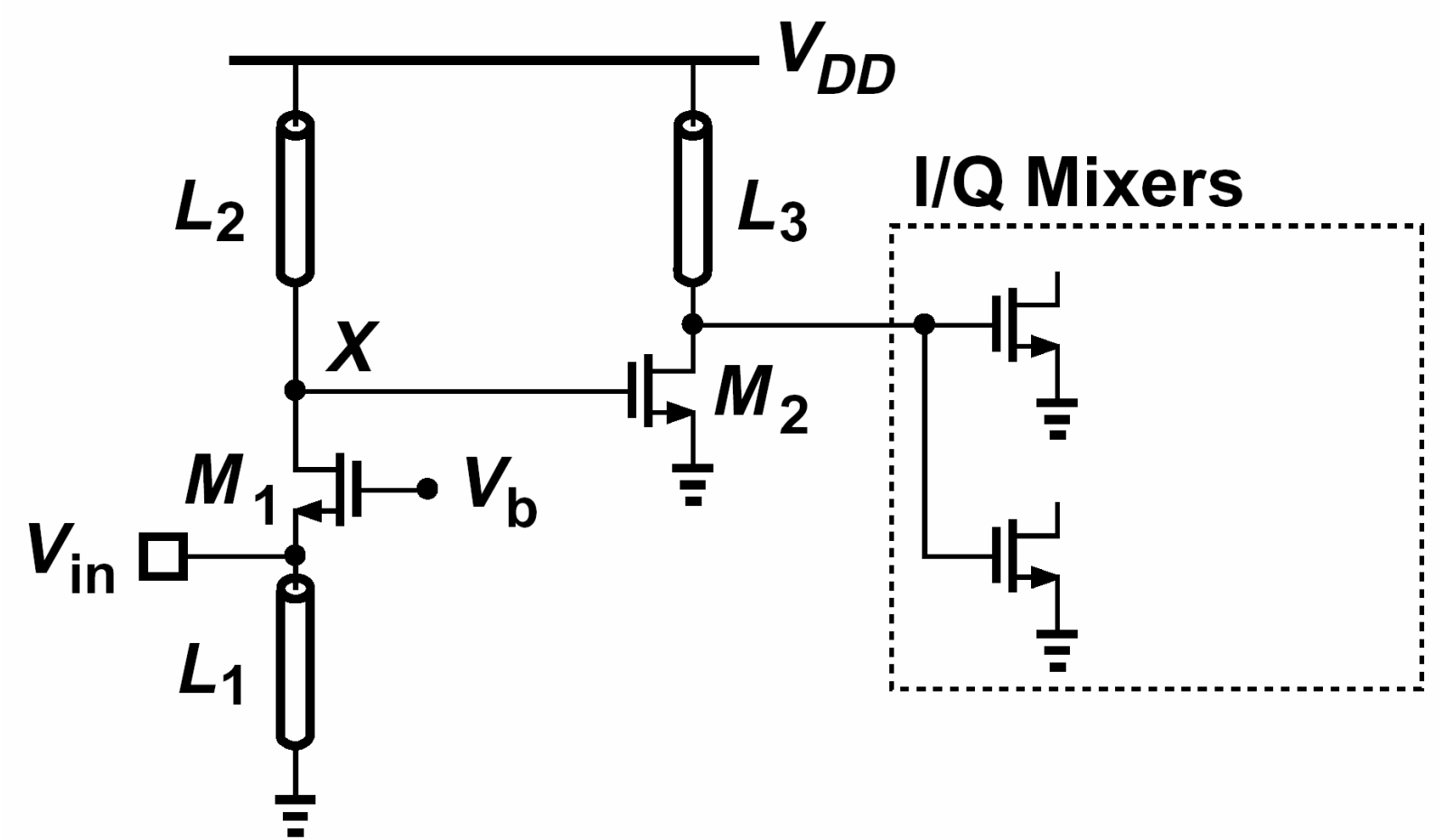




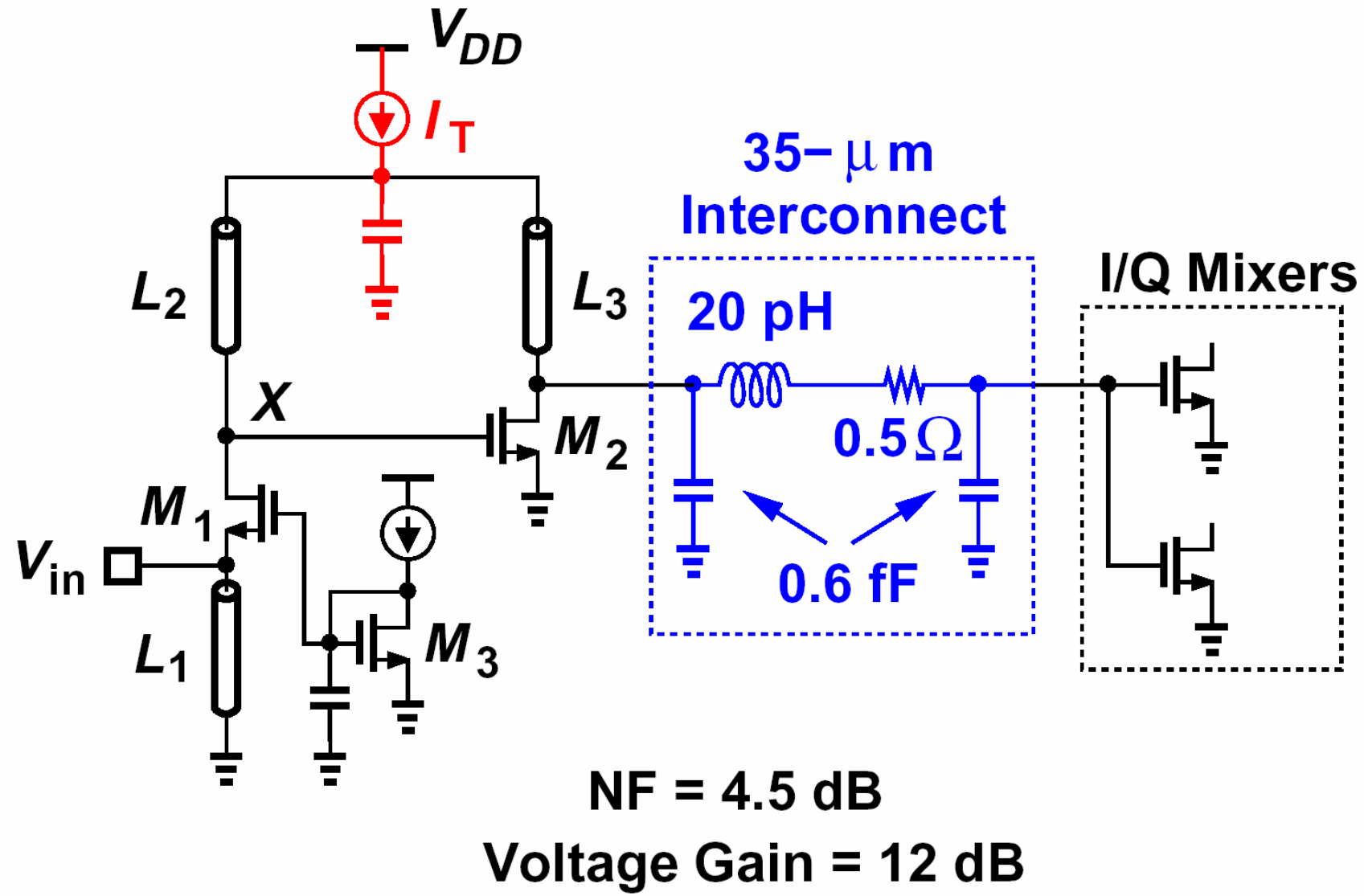
Cascode vs. Common-Gate LNA



Simplified LNA



Complete LNA

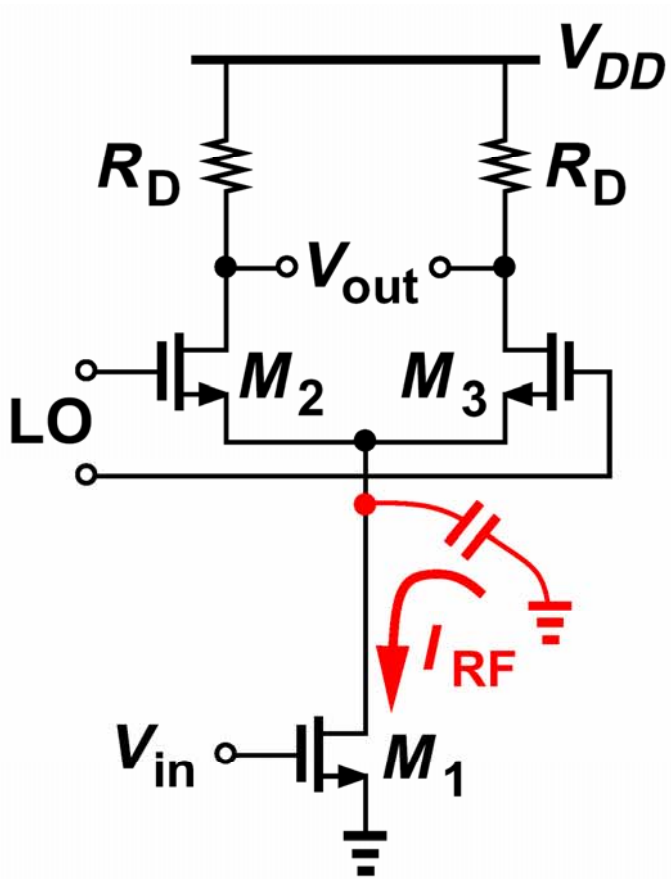


NF = 4.5 dB

Voltage Gain = 12 dB

Mixer Design

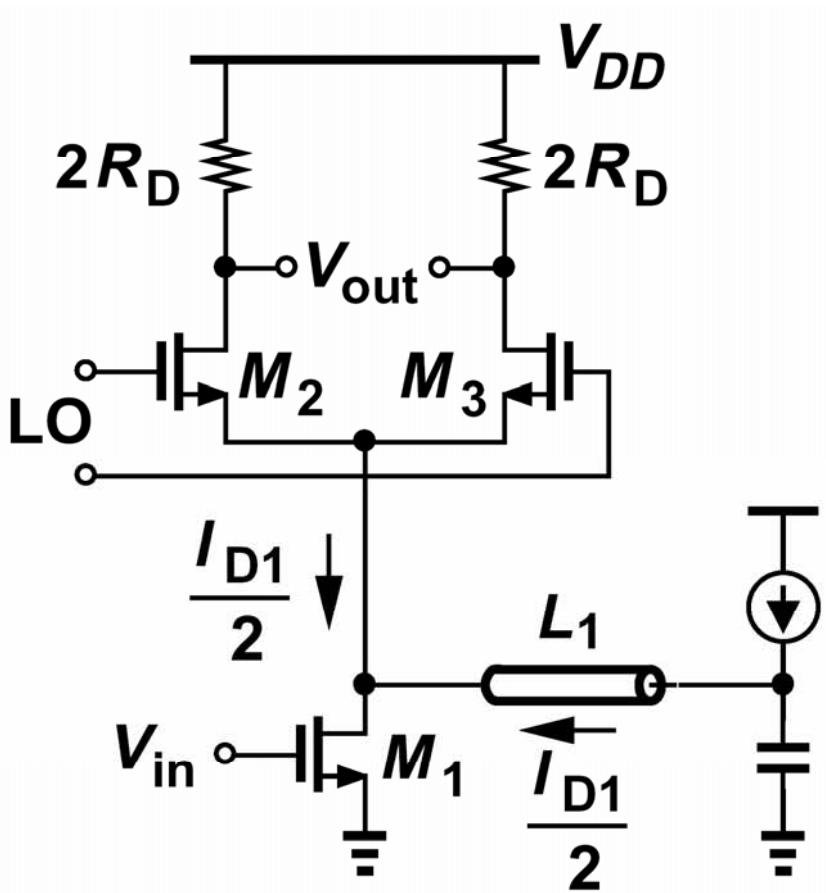
Conventional Mixer



NF = 26 dB

Conversion Gain = 0 dB

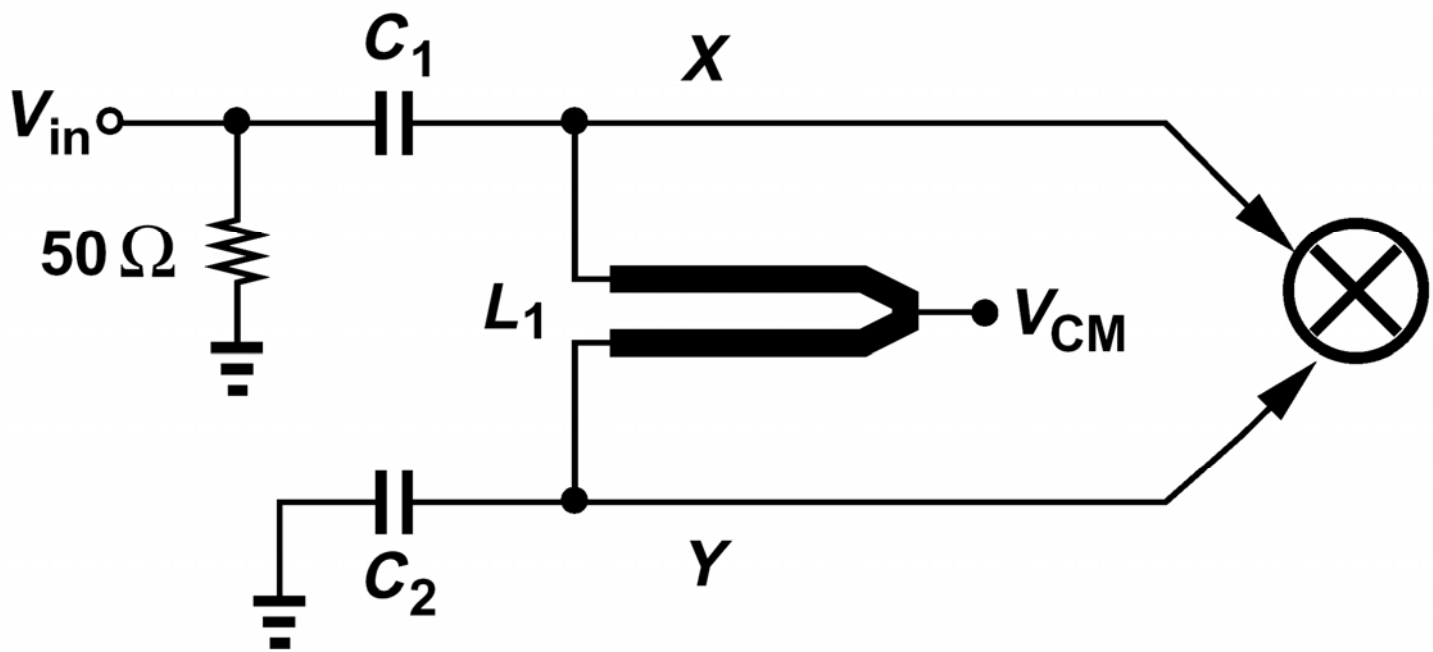
Proposed Mixer



NF = 17 dB

Conversion Gain = 12 dB

On-Chip Balun

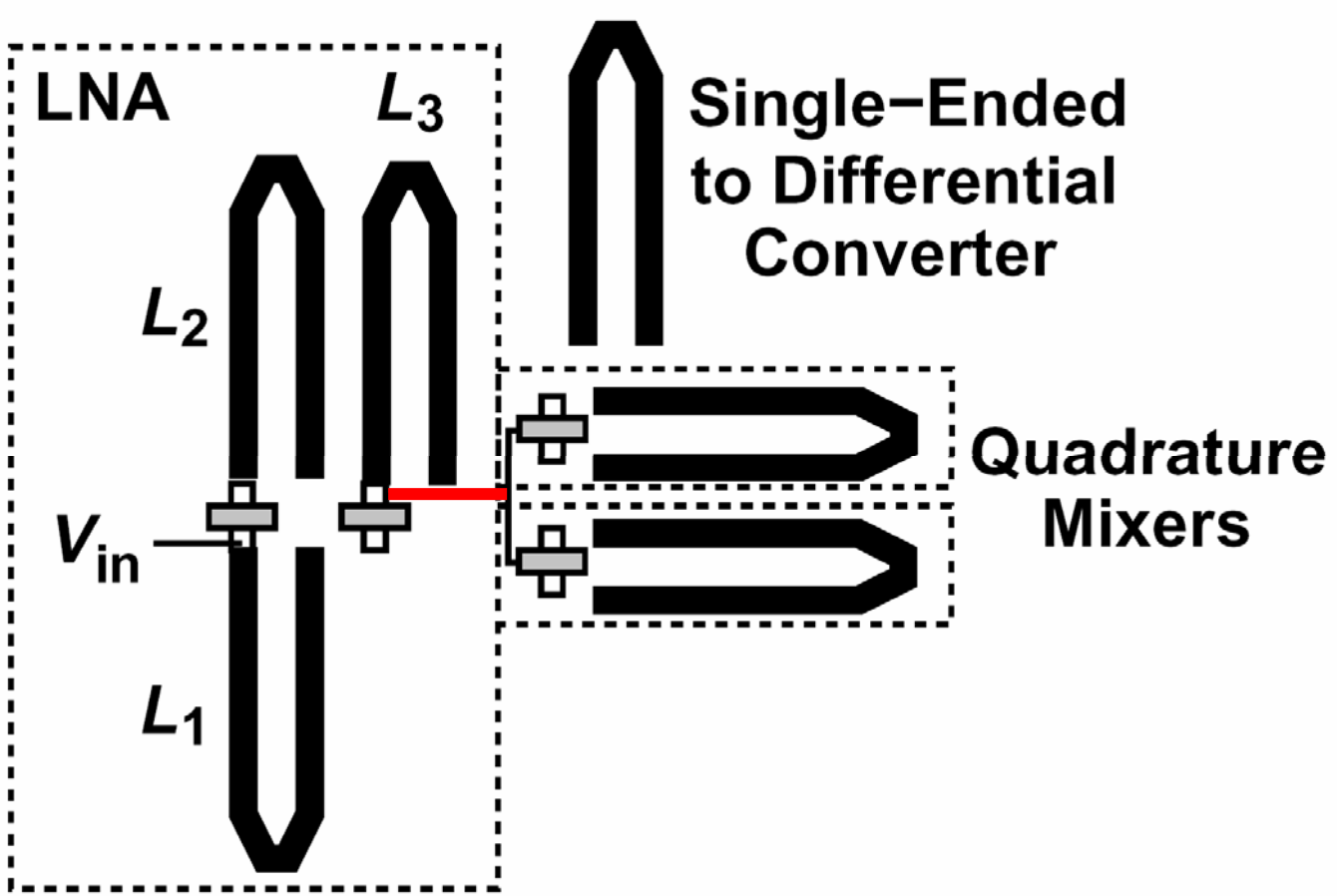


$$C_1 = C_2 = C$$

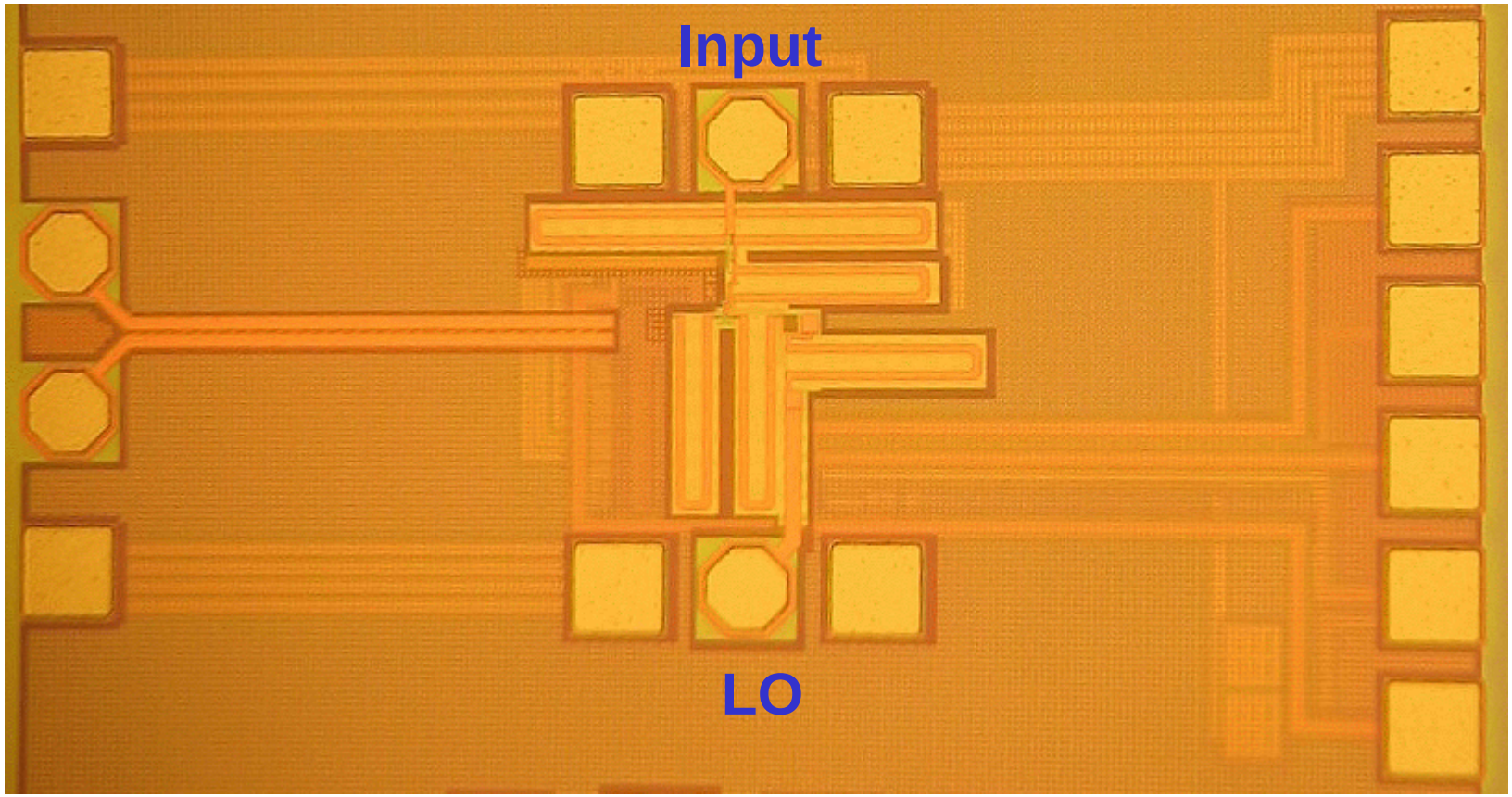
$$\frac{V_X}{V_Y} = 1 - L_1 C \omega^2$$

$$= -1 \text{ @ } \omega_0 = \frac{1}{\sqrt{L_1 \frac{C}{2}}}$$

Receiver Floor Plan



Die Photograph

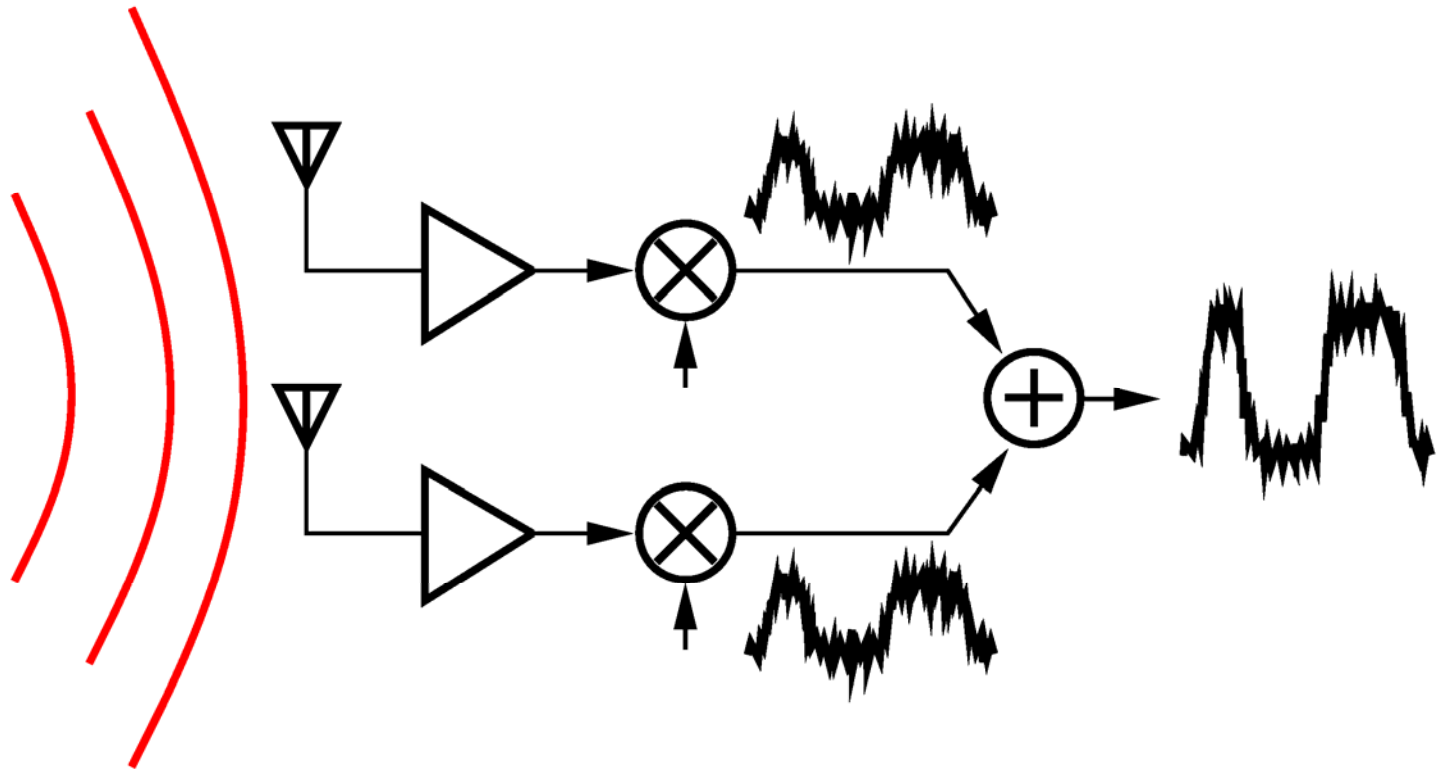


Active Area = 300 um x 400 um

Measured Performance

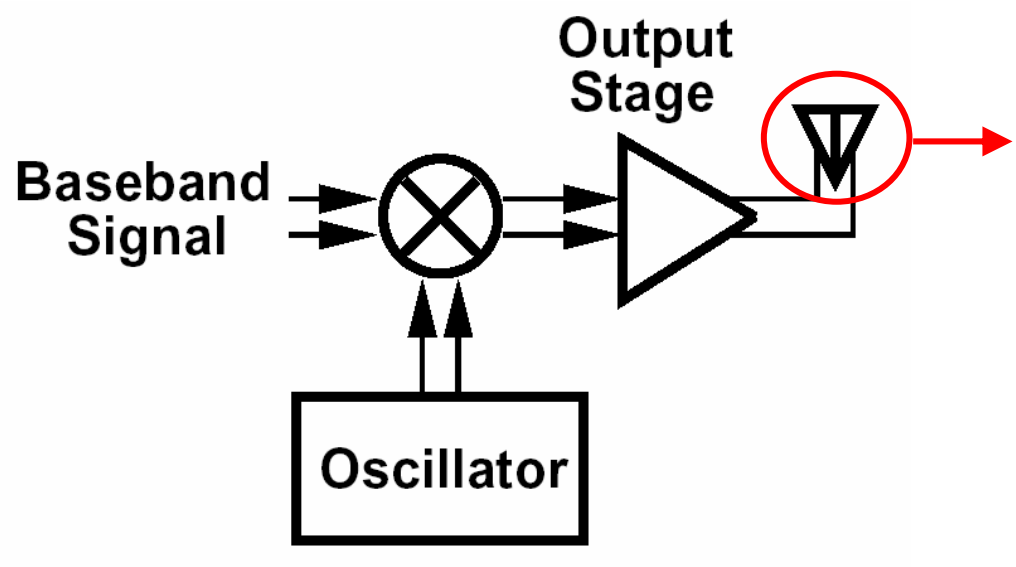
Voltage Gain	28 dB
Noise Figure	12.5 dB
1−dB Compression Point	−22.5 dBm
Power Dissipation	9 mW
Supply Voltage	1.2 V
Active Area	300 um x 400 um
Technology	0.13−um CMOS

Other Thoughts



- **3-dB improvement in SNR for twice the power consumption and area.**

Transmitter Front End

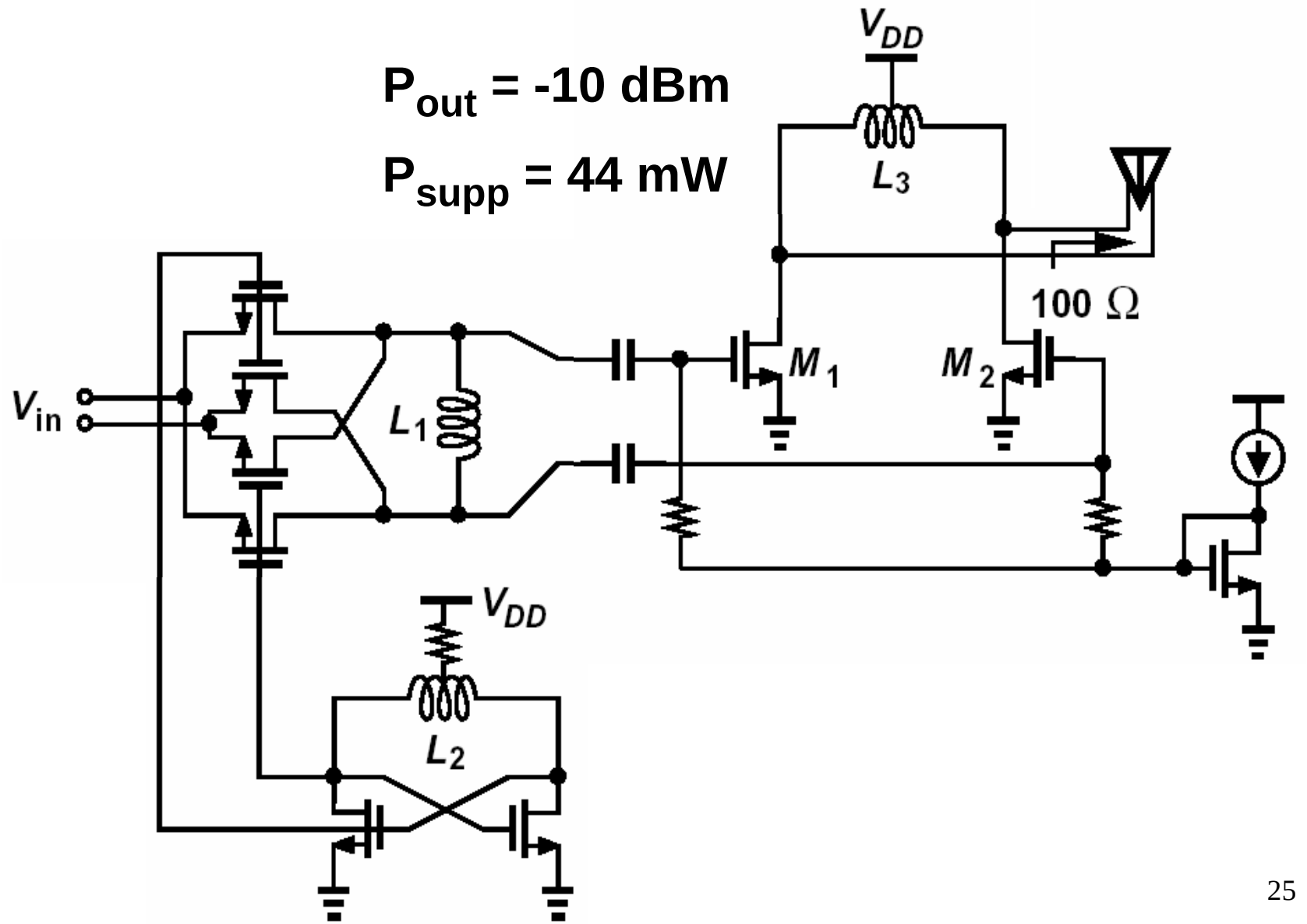


- Slot Antenna
  - Large Area
  - High Loss
- Dipole
  - Narrow Footprint
  - Moderate Loss (~6 dB)

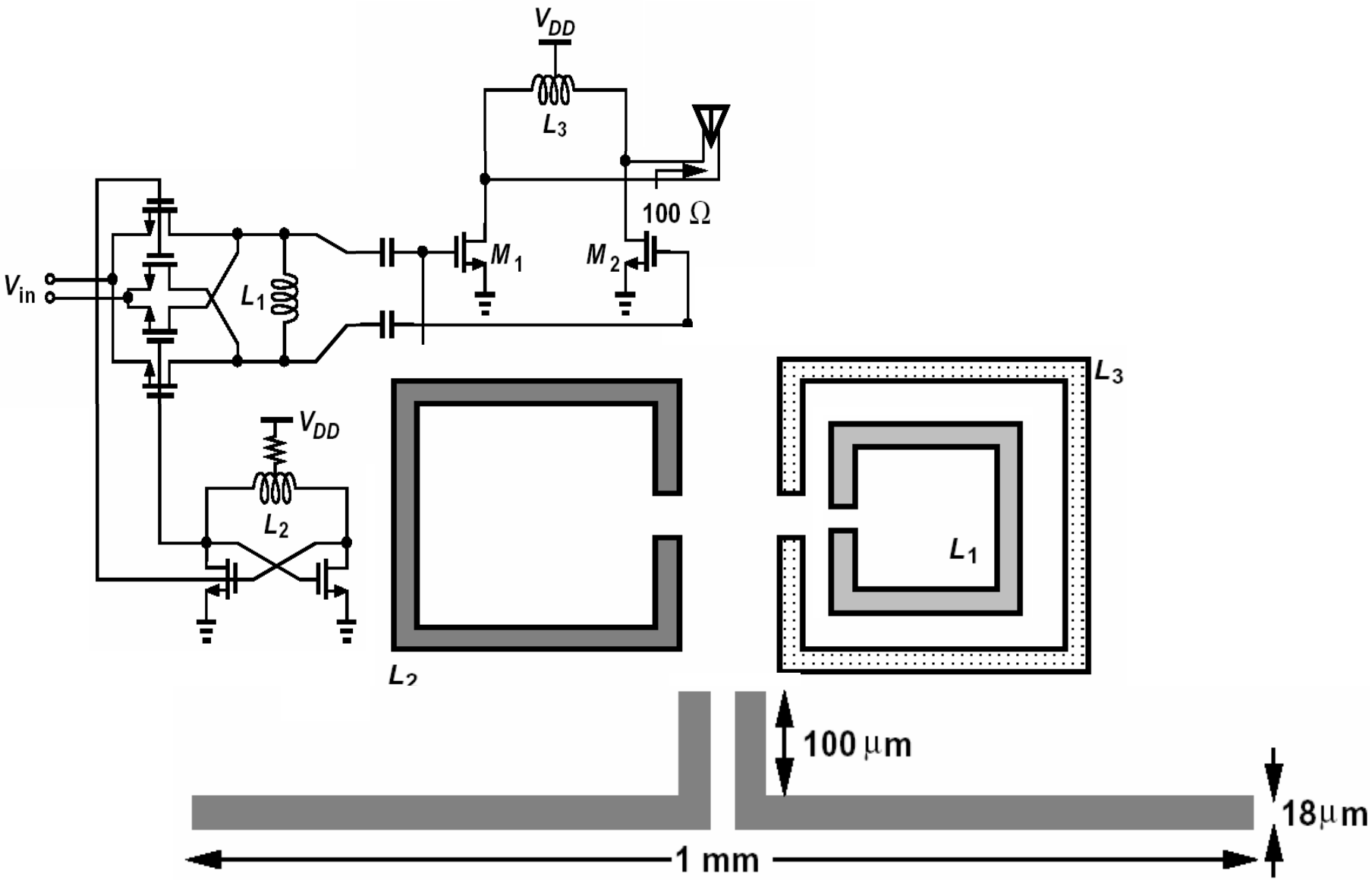
Transmitter Design

P_{out} = -10 dBm

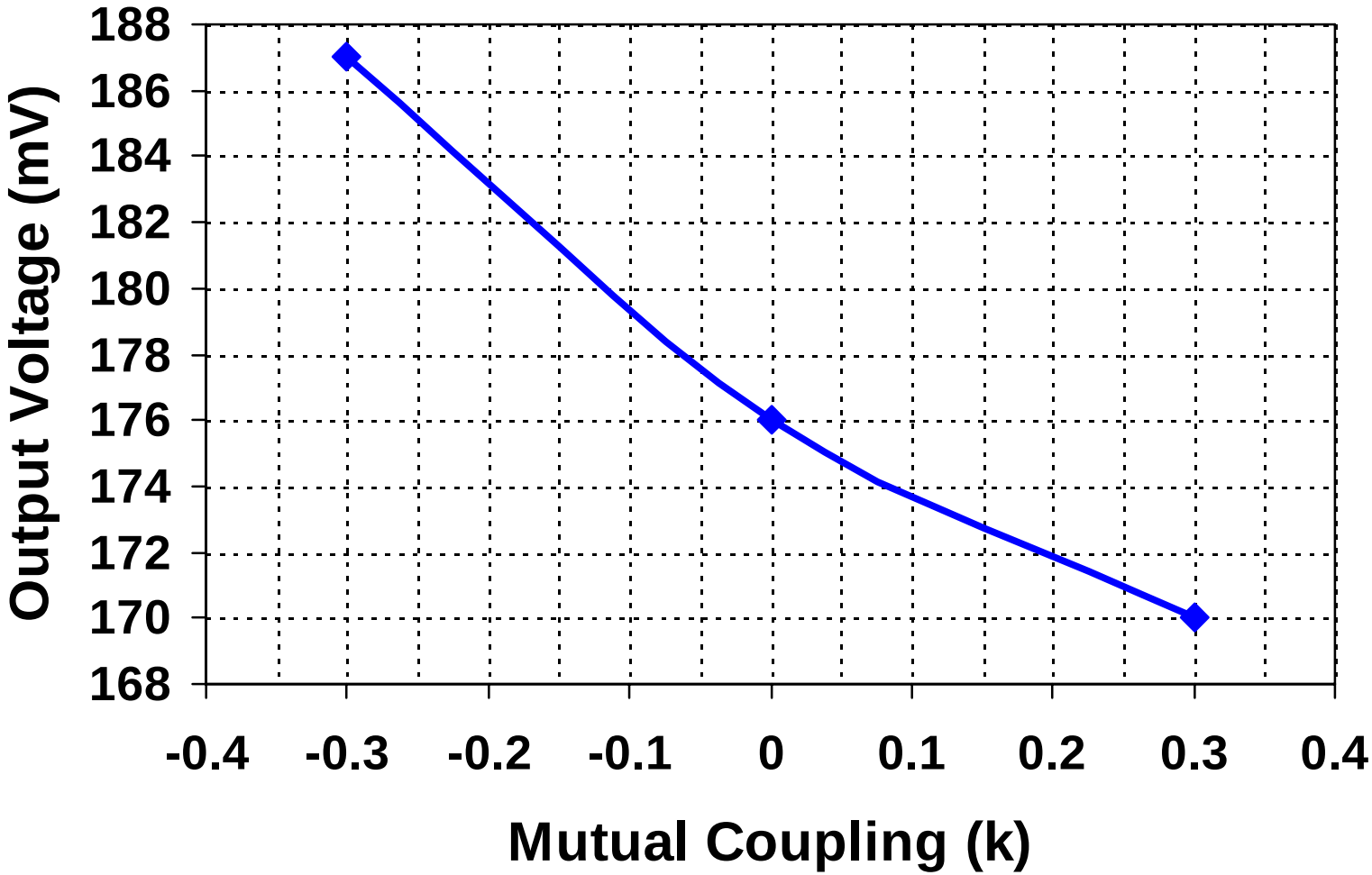
P_{supp} = 44 mW



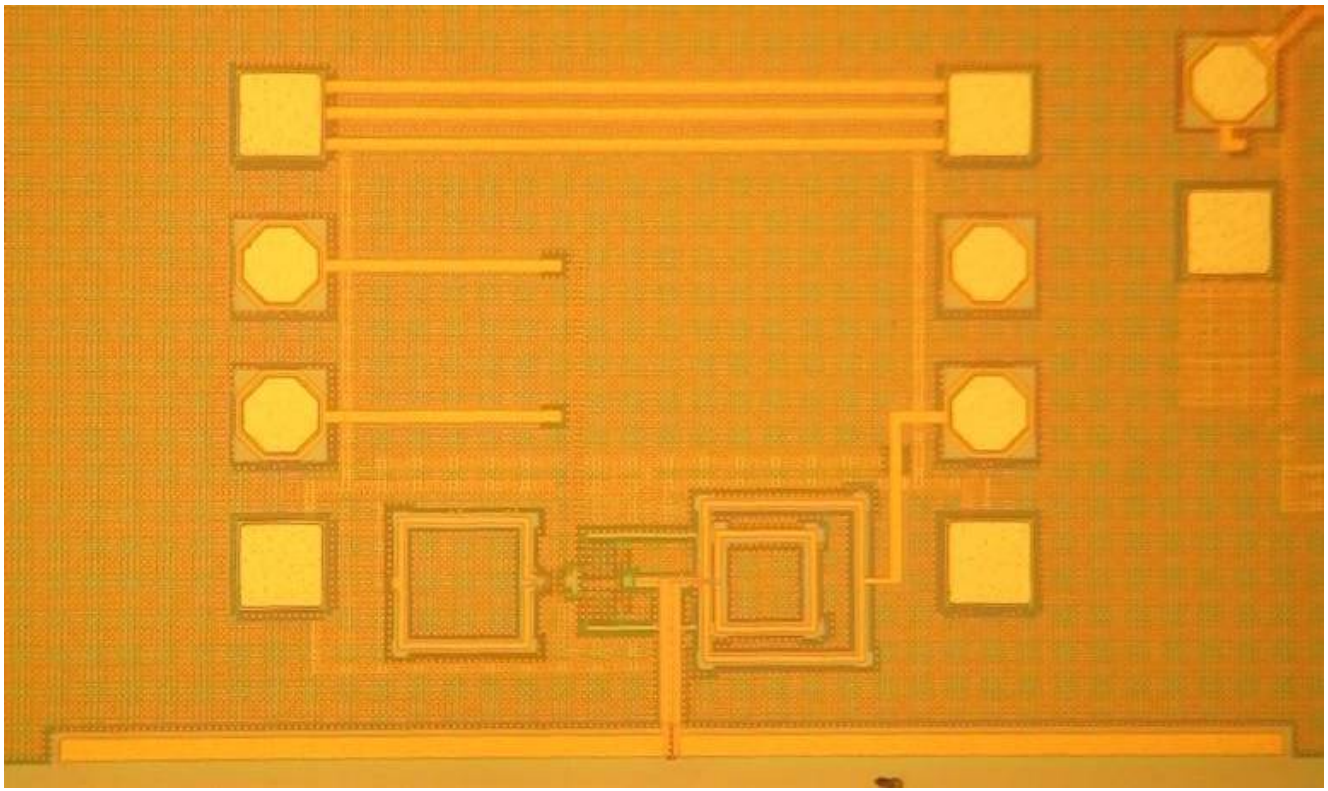
Nested Inductors



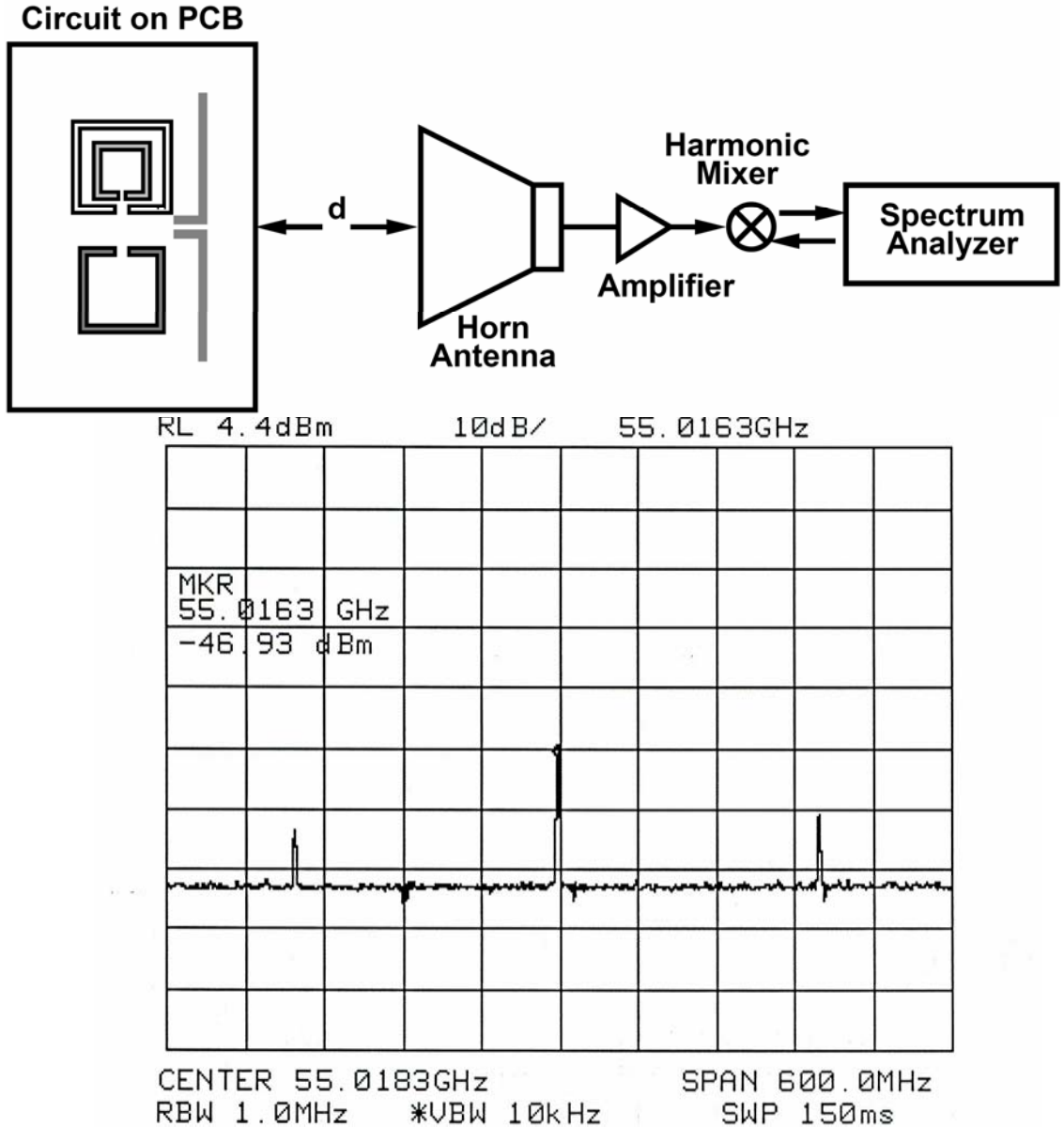
Effect of Mutual Coupling



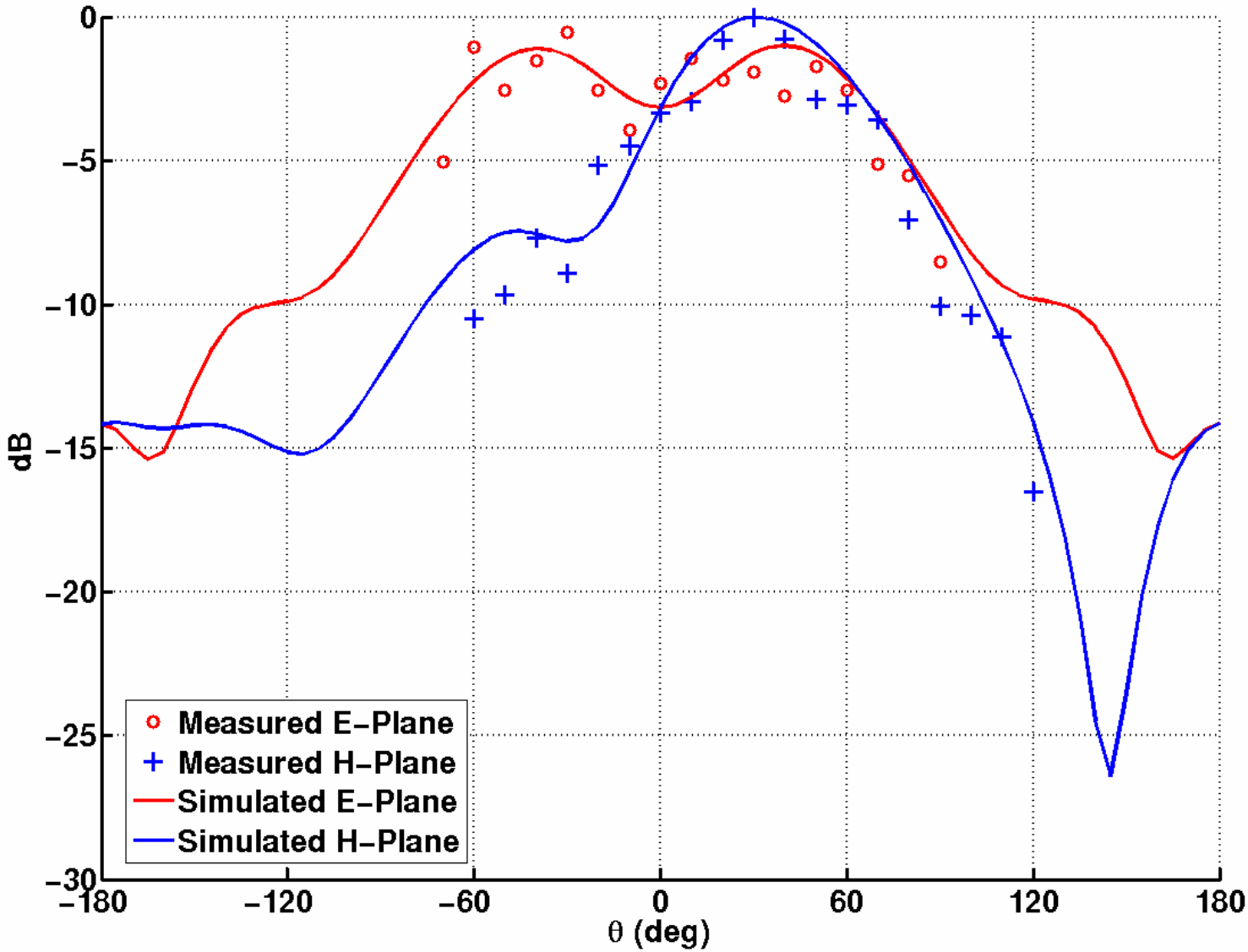
Die Photograph



Measurement Setup



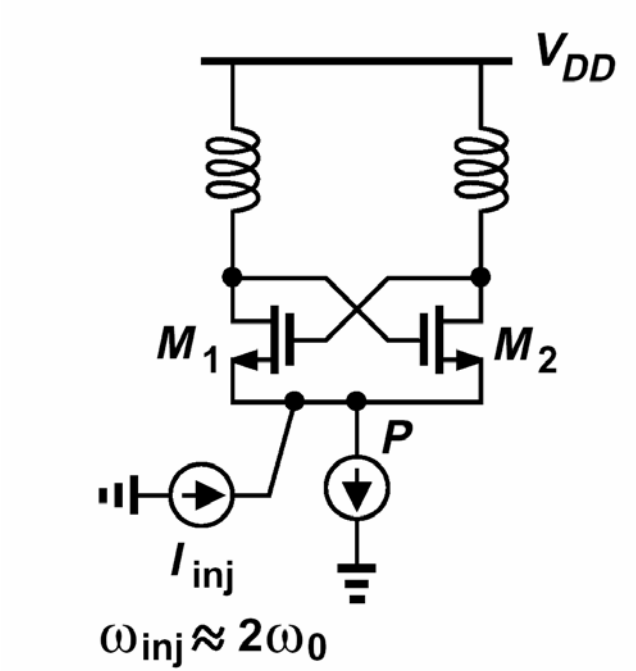
Antenna Radiation Pattern



Conventional Divider Topologies

- **Flipflop-Based Dividers**
- **Miller Divider**
- **Injection-Locked Divider**

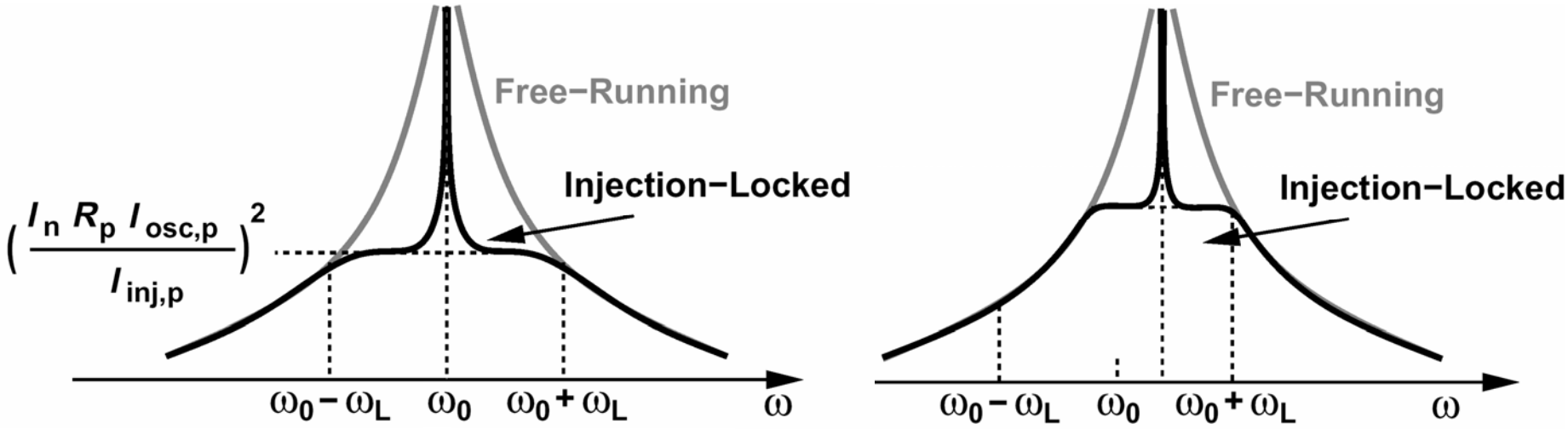
Injection-Locked Divider



- **Narrow frequency range; inversely proportional to tank Q:**

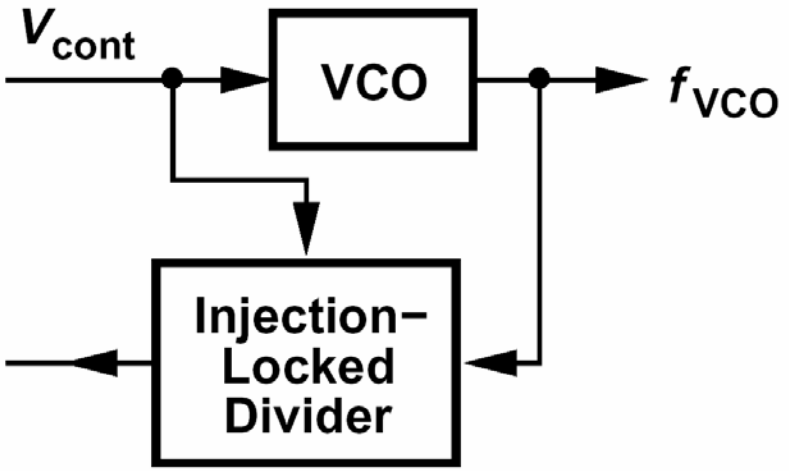
$$\Delta\omega = \frac{I_{inj}}{I_{osc}} \cdot \frac{\omega_0}{2Q} \cdot \frac{4}{\pi}$$

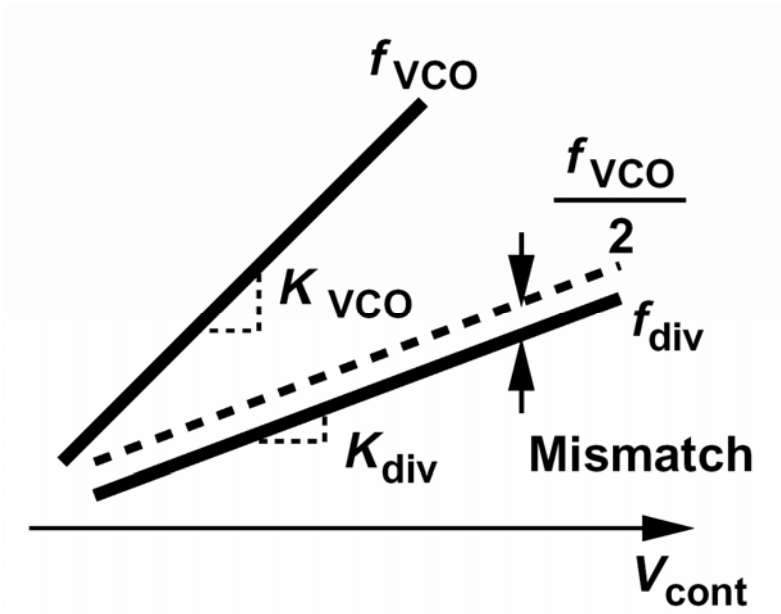
Phase Noise Degradation



- **Phase noise degrades if, due to mismatches, input frequency is not equal to $2\omega_0$.**

Increasing the Range

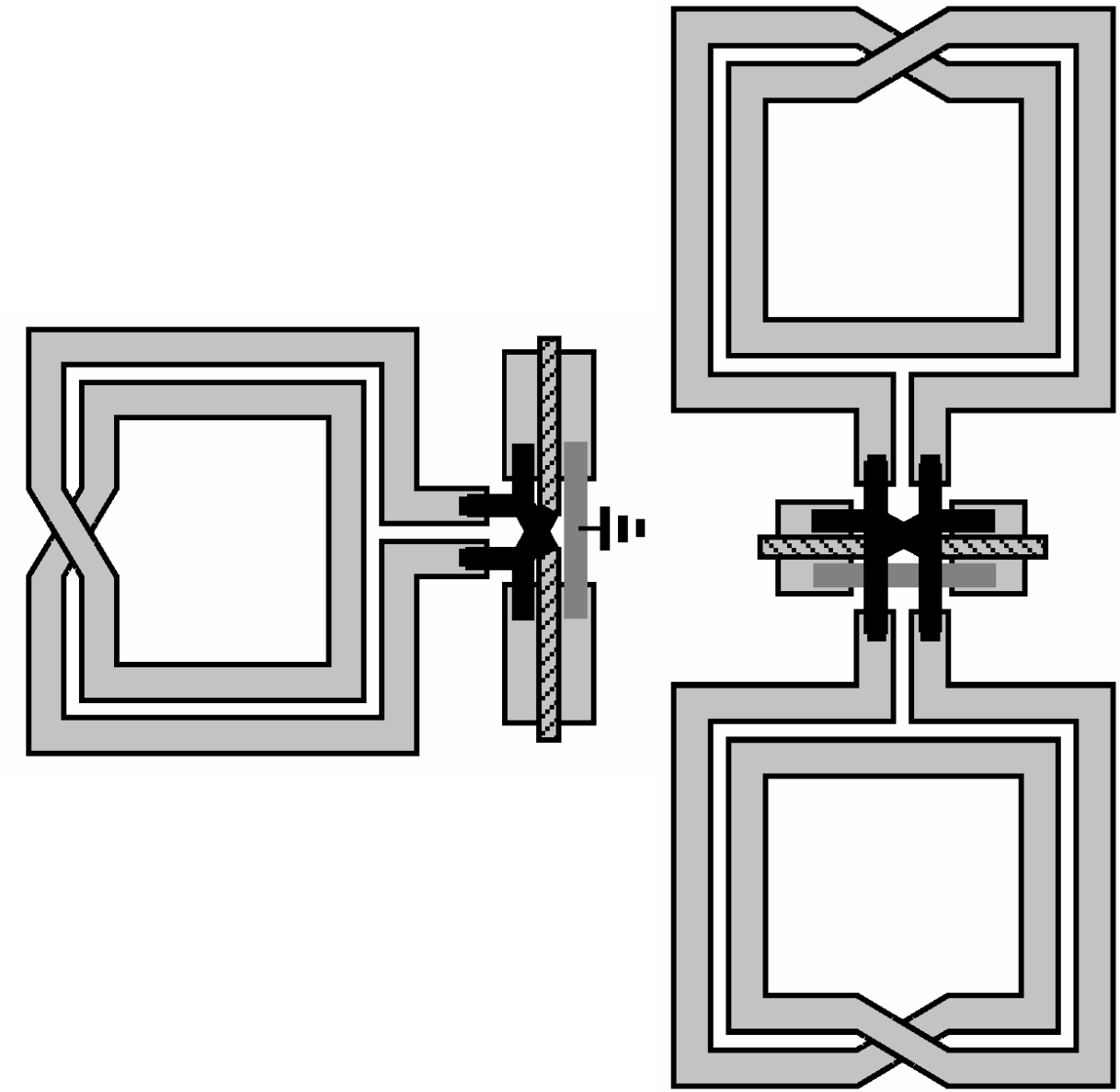




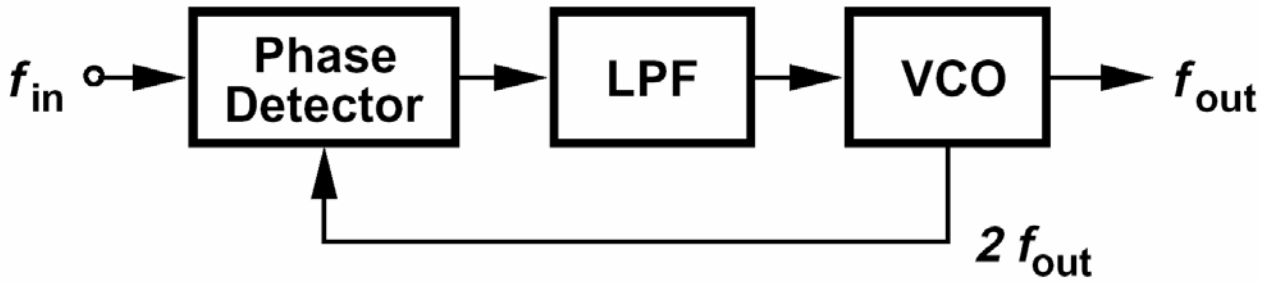
[Rategh et al, JSSC, May 00]

- **Ganged tuning does not overcome frequency mismatch.**
- **Difficult to guarantee natural frequency of divider tracks that of VCO.**

Tracking Issues

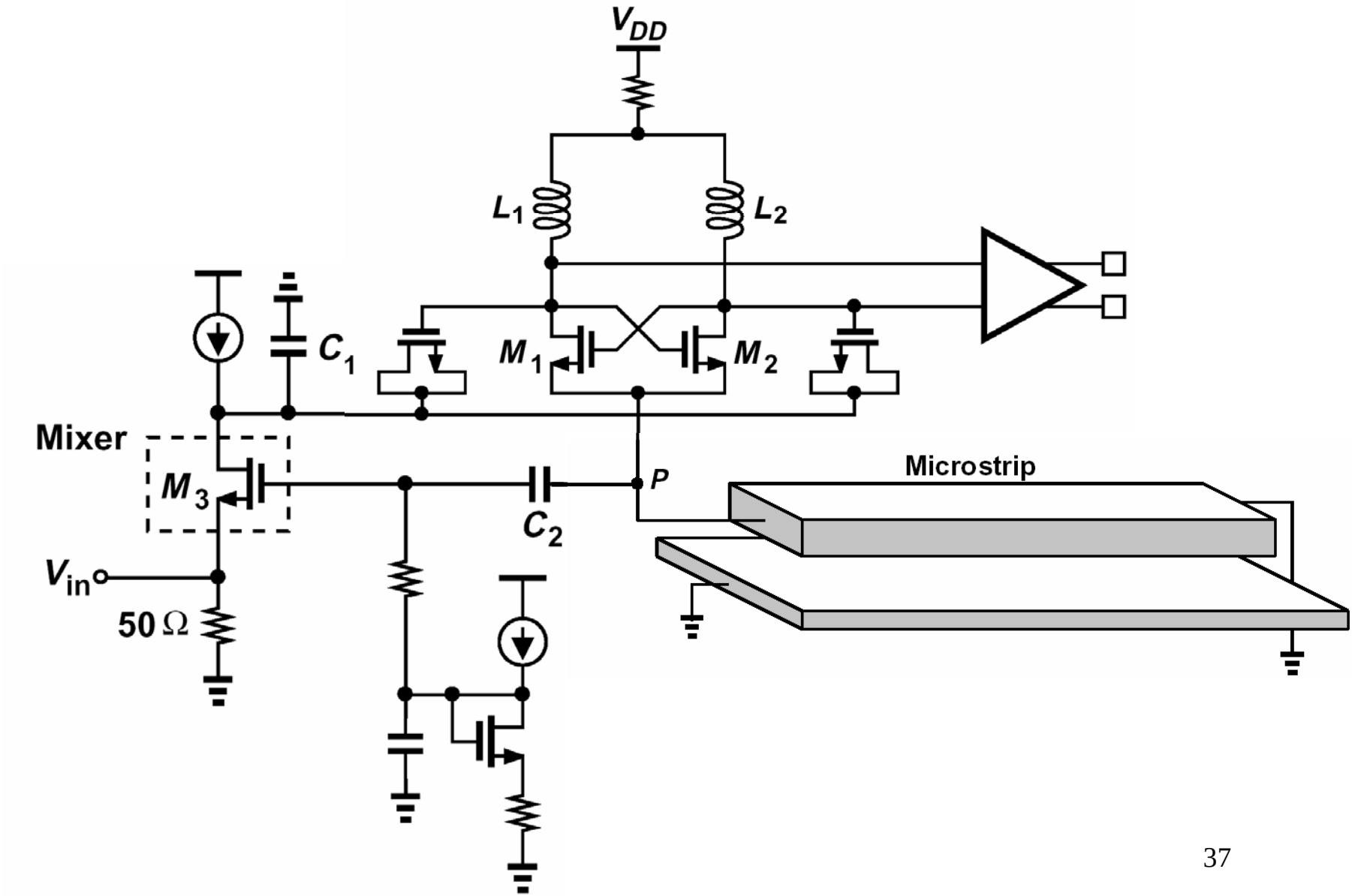


Phase-Locked Divider

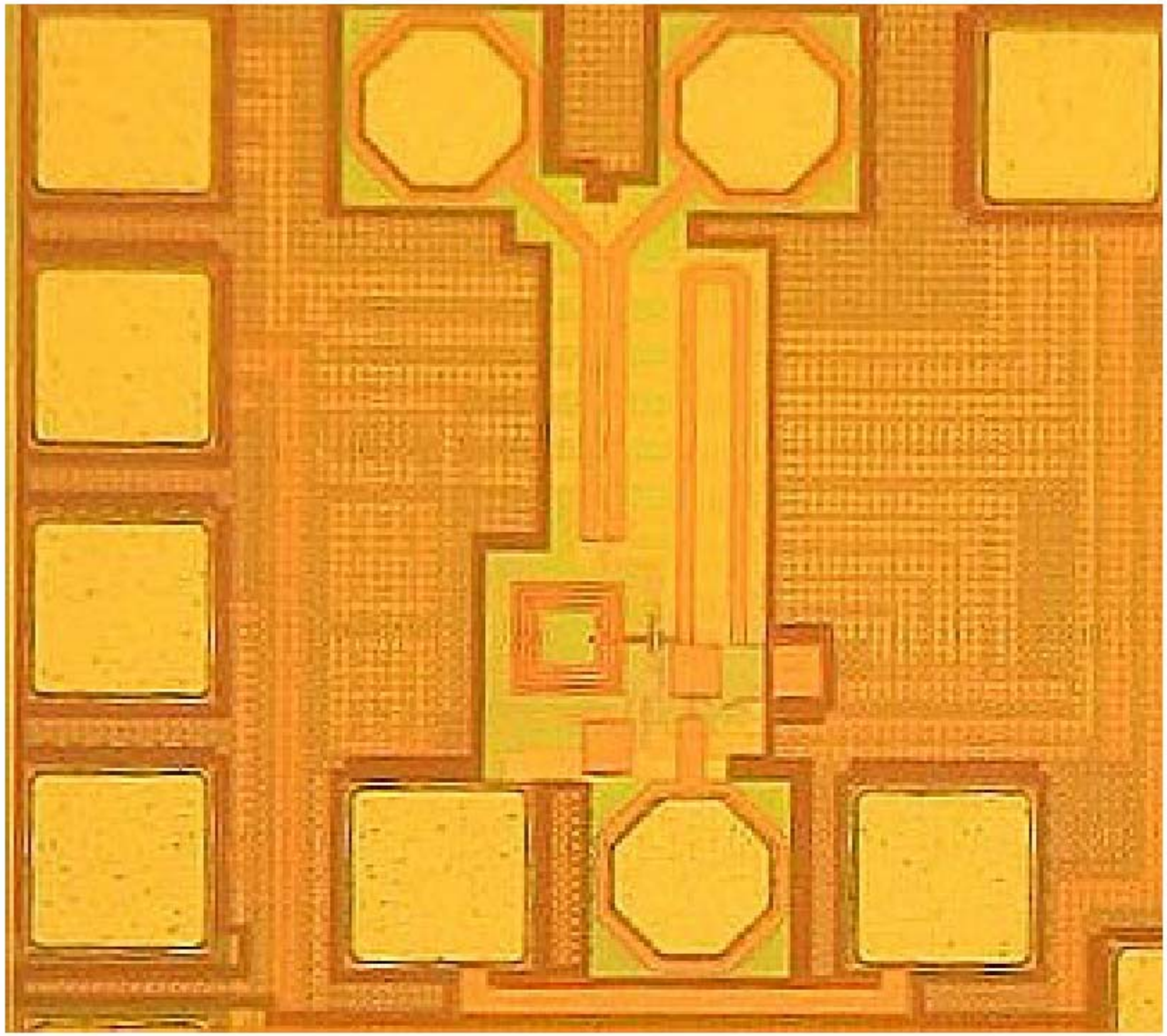


- Constant phase noise across range if gain of PD remains constant.
- No trade-off with tank Q.
- PD circuit must be very simple and experience complete switching.

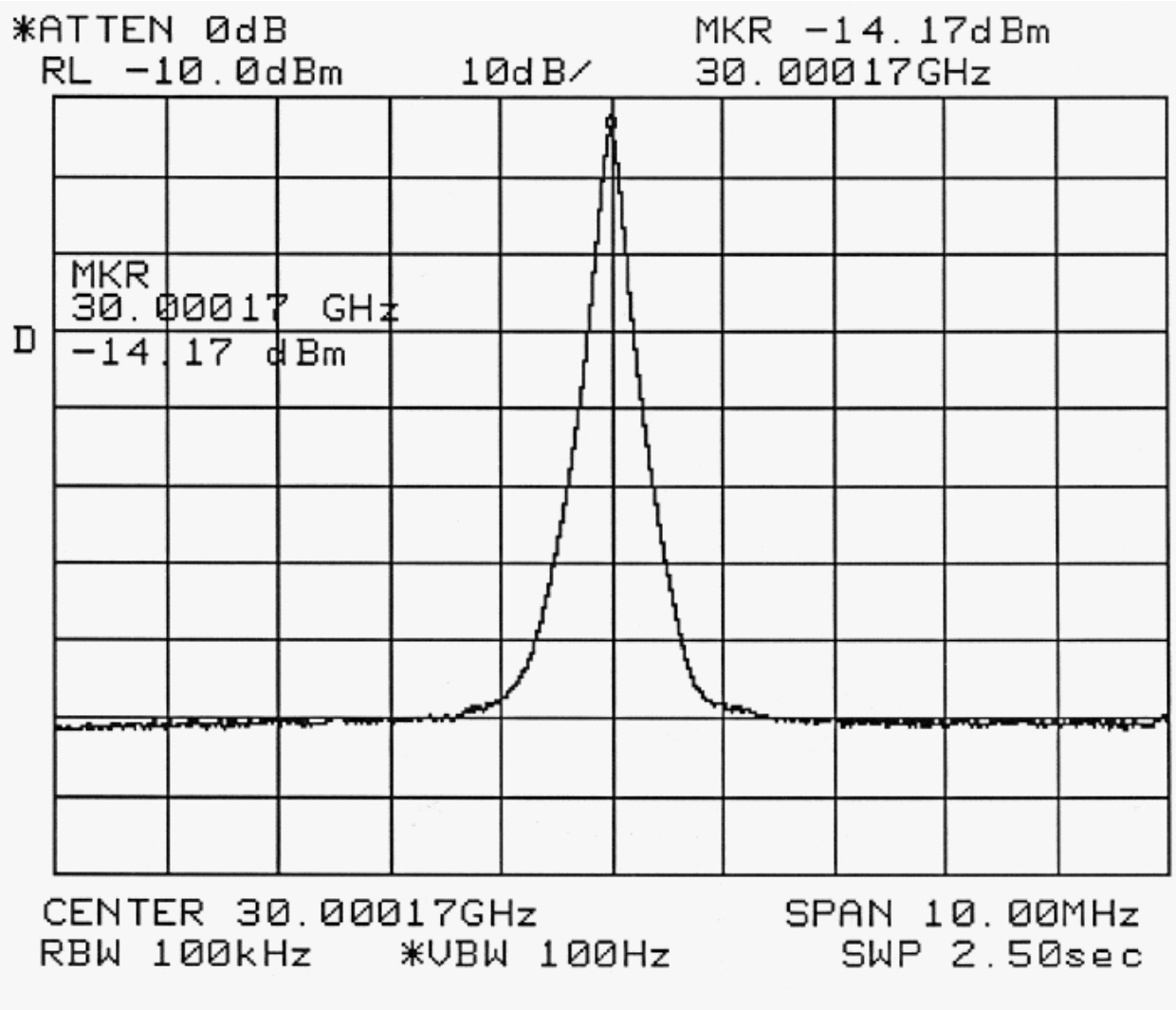
Phase-Locked Divider



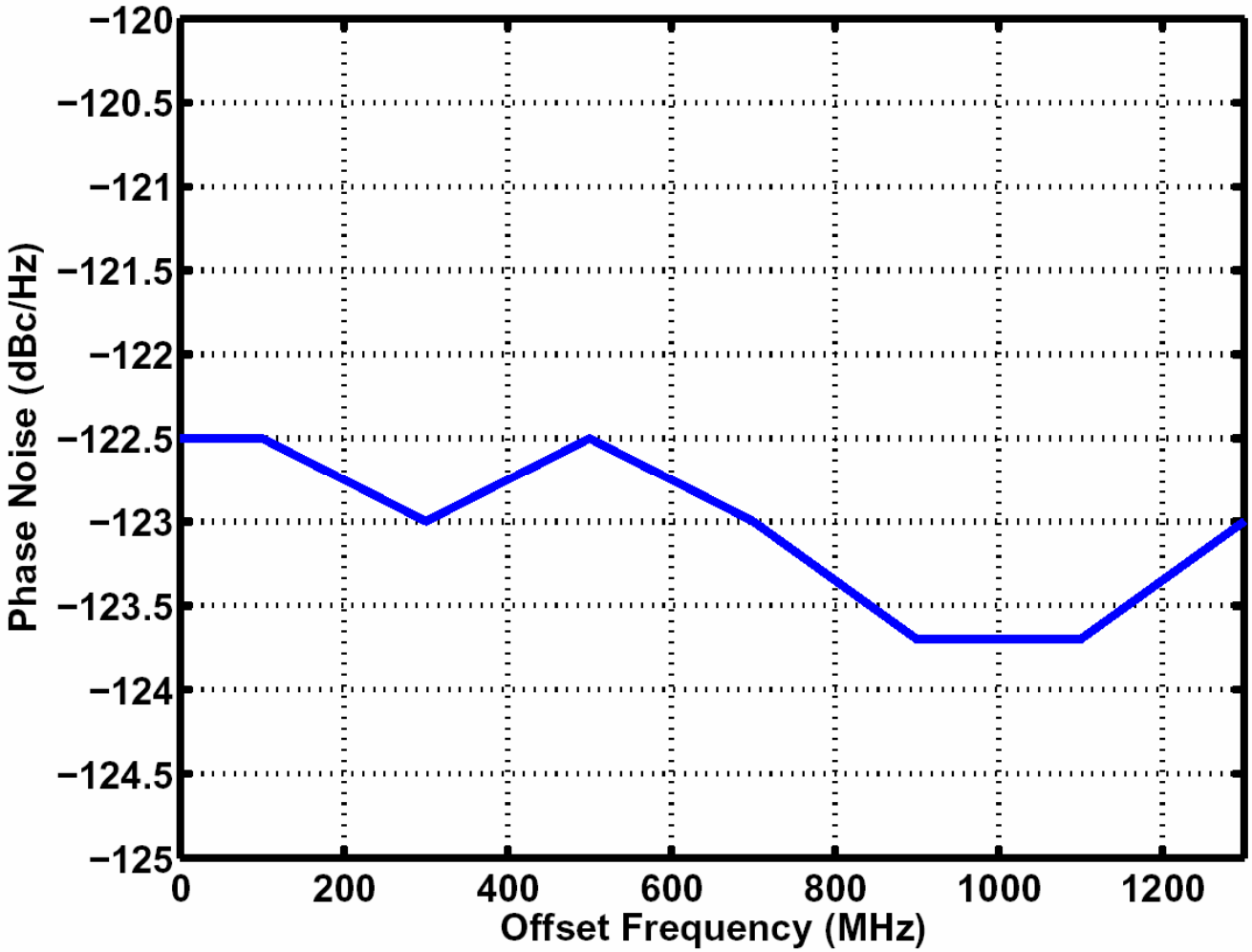
Die Photograph



Measured Output

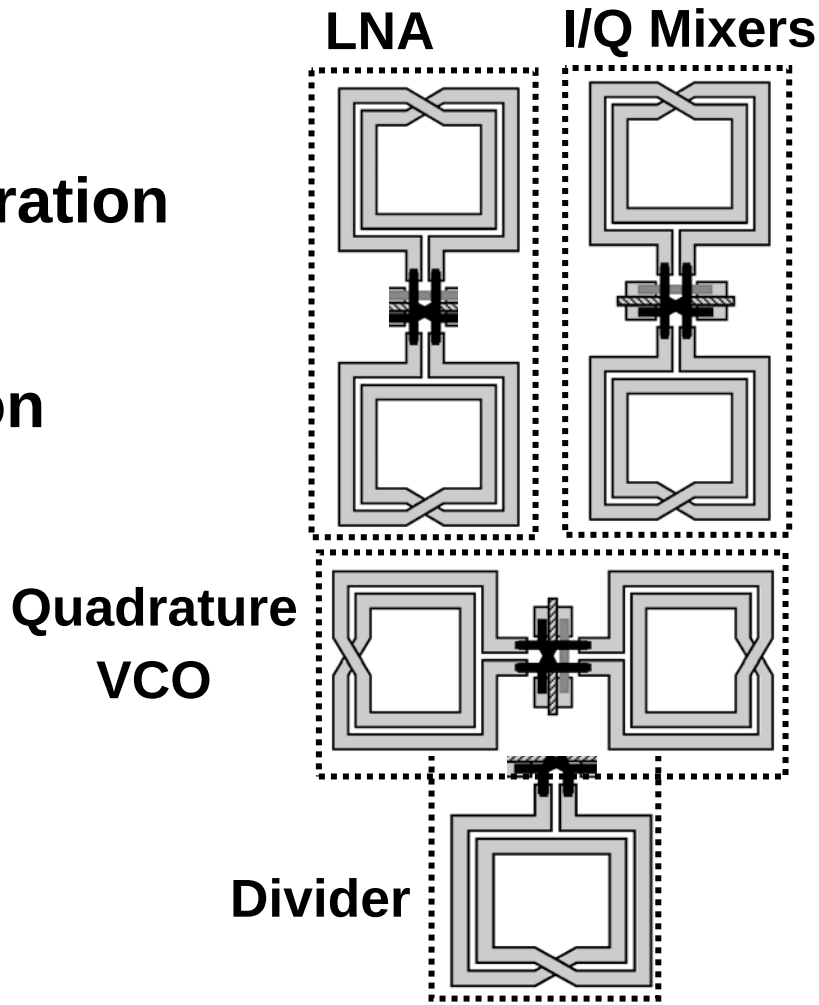


Phase Noise across Range



Challenges Revisited

- LO (I/Q) Generation
- LO Division
- LO Distribution



Conclusion

- 60-GHz transceivers can form highly-interconnected networks carrying high data rates.
- Nested inductors allow compact layout and shorter interconnects.
- Phase-locked dividers can provide a wide frequency range.
- Direct-conversion transceivers face difficult issues with respect to LO generation, division, and distribution.