IBM Research

Challenges in Serial Electrical Interconnects at 5 to 10 Gb/s and Beyond

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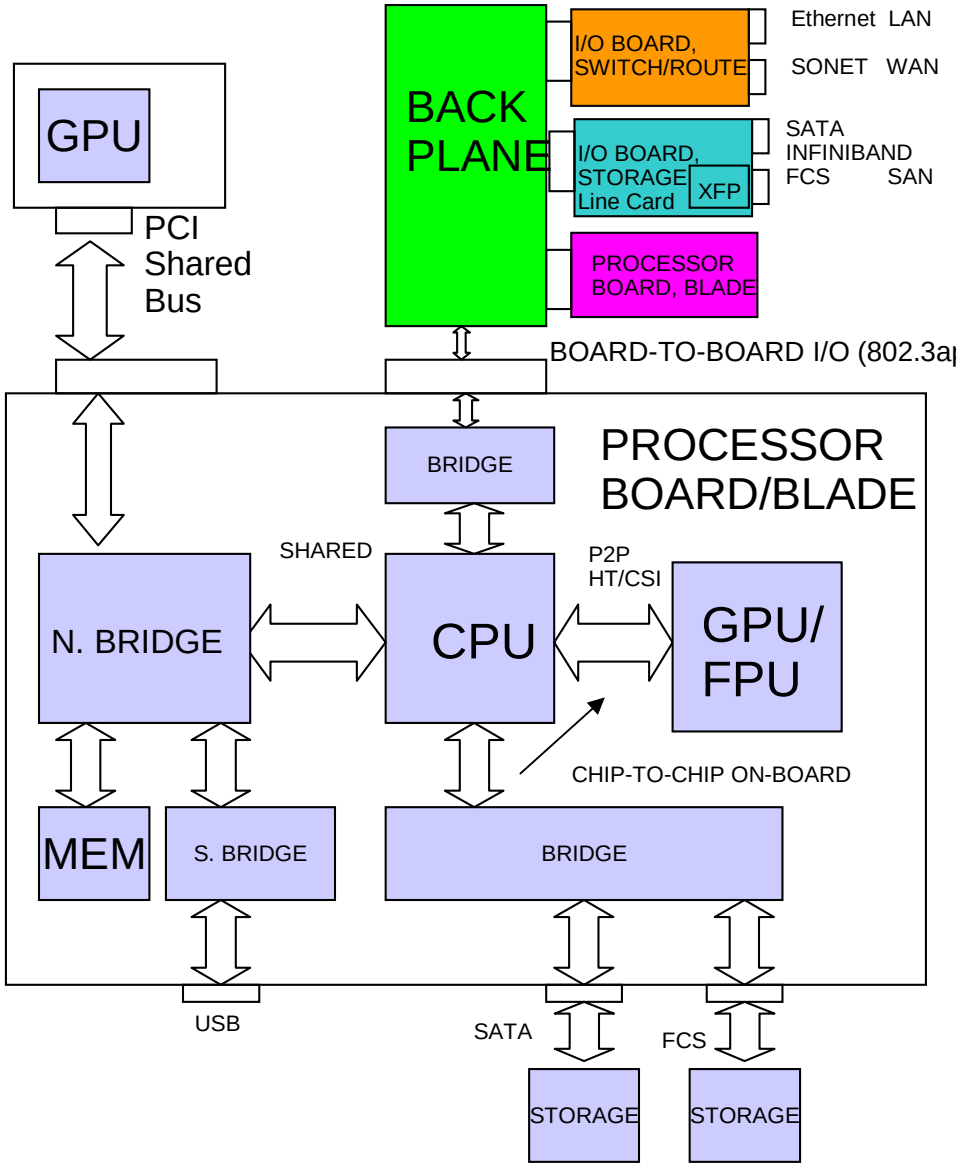
Outline

- Introduction
  - I/O Applications in modern system designs
  - Electrical Signaling Approaches
  - Line Signaling Approaches
- Electrical Channel Characteristics
  - Line Model
  - Line Degradations
- I/O core System Design
  - SERDES Architectures
  - FFE Equalization
  - DFE Equalization
  - 6-10Gb/s FFE/DFE System architecture
- Serial Link Modeling and Simulation
  - Link simulation tool
  - Eye Diagram BER Analysis
  - I/O Core Degradations
- Simulation and Measurement Results
  - IEEE 802.3ap Informative Channel Link Simulations
  - Simulated Performance vs. FFE and DFE Tap Length
  - 25Gb/s simulation results
- Summary

Applications for 5Gb/s-10Gb/s+ Electrical I/O



Protocol	RATE
Legacy shared bus Single-Ended	
DDR/DDR2/DDR3	33/66/100/133..866MHz
PCI	33/66MHz
AGP	66(x1)-533 MHz(x8)
ATA/SCSI	33/66/100 MB/s
High Rate Serial, point-to-point, Differential Transmission Line	
HyperTransport	1.6-3.2-4.8Gb/s+
CSI	6.4Gb/s
FB-DIMM	2.4-4.8-9.6Gb/s+
XDR	3.2-8.0Gb/s+
PCI-E	2.5 Gb/s, 5-6Gb/s.
INFINIBAND	2Gb/s+
SATA (Serial ATA)	1.3-3.0-6Gb/s
FCS (Fibre Channel)	1-2-4-8-10-16Gb/s
SAS (Serial Attached SCSI)	1.5Gb/s
OIF-CEI	6-10Gb/s (to 25Gb/s)
802.3ap	10Gb/s
XFP (Optics module)	9-11Gb/s

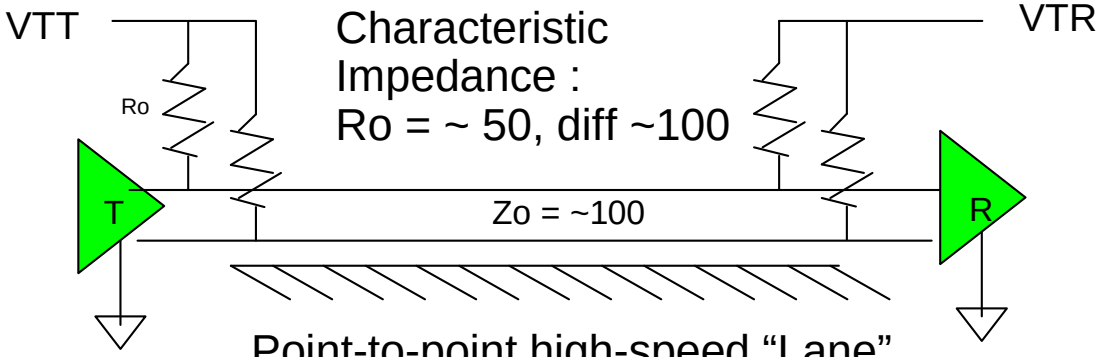
Electrical Signaling Underpinning Rate Boost

Legacy Parallel Shared-Bus Oriented :
Single-Ended
Transmission-Line Effects lower due to slower rate

Rates above1Gb/s challenging
(advanced systems pushing more)
Problems at higher speeds :
- Crosstalk
- Ground bounce
- Switching Noise
- EMI

Large number of lines in buses such as ATA to a disk

Modern Serial Point-to-Point Oriented :
Differential, Termination Matched to impedance controlled Transmission Line



Line Characteristic Impedance :
Ro = ~ 50, diff ~100

Point-to-point high-speed “Lane”
3 to 5 to 10 Gb/s in developing standards

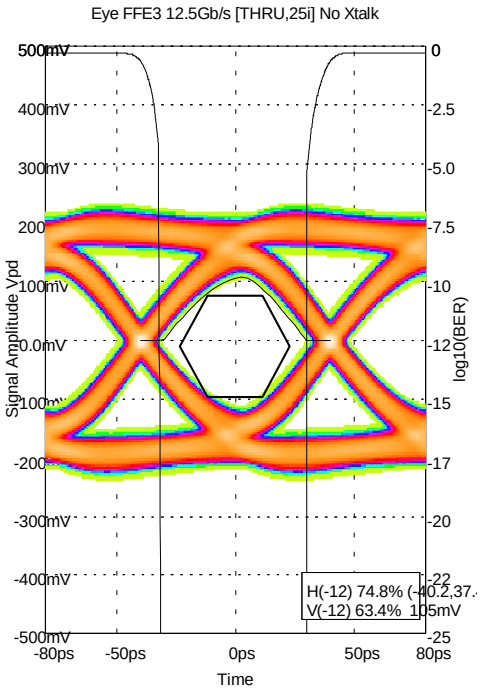
Two lines used, but more than Makes up for extra line by 2x, 4x, 8x Single-ended speed

Problems Addressed :
- More Crosstalk/Noise Immunity
- Ground bounce resistant
- Switching noise resistant
- Less noise generated
- Impedance matched to line
- Less SE swing needed
- Lower EMI
- Less signal lines for disk attach

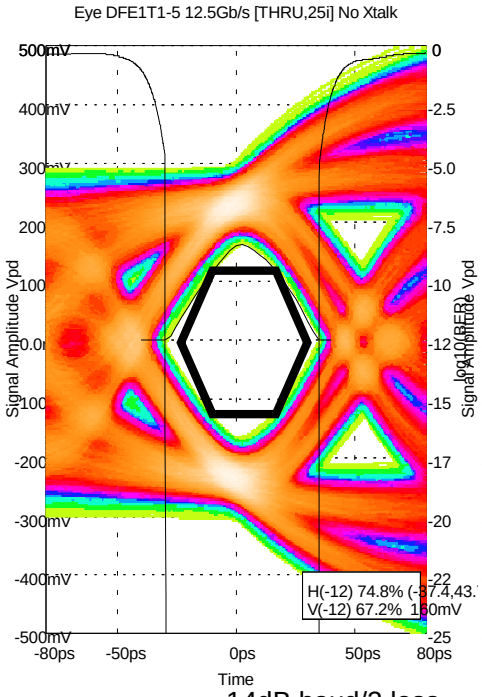
Line Signaling Methods : 12.5Gb/s on 25” Tline

BEST!

NRZ-FFE3



NRZ-DFE5

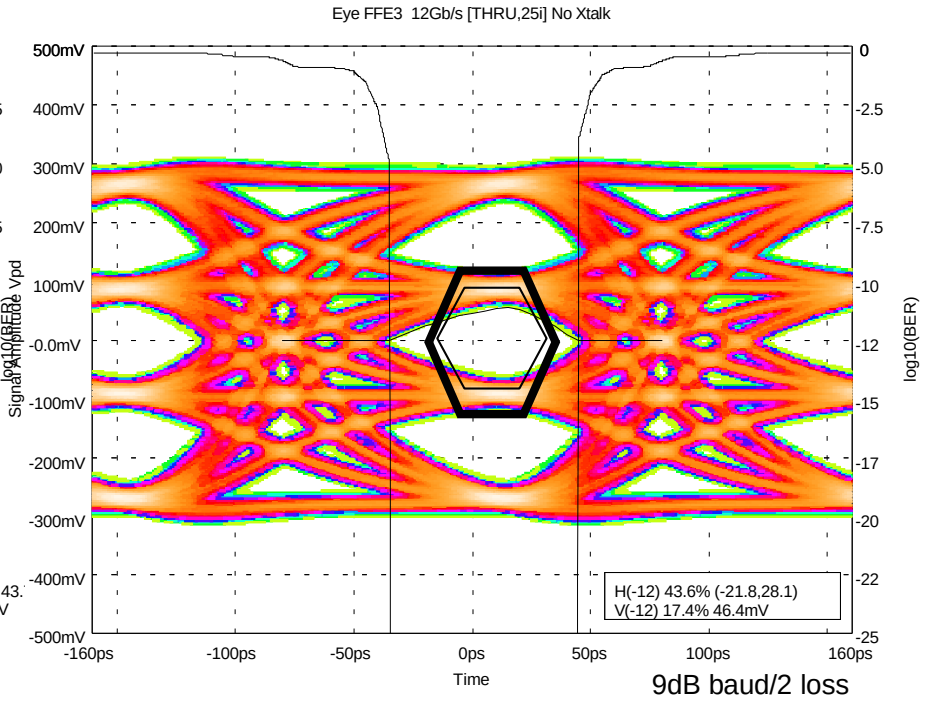


14dB baud/2 loss

Pro : NRZ Common signaling in standards
When RxDFE used, almost always superior performance to 4-level
Low peak/average power
Simple driver/slicer : good for low V

Con : Not good in terms of spectral efficiency (Bit/s/Hz)

PAM4/FFE3



9dB baud/2 loss

Pro : 2x data rate in same BW

Con : more complex Tx, Rx slicer,
may need higher drive level
needs higher SNR for given BER
more sensitive to nonlinearity
more jitter in edge crossover
3x higher peak/error threshold
-> 3x more sensitive to xtalk, ISI

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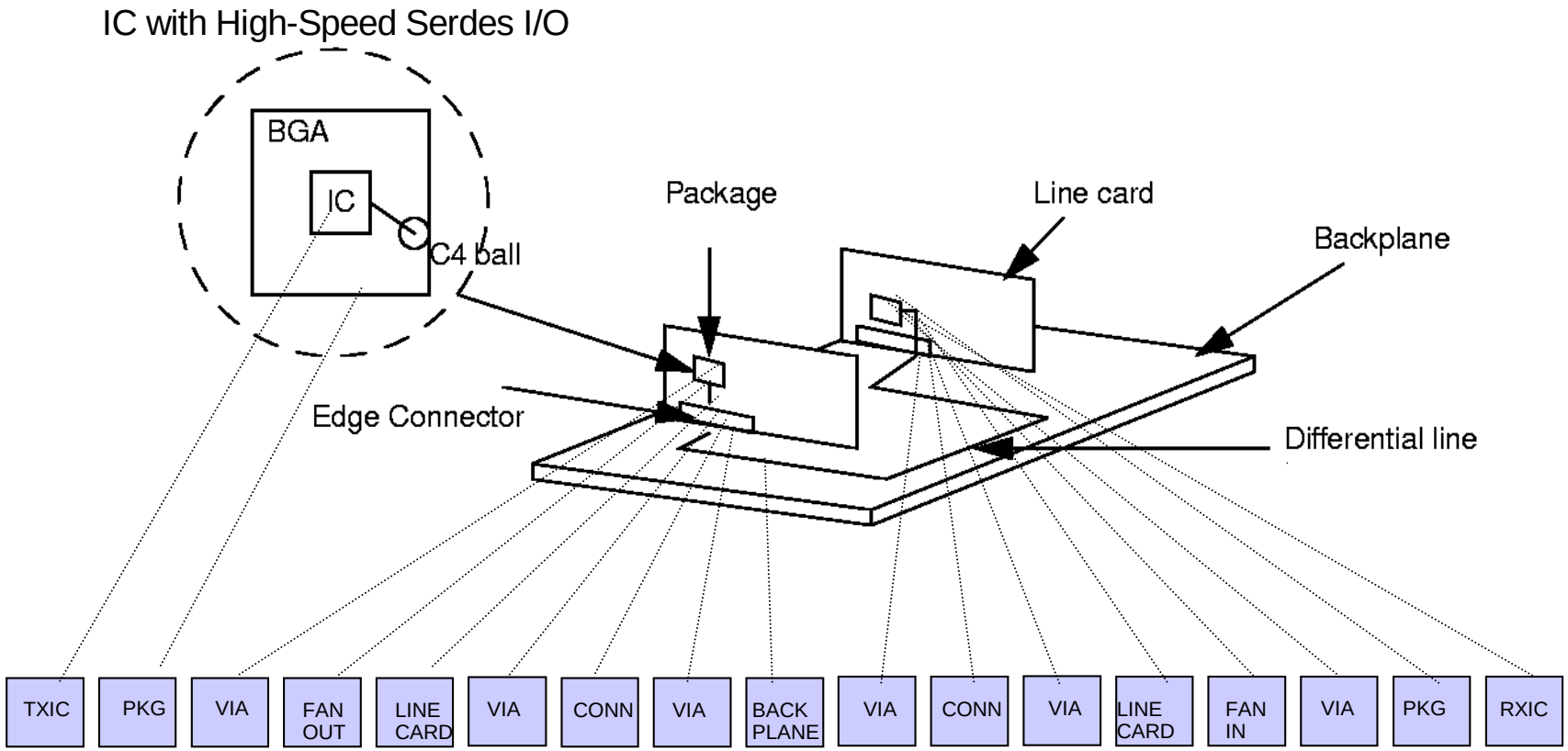
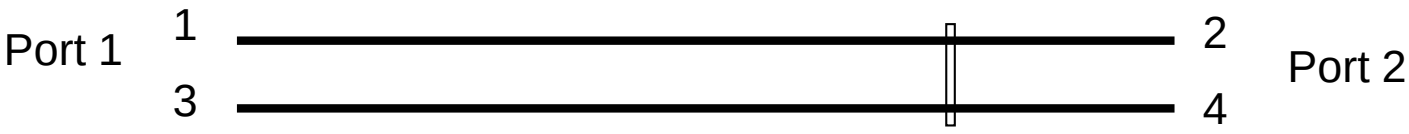
Backplane Channel Model



Typical Backplane Environment :
Line card 3" to 10" from edge connector
Total of two connectors in link
Backplane line 20" to 30" in length, total line run up to 40" (1m)
Plastic or ceramic BGA package
Multiple Lane I/O Buses... 4 to 8 lines wide or more
Asynchronous clocks

CHALLENGE :
To accurately model this channel, need high-order N ports (20+) which describe through and crosstalk responses of each link component, including IC, to high freq (10-20GHz or BAUD*2 to BAUD*3
Need multiple results for each block due to build variation and temp/humidity/aging variation!
17 BLOCKS, 3 VARIATIONS, 17**3 = ~5000 COMBOS

Characteristics of Differential Transmission Line



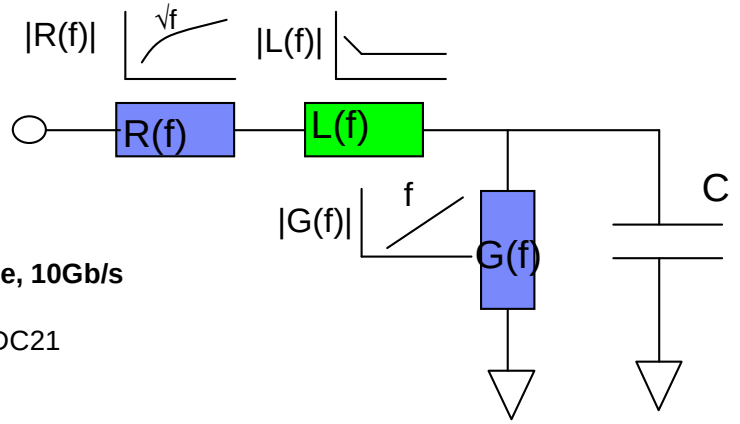
Diff port voltage = V(1) – V(3)
Common mode port voltage = (V(1) + V(3))/2

Incremental piece of line :
"Per Unit Length" or PUL RLGC model

Propagation modes for a differential line :

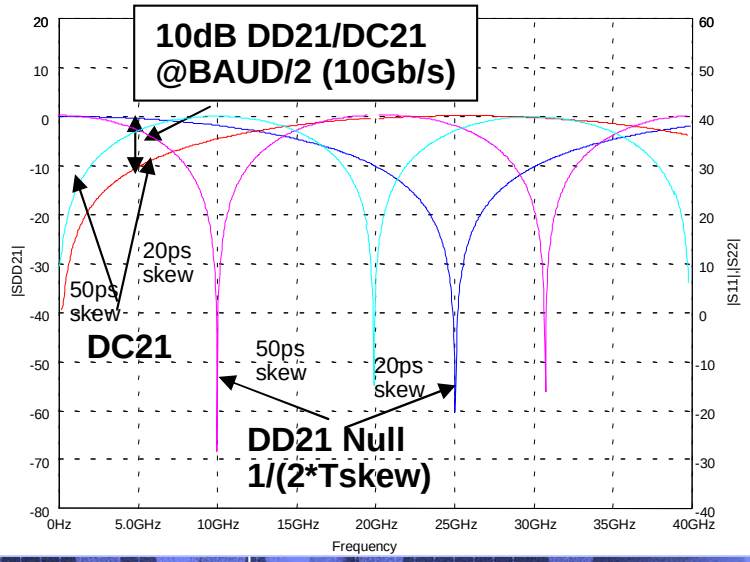
DD21	Differential 1 to Differential 2
DC21	Common 1 to Differential 2 (mode conversion)
CD21	Differential 1 to Common 2 (mode conversion)
CC21	Common 1 to Common 2

Incremental Lossy Transmission Line Model



R : Skin effect R = Ro + Rf *sqrt(f)
G : Dielectric loss : G = Go + Gf *f
L : Inductance : L = Lo + Lfreq(f)
C : Capacitance : C = Co + Cfreq(f)

[D,D,2,1] & [D,C,2,1] Channel Response : 20ps & 50ps PNskew



Mode conversion table, 10Gb/s

Skew	-DD21	DD21/DC21
0	0	inf
10ps	0.1dB	15dB
20ps	0.5dB	10dB
30ps	1dB	6dB
40ps	2dB	3 dB
50ps	3dB	0dB

20ps of Δ delay (0.2 UI @10Gb/s)
(relv = 0.5) = 3mm of line

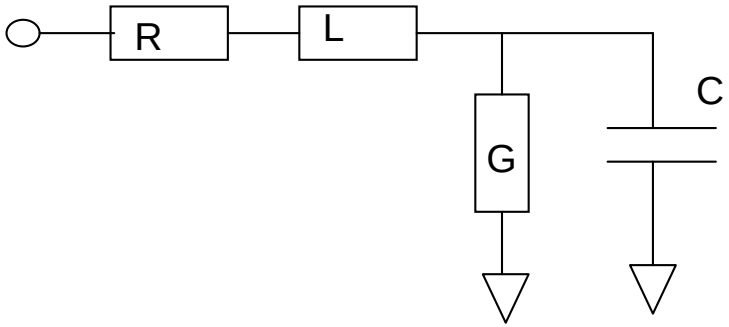
γ = sqrt((R + jωL)(G+jωC))
Zo = sqrt((R + jωL)/(G+jωC))
ν = 1/sqrt(L*C)

CHALLENGES : Tightly Matched PN skew through end-to-end channel
Low Dielectric Loss (Gf small, etc.)
Repeatable/low variation γ/Zo, Low temp coefficient

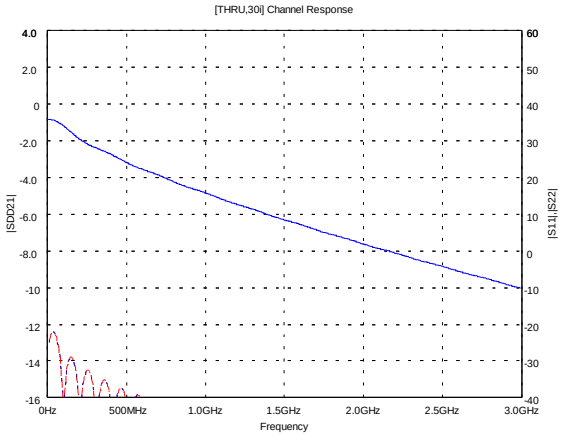
Line Characteristics : Bandwidth Loss

30i Nelco 4000-13

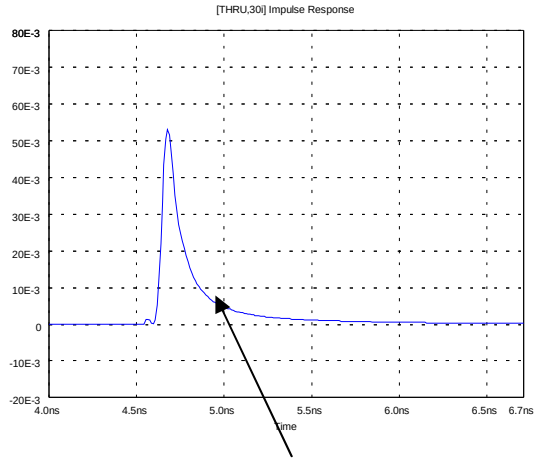
Lossy Transmission Line :



Freq Response



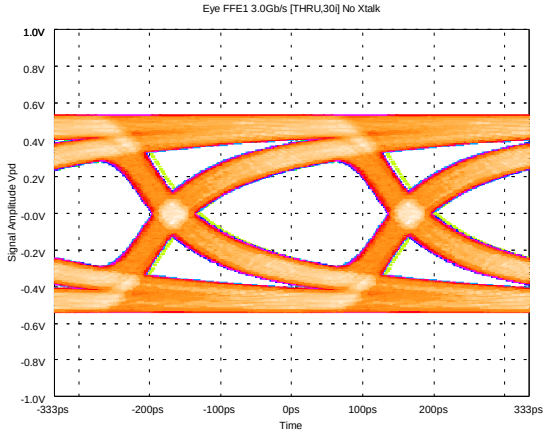
Impulse Response



Unipolar post-cursor ISI

Modern high quality board substrates (Nelco 4000-13) and cables keep the dielectric loss from dominating out to very high freq (> 10GHz), but still have conductor (skin effect) loss to deal with.

3Gb/s Unequalized eye

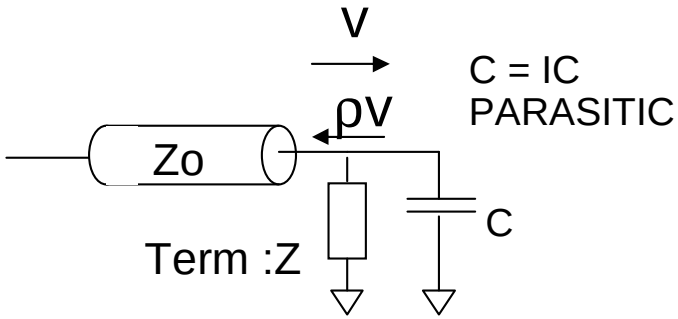


This is the easiest of the channel impairments to deal with. FFE/DFE can handle loss to 35dB+ at half-baud in absence of other impairments.

CHALLENGE : enable reliable operation with 30dB+ end-to-end channel loss at f=BAUD/2

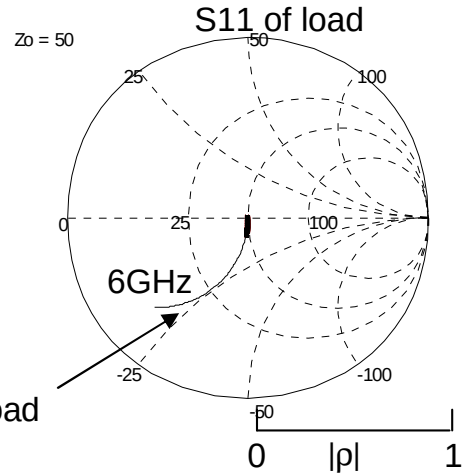
Reflections from Load Mis-match and Via Stubs

1) Load Mismatch



Reflection coefficient :ρ = (Z - Zo)/(Z+Zo)

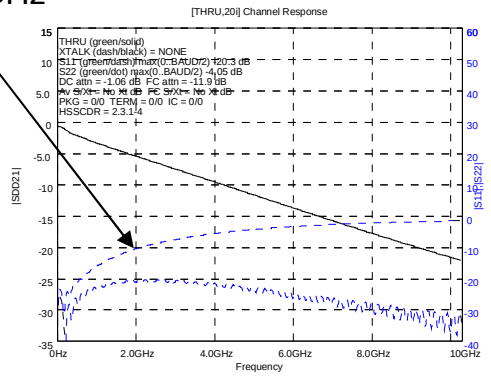
Results in level loss, sets
Up standing waves/reflections



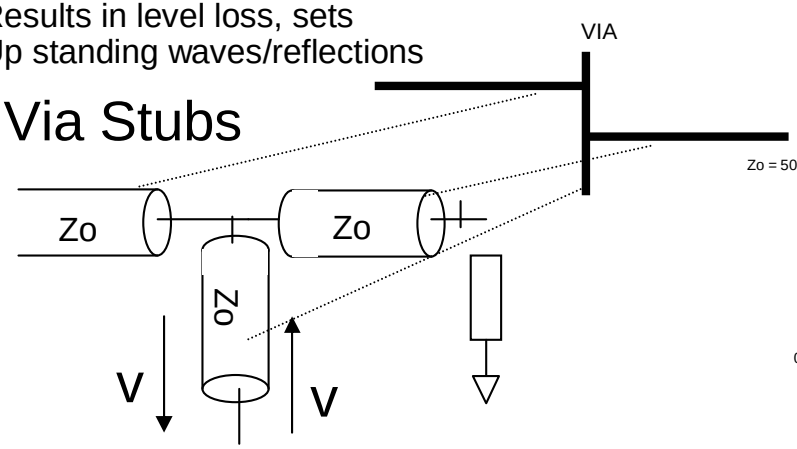
Example 20" T-line at 10.3Gb/s
with 1000fF load

11.6dB attenuation
At 5GHz

-10dB S11
at 2GHz

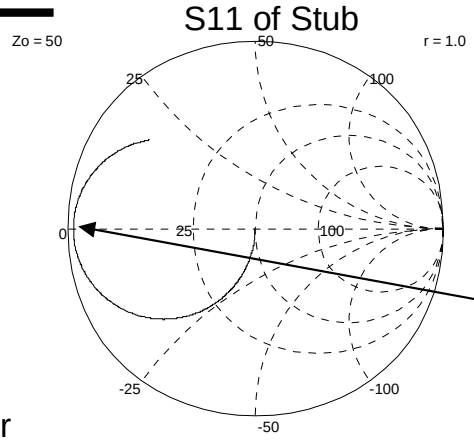


2) Via Stubs

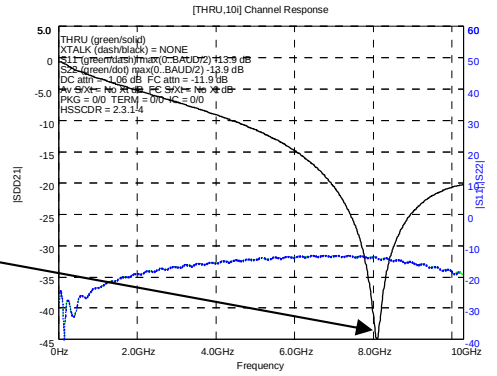


Z = infinity, ρ = 1.0

Adds notch in frequency Domain. Notch goes lower
In frequency as via stub length (i.e. board thickness)
Increases. Results in large level loss at resonance,
Signal Time dispersion

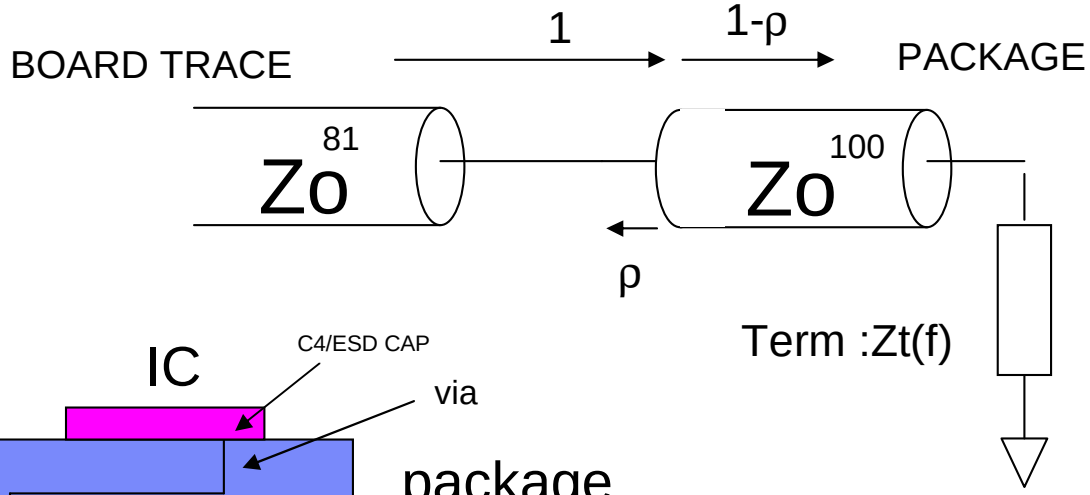


11.9dB attenuation
At 5GHz

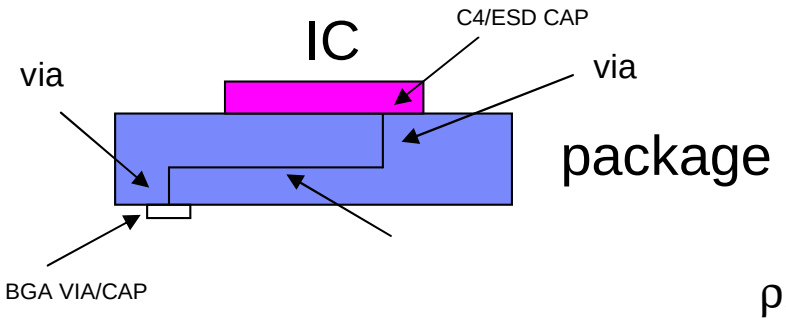


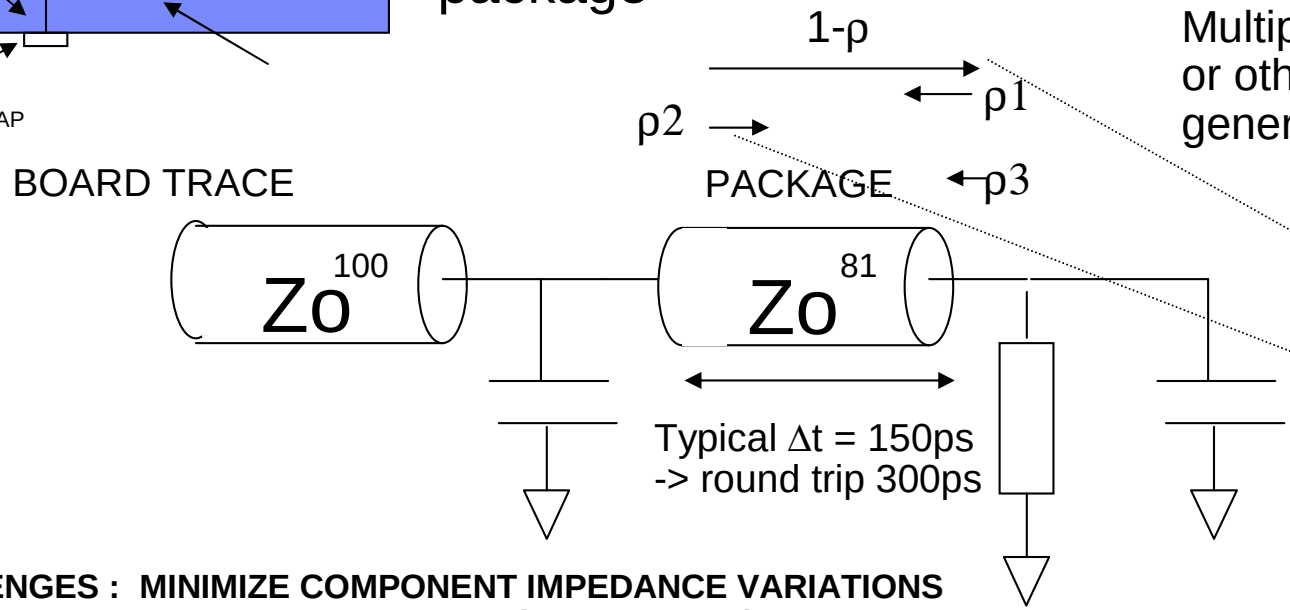
CHALLENGES : LOWER PARASIC LOAD C (T-COIL, ETC.)
ELIMINATE VIA STUB (BACKDRILL, ETC.)

Reflections from Non-Homogenous Components

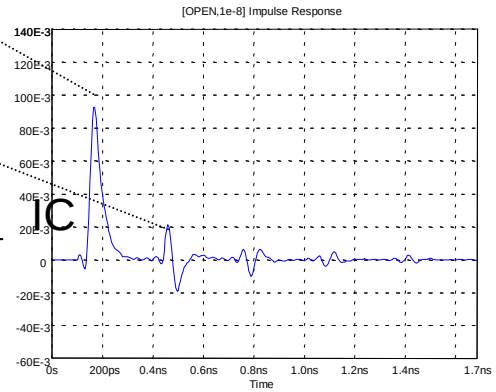


ρ= (Z - Zo)/(Z+Zo) =
(81-100)/(81+100) = -0.1
10% signal level gone back up line, loses signal level (most benign reflection)





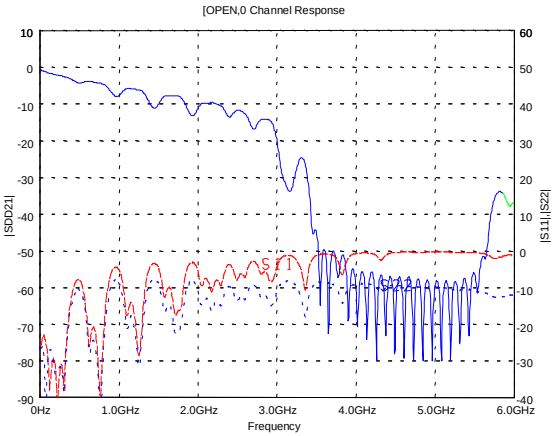
Multiple Reflections in package or other link components generate ISI, not just loss!



CHALLENGES : MINIMIZE COMPONENT IMPEDANCE VARIATIONS
MINIMIZE PARASITICS (BGA cap, etc.)

Un-Equalizable ISI from Reflections

Freq Response



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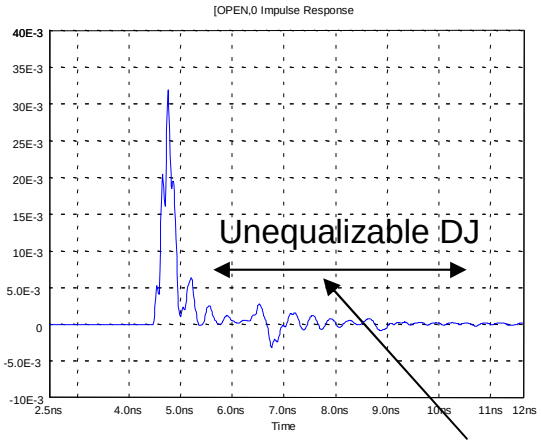
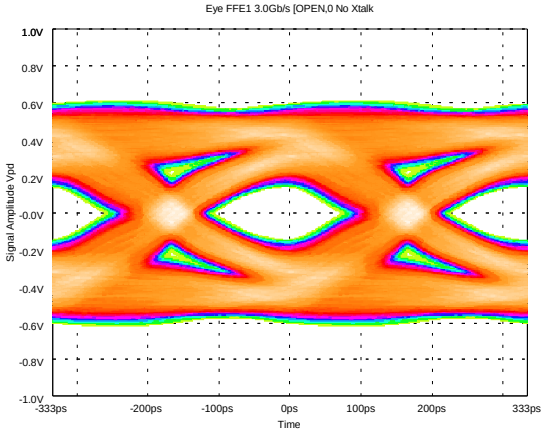


FFE DOESN'T EQUALIZE (NOT UNIPOLAR)
DFE DOESN'T REACH

3Gb/s Unequalized eye

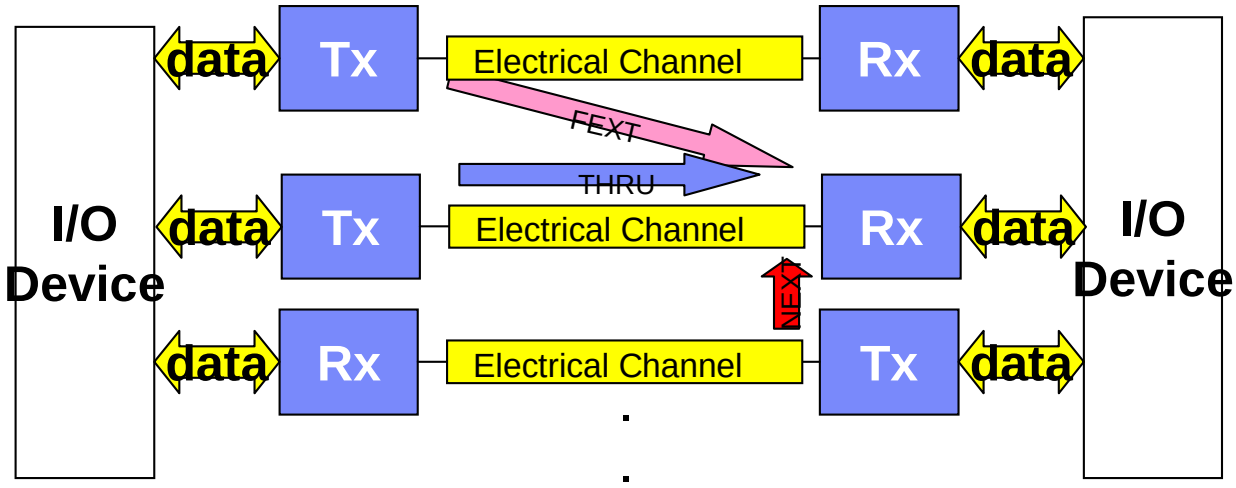


Eye Degradations :

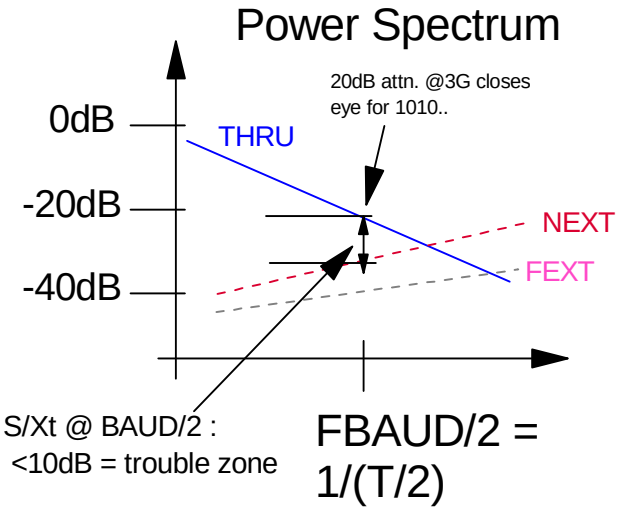
1) Large Unequalizable DJ
2) Asymmetric eye, off center

CHALLENGE :
Operate in presence of reflections on short, low-loss channels with significant impedance variation and/or impedance discontinuities.

Channel Characteristics : Crosstalk

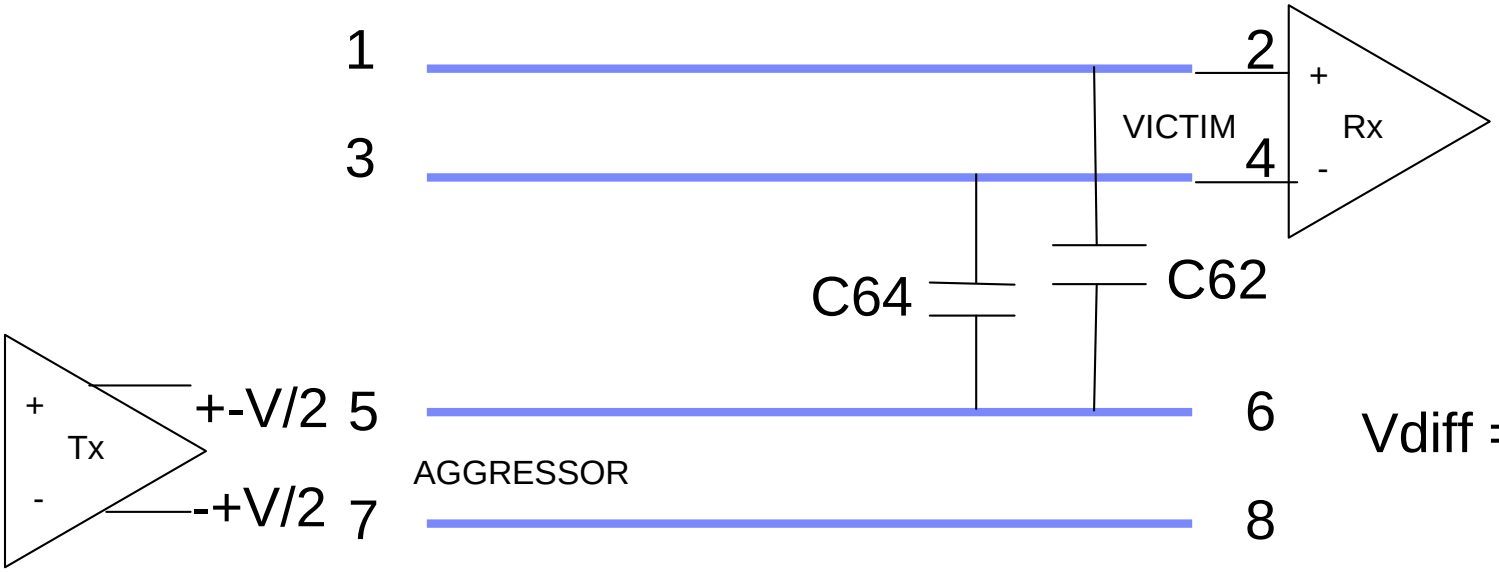


THRU : Through-Channel
NEXT : Near-End Crosstalk
FEXT : Far-End Crosstalk



CHALLENGE :
Keep S/Xt > ~10dB at half baud rate on lossy channels.

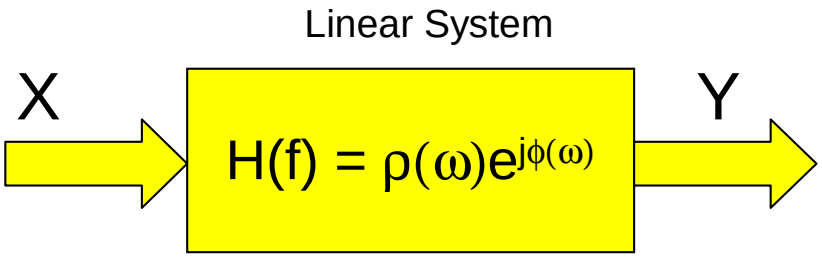
Differential Mode Crosstalk Suppression



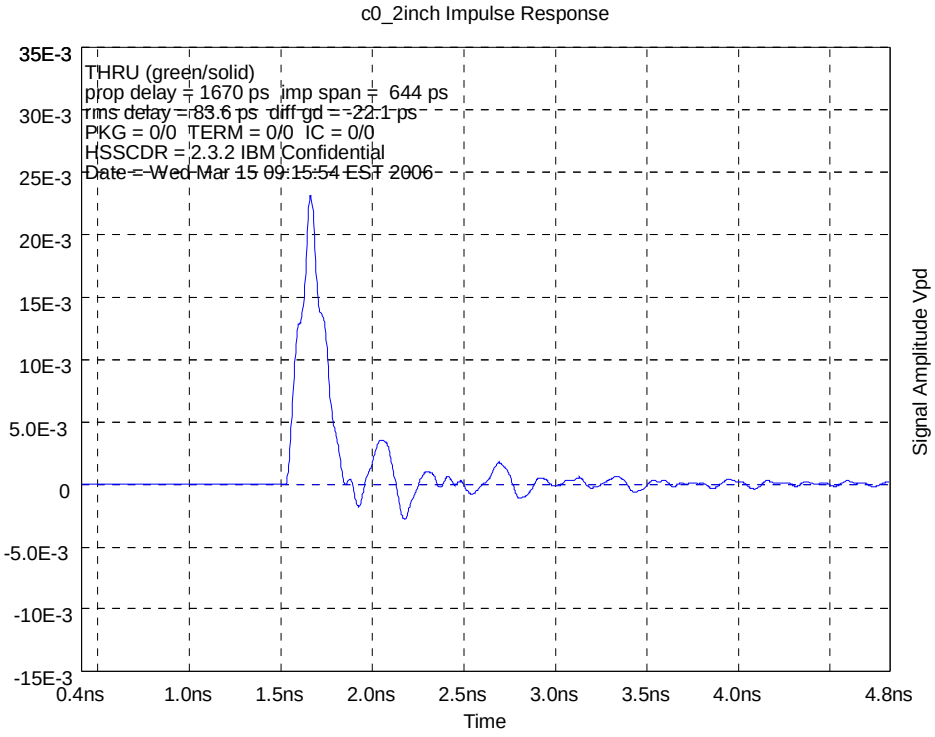
Single-ended drive on diff channel = ½ drive on single-ended (SE) for same received signal swing.
Therefore closest aggressor couples ½ noise onto nearest victim
-> 6dB (2x) inherent crosstalk suppression for diff mode vs. SE

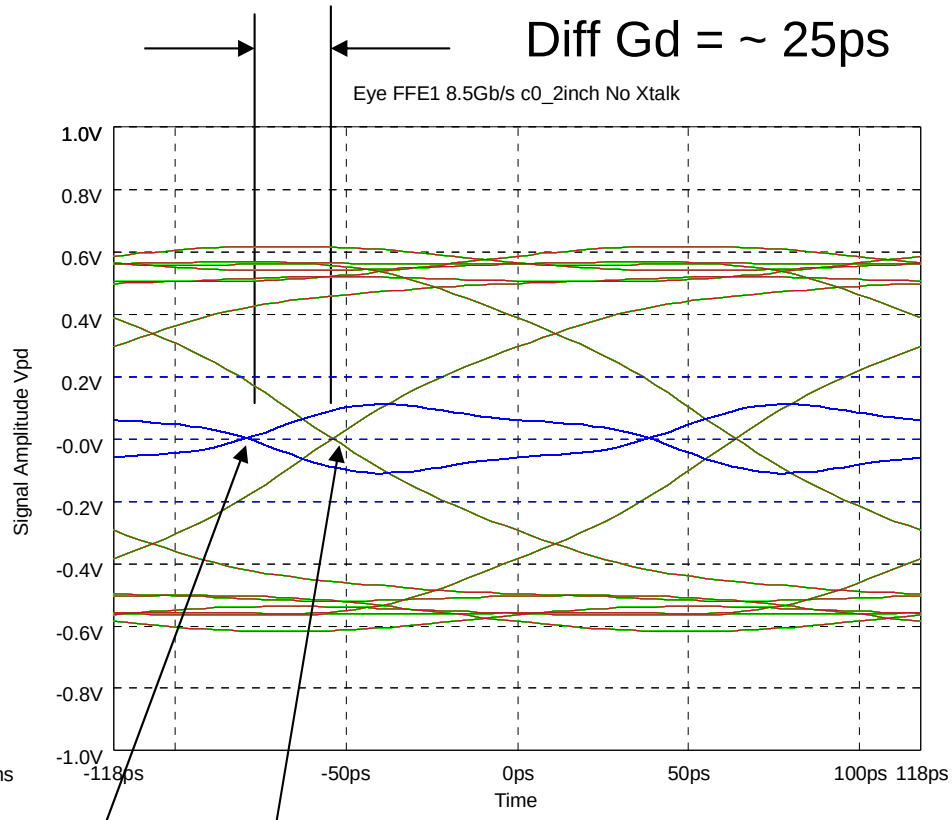
More crosstalk suppression is realized when closest aggressor couples correlated signal onto opposite-polarity victim line.
-> common-mode crosstalk noise is rejected by differential amplifier

Channel Characteristics : Differential Group Delay



Group Delay : $\tau(\omega) = -d\phi(\omega) / d\omega$



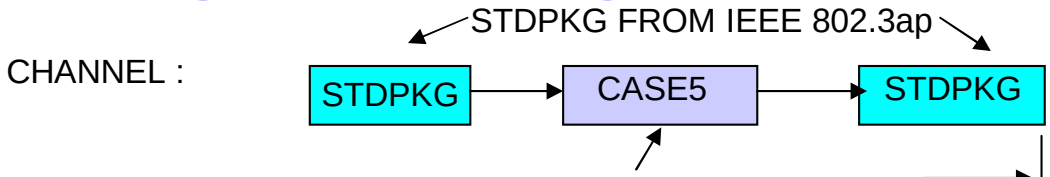


Example xaui 2” test channel

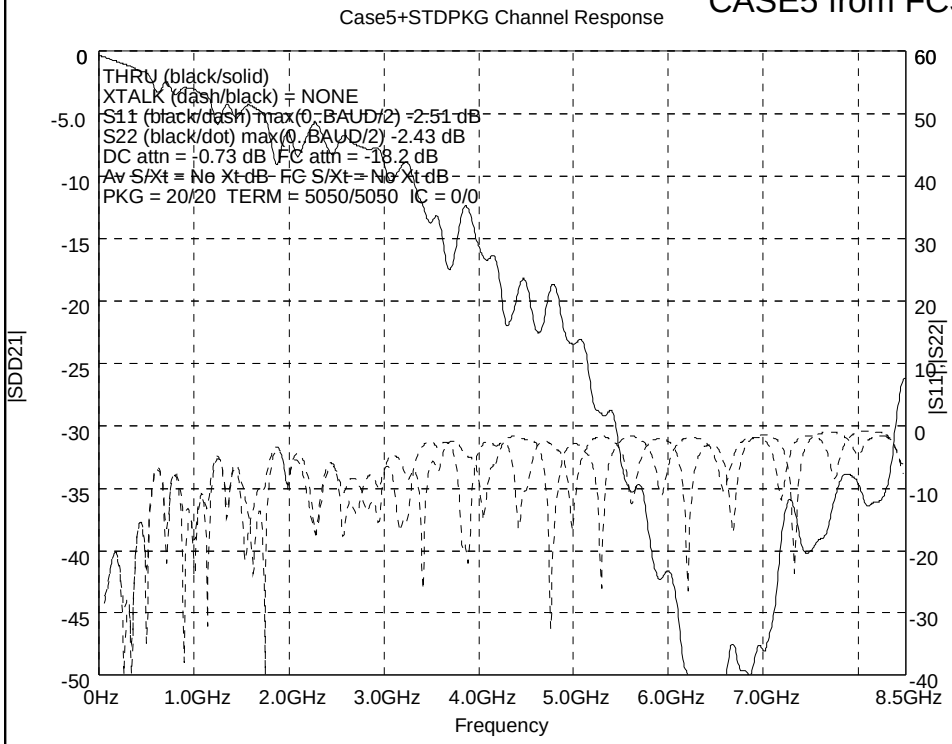
High-Freq crossing

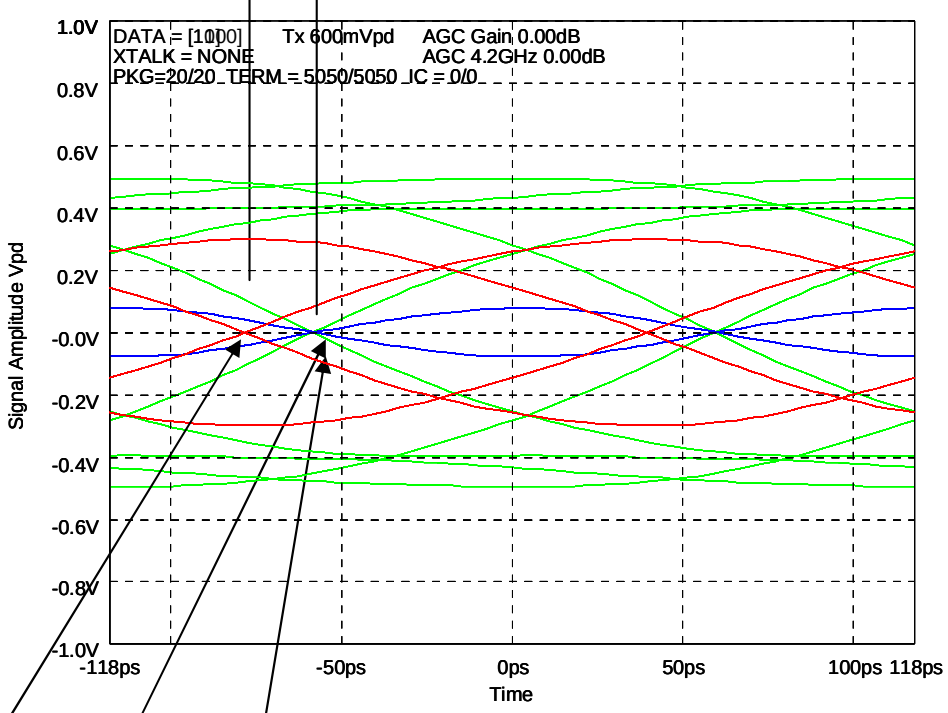
Low-Freq crossing

Edge Crossing Data Pattern Dependency



"Diff Gd" = ~ 20ps





Med-Freq Crossing (11001100) red

High-Freq Crossing (10101) blue

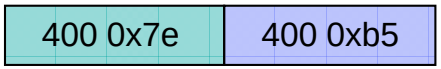
Low-Freq Crossing (1111100000), green

CHALLENGE :
Data-dependent CDR bias if scrambling not used to break up repeated patterns.

Data Dependency Test Patterns for CDR

JTPAT (Jitter Tolerance Pattern)

octet data



The JTPAT octet data generates the following 8/10 encoded bit stream :
Low Freq Run length (RL) = 3,4 High Freq Run length (RL) = 1
1000011100011110001110000….. Followed by 10101010101010101010101

CJTPAT (Compliant Jitter Tolerance Pattern)

JTPAT payload data in a “compliant” frame format

PROBLEM WITH JTPAT AND CJTPAT :
Not enough random data content to excite sufficient ISI patterns after
CDR is biased, can give a false-confidence in eye opening while
the CDR is biased a large amount. These are not necessarily worst case test patterns.
To address this problem a new data dependency stress-test format was defined :

DJTPAT (Data interleaved Jitter Tolerance Pattern : not a standard, defined here)

octet data:

High freq (RL 1) Med freq (RL 2) Low freq (RL 3 and 4)

This pattern excites 1010, 11001100, and low freq patterns, followed by randomized data
to eliminate false confidence in non-random data test patterns (JTPAT/CJTPAT)
20 of the above sequences are generated with different random data in each sequence.

Data Scrambler breaks up DJTPAT and CJTPAT : Proposed to FCS 8.5Gb, Accepted
Recommend use of data scrambling in ALL high rate serial links!

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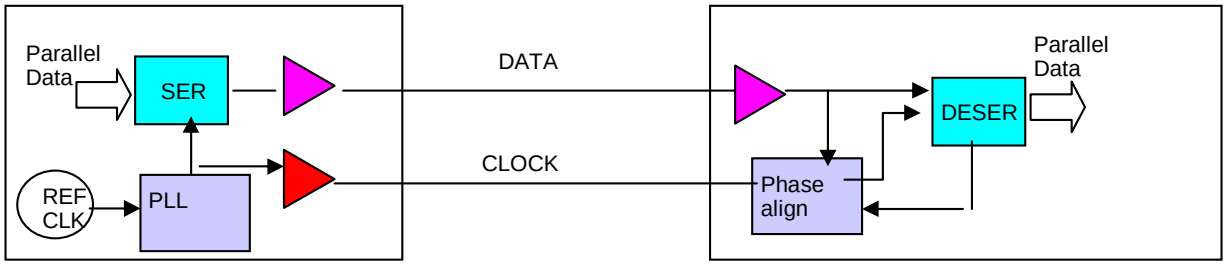
Classes of SERDES I/O

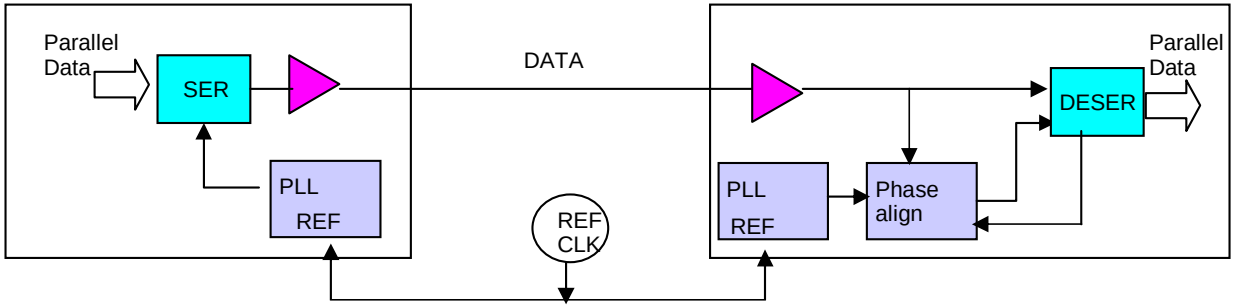
1) Source Synchronous (forwarded clock) : short, low-loss links (CPU-MEM)



PRO : TRACKS CLOCK RJ WELL

CON : EXTRA CLOCK LINE
CLOCK/DATA DESKEW IN LONG LINE
NOISE PICKUP ON CLOCK
PHASE NOISE FLOOR dBc INCREASE IN LONG LINE WITH LOSS IN CLK AMP

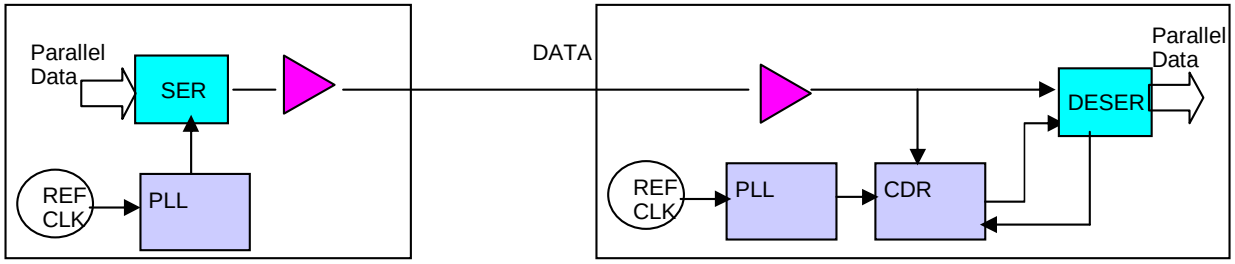
2) Mesochronous (common clock reference frequency)



PRO : GETS RID OF CLOCK LINE
STILL SOURCE SYNC

CON : TX/RX BOTH NEED PLL
TX/RX NOISE DECORRELATE
NOISE CORRELATES ONLY IN PLL BW

3) Asynchronous (no common reference frequency)

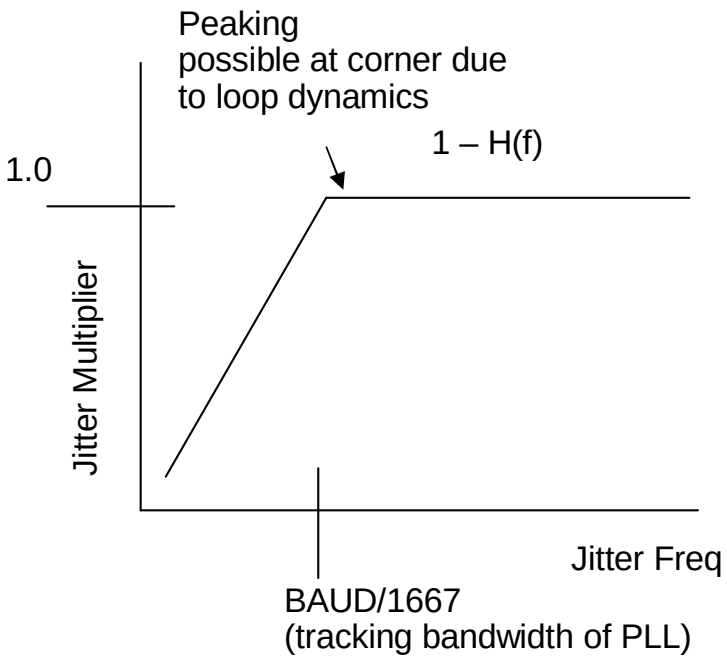


PRO : NO COMMON CLOCK NEEDED AT TX/RX
GOOD FOR LONG LINES

CON : CDR MUST TRACK PHASE AND FREQ BOTH
NO T/R NOISE CORRELATION
CDR MUST TRACK PHASE NOISE OUT

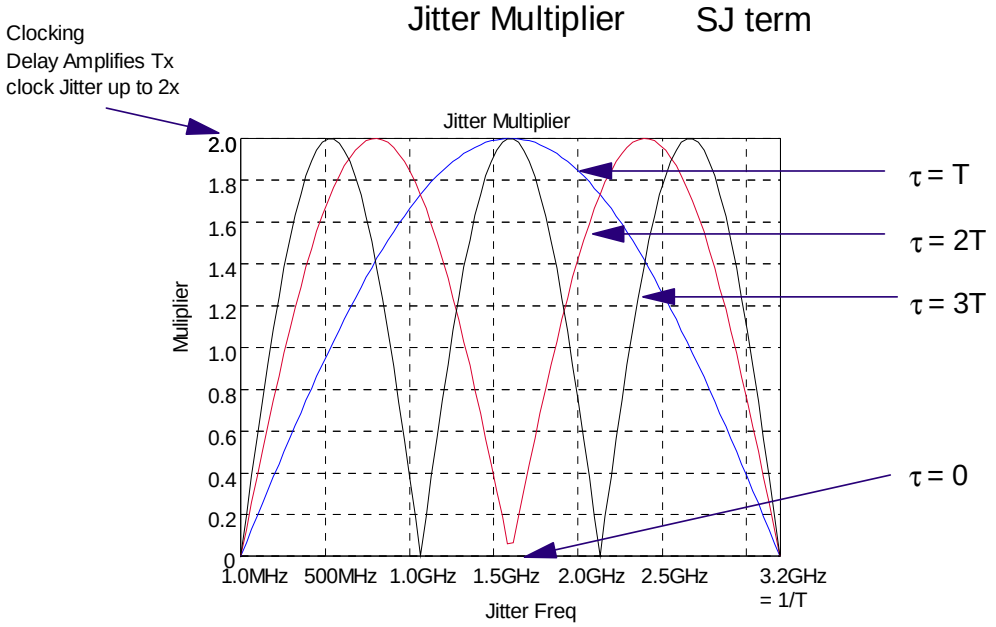
Jitter Suppression vs. Clocking Method

ASYNC CDR Jitter Suppression



Jitter Multiplier = 1 – H(f)
H(f) = CDR Transfer Function
PRO : No jitter amplification (if H(f) good)
CON : need control loop (PLL) to track jitter

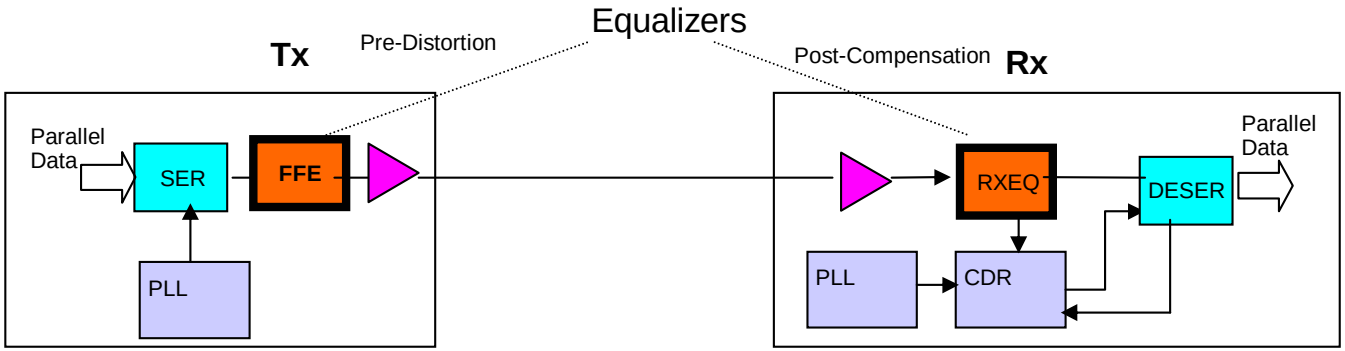
Forwarded Clock Jitter Suppression



Jitter Multiplier = 2 sin ($\pi * f * \tau$)
τ= delay from clock to data

PRO : Large “automatic” jitter suppression at low freq with no control loop/PLL
CON : Amplifies jitter 2x in regions, less suppression as clock and data get separated

SERDES with Line Equalization



Transmitter Adds Feed-Forward Equalizer used commonly due to ease of realization of tapped delay line @ Tx

Receiver Adds Equalizer

Possible Variants :

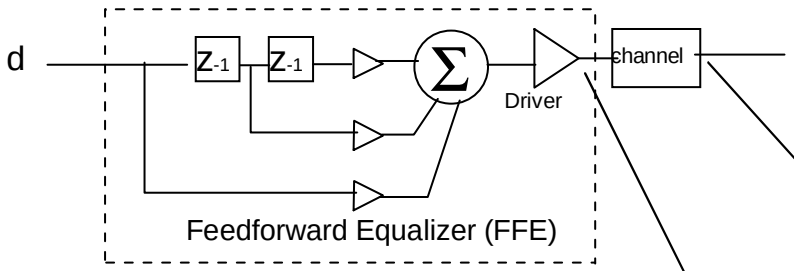
- LINEAR (FFE) FIXED
- LINEAR (FFE) ADAPTED
- DFE FIXED
- DFE ADAPTED
- LINEAR FIXED DFE ADAPTED
- LINEAR ADAPTED DFE ADAPTED

THIS IS A GOOD COMBO. POWERFUL ENOUGH TO BLIND EQUALIZE CHANNEL WITH NO TX FFE IF ENOUGH LINEAR FFE RANGE AVAILABLE

Challenge : maintain low power/area IO Core while giving high performance line equalization. Power efficiency goals for I/O in range of 20-30mW/Gb/s are challenging for 5-10Gb/s rates in 90, 65nm CMOS.

Feed-Forward Equalization

Linear T-spaced FFE

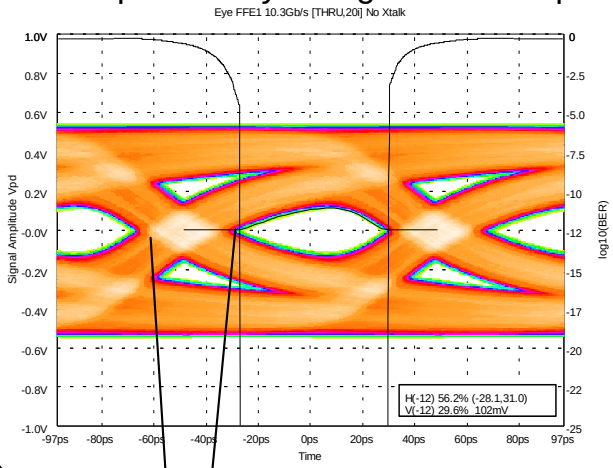


Tx FFE effectively lowers low-frequency waveform envelope to level of high frequency, also compensates group delay

~500mvp

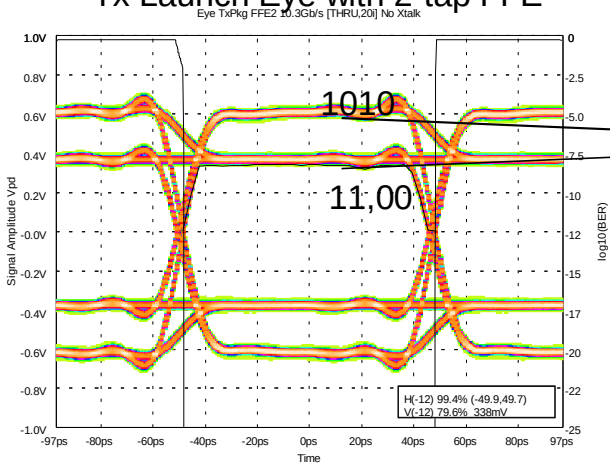
Example 20” T-line at 10.3Gb/s

Un-Equalized Eye Diagram : 50% open

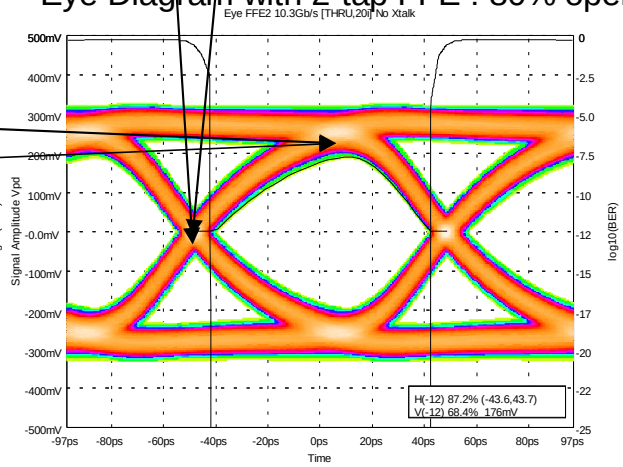


- **Problems Addressed by FFE**
  - **No feedback settling time problems as in DFE**
  - **Low-power, low area method for line equalization**
  - **Compensates line group delay**
  - **FFE compensates unipolar ISI over wide time span**
- **Problems with Tx FFE**
  - **Lower signal level @ Rx due to de-emphasis @ Tx**
  - **Decreases SXR (Signal/Crosstalk Ratio)**
  - **Decreases SNR (Signal/Noise Ratio)**
  - **Increases effect of line reflections**
  - **Tx FFE needs a back-channel from Rx for adaptive equalizer**

Tx Launch Eye with 2-tap FFE

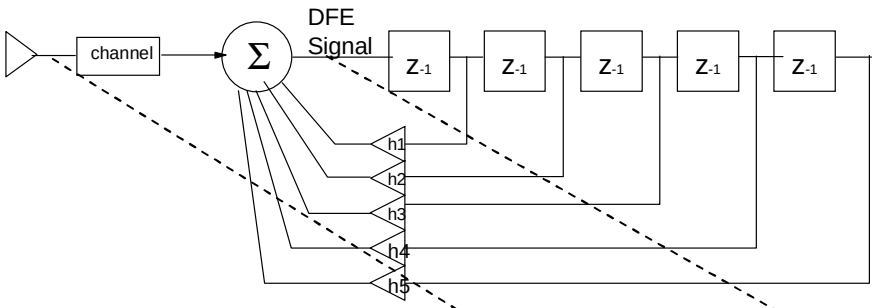


Eye Diagram with 2-tap FFE : 80% open



Receiver Equalization : DFE

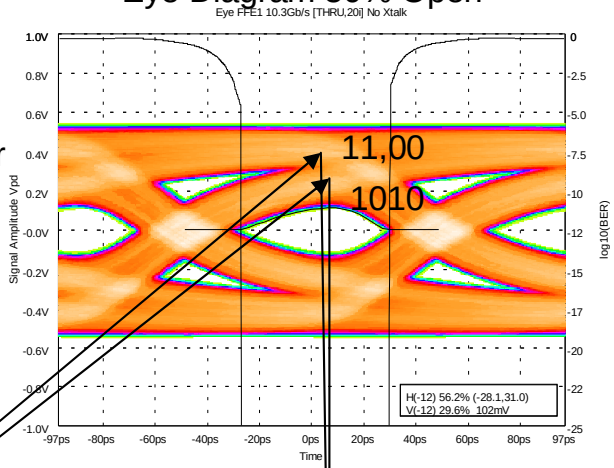
Nonlinear Equalizer :
Feeds back limited estimates of Rx data



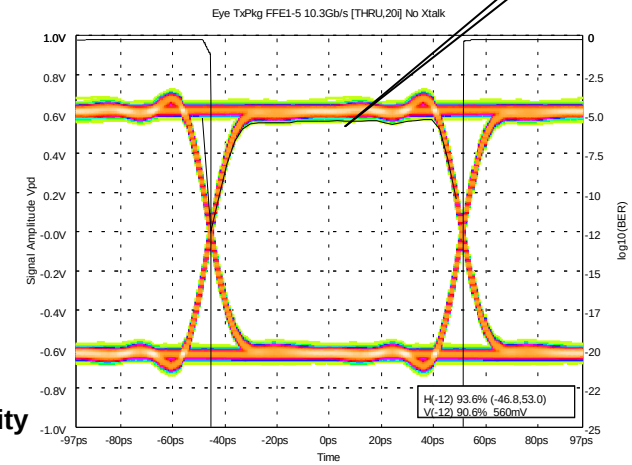
Rx DFE cancels post-cursor ISI at the data sampling time with no high-frequency noise amplification due to the non-linear feedback

Example 20" T-line channel at 10.3Gb/s

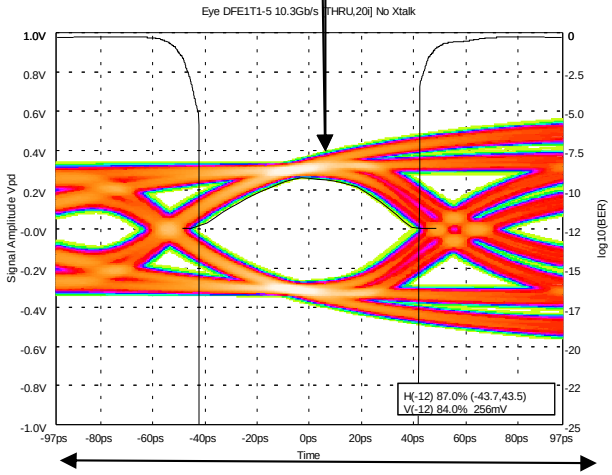
Eye Diagram 50% Open



Tx Launch Eye with 1-tap FFE



Eye Diagram with 5-tap DFE 87% Open



Problems Addressed by DFE

- Larger signal @ Rx due to less de-emphasis @ Tx
- Greater SXR
- Greater SNR
- More energy in low-frequency regime where match is better

Problems with DFE

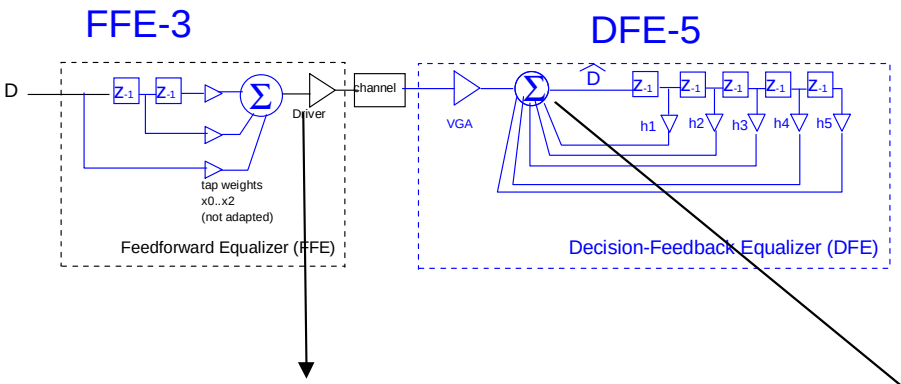
- Error propagation tendency due to non-linear feedback
- Need Linear Rx DFE sum
- Increases power draw and area
- Settling time of feedback
- Adaptation algorithm -> adds logic complexity
- Does not compensate pre-cursor ISI
- Only cancels ISI over a fixed time span = DFE length

DFE feedback held constant across 2UI to illustrate "DFE eye"

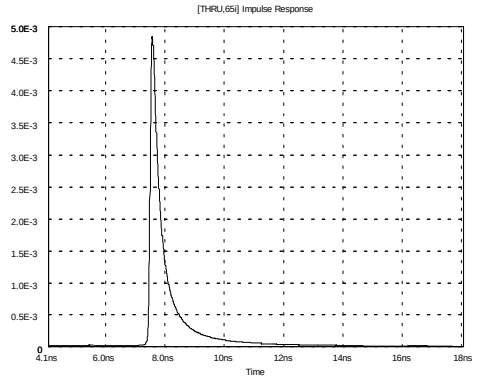
Transmitter FFE/ Receiver DFE Equalization

FFE/DFE = Powerful combination…potential to handle large line loss, Example 32dB loss channel at 5GHz.

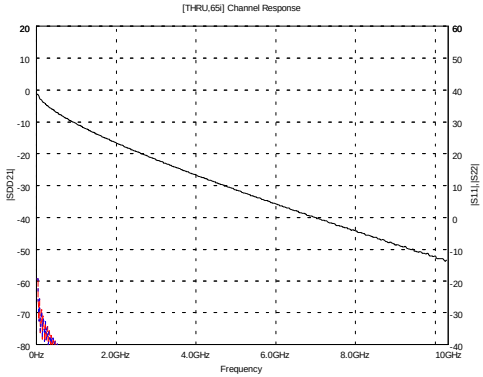
Example 65” T-line at 10.3125Gb/s



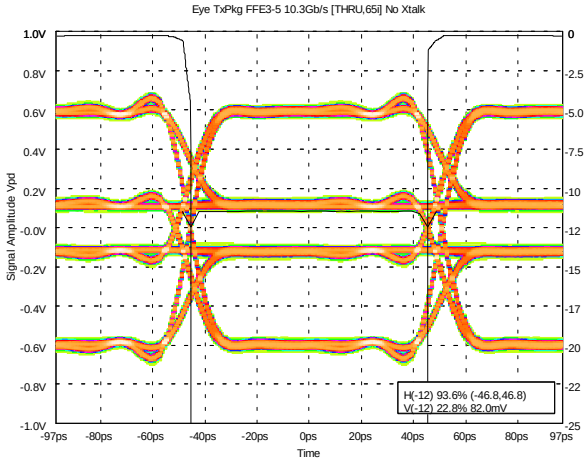
Impulse Response



32dB loss at 5GHz



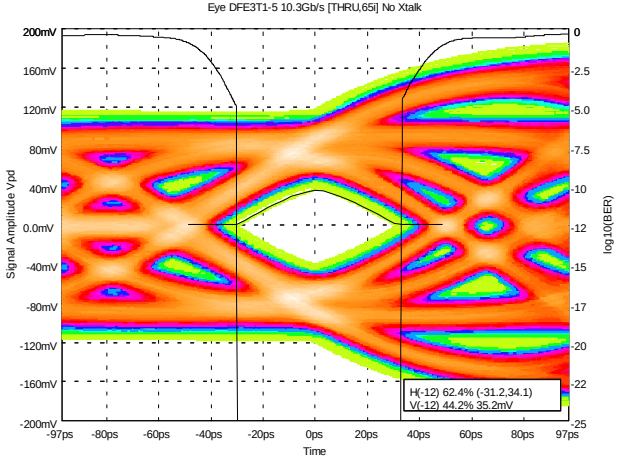
Tx Launch Eye with 3-tap FFE



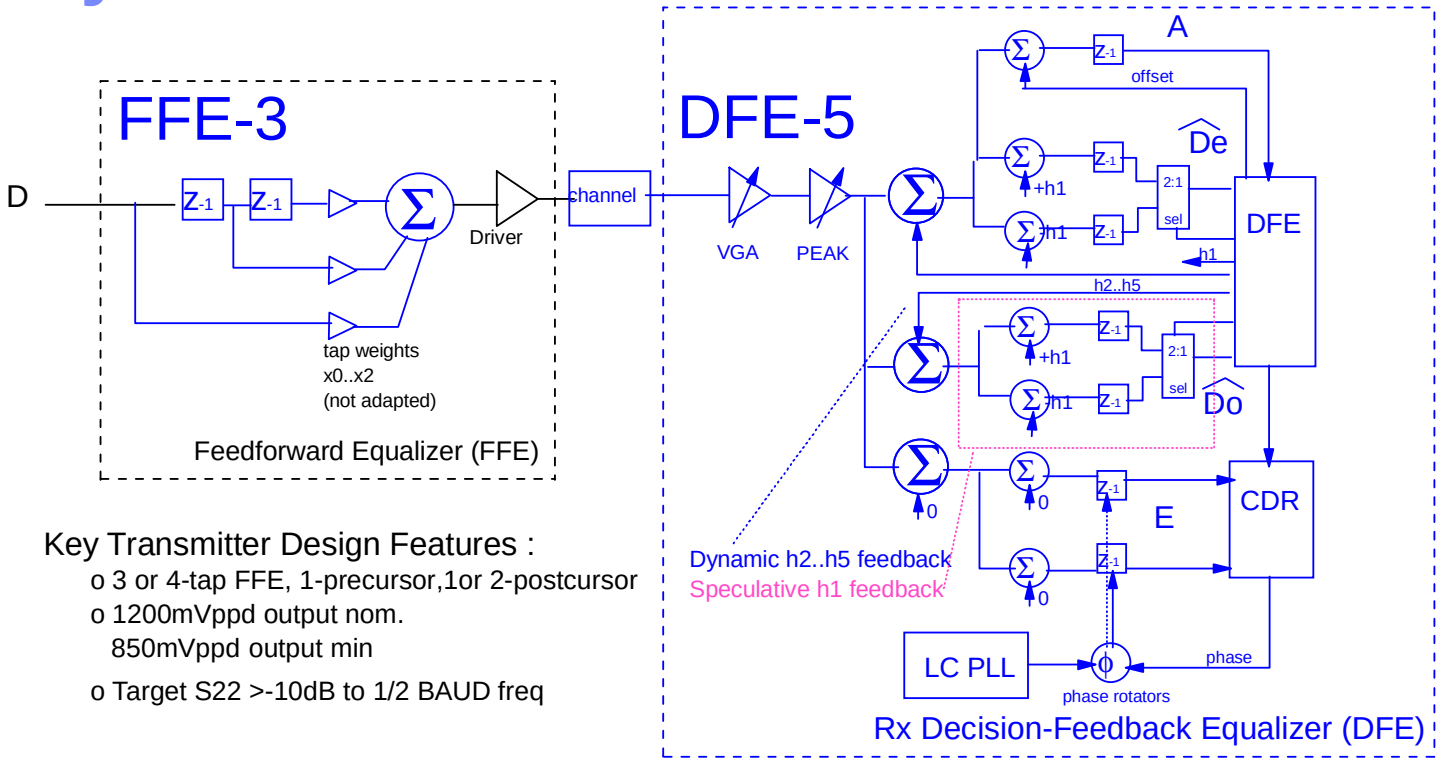
FFE compensates ISI > 5 bits distant, Equalizes group delay

DFE enables less FFE to be used, fine tunes channel equalization for 0 ISI in range of 1-5 bits delayed.

DFE Eye Diagram FFE3-DFE5 62% Open



System Architecture for 6-10Gb/s FFE/DFE[1]



Key Transmitter Design Features :

- o 3 or 4-tap FFE, 1-precursor,1or 2-postcursor
- o 1200mVppd output nom.
  850mVppd output min
- o Target S22 >-10dB to 1/2 BAUD freq

Tx and Rx :

- o Target S21 for minimal loss at 1/2 BAUD freq
- o Term R from 42 to 58 ohm SE or better,
- o Clocks <1% RMS RJ (TX+Rx)
- o Power : 130nm 43mW/Gb/s (6.4G product)
  90nm 30mW/Gb/s (10G prototype)

Key Receiver Design Features :

- o VGA to maintain linearity for DFE
- o Combination of 1/2 rate architecture
  + speculative 1st-tap feedback with dynamic h2..h5 feedback to enable operation of DFE to 10Gb+
- o Target S11 >-10dB to 1/2 BAUD freq
- o Low jitter LC PLL (0.5% UI RMS RJ typ)

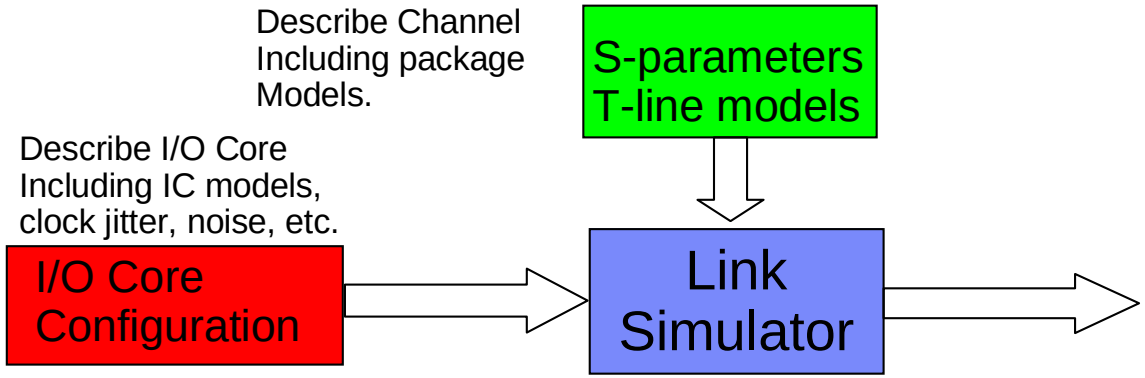
Challenges : PVT variations increasing, VDD going down vs. process : 130nm->90nm->65nm->45nm->30nm->…
Keep power and area under control while realizing high performance equalizer

[1] Michael Sorna et al. , ISSCC2005, “A 6.4Gb/s CMOS Serdes Core with Feedforward and Decision-Feedback Equalization”
Troy Beukema et. al. IEEE J. Solid State Circuits, “A 6.4Gb/s CMOS SerDes Core with FFE and DFE”, December 2005.
Mounir Meghelli et. al. ISSCC2006, “A 10Gb/s 5-tap DFE/4-Tap-FFE Transceiver in 90nm CMOS”
John Bulzacchelli et. Al. IEEE J. Solid State Circuits, “A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology”, December 2006

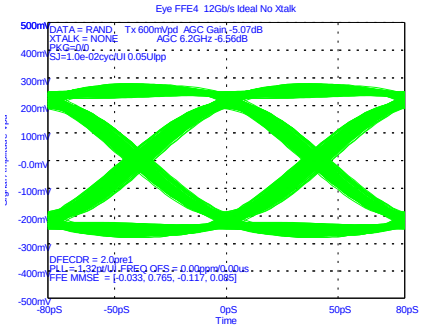
Outline

- Introduction
  - I/O Applications in modern system designs
  - Electrical Signaling Approaches
  - Line Signaling Approaches
- Electrical Channel Characteristics
  - Line Model
  - Line Degradations
- I/O core System Design
  - SERDES Architectures
  - FFE Equalization
  - DFE Equalization
  - 6-10Gb/s FFE/DFE System architecture
- Serial Link Modeling and Simulation
  - Link simulation tool
  - Eye Diagram BER Analysis
  - I/O Core Degradations
- Simulation and Measurement Results
  - IEEE 802.3ap Informative Channel Link Simulations
  - Simulated Performance vs. FFE and DFE Tap Length
  - 25Gb/s simulation results
- Summary

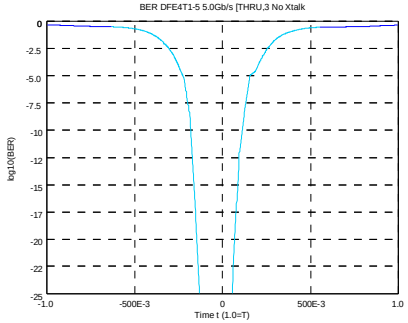
Behavioral Link Simulator



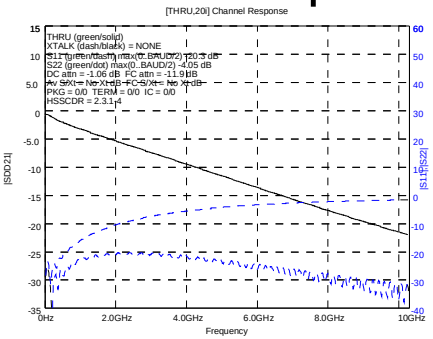
Eye Diagrams



BER Results

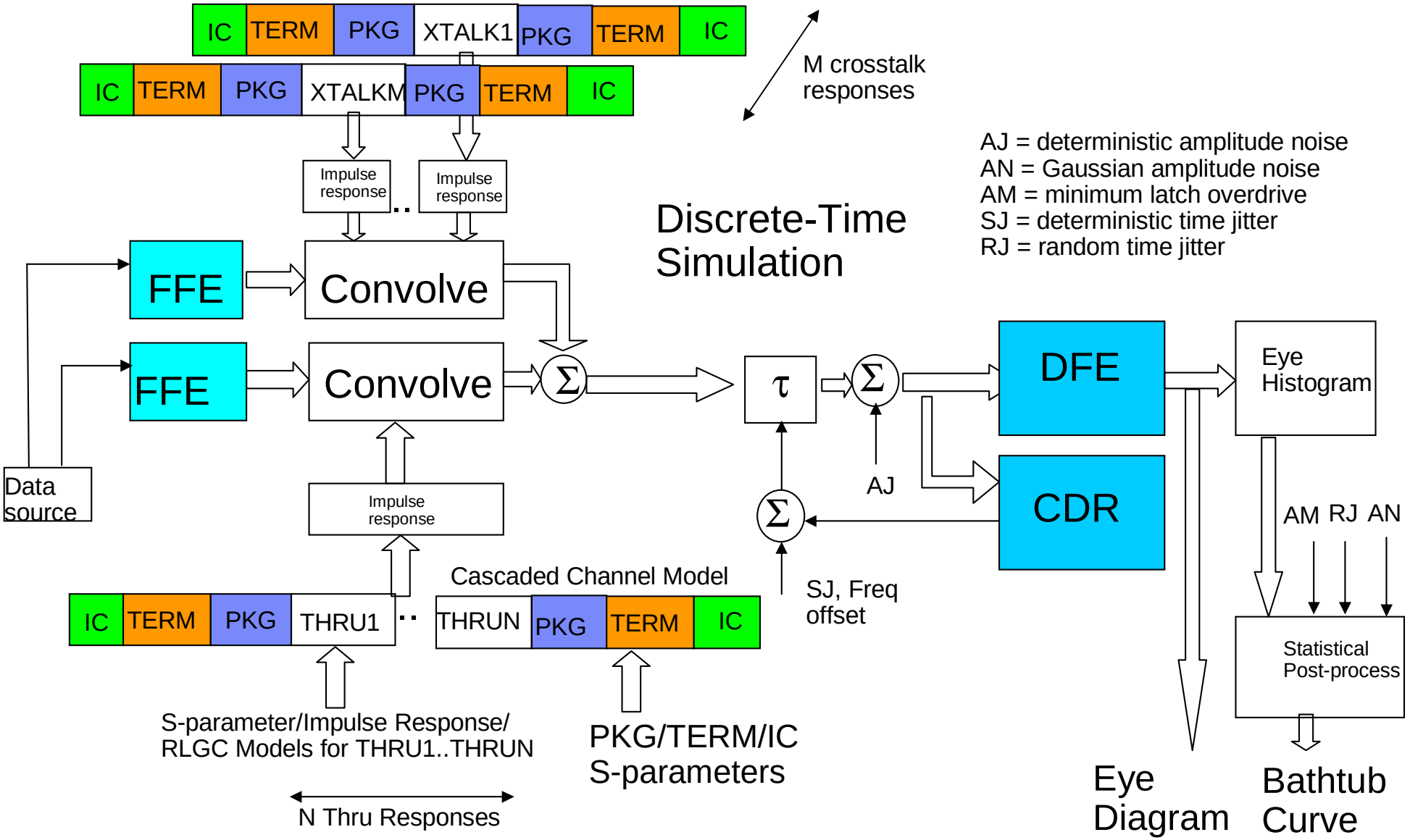


Channel Response



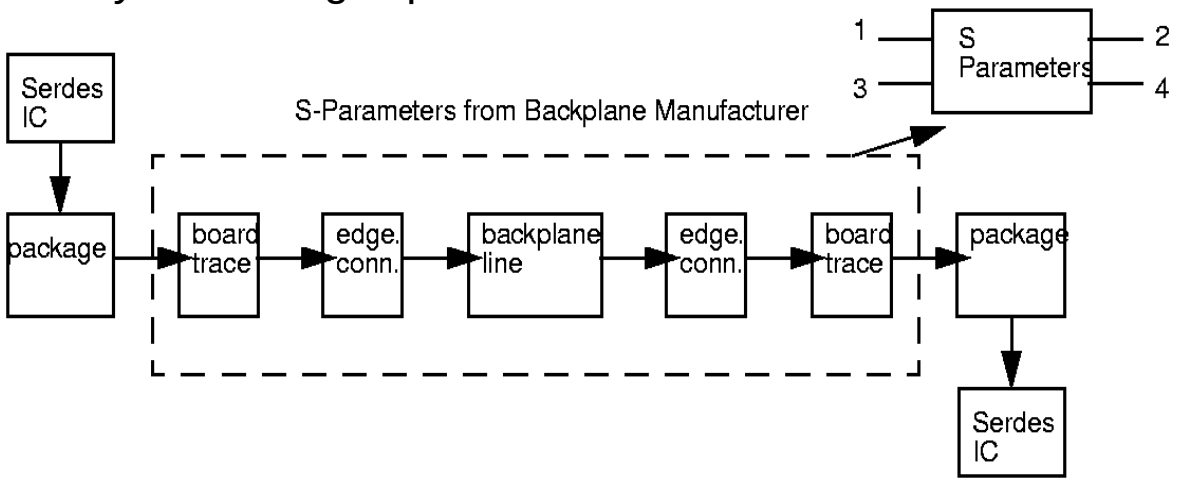
- **Inputs**
  - Link Channel Parameters (Package/IC/Thru/Xtalk responses)
  - I/O Core characteristics (CDR & DFE algorithm #FFE/DFE taps, RJ, SJ..)
- **Outputs**
  - Cascaded Channel Responses (Freq, Time, S11, delay, attn, etc.)
  - Eye Diagrams
  - Bathtub Curves (BER vs. Eye position) and BER floor
  - Vertical eye statistics
  - PLL statistics, Jitter Tolerance Plots
  - FFE tap weights and adapted DFE tap weights
- **Features**
  - Fast concatenation of high order N-ports (15 20 ports, 20 seconds)
  - 1Mb/minute typical simulation speed on modern 2GHz SSE laptop

System Diagram for Behavioral Link Simulator

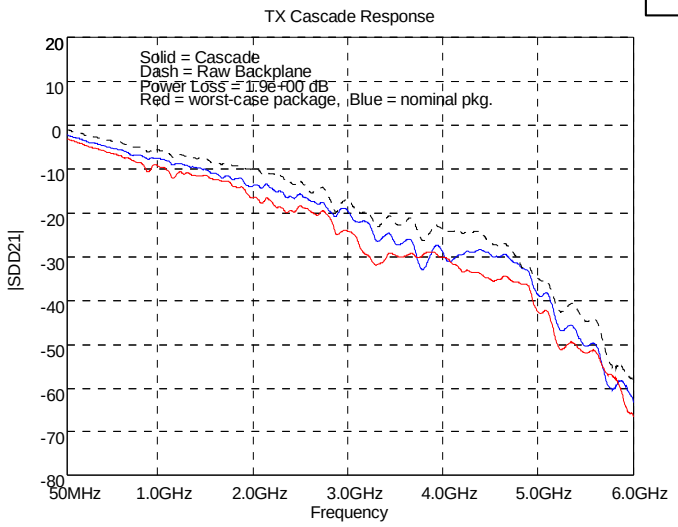


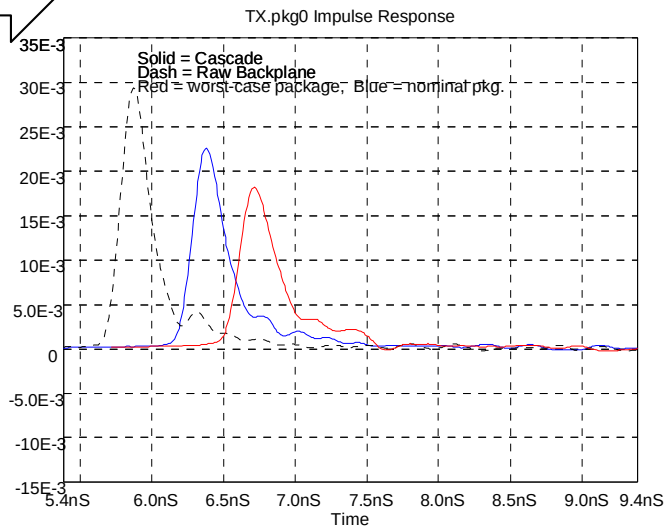
Combined Channel Model : S-Parameter Cascade

Model end-to-end link including IC/package model (driver out to Rx sample latch in)
Link constructed by cascading S-parameters of link sections



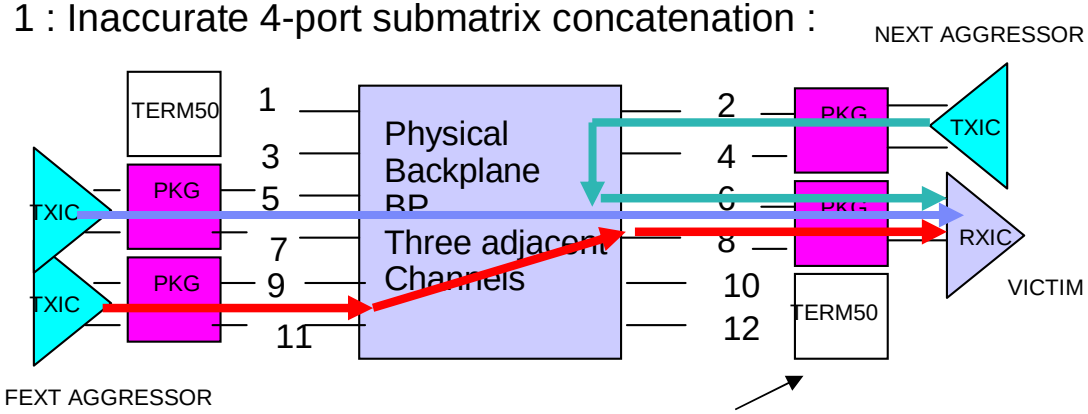
Frequency Domain SDD21 → IDFT → Time Domain





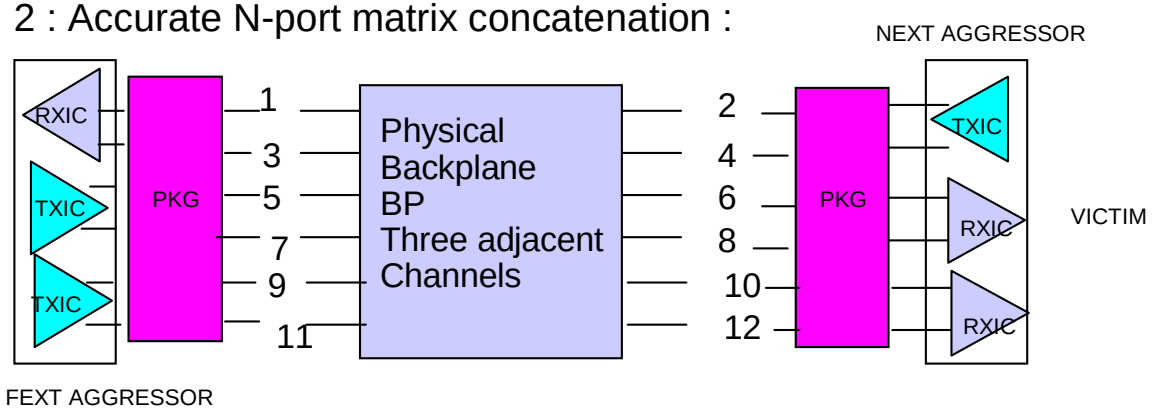
Accurate N-port Link Concatenation

1 : Inaccurate 4-port submatrix concatenation :



Implicit 50-ohm termination

2 : Accurate N-port matrix concatenation :



Challenge : Accurate N-port measurement/modeling/extraction to create IC, PKG, BP N-ports (N=12 to 28) to a frequency of 2x to 3x BAUD rate.

1 : OEM provides :
4-port submatrixTHRU : BP[5,6,7,8]
4-port submatrix NEXT : BP[2,6,4,8]
4-port submatrix FEXT : BP[9,6,11,8]

Individual 4-ports then concatenated :
T : TXIC : PKG : THRU : PKG : RXIC
N1 : TXIC : PKG : NEXT : PKG : RXIC
F1: TXIC : PKG : FEXT : PKG : THRU

This is **NOT ACCURATE** since the 4-port NEXT/FEXT/THRU are computed assuming all other ports are terminated in 50 ohm, but in real system they will be terminated in package/IC loads.

2 : OEM PROVIDES :
12-port backplane model BP

The following 12-port concatenation is done :

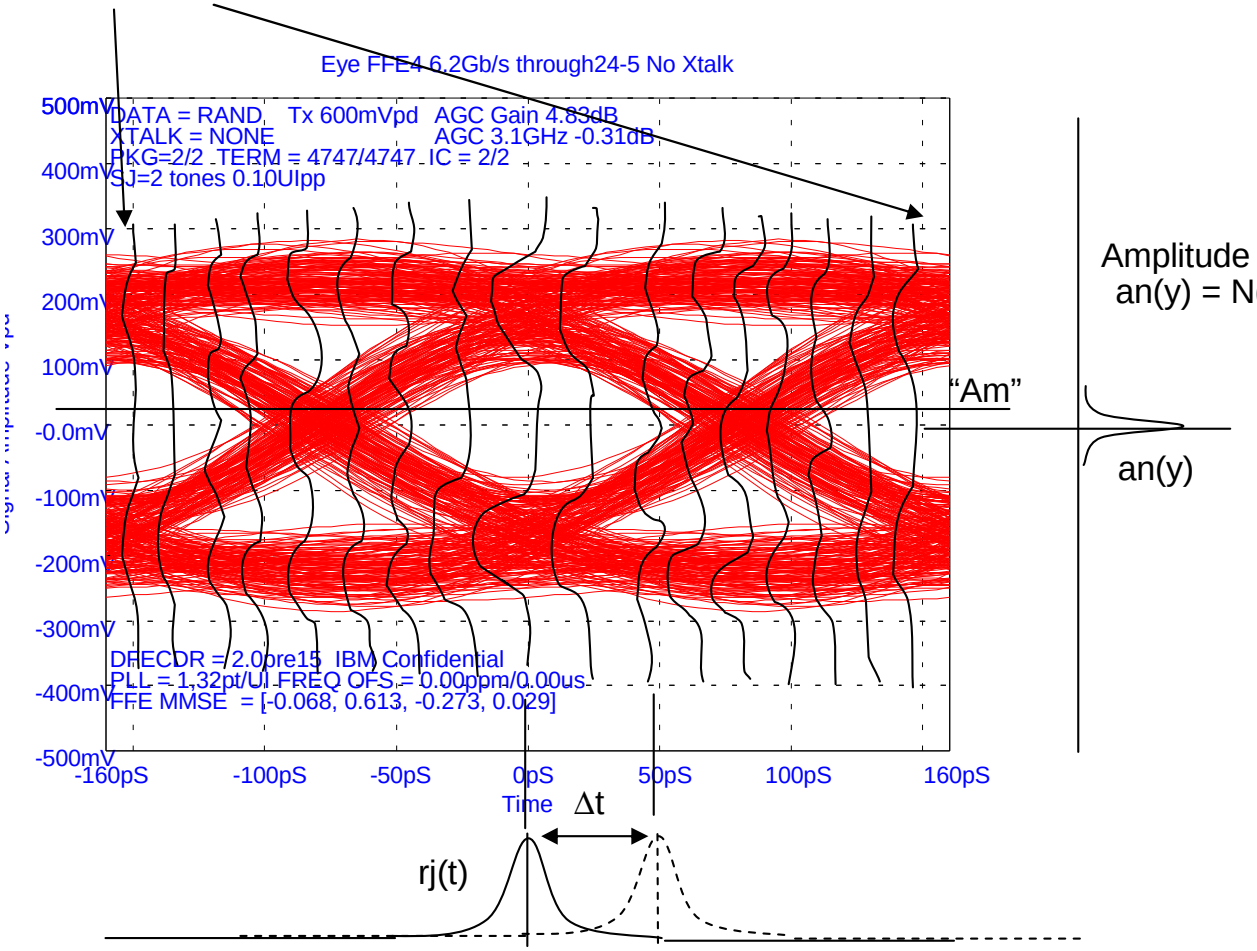
CASC = TXIC : PKG : BP : PKG : RXIC

Individual 4-ports are now taken from CASC :
T : CASC[5,6,7,8]
N1 : CASC[2,6,4,8]
F1 : CASC[9,6,11,8]

This method is accurate. Crosstalk levels are the most impacted by inaccurate approach.

Eye Diagram BER Analysis

$Py_0..Py_{64}$ = deterministic vertical eye distributions from DTS



Clock RJ distribution rj(x) = $N(\sigma_{RJ},\Delta t)$

1) Add non-deterministic Noise to vertical PDFs : convolve an(y) with $Py_i(y)$ to produce Pya_{ii}

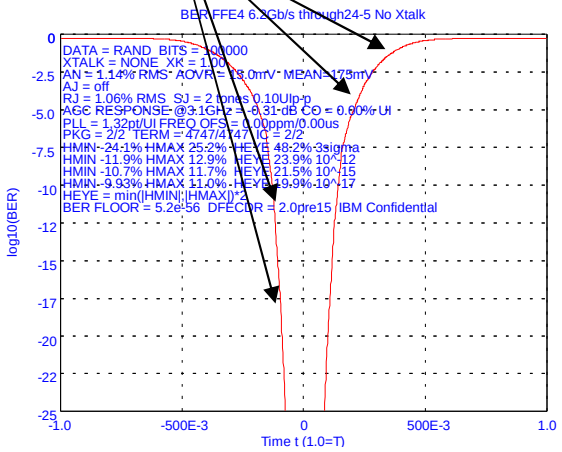
2) Build RJ weighted Sum of vertical PDFs at Each of the 65 time points.

$$Pyar_i = \frac{\Sigma\,(Pya_i\ rj(x,\Delta t_i))}{\Sigma\,(rj(x))}$$

3) BER computed from area of $Pyar_i$ below "Am" Threshold :

$$BER_i = \int_{-\infty}^{Am} Pyar_i$$

"Bathtub" Curve



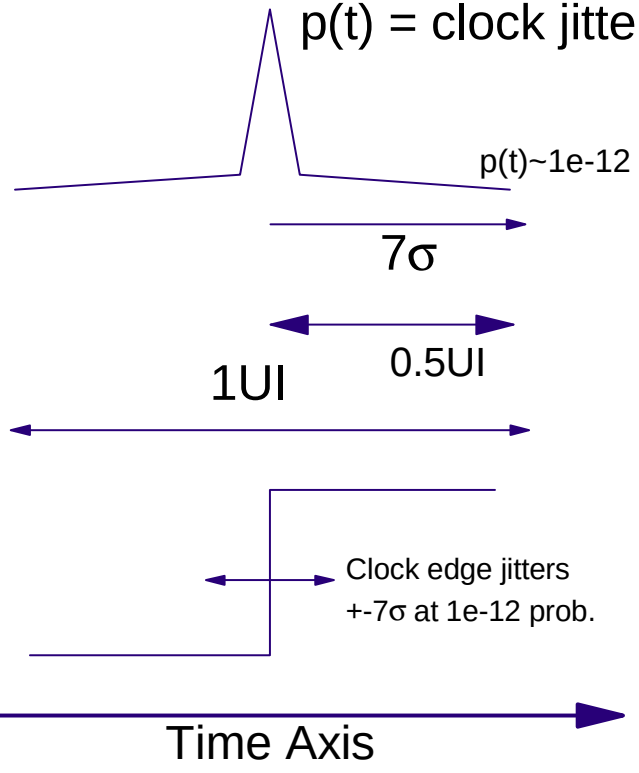
I/O Core Related Link Degradations

- Clock Jitter
  - Random Jitter (RJ) from VCO phase noise
  - Sinusoidal Jitter (SJ) from power supply clock trees etc.
  - Deterministic Jitter (DJ) from IC/package/channel
  - Duty Cycle Distortion (DCD) at Transmit Launch
- Amplitude Noise
  - Non-Deterministic Amplitude Noise (AN) (thermal/kT noise)
  - Deterministic Amplitude noise (AJ) : power-supply, switching noise
  - Crosstalk : In IC substrate/package (as opposed to line alone)
- Minimum-Latch Overdrive (AM)
  - Important for small signal swing/low V systems

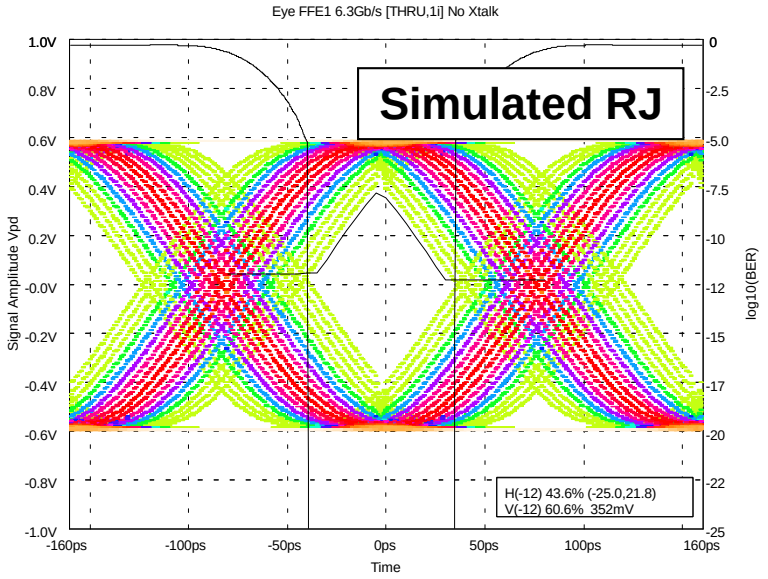
Random Jitter (RJ) Distortion

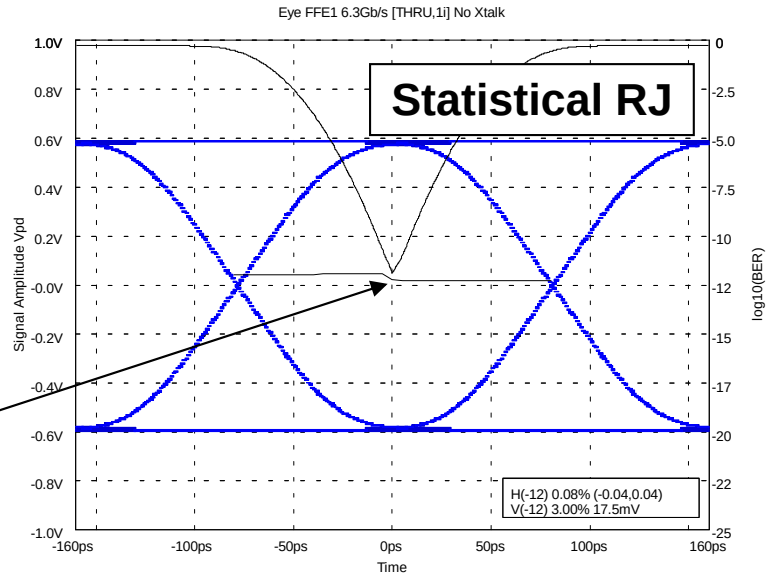
Gaussian Noise Modulates Clock Phase

p(t) = clock jitter PDF



Eye closed
RJ=50%UI /7
= 7% UI RMS



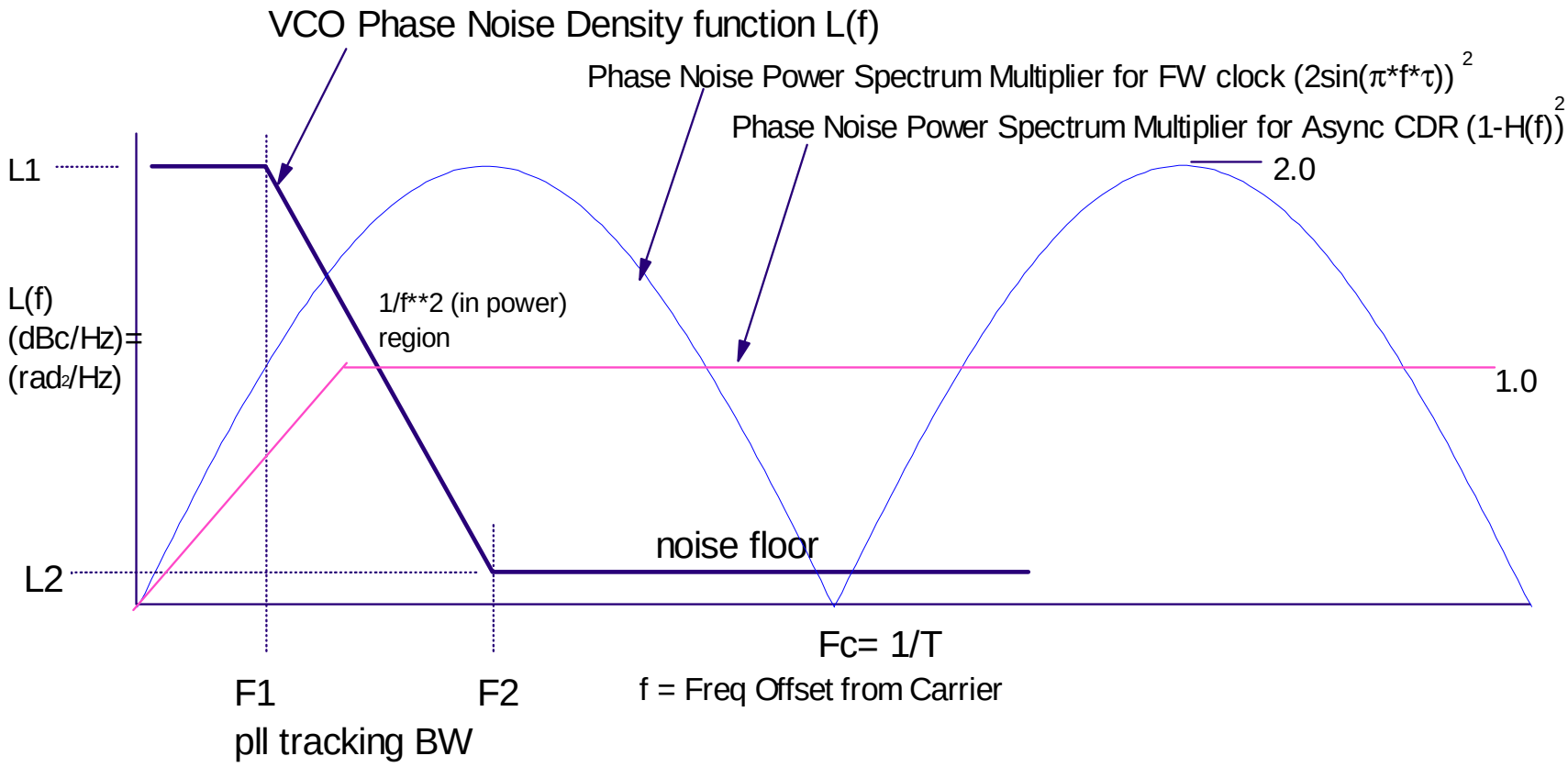


Eye closure = 14*RJ

7% RMS RJ
BER floor ~ 1E-12

CHALLENGE : KEEP TOTAL RJ FROM TX/RX < 1% RMS

RJ Computation from PLL Phase Noise



$$\text{RMS Jitter } (\tau) = \frac{1}{2\pi Fc}\sqrt{2\int_{0}^{\sim Fc/2} S^2(f) * L(f)\, df}$$

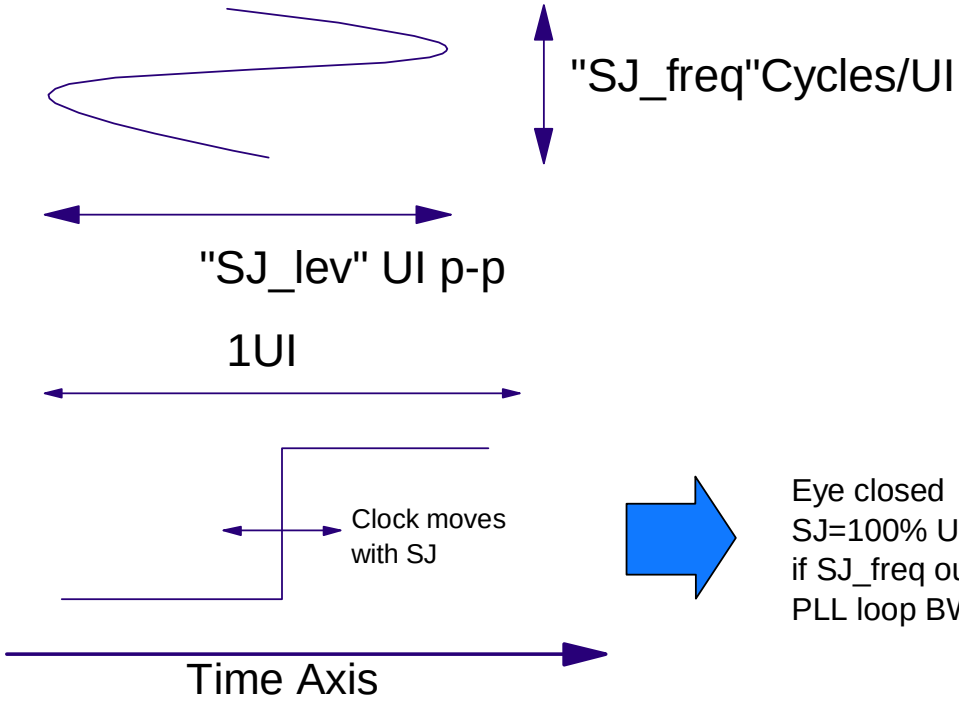
Phase Noise Multiplier :

Async CDR : S(f) = 1 - H(f)

Ssync CDR : S(f) = (2 * sin(π*f*τ))

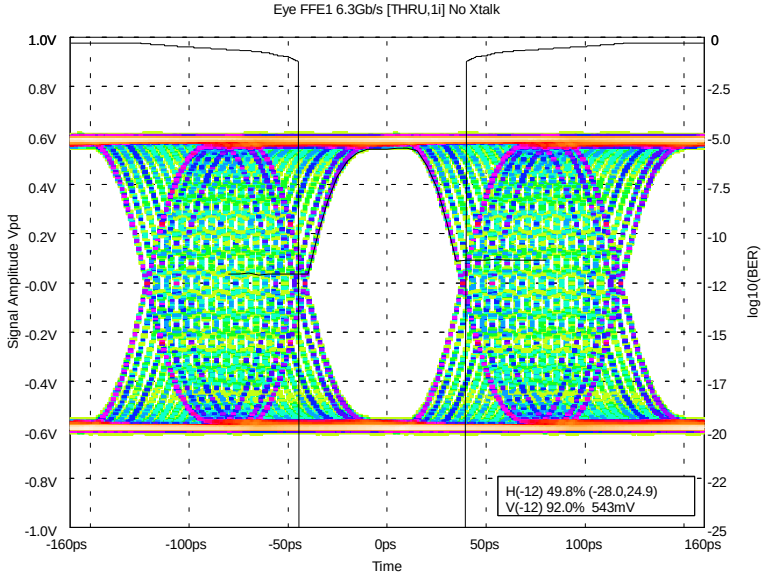
Sinusoidal Jitter (SJ) Distortion

Sine Wave Modulates Clock Phase

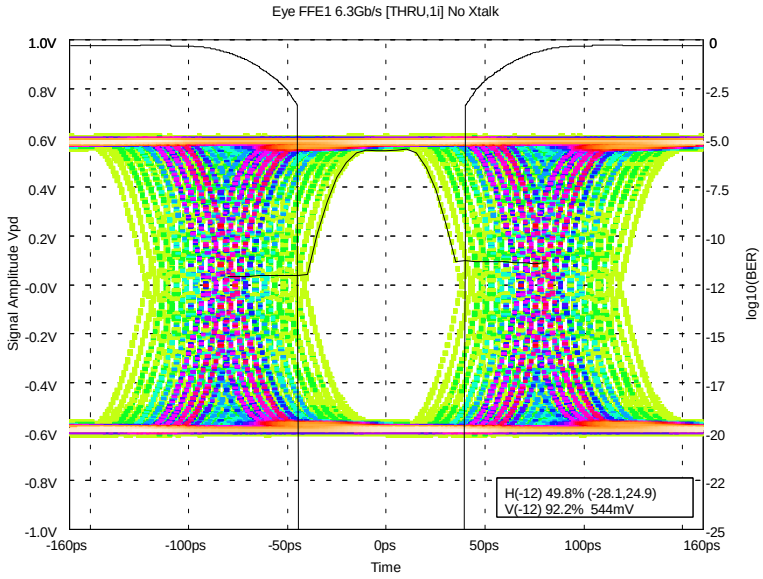


Eye closed
SJ=100% UI P-P
if SJ_freq outside
PLL loop BW

1 SJ TONE 50% UI PP

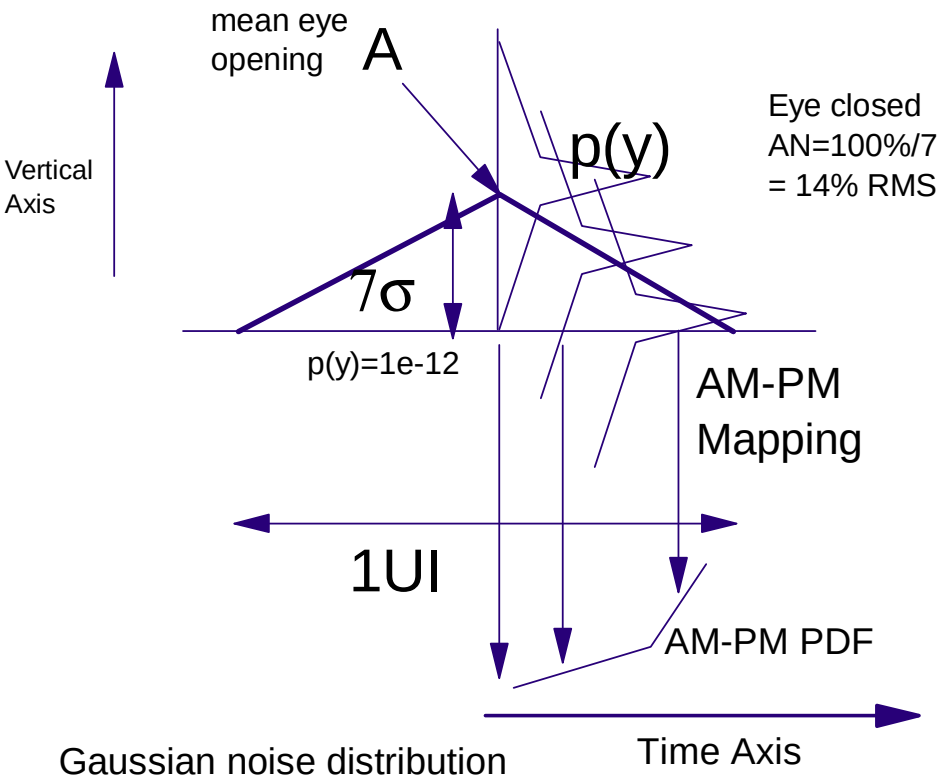


5 SJ TONES EACH 10% UI PP

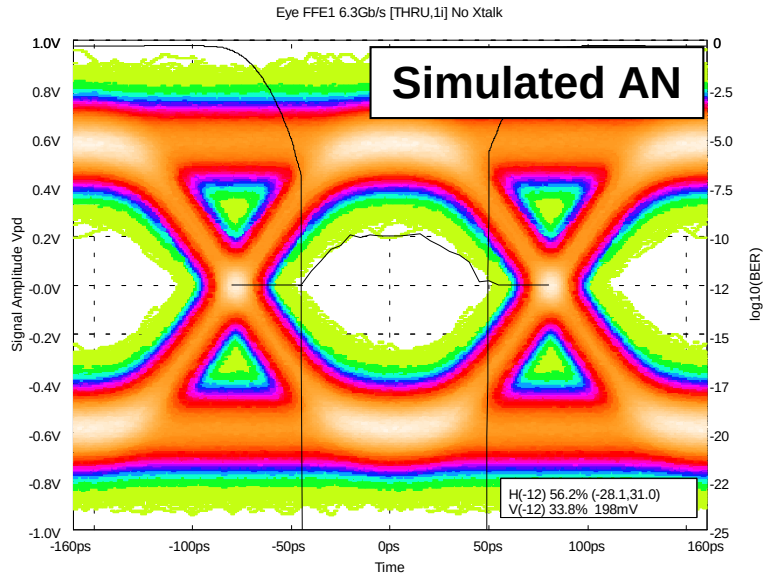


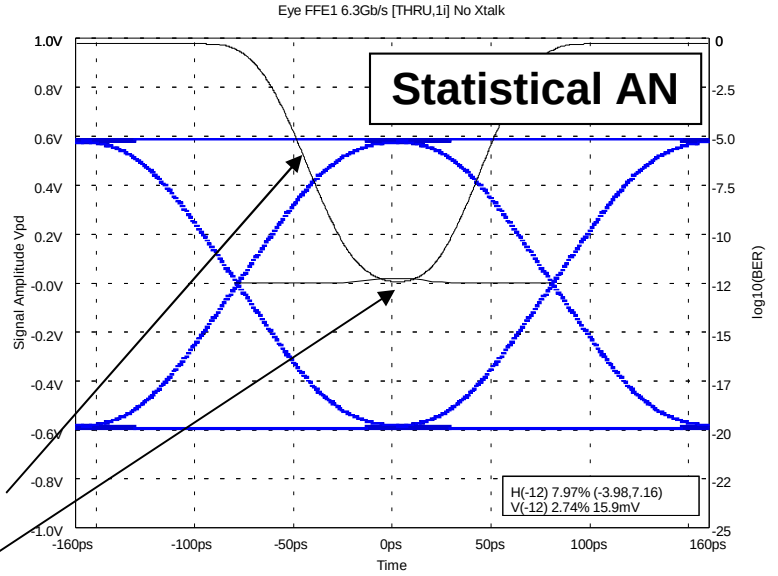
Challenge : Minimize Effect of Supply Noise to minimize SJ component of clock

Non-Deterministic Amplitude Noise



Eye closed
AN=100%/7
= 14% RMS "A"





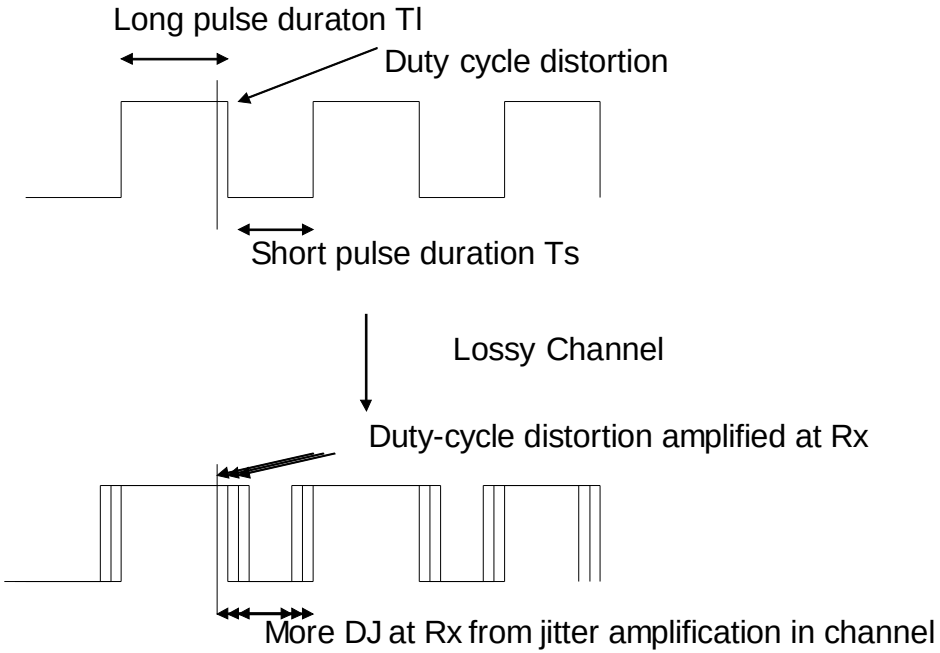
Gaussian noise distribution convolves with vertical eye distribution across eye, producing an AM-PM RJ function on time axis

AM-PM

14% RMS AN : 1E-12 BER FLOOR

Tx Duty Cycle Distortion

Signal with Duty Cycle Distortion



DCD = Ts/(Ts+Tl)

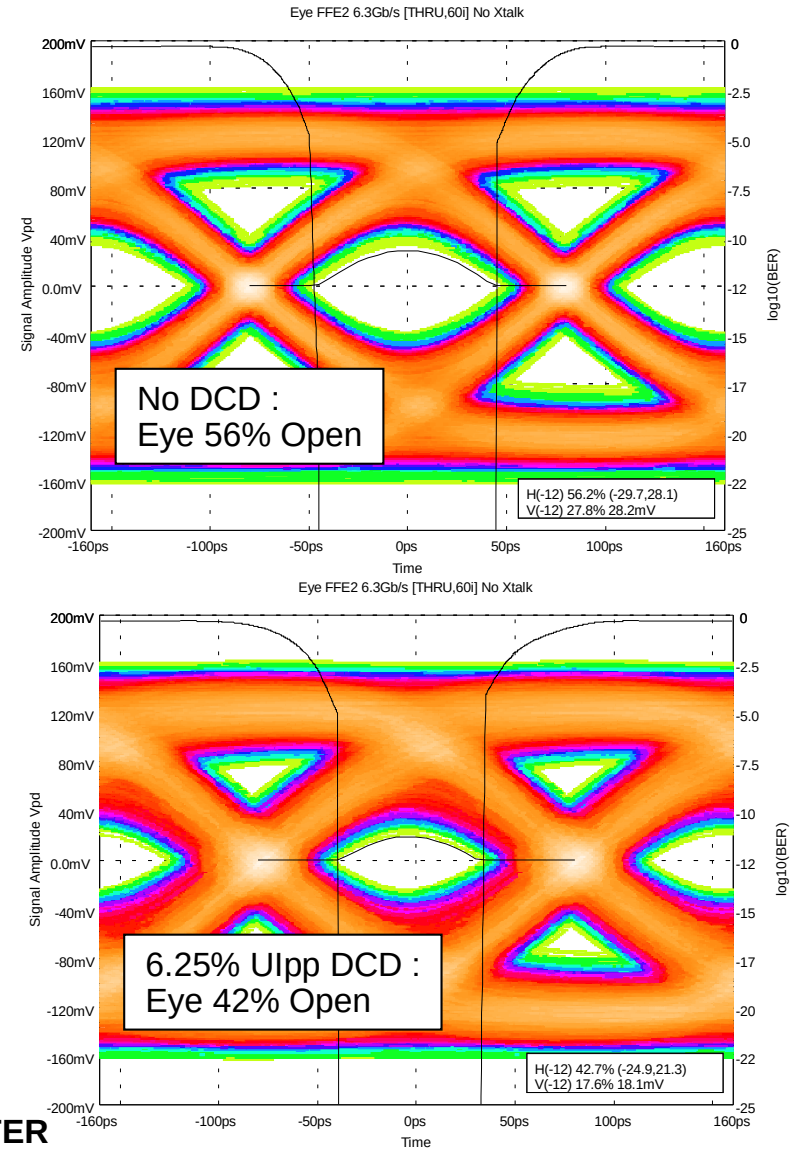
Example :

48:52 DCD, short pulse = 48 units

mean UI 50 units

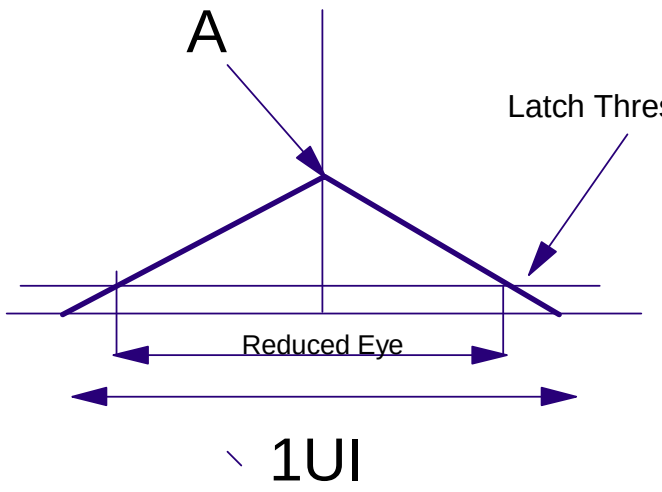
-> 4% UIpp DCD shutdown in low-loss channel

can result in 8% or more shutdown in lossy channel

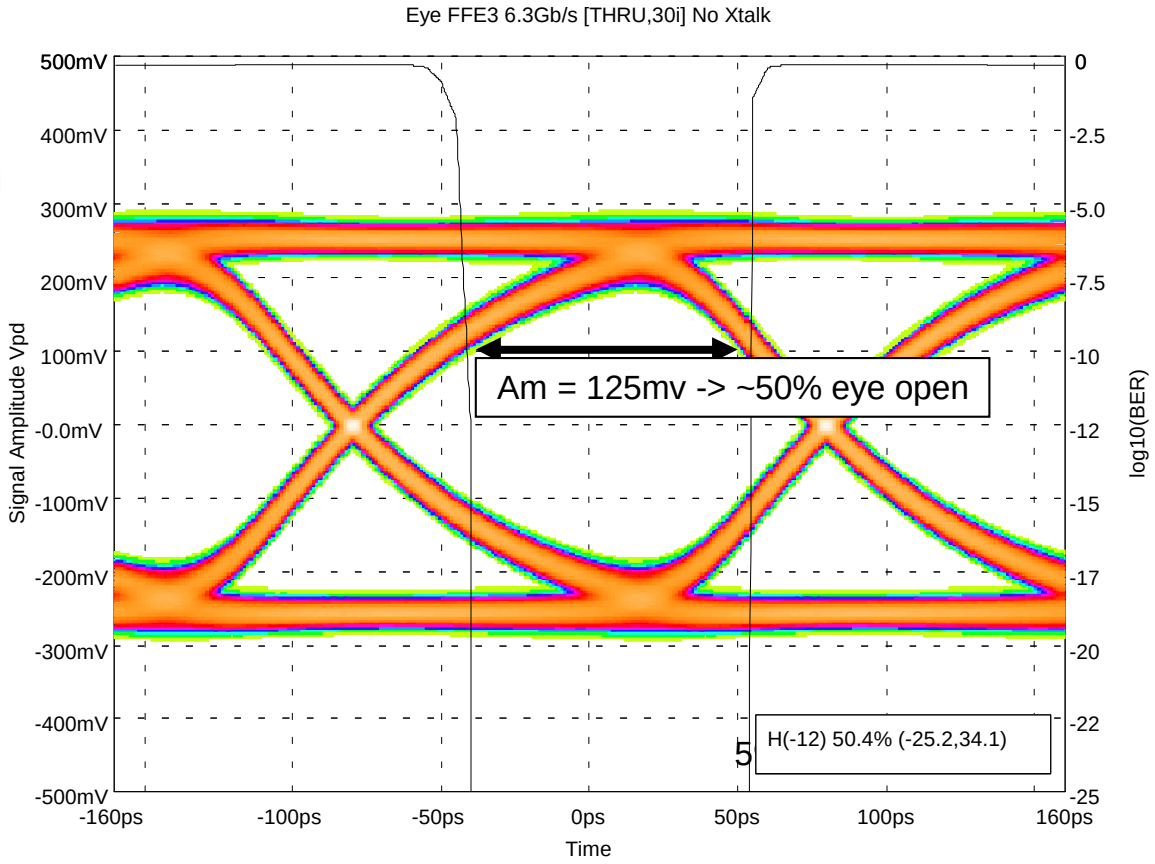


CHALLENGE : REALIZE STRINGENT 3% UIpp DCD AT TRANSMITTER

Minimum-Latch Overdrive



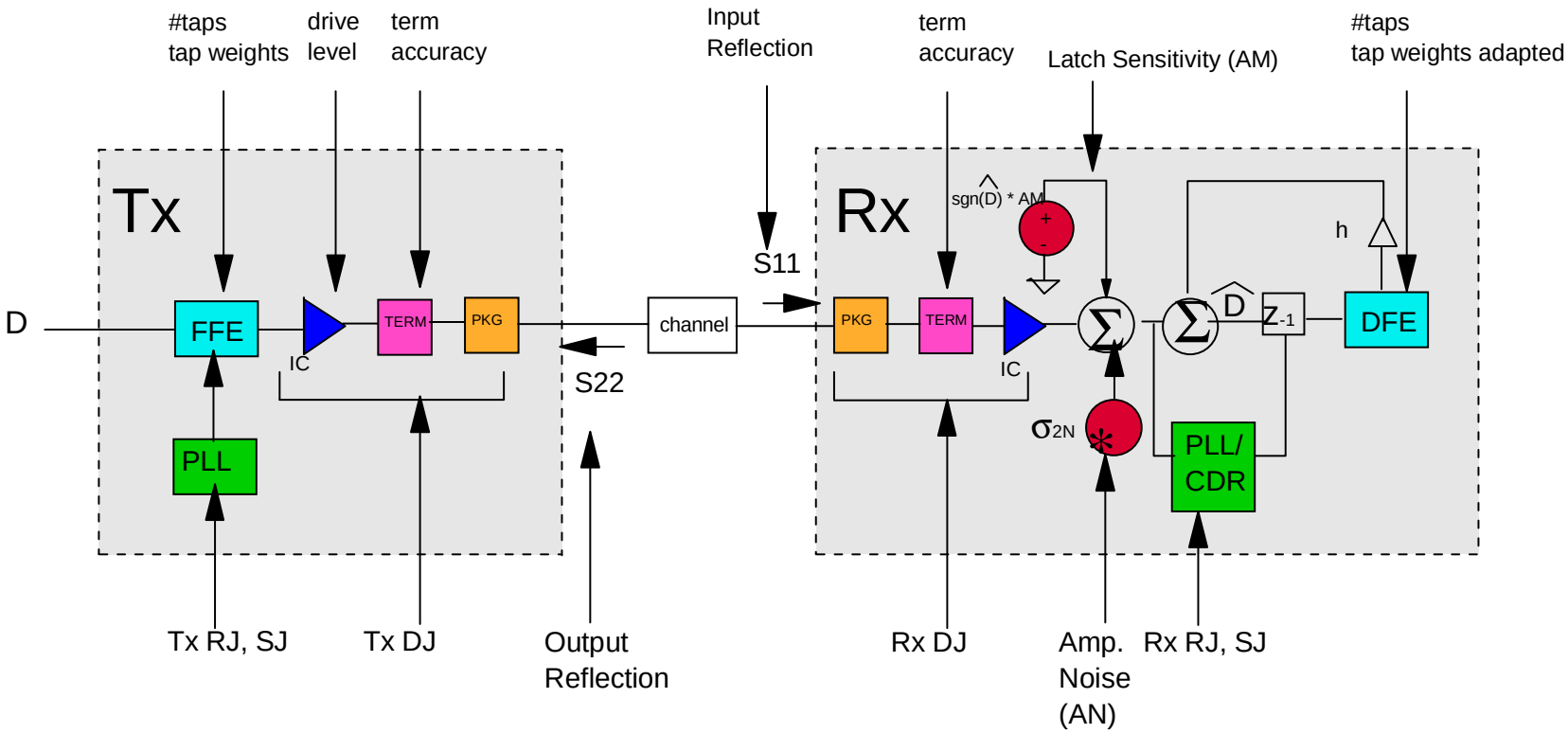
Observed Eye closure ~0.1UI for 20mV overdrive, 150mV "A"
As "A" gets bigger, waveform slope is larger and effect is reduced.



Outline

- Introduction
  - I/O Applications in modern system designs
  - Electrical Signaling Approaches
  - Line Signaling Approaches
- Electrical Channel Characteristics
  - Line Model
  - Line Degradations
- I/O core System Design
  - SERDES Architectures
  - FFE Equalization
  - DFE Equalization
  - 6-10Gb/s FFE/DFE System architecture
- Serial Link Modeling and Simulation
  - Link simulation tool
  - Eye Diagram BER Analysis
  - I/O Core Degradations
- Simulation and Measurement Results
  - IEEE 802.3ap Informative Channel Link Simulations
  - Simulated Performance vs. FFE and DFE Tap Length
  - 25Gb/s simulation results
- Summary

Key I/O Core Parameters for simulation



Tx : Example I/O configuration for a transmitter

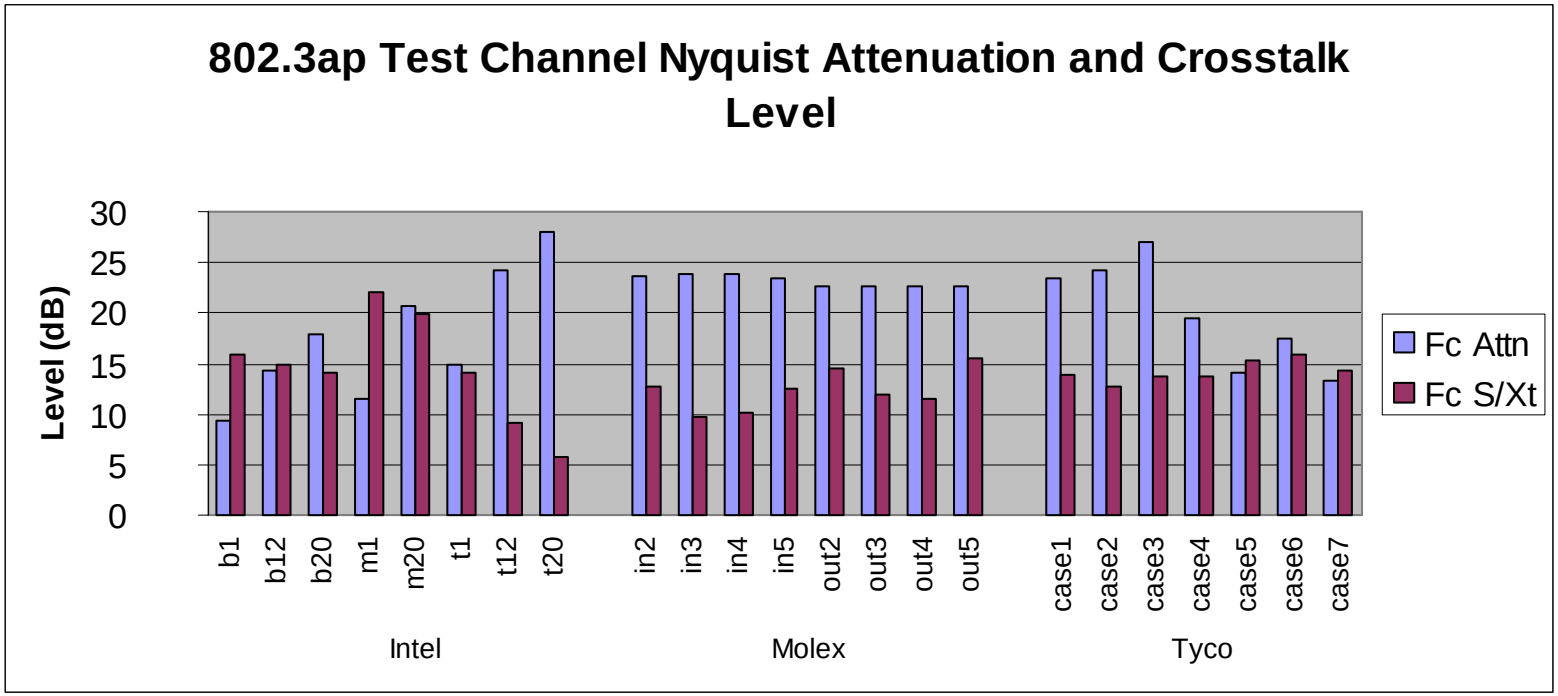
Drive Level	400mVpd min
RJ	1.07% RMS ui
DJ[1]	15% p-p UI @1e-12
TERM	40-60
S22	-10dB @ Baud/2

Assumed to include pkg, ESD, IC, DCD

Rx : Example I/O configuration for a receiver

AN	1.4mV RMS input ref.
AM[2]	15mV
RJ	1.07% RMS ui
DJ	10% p-p UI @1e-12
TERM	40-60
S11	-10dB @ Baud/2

Baud/2 Loss and S/Xt for 802.3ap Test Channels[1]



As Fc attenuation increases, S/Xt decreases

	Min	Max	Mean	Median
Fc Attn	9.30	28.10	20.25	22.60
Fc S/Xt	5.69	22.10	13.63	13.90

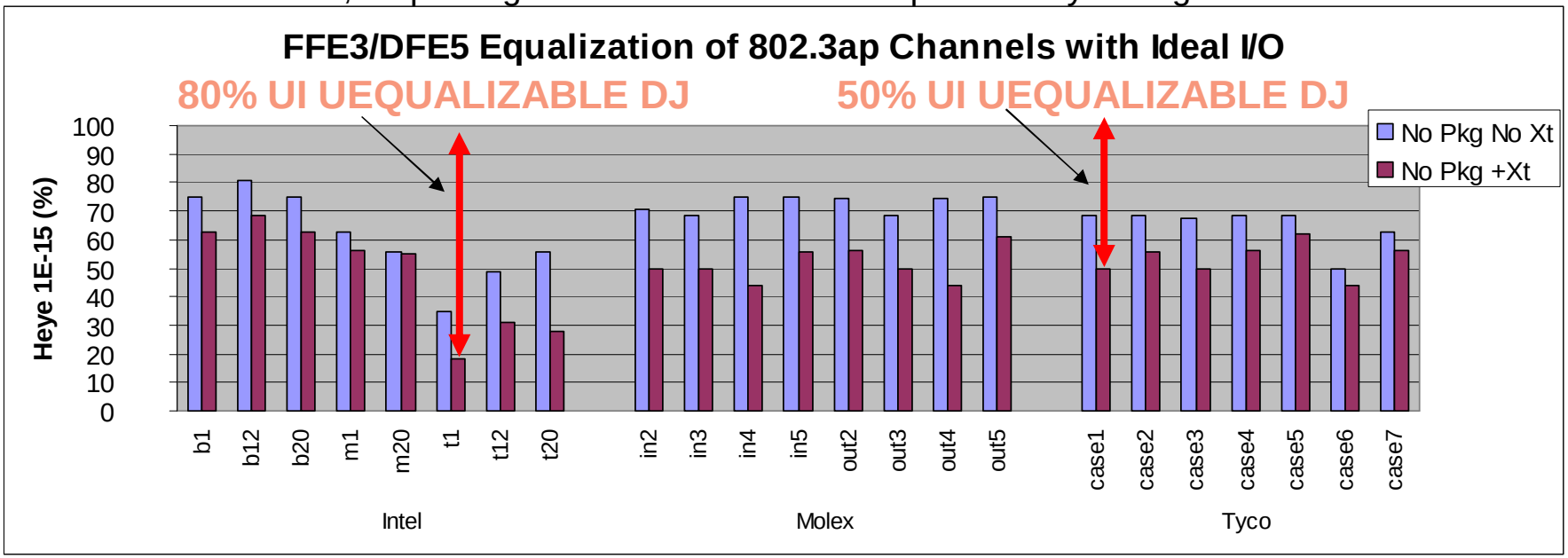
Crosstalk channels

Channels	#FEXT	#NEXT
Intel	2	6
Molex	3	4
Tyco	2	2
Tyco case6	2	1

[1]http://grouper.ieee.org/groups/802/3/ap/public/channel_model
"Channels for consideration by the signaling ad-hoc", John D'Ambrosia, Tyco
"Improved HVM ATCA Measurement Data", William Peters, Intel
"1m Test vehicle (FR408)", Gourgen Oganessyan, Molex

FFE3/DFE5 Equalization, No Pkg or I/O Jitter/Noise[1]

Use ideal I/O core, no package to determine maximum possible eye margin with FFE3/DFE5



Tx Lev	400mVpd
Tx RJ	0% RMS UI
Tx DJ	0% UIp-p
Tx Pkg	None
Tx TERM	50
Tx IC	None

Rx CDR	ON
Rx An	0mV RMS
Rx Am	0mV
Rx RJ	0% RMS UI
Rx DJ	0% UIp-p SJ
Rx Pkg	None
Rx TERM	50
Rx IC	None

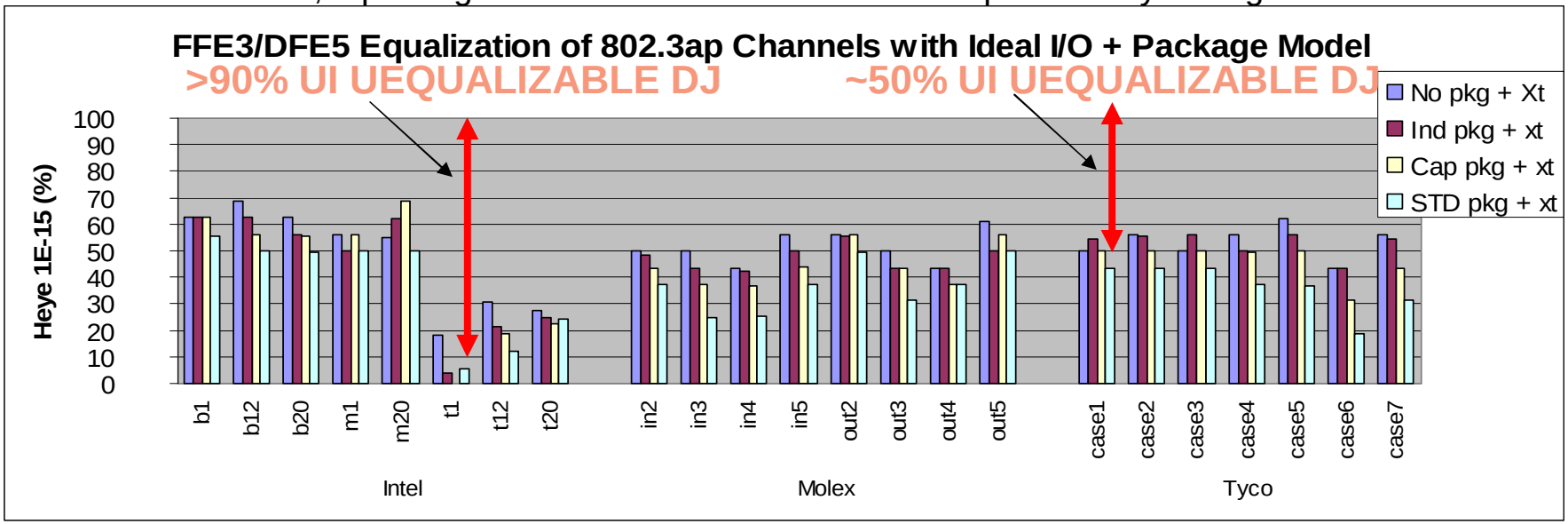
Eye Opening in %

	Min	Max	Mean	Median
HEYE no Xt	34.80	80.80	66.19	68.60
HEYE with Xt	18.20	68.60	50.63	55.00
Xt H loss	16.60	12.20	15.56	13.60
VEYE no Xt	28.60	76.60	66.58	72.40
VEYE with Xt	12.80	65.60	45.99	50.20
Xt V loss	15.80	11.00	20.59	22.20

[1]Async CDR running in all simulations

FFE3/DFE5 Equalization with Package, no I/O Jitter/Noise

Use ideal I/O core, 3 package models to determine maximum possible eye margin with FFE3/DFE5



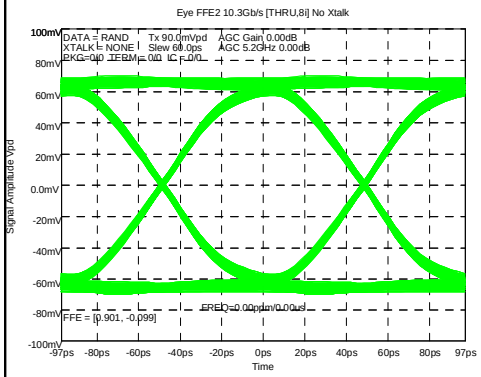
Vertical Eye Opening in %

	Min	Max	Mean	Median
VEYE no Pkg	12.80	65.60	45.99	50.20
VEYE C Pkg	6.60	69.80	41.26	45.40
VEYE L Pkg	0.80	58.80	42.29	46.80
VEYE S Pkg	1.40	51.40	33.12	35.80
LOSS C Pkg	6.20	-4.20	4.73	4.80
LOSS L Pkg	12.00	6.80	3.70	3.40
LOSS S Pkg	11.40	14.20	12.87	14.40
LOSS Xt	15.80	11.00	20.59	22.20

Horizontal Eye Opening in %

	Min	Max	Mean	Median
HEYE no Pkg	18.20	68.60	50.63	55.00
HEYE C Pkg	0.00	68.60	44.28	49.40
HEYE L Pkg	3.95	62.40	47.39	49.80
HEYE S Pkg	5.41	55.60	36.69	37.40
LOSS C Pkg	18.20	0.00	6.35	5.60
LOSS L Pkg	14.25	6.20	3.24	5.20
LOSS S Pkg	12.79	13.00	13.94	17.60
LOSS Xt	16.60	12.20	15.56	13.60

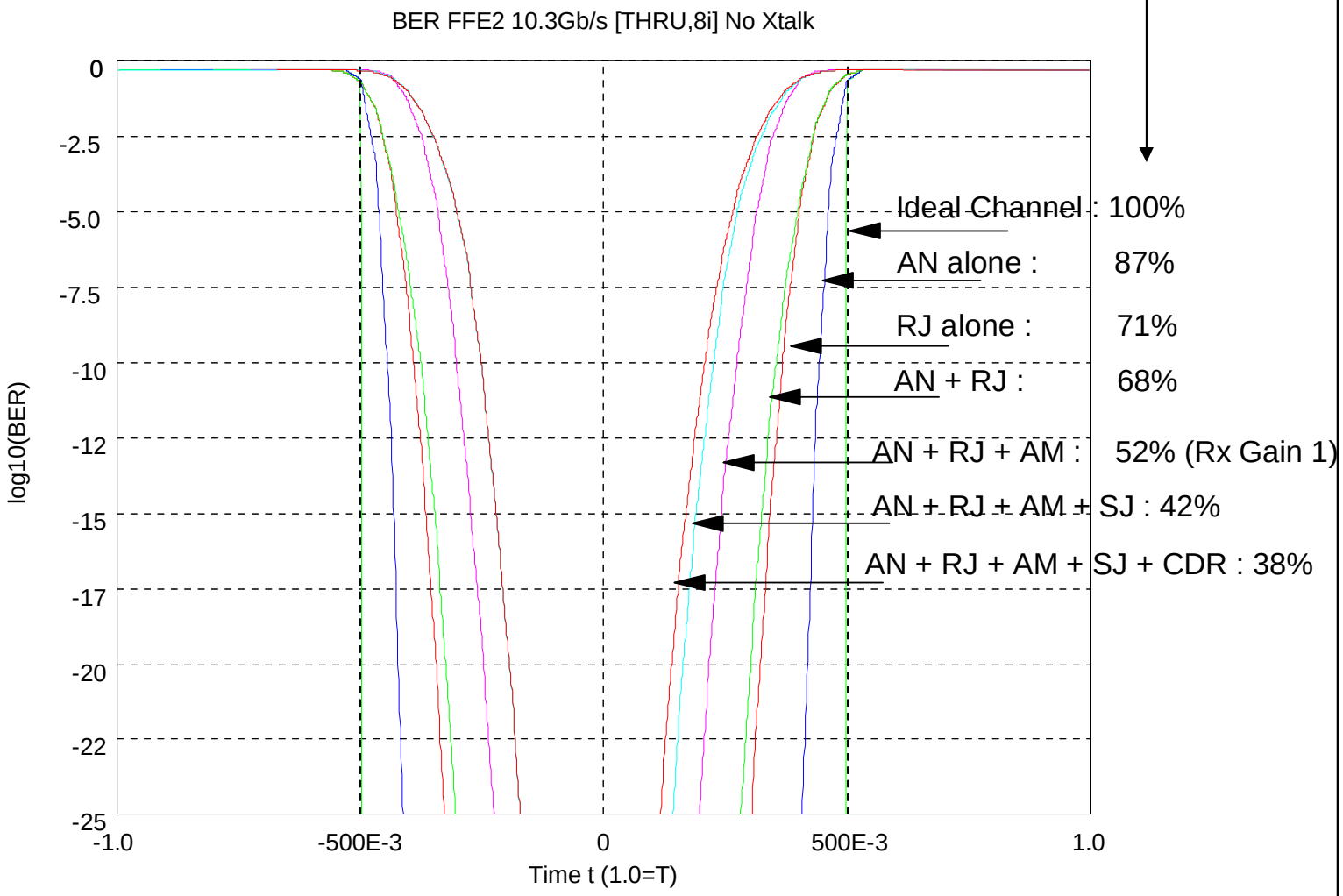
Example I/O Jitter/Noise Impact to Clean Channel



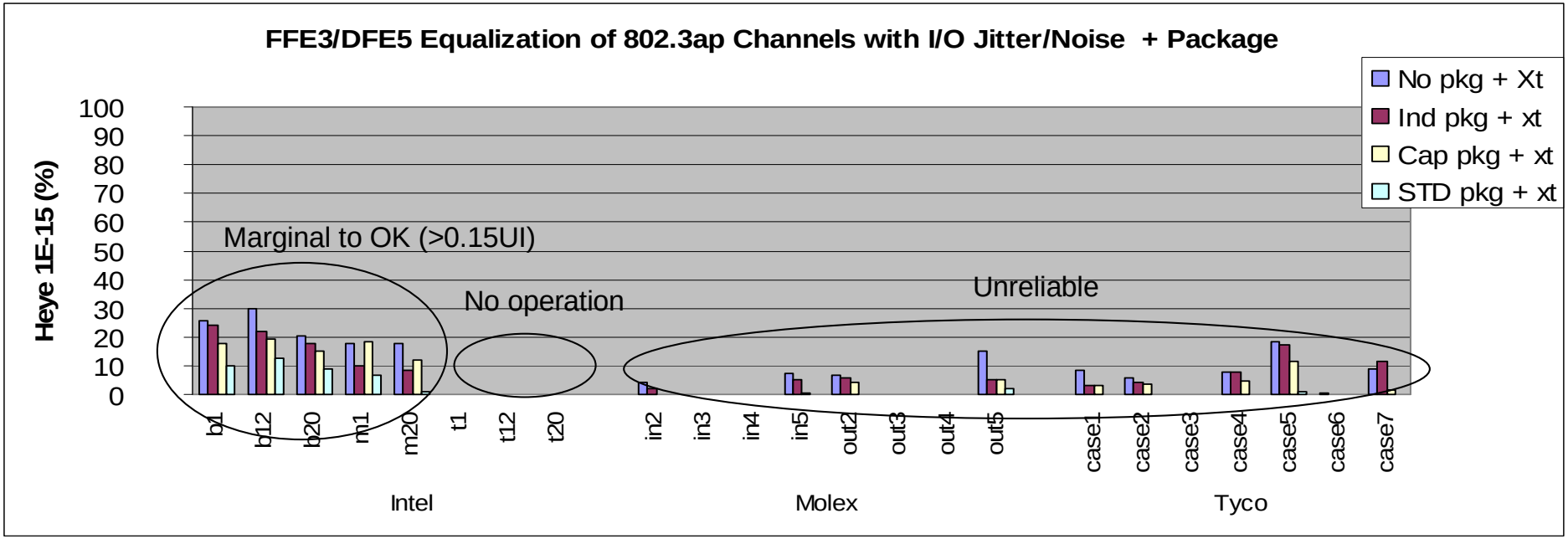
Tx Lev	400mVpd
Tx RJ	1.07% RMS UI
Tx DJ	5% UIp-p SJ
Tx Pkg	None
Tx TERM	50
Tx IC	None

Rx CDR	ON
Rx An	1.4mV RMS
Rx Am	15mV
Rx RJ	1.07% RMS UI
Rx DJ	5% UIp-p SJ
Rx Pkg	None
Rx TERM	50
Rx IC	None

Eye Opening at 1E-12 vs. added I/O Jitter/Noise



FFE3/DFE5 Equalization with Package and I/O Jitter/Noise



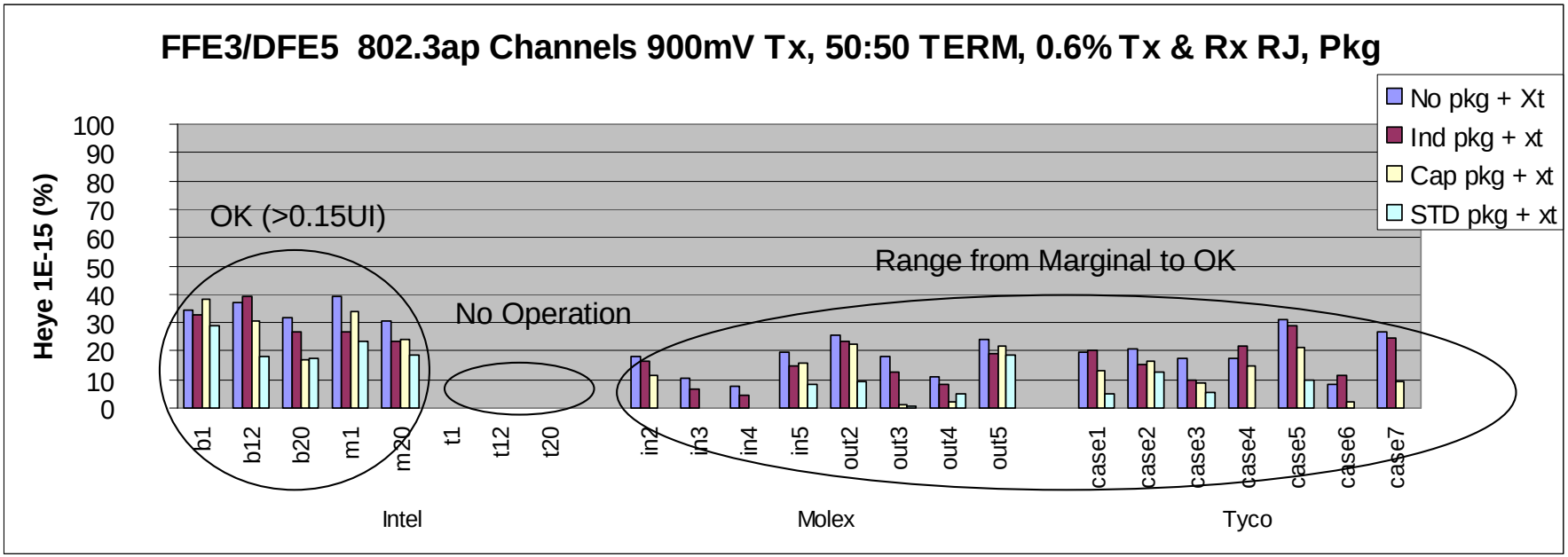
Tx Lev	400mVpd
Tx RJ	1.07% RMS UI
Tx DJ	5% SJ + Pkg
Tx Pkg	Cap-like
Tx TERM	40
Tx IC	None

Rx CDR	ON
Rx An	1.4mV RMS
Rx Am	15mV
Rx RJ	1.07% RMS UI
Rx DJ	5% SJ + Pkg
Rx Pkg	Cap-Like
Rx TERM	60
Rx IC	None

Horizontal Eye Opening in %

	Min	Max	Mean	Median
HEYE no Pkg	0.00	29.80	8.46	6.81
HEYE C Pkg	0.00	19.20	5.10	1.50
HEYE L Pkg	0.00	24.10	6.28	4.19
HEYE S Pkg	0.00	12.80	1.85	0.00
LOSS C Pkg	0.00	10.60	3.36	5.31
LOSS L Pkg	0.00	5.70	2.18	2.62
LOSS S Pkg	0.00	17.00	6.61	6.81
LOSS Xt	0.00	5.80	12.30	16.39

FFE3/DFE5 Equalization with Reduced Jitter I/O[1]



[1]Clock noise 5dB cleaner
Amplitude noise ½ level
Drive level boosted 50mV
Impedance set to 50 ohm

Tx Lev	450mVpd
Tx RJ	0.6% RMS UI
Tx DJ	5% SJ + Pkg
Tx Pkg	Varied
Tx TERM	50
Tx IC	None

Rx CDR	ON
Rx An	0.7mV RMS inputRef
Rx Am	15mV
Rx RJ	0.6% RMS UI
Rx DJ	5% SJ + Pkg
Rx Pkg	Varied
Rx TERM	50
Rx IC	None

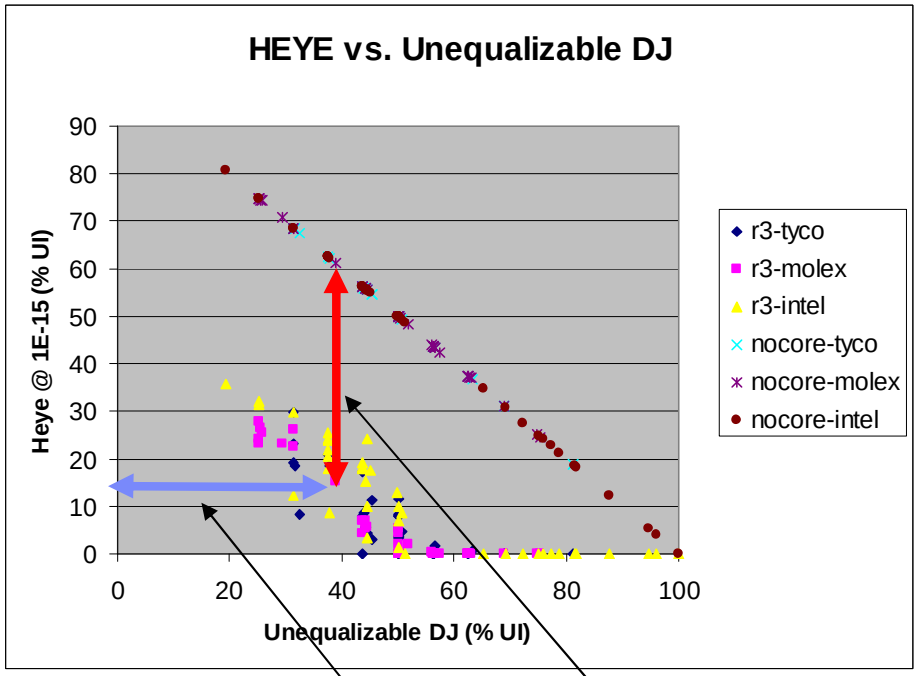
Horizontal Eye Opening in %

	Min	Max	Mean	Median
HEYE no Pkg	0.00	39.20	19.20	18.90
HEYE C Pkg	0.00	38.00	13.40	13.80
HEYE L Pkg	0.00	39.20	16.47	15.75
HEYE S Pkg	0.00	29.10	8.30	5.36
LOSS C Pkg	0.00	1.20	5.80	5.10
LOSS L Pkg	0.00	0.00	2.73	3.15
LOSS S Pkg	0.00	10.10	10.90	13.54
LOSS Xt	0.88	10.30	17.46	23.05

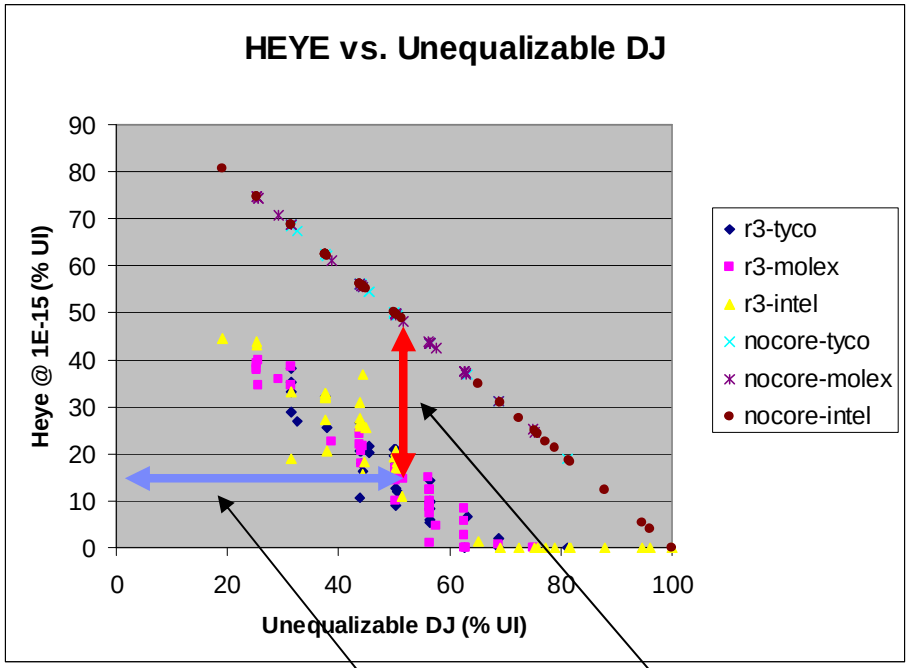
Eye Opening vs. Unequalizable DJ

Unequalizable DJ = Non equalized BW loss + Unequalizable Reflections + Crosstalk

Nominal Jitter I/O



Reduced Jitter I/O



Core Loss =~45% (too much)

Unequalizeable DJ Tolerance =~35% (too little)

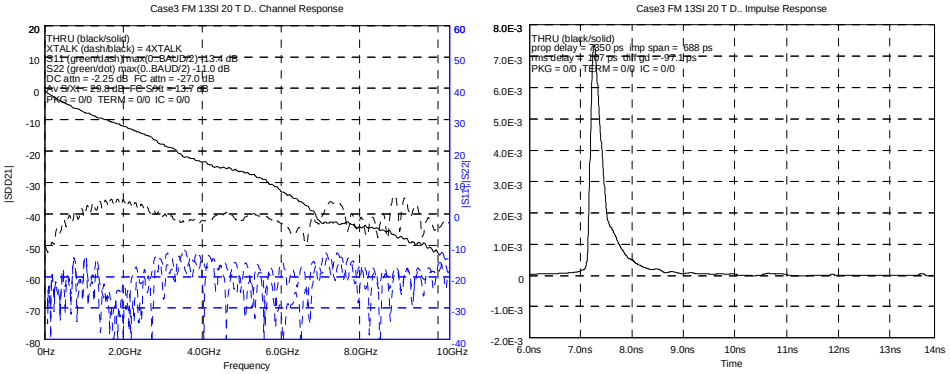
Core Loss =~30%

Unequalizeable DJ Tolerance =~50%

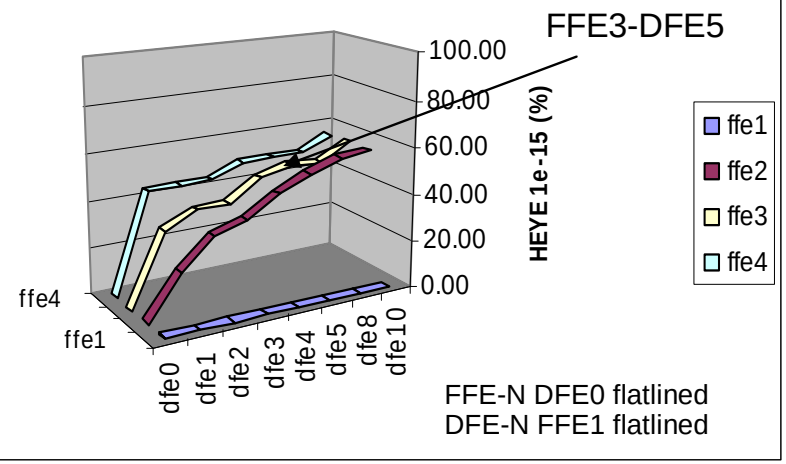
Challenge : Keep intrinsic channel unequalizable DJ < 50% UI for practical equalizers

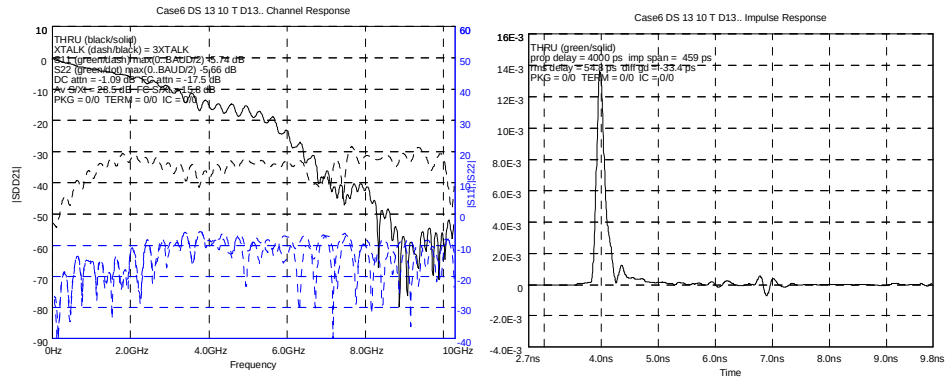
FFE-N/DFE-M Equalization Case3, Case6

"Ideal" I/O core (async CDR running), Cap-Like package models

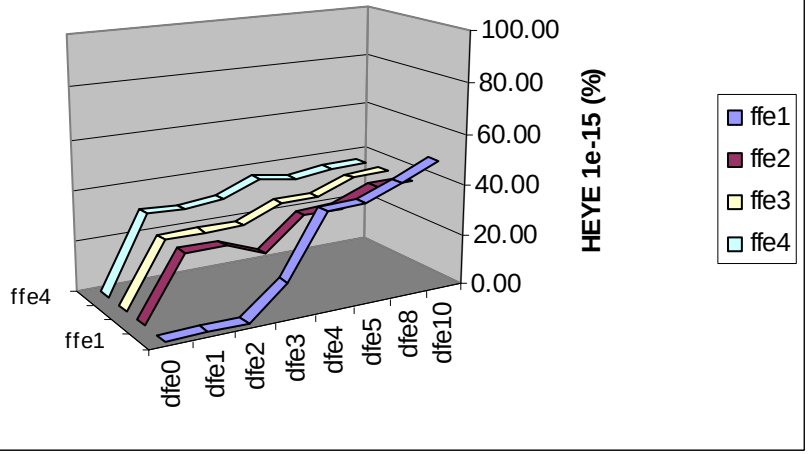


Lossy channel benefits from FFE/DFE Combo



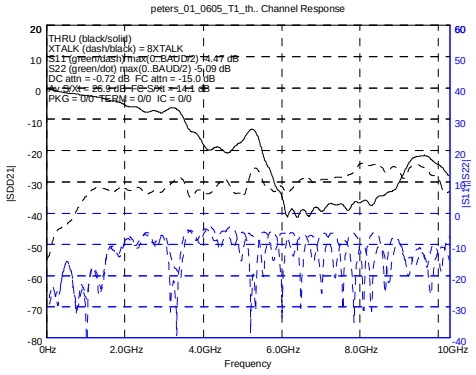


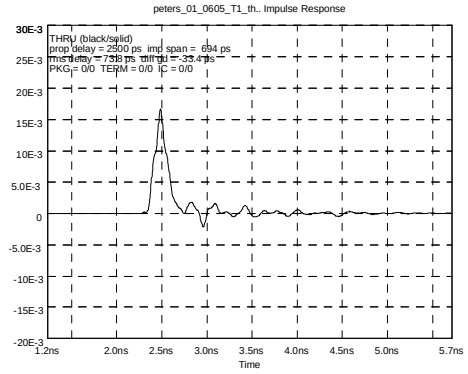
Channel with reflections benefits from FFE/DFE combo
DFE-only help suppress crosstalk



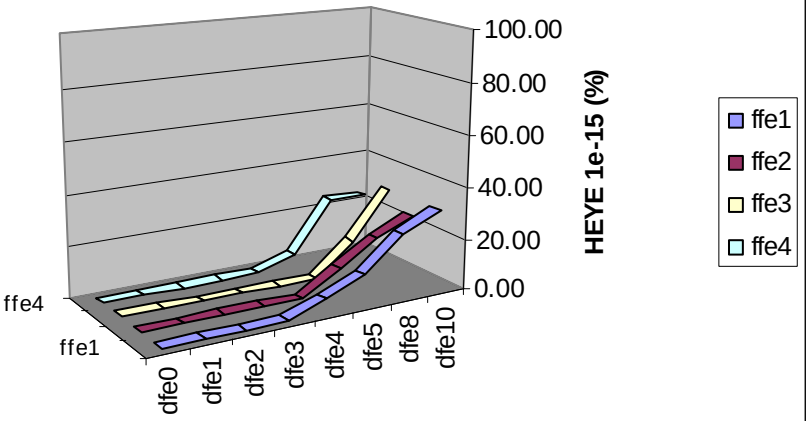
FFE-N/DFE-M Equalization T1, B20

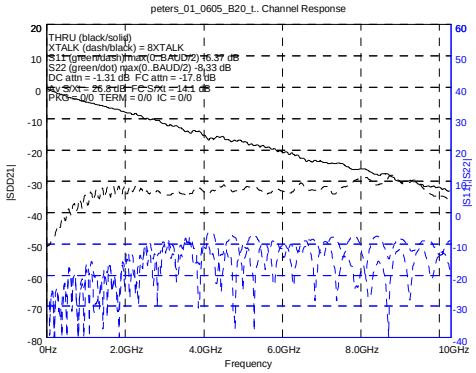
"Ideal" I/O core (async CDR running), Cap-Like package models

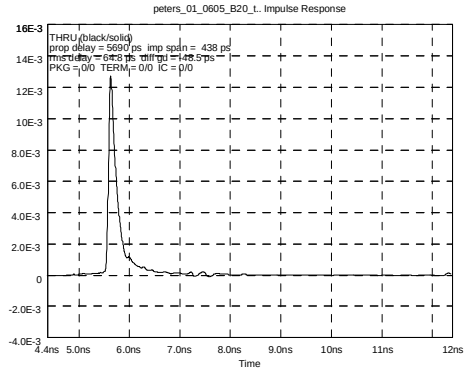




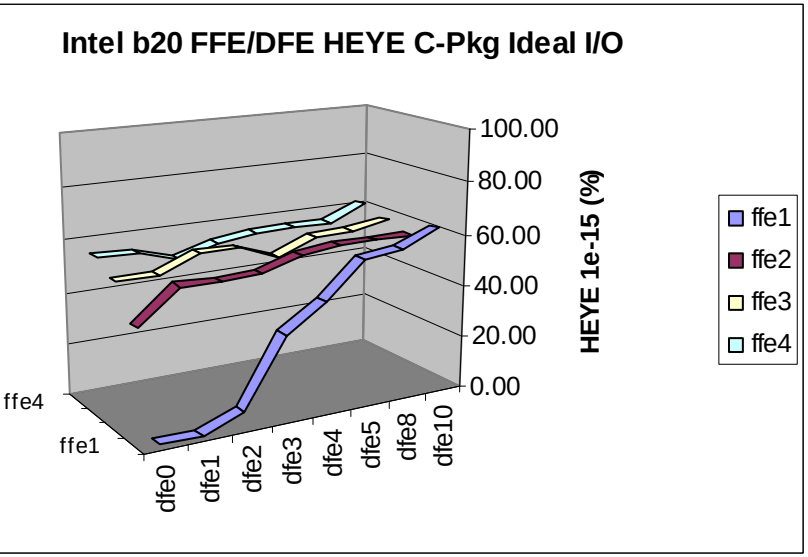
Large reflections : even DFE10 only opens eye 30%, insufficient





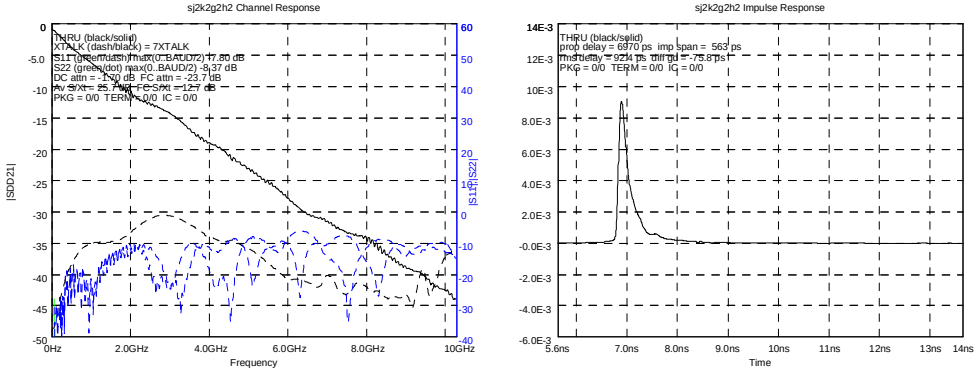


Clean low loss channel equalizes with FFE3 alone

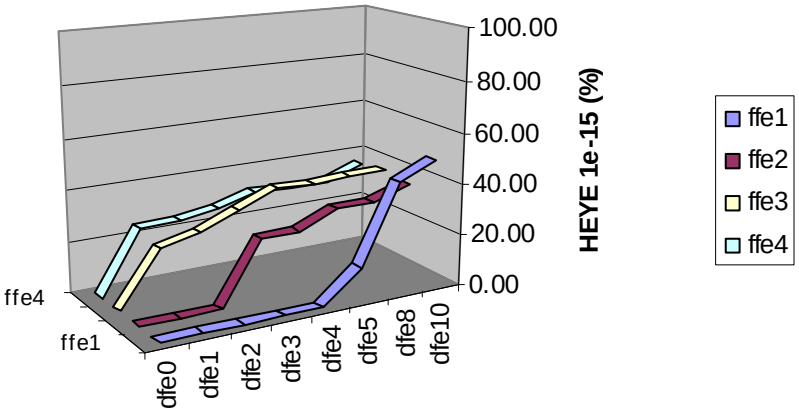


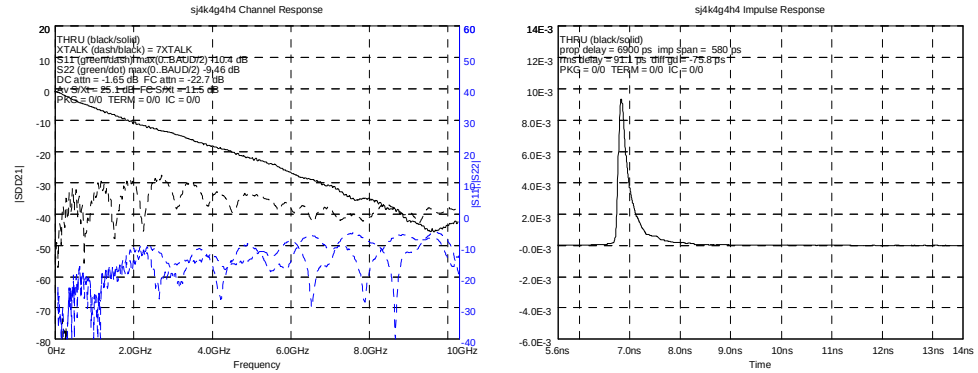
FFE-N/DFE-M Equalization In2, Out4

"Ideal" I/O core (async CDR running), Cap-Like package models

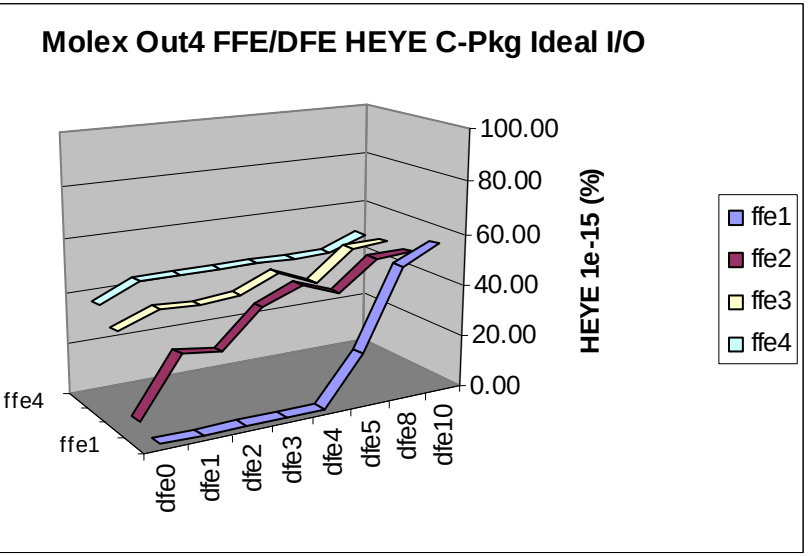


Similar performance with FFE3 + DFE4…DFE10

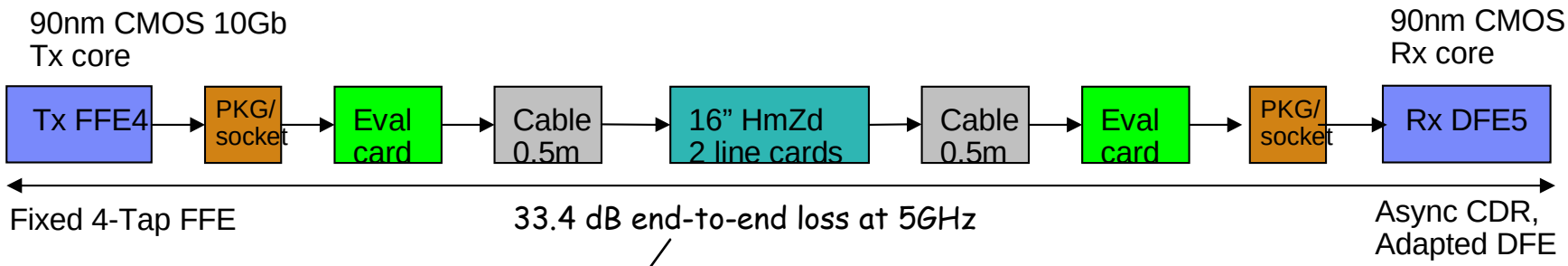


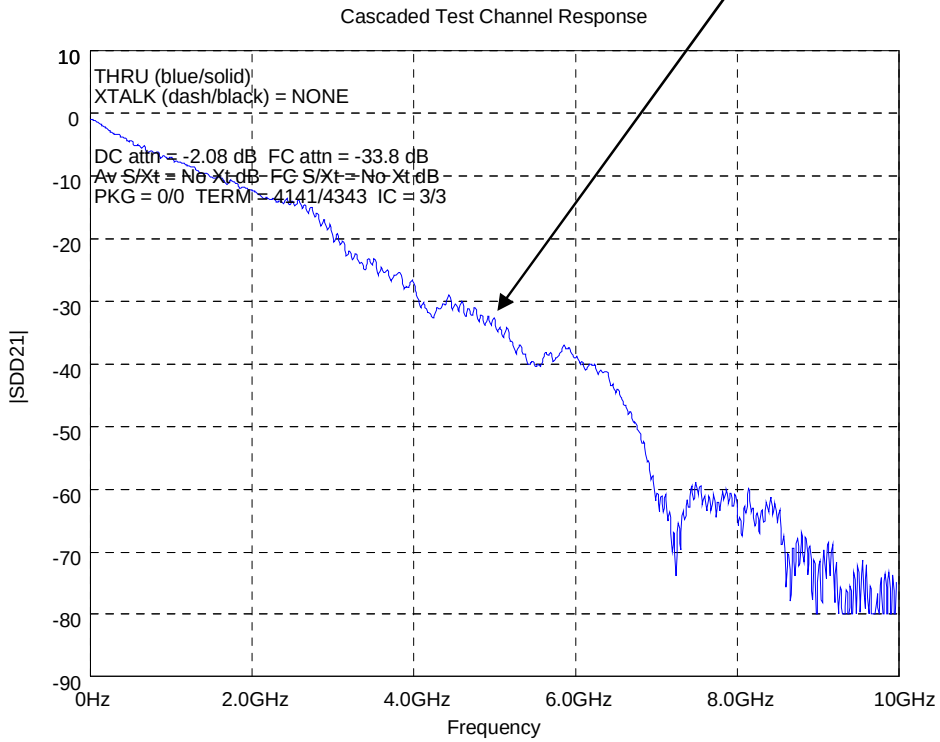


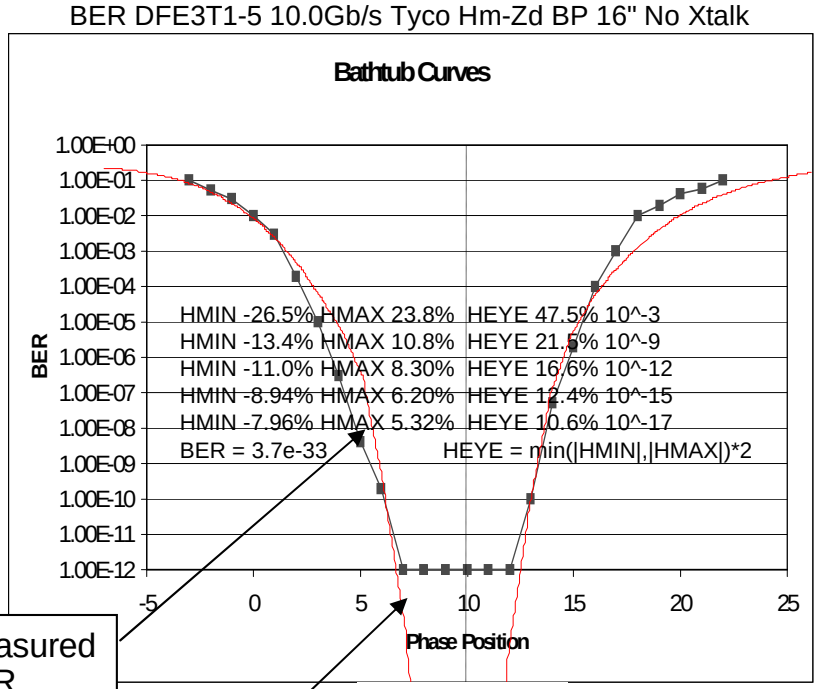
Similar performance For FFE3 + DFE1…DFE10



Hardware 10Gb/s FFE DFE on 16” Channel[1]







Measured BER

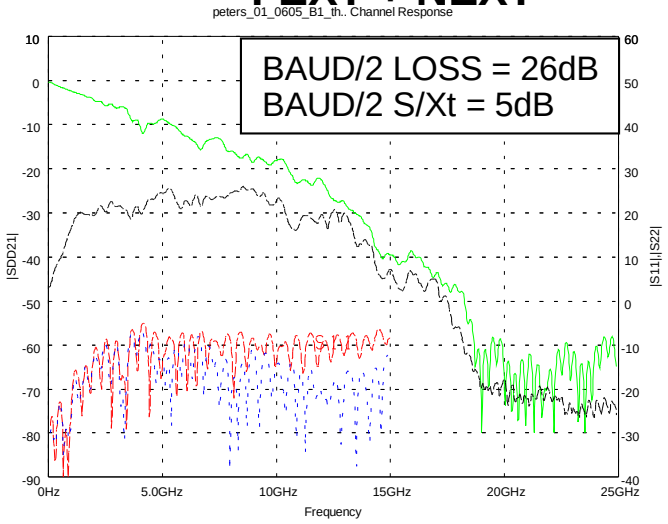
Simulated BER

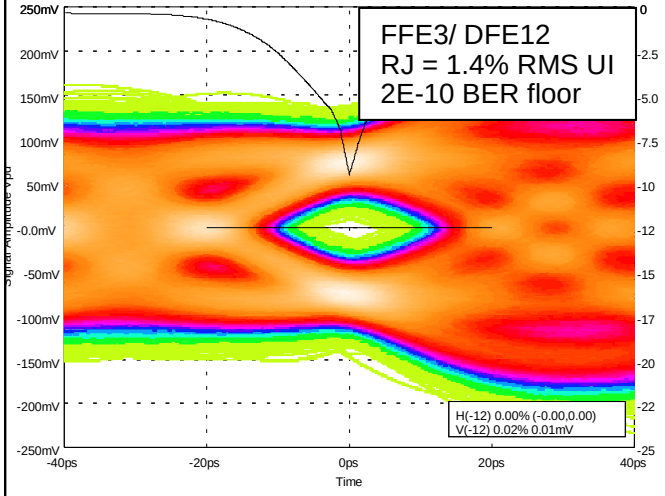
Tx & Rx PLL Ref Lock, CDR off
~1.18ps total RJ, 0.83 ps for Tx, Rx
L(f) Integ. 2.5MHz ->5GHz implies
approx -85dBc/Hz @ 1M VCO

[1]Meghelli, ISSCC2006, “A 10Gb/s 5-tap DFE / 4-tap FFE Transceiver in 90nm CMOS Technology”

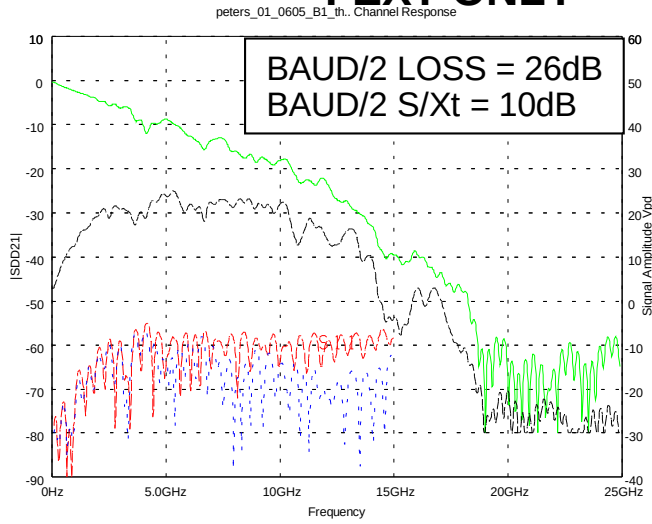
25Gb/s on Intel B1 Channel : 2-level FFE/DFE

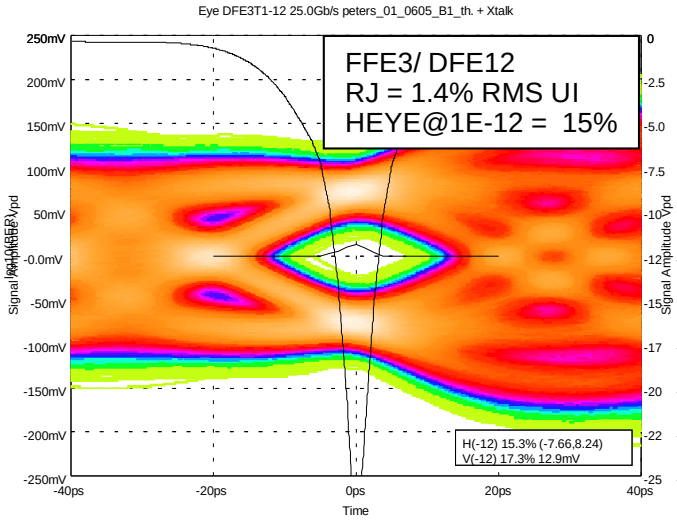
FEXT + NEXT



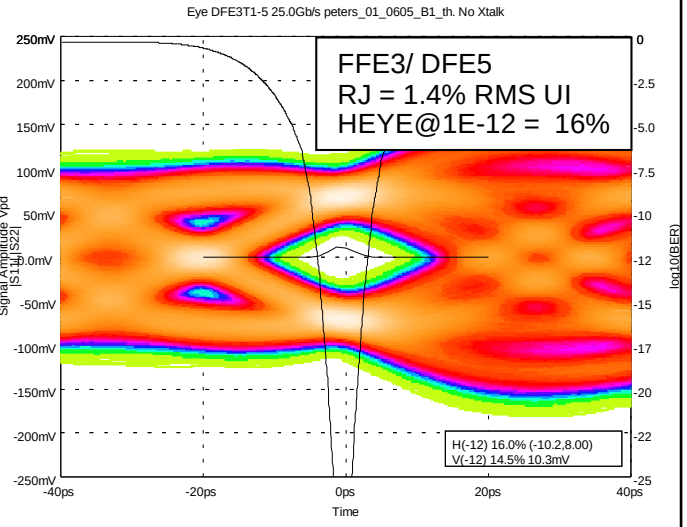


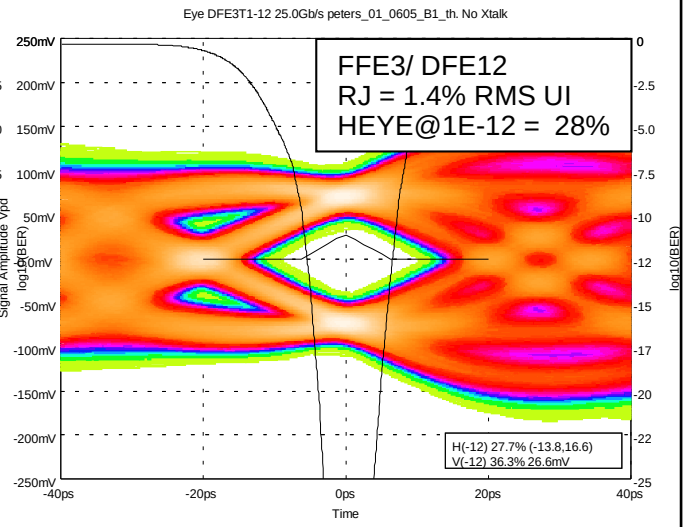
FEXT ONLY





NO XT

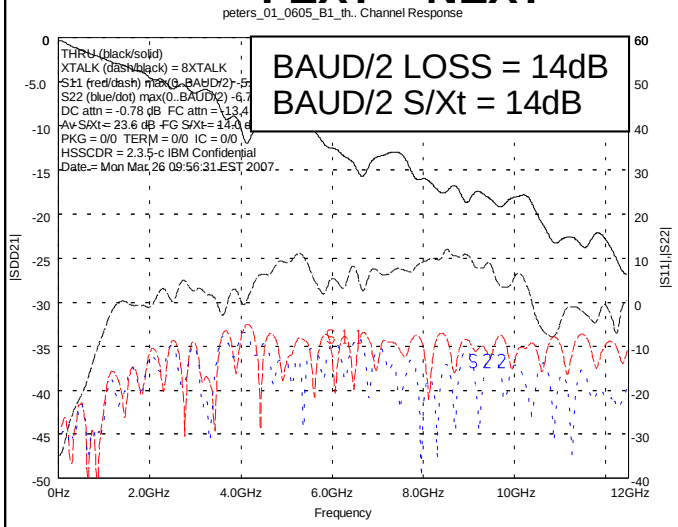




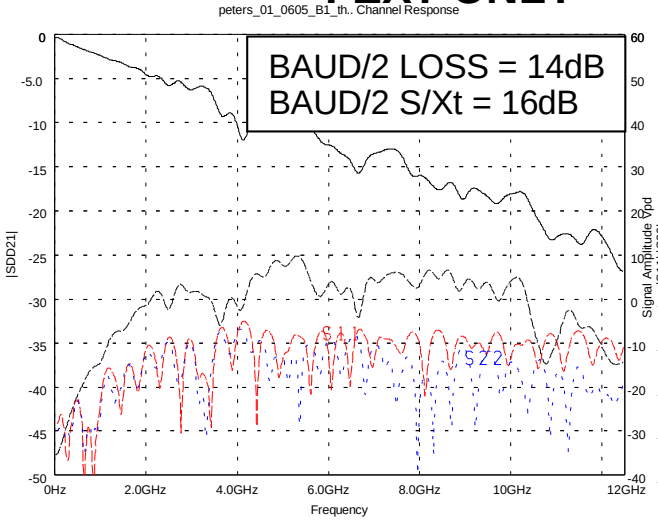
Reflections are equalizable : Crosstalk is not. Challenge : Contain Xt (NEXT) @ 25Gb/s

25Gb/s on Intel B1 Channel : 4-Level FFE/DFE

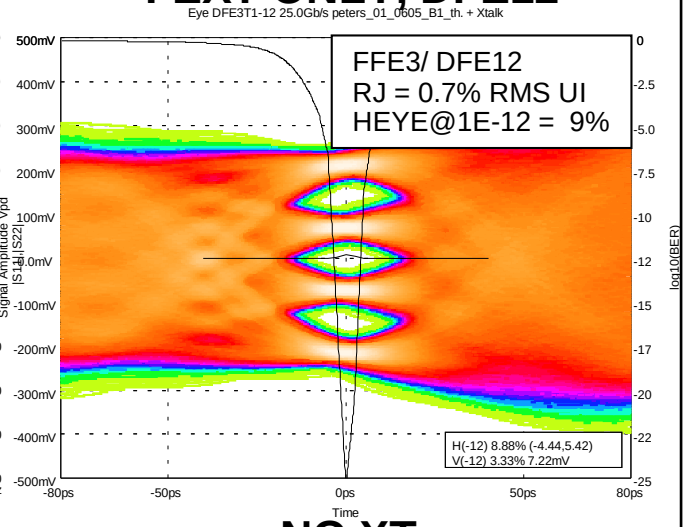
FEXT + NEXT



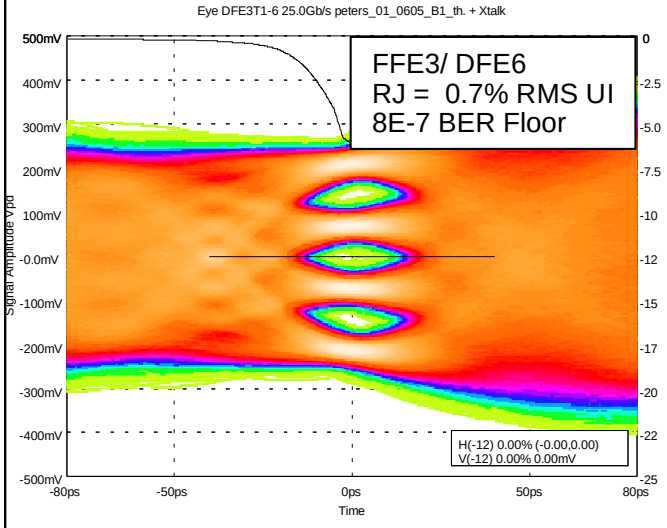
FEXT ONLY

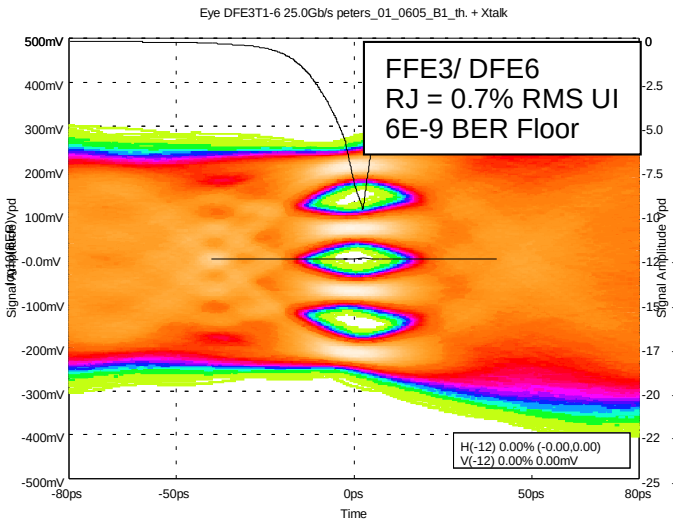


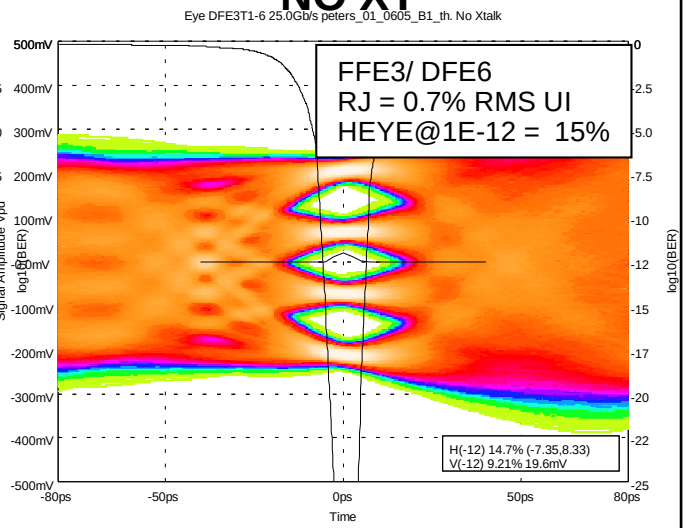
FEXT ONLY, DFE12



NO XT







4-level worse with ½ RJ, same DFE span. Marginal improvement with 2x DFE span. Simplistic comparison with RJ and FFE/DFE only, not complete analysis.

Summary of Challenges in Electrical Channel

- **Electrical Channel Problems**
  - Large end-to-end loss at high frequencies (25dB + at baud/2)
  - Impedance and loss variations in line components (+-15% Zo or more)
  - Impedance discontinuities at package/connector junctions
  - Crosstalk in line components, NEXT in particular (in vias,connector, package, IC)
  - Accurate modeling/measurement of line component N-ports to high frequency
  - Large number of permutations of channel with disparate impedance elements
  - PN skew in diff pairs
- **Challenges for Electrical Channel Design**
  - Keep worst case end-to-end (+PKG,IC) cascaded channel loss < 32dB at BAUD/2

    As reflections/crosstalk get worse, less end-to-end loss is tolerable
  - Keep Signal to Crosstalk ratio > 10dB at Baud/2
  - Keep unequalizable DJ component (i.e. residual eye post equalization) contained to < 50% horizontal UI to enable practical Tx + Rx I/O core degradations
  - Keep P/N skew aligned to <0.2 UI separation (SDD21/SDC21 > 10dB)

Summary of Challenges in I/O Core

- **I/O Core Problems**
  - Power and area added by line equalization analog/digital circuitry
  - As data rates go higher, need more and more DFE taps (5 to 10 to more at 20+Gb/s?)
  - PLL RJ/SJ, supply noise modulation : as data rates go higher, less and less absolute jitter can be tolerated (UI 200ps/5Gb, 100ps/10Gb, 50ps/20Gb…)
  - Loss added by analog circuitry at high frequencies. Larger I/O power to get wide BW.
  - Loss in signal isolation in package and on die at high frequencies
  - Impedance mismatch (S11/S22) due to ESD/IC parasitics
  - PVT variations increasing as feature size gets smaller (130nm->90nm->65nm->45nm->….)
  - Voltage headroom dropping as VDD goes down (1.5->1.2->1.0->0.8->0.5)
    - Supply noise rejection harder, Linear dynamic range lower
  - Clock and Data Recovery bias from data dependent edge crossovers
- **Challenges for I/O Core Design**
  - Minimize extra loss added by I/O core electronics and package : <8dB total @BAUD/2 w.c.
  - Provide Tx FFE3 Rx DFE5 minimum equalization, desire FFE in Rx
  - <1% RMS Composite RJ from Tx and Rx PLL (tighter than 802.3ap)
  - <10% UIpp Composite PLL SJ from supply noise
  - < 3% UIpp Tx DCD
  - Power <30mW/Gb/s and lower for backplane I/O, 10mW/Gb/s and lower for C2C/memory I/O