Bandwidth Extension Techniques for CMOS Amplifiers

David J. Allstot, Sudip Shekhar, and Jeffrey S. Walling

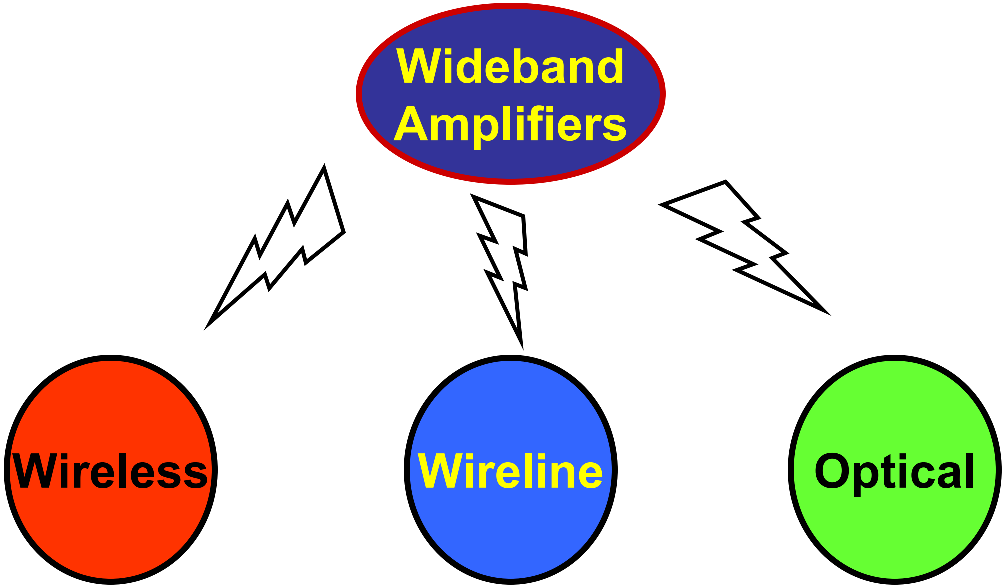
Dept. of Electrical Engineering
University of Washington
Seattle, WA 98195-2500

Outline

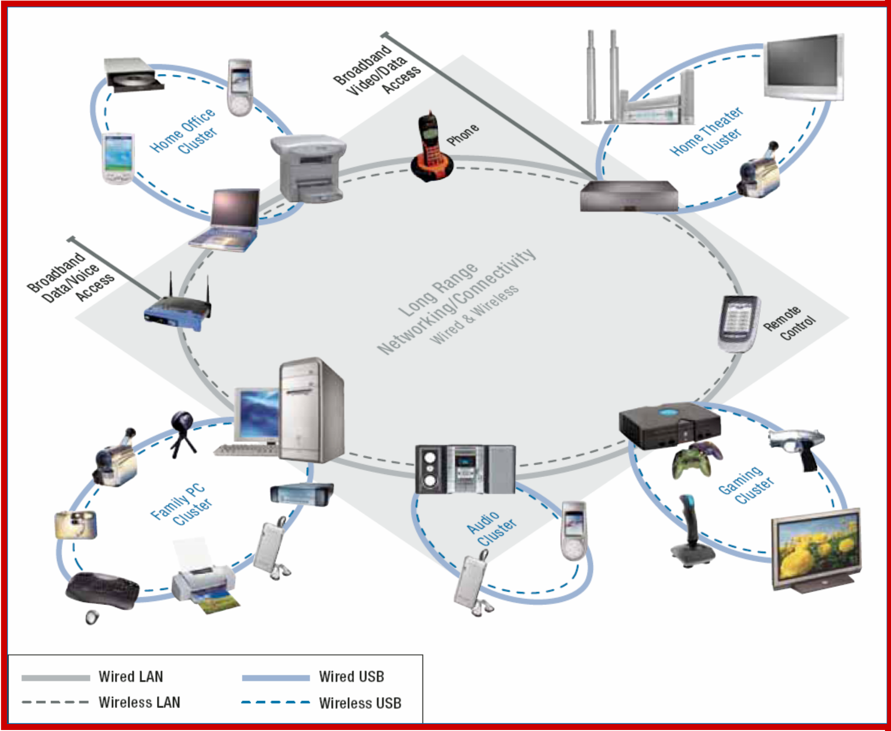
- Motivations: Performance and Low Power (bandwidth α g_m α $[I]^{1/2}$, settling time, rise time)
- Bridged-Shunt Peaking
- Bridged-Shunt-Series Peaking
- Asymmetric T-coil Peaking
- Wideband Amplifiers
- Results
- Conclusions

Motivation

- Broad Band Amplifiers
- Ultra Wideband (UWB) Receivers
- Transimpedance Amplifiers (TIAs)
- Pre-drivers and Mux/Demux



UWB Standards



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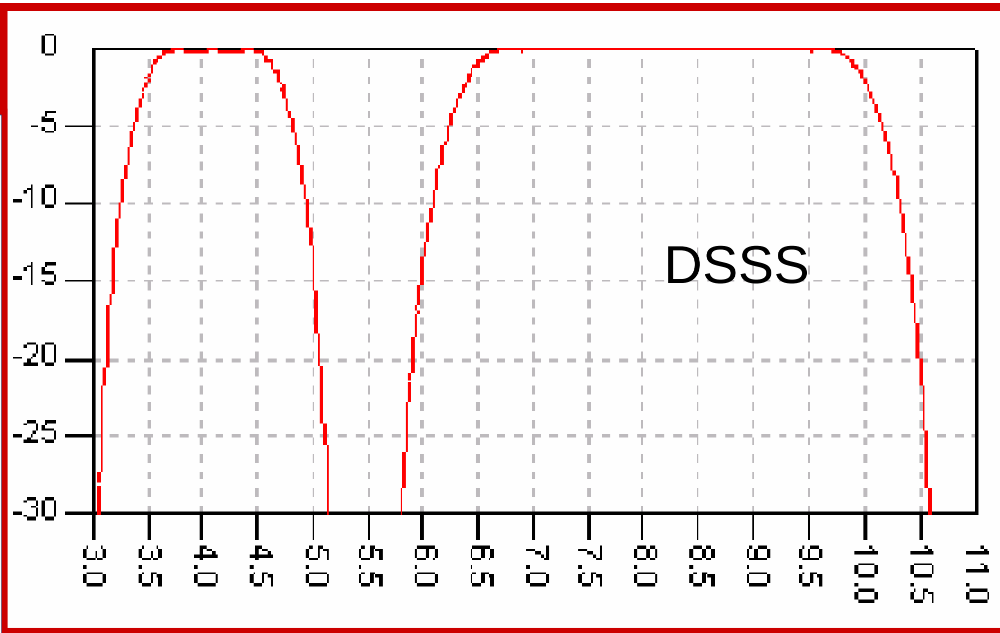
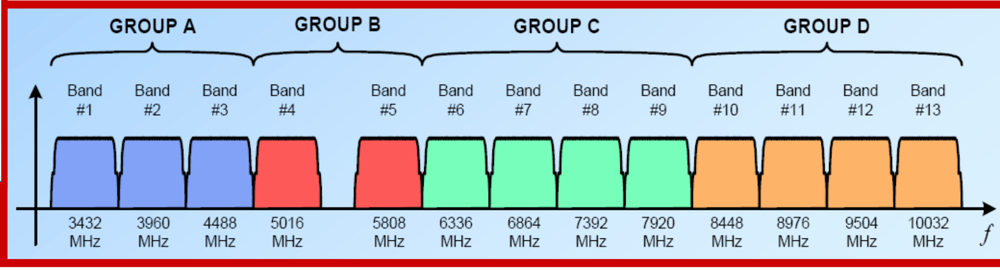
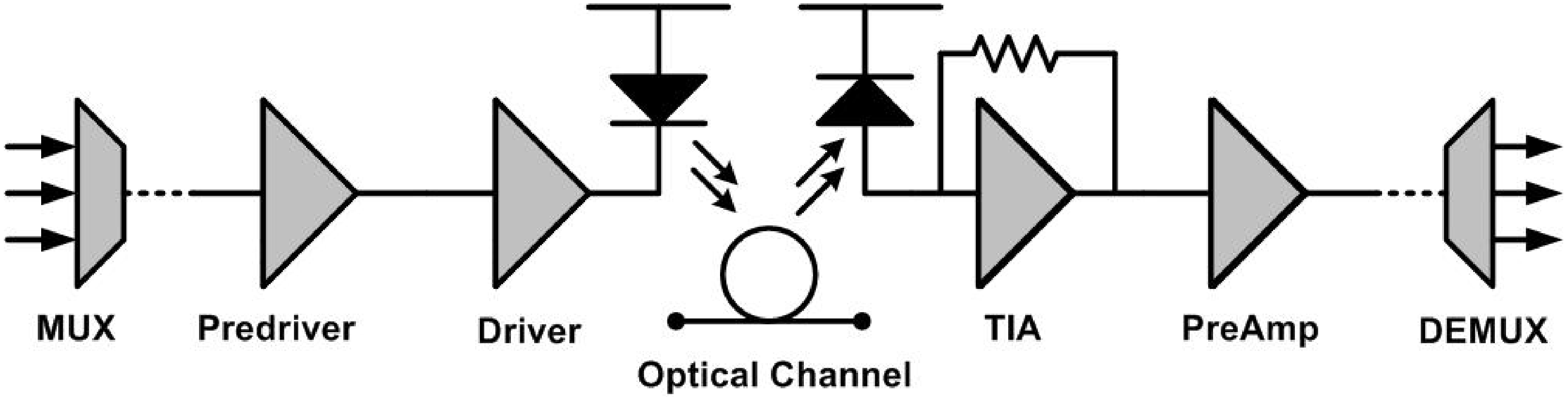




MBOA (Multi-band OFDM Access) is supported by most of industry.
Direct Sequence Spread Spectrum (DSSS) is primarily supported by Motorola/Freescale.

Optical Communications



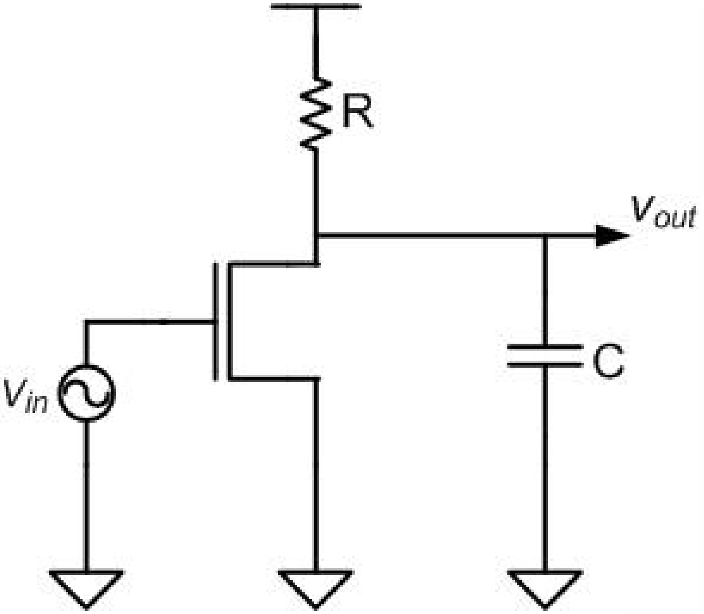
Large Bandwidth Needed (~ 40Gb/s)

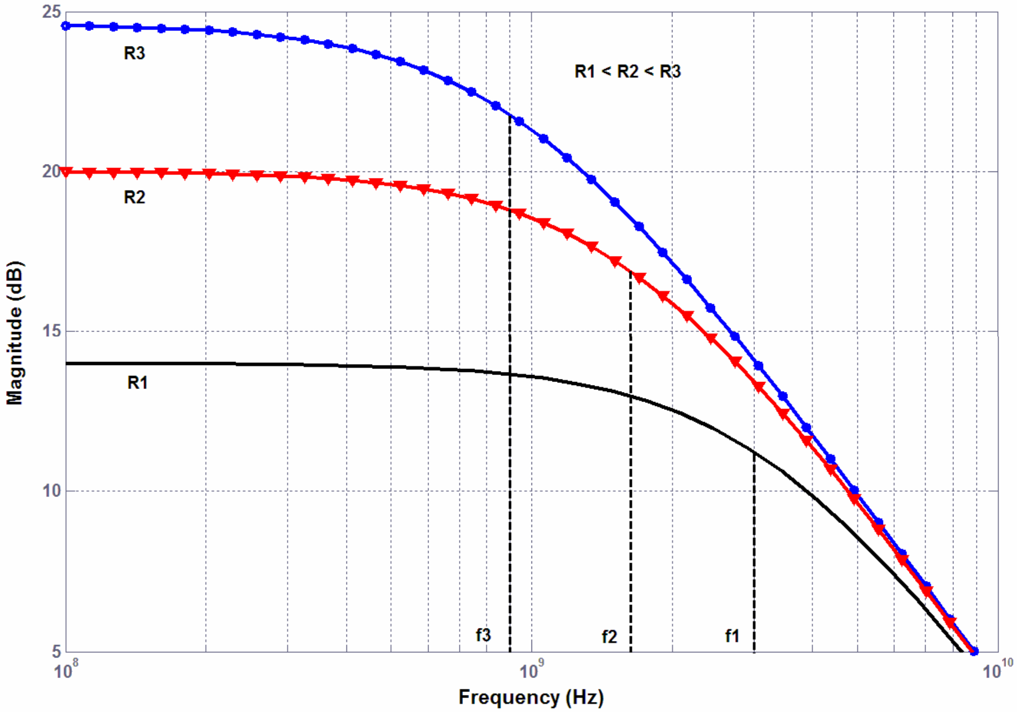
S. Galal and B. Razavi, “40Gb/s amplifier and ESD protection circuit in 0.18um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2389-2396, Dec. 2004.

H. Wheeler, "Wide-band amplifiers for television," *Proc. of the I.R.E*, pp. 429-438, July 1939.

F. A. Muller, "High-frequency compensation of RC amplifiers," *Proc. of the I.R.E*, pp. 1271-1276, Aug. 1954.

Common-Source Reference Amplifier





$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_m R}{1 + sRC}$$

Gain-BW Tradeoff

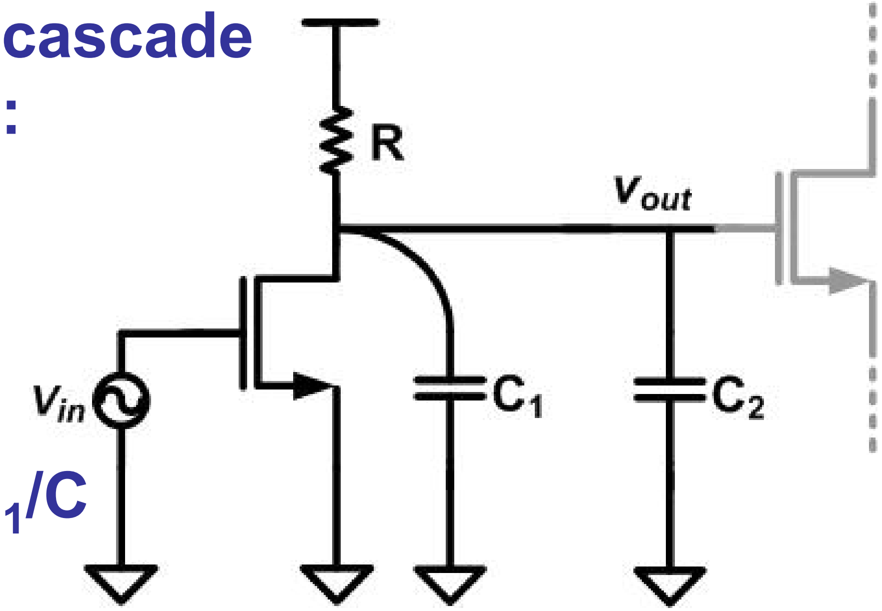
→Desire BW extension for a given gain

→Power Dissipation Fixed for Comparison

Multi-Stage Amplifier Parasitics

- CS amplifier in multi-stage cascade
- Transistor W/L depends on:
  - Gain
  - Voltage Swing
  - Supply Current
  - Noise Figure
- Define: $k_C = C_1/(C_1 + C_2) = C_1/C$

→ design constraint



→ Desire BW extension for a given k_C

Peaking Techniques

Modify Conventional Peaking Techniques:

- Obtain larger BW extension ratio (BWER), smaller settling time
- Include (and exploit) parasitic effects
- Retain simplicity and generality
- Comprehensive design for different k_C values
  - Important Result: Use different techniques for different k_C values

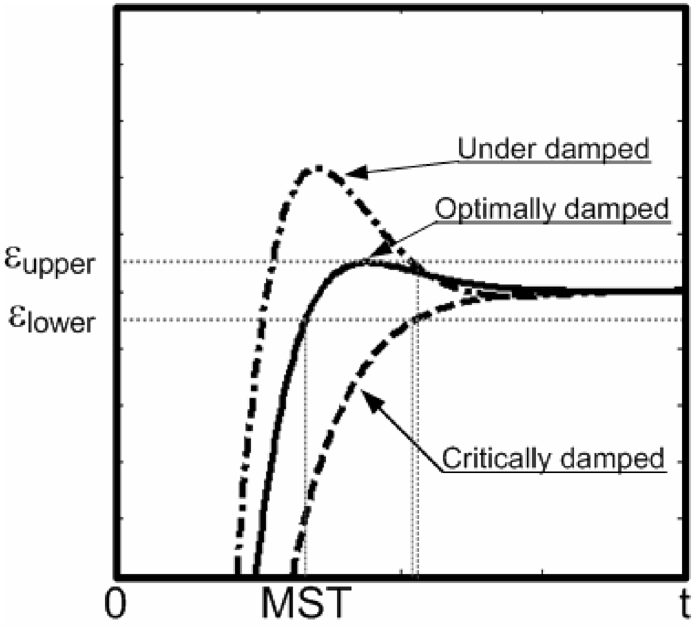
Bandwidth extension approaches:

- Resonance, capacitor splitting, magnetic coupling

Terminology

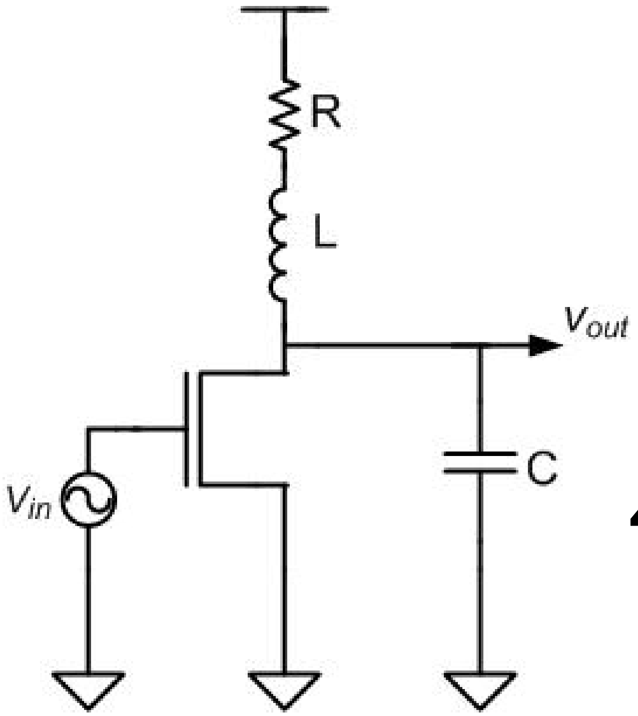
- BW extension ratio (BWER) = $f_{3dB,\ peak} / f_{3dB,\ ref}$
- Settling Time (1%) reduction ratio (STRR) = $\tau_{s,\ ref} / \tau_{s,\ peak}$
- Rise Time (10-90%) reduction ratio (RTRR) = $\tau_{r,\ ref} / \tau_{r,\ peak}$

BWER, STRR & RTRR hard to maximize simultaneously. Optimize for desired application.



MST = Minimum settling Time

Conventional Shunt Peaking

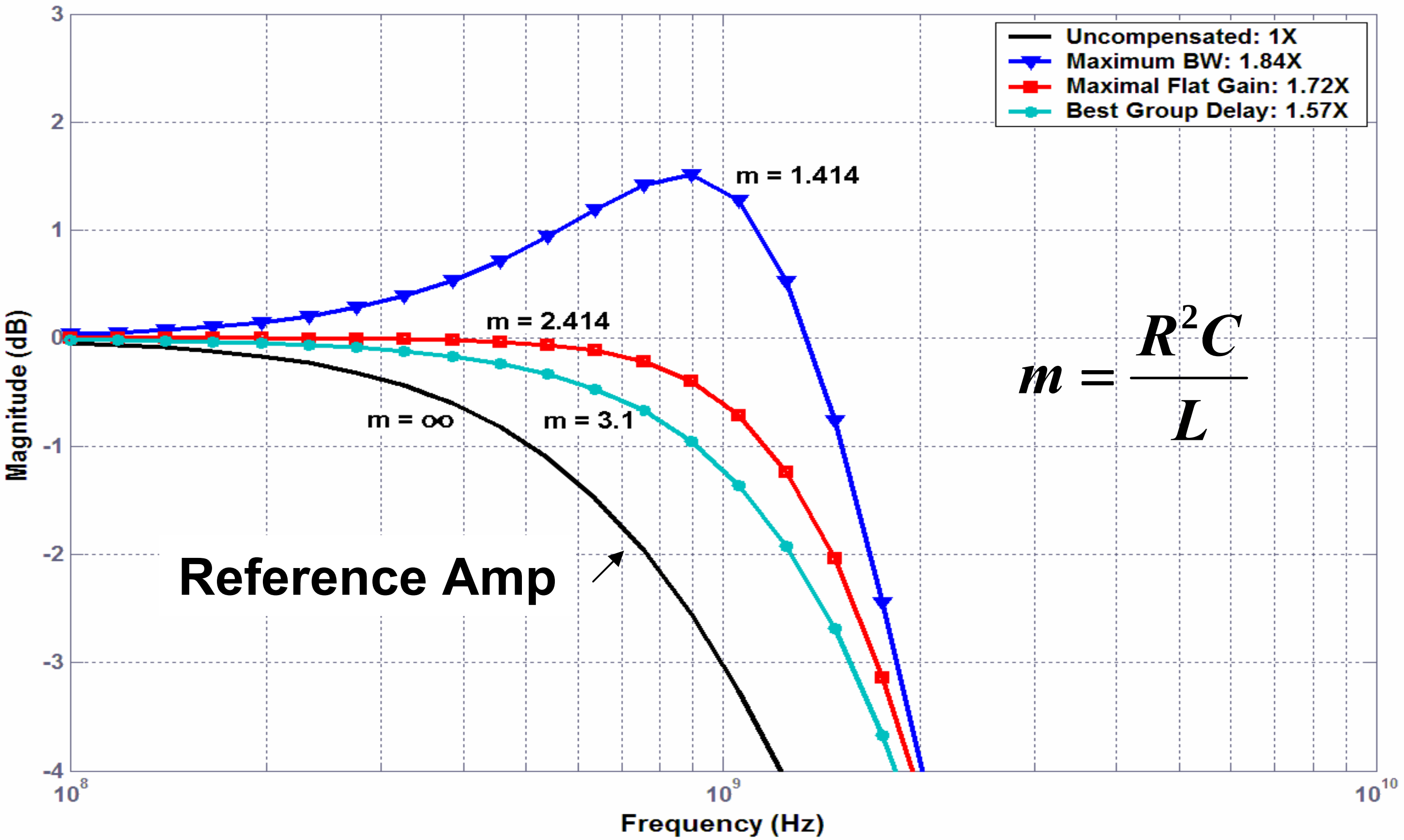


$$Z(s) = \frac{R + sL}{1 + sRC + s^2 LC}$$

$$m = \frac{R^2 C}{L} \qquad \omega_0 = \frac{1}{RC}$$

$$Z_N(s) = \frac{1 + s/m\omega_0}{1 + s/\omega_0 + s^2/m\omega_0^2}$$

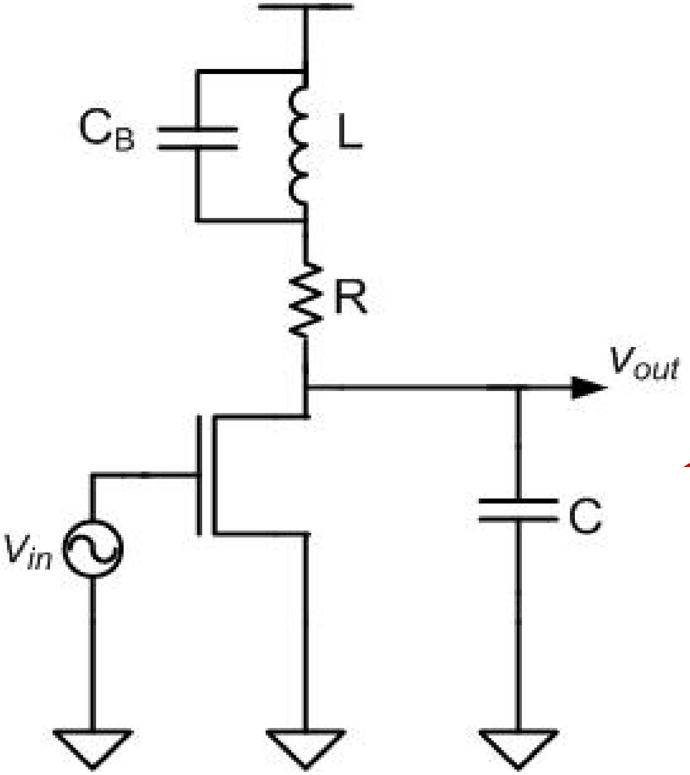
Conventional Shunt Peaking - II



$$m = \frac{R^2 C}{L}$$

m = √2 → 1.84X & 1.5dB Peaking

Bridged-Shunt Peaking



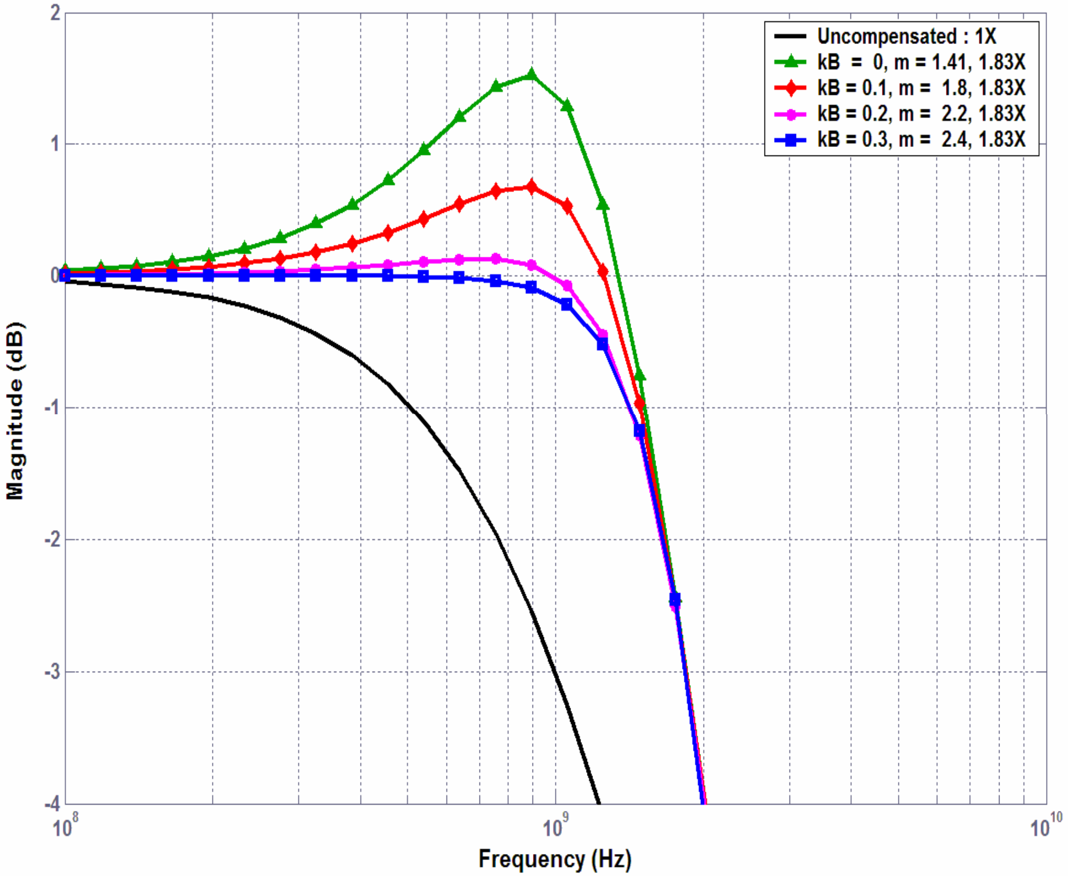
$$Z_N(s)=\frac{1+\left(\frac{1}{m}\right)\frac{s}{\omega_0}+\left(\frac{k_B}{m}\right)\frac{s^2}{\omega_0^2}}{1+\frac{s}{\omega_0}+\left(\frac{k_B+1}{m}\right)\frac{s^2}{\omega_0^2}+\left(\frac{k_B}{m}\right)\frac{s^3}{\omega_0^3}}$$

$$m=\frac{R^2C}{L}\quad \omega_0=\frac{1}{RC}\quad k_B=\frac{C_B}{C}$$

$$Z_N(s)=\frac{1+s/m\omega_0}{1+s/\omega_0+s^2/m\omega_0^2}$$

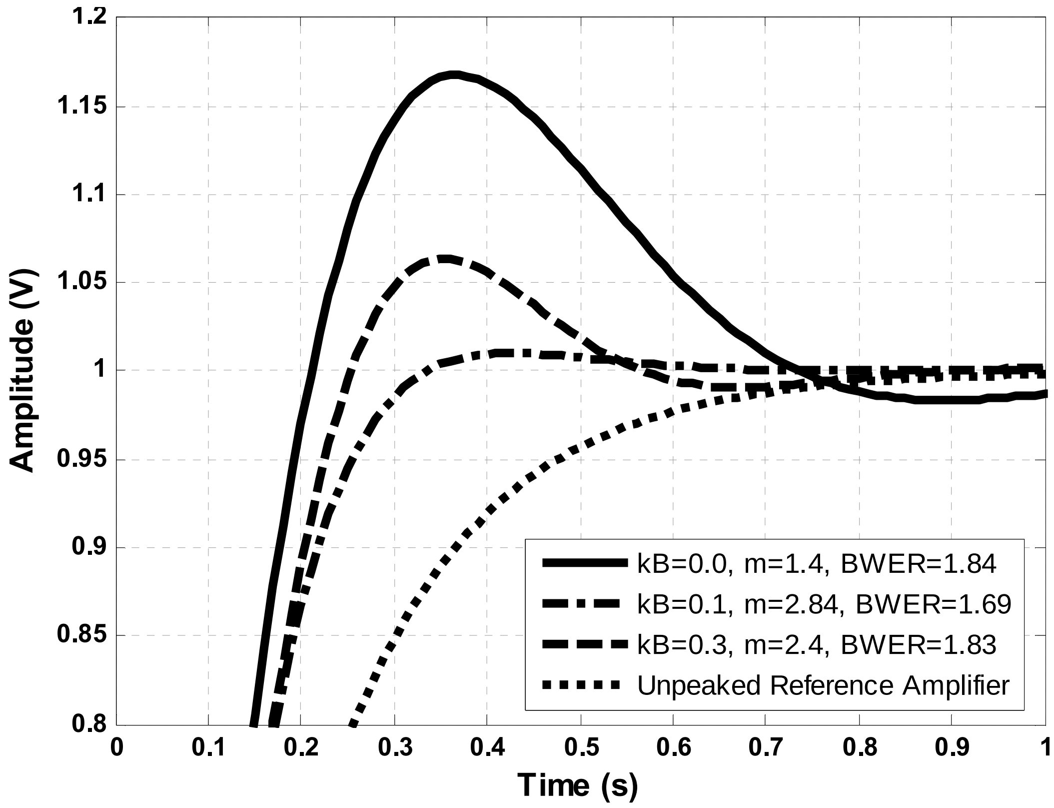
Note: Inductor parasitic forms C_B
Question: Interchange *L* and *R*?

Bridged-Shunt Peaking



m = 2.4, k_B = 0.3 → 1.83X and flat gain

Bridged-Shunt Peaking - II



Optimum Depends On Application

K_B	*m*	*STRR*	*RTRR*	*BWER*
0.0	1.4	0.70	2.18	1.84
0.1	2.84	2.40	1.74	1.69
0.3	2.4	1.39	1.87	1.83

Bridged-Shunt Peaking

Advantages☺

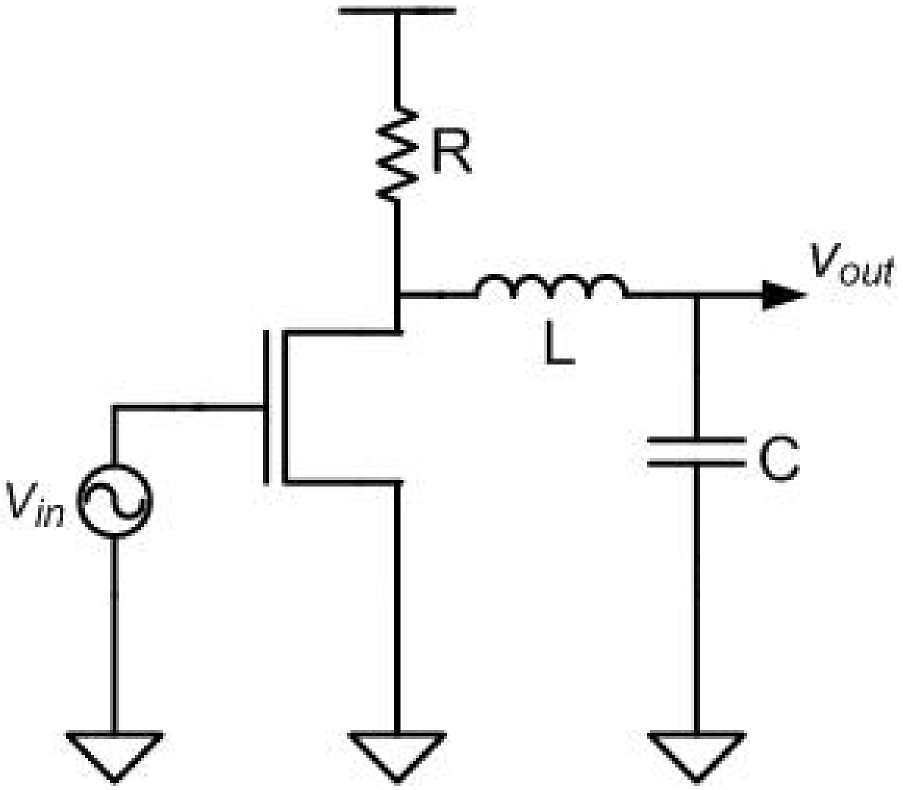
- **Incorporates inductor parasitics (Add more C_B if needed)**

✓Maximum BW possible with flat gain (No 1.5dB peaking)

✓m ↑ == L ↓ → Smaller Area

✓Area overhead for added C_B minimal

Conventional Series Peaking



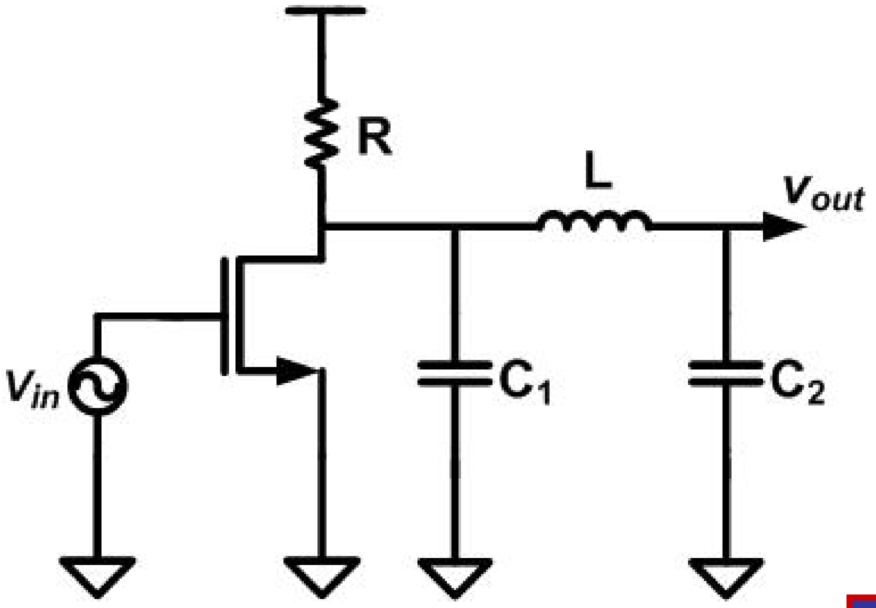
$$Z_N(s) = \frac{1}{1 + s/\omega_0 + s^2/m\omega_0^2}$$

- **Lack of Zero**
- **Inferior to Shunt peaking**

m = 2 ⟹ 1.41X

Series Peaking with Drain Parasitics

$$Z_N(s) = \frac{1}{1 + \frac{s}{\omega_0} + \left(\frac{1-k_C}{m}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_C(1-k_C)}{m}\right)\frac{s^3}{\omega_0^3}}$$

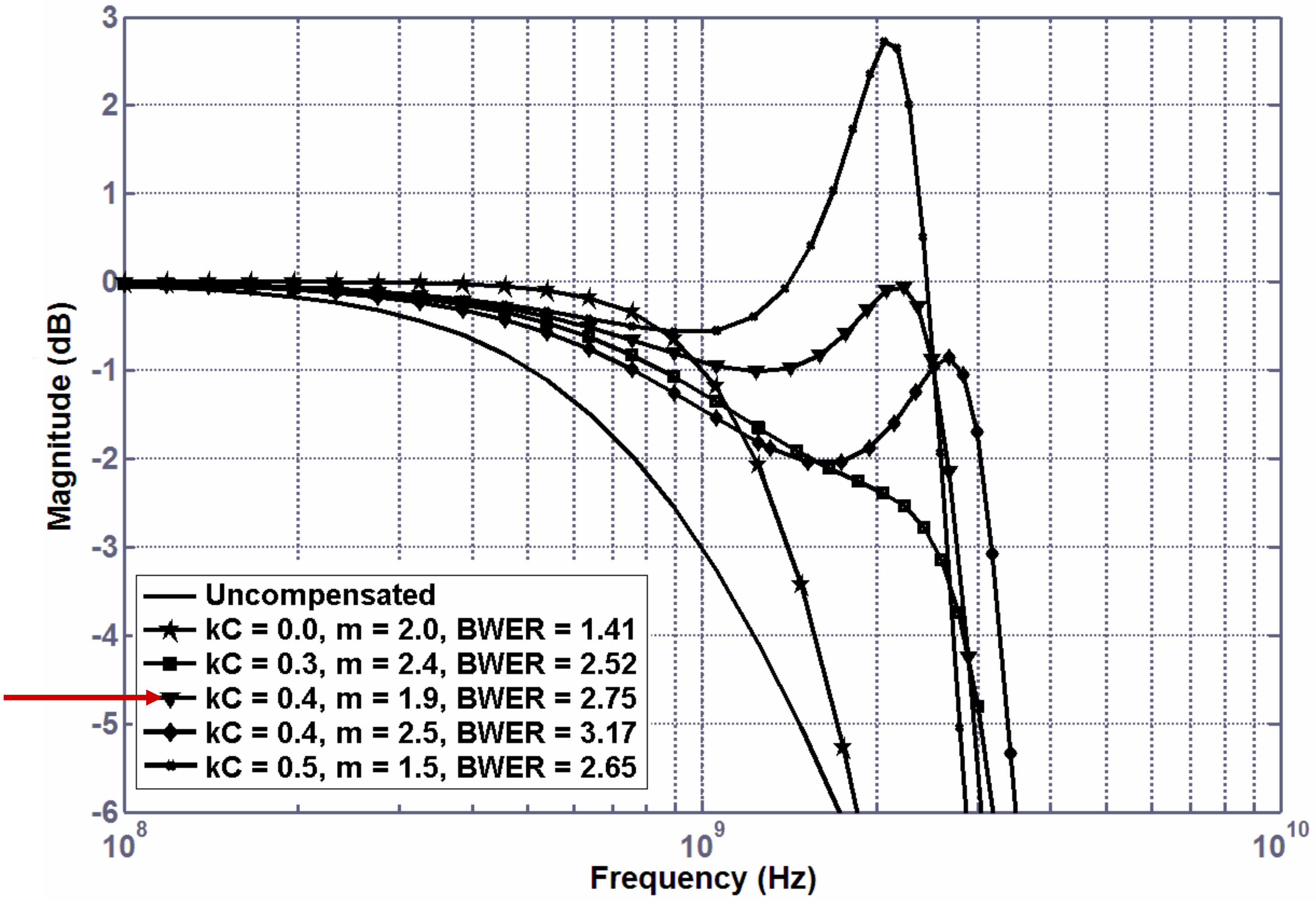


$$k_C = \frac{C_1}{C}$$

$$Z_N(s) = \frac{1}{1 + s/\omega_0 + s^2/m\omega_0^2}$$

Conventional Series Peaking
Capacitor Splitting Idea

Series Peaking vs. k_C

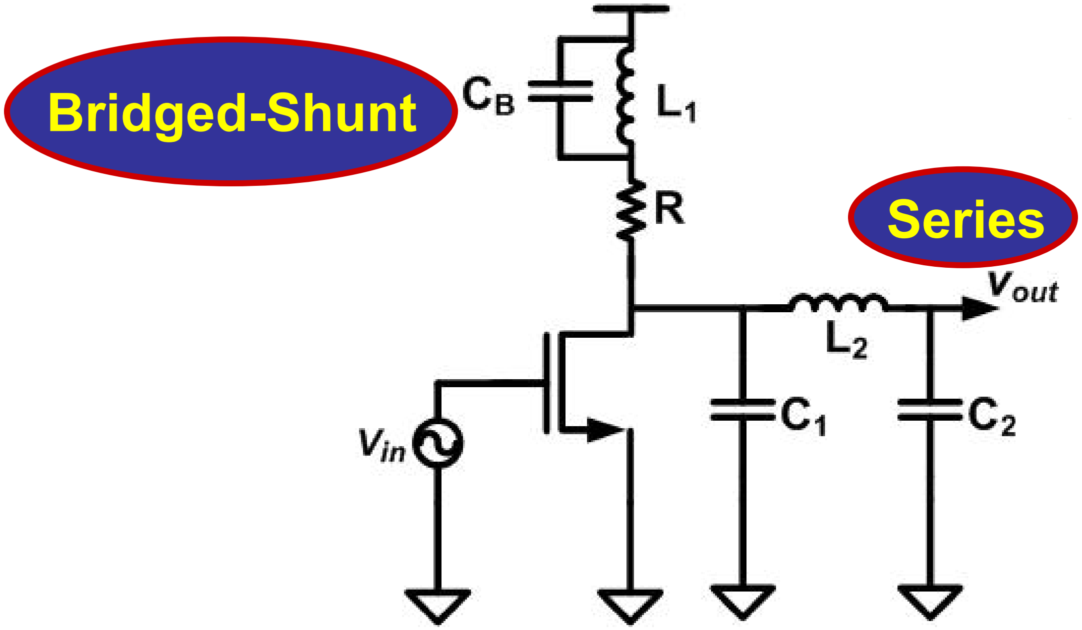


Series Peaking with C_1: Summary

$k_C = C_1/C$	Peaking (dB)	$m = R^2C/L$	BWER
0	0	2	1.41
0.1	0	1.8	1.58
0.2	0	1.8	1.87
0.3	0	2.4	2.52
0.4	1	1.9	2.75 ←
	2	2.5	3.17
0.5*	3.3	1.5	2.65

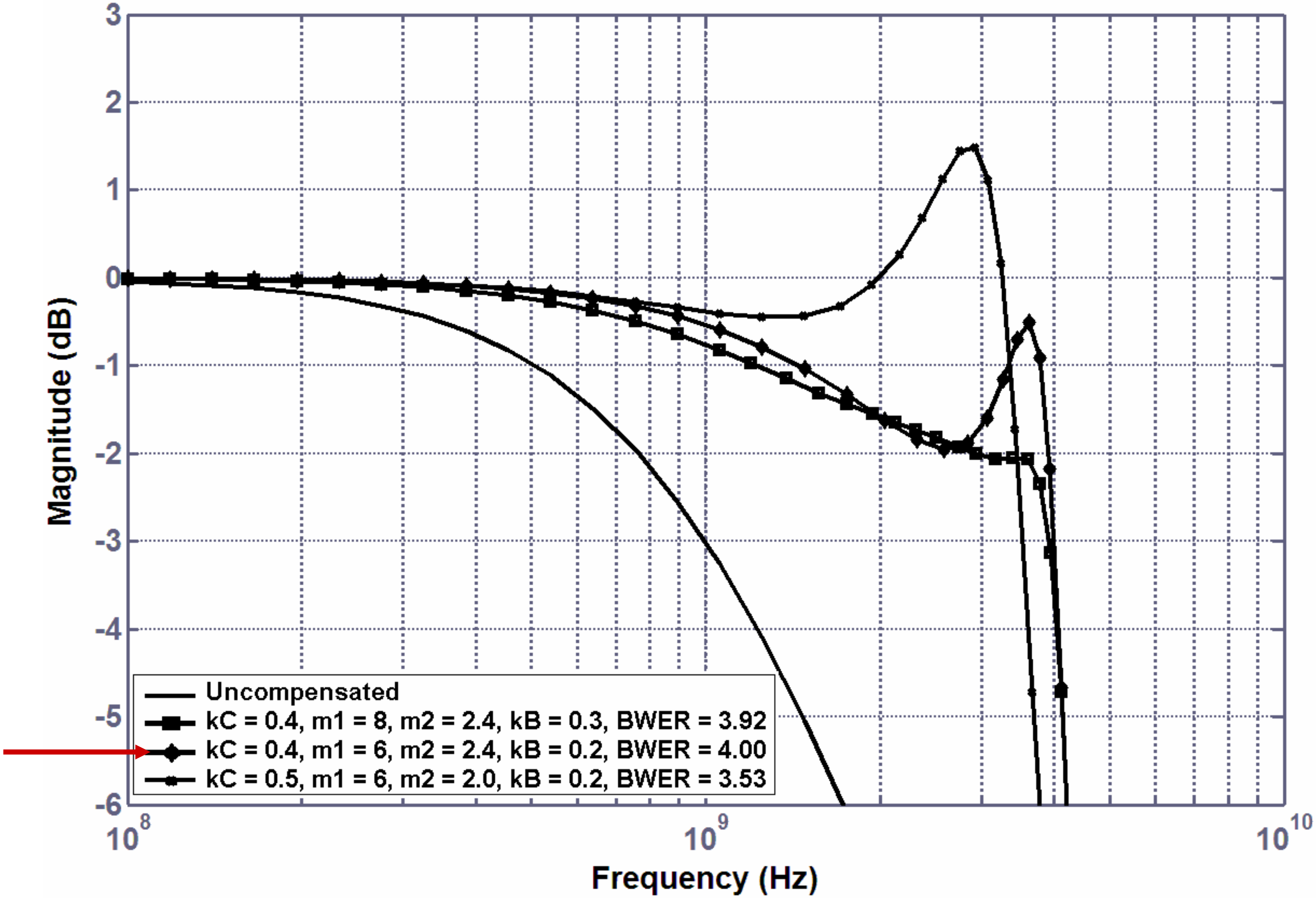
* B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1263-1270, Aug. 2004.

Bridged-Shunt-Series Peaking



$$Z_N(s)=\frac{1+\left(\frac{1}{m_1}\right)\frac{s}{\omega_0}+\left(\frac{k_B}{m_1}\right)\frac{s^2}{\omega_0^2}}{1+\frac{s}{\omega_0}+\left(\frac{1+k_B}{m_1}+\frac{1-k_C}{m_2}\right)\frac{s^2}{\omega_0^2}+\left(\frac{k_B}{m_1}+\frac{k_C(1-k_C)}{m_2}\right)\frac{s^3}{\omega_0^3}+\left(\frac{(k_C+k_B)(1-k_C)}{m_1m_2}\right)\frac{s^4}{\omega_0^4}+\left(\frac{k_Bk_C(1-k_C)}{m_1m_2}\right)\frac{s^5}{\omega_0^5}}$$

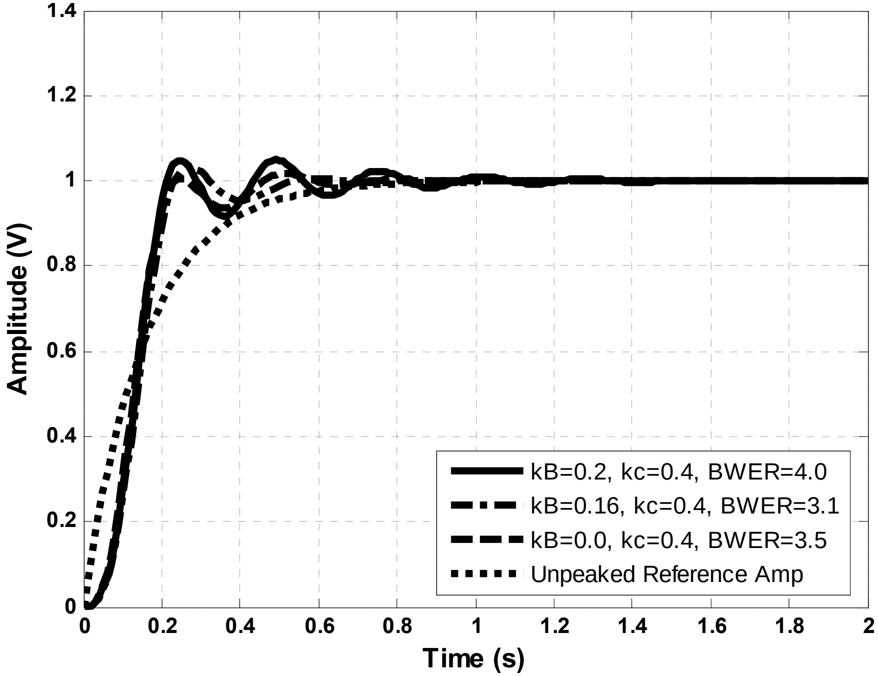
Bridged-Shunt-Series Peaking - II



Bridged-Shunt-Series Summary - I

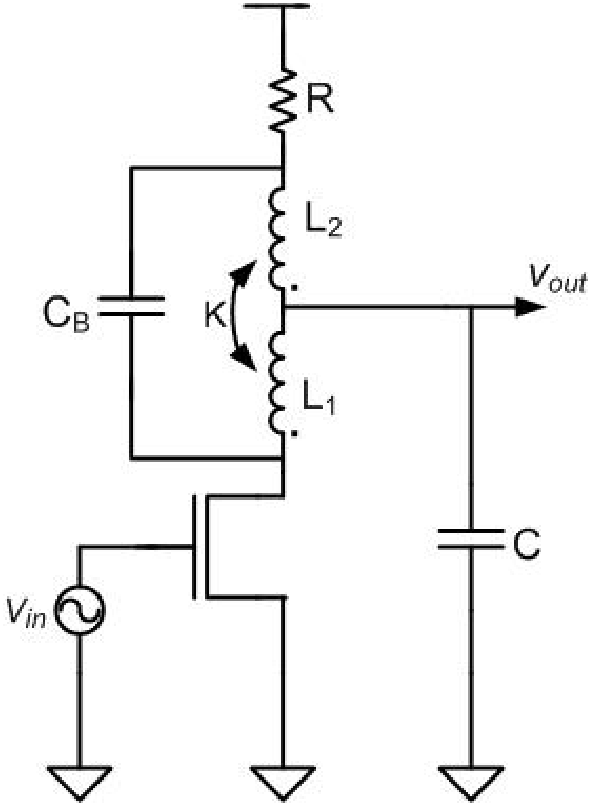
$k_C=C_1/C$	Peak (dB)	$m_1=R^2C/L_1$	$m_2=R^2C/L_2$	$k_B=C_B/C$	BWER
0.4	0	8	2.4	0.3	3.92
	2	6	2.4	0.2	4
0.5	2	6	2	0.2	3.53

Bridged-Shunt-Series Summary - II



k_C	k_B	m_1	m_2	*STRR*	*RTRR*	*BWER*
0.4	0.0	6.3	2.6	1.32	2.73	3.47
	0.16	8	2.2	1.46	2.78	3.11
	0.2	6	2.4	0.71	2.89	4.00
	0.3	8	2.4	0.95	2.66	3.92
0.5	0.1	6	2	0.75	2.91	3.40
	0.2	6	2	0.77	2.88	3.53

Conventional Bridged T-Coil Peaking



$$Z_N(s) = \frac{1}{1 + (s/\omega_n)2\zeta + s^2/\omega_n^2}$$

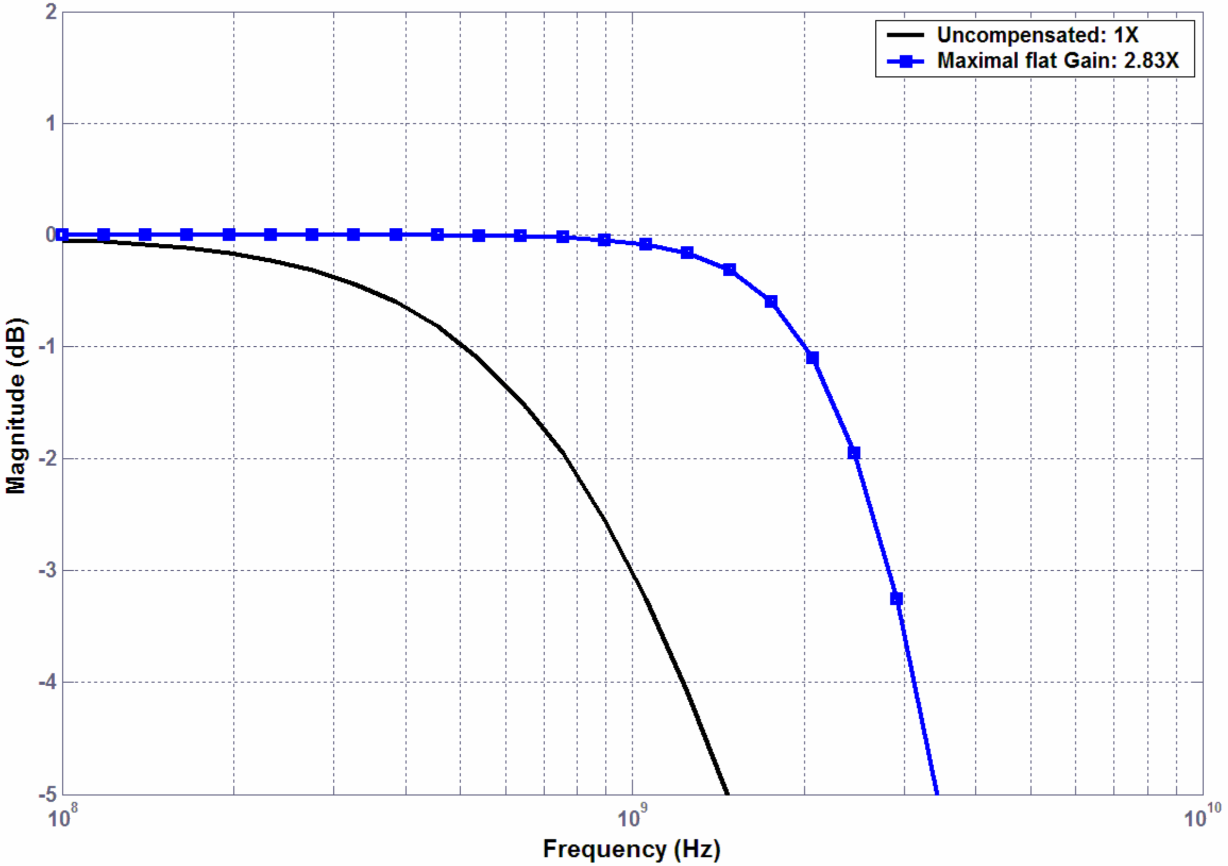
- $L_1 = L_2$
- Butterworth response
- Double shunt-series peaking

$\zeta = 1/\sqrt{2}$ k = -1/3 ➡ 2.83X

Capacitor Splitting + Magnetic Coupling

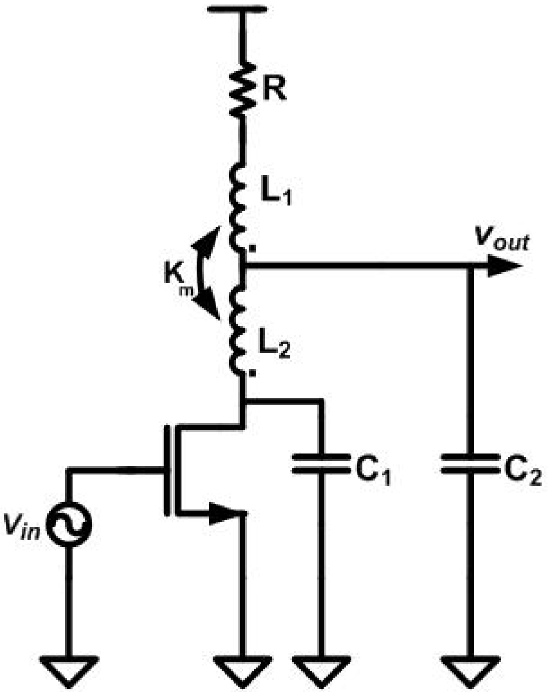
B. Hofer, *Amplifier Frequency and Transient Response (AFTR) Notes*: Tektronix, Inc. , 1982. Original notes from Carl Battjes. Tektronix used package lead inductors to implement T-coils circa 1970.

Conventional Bridged T-Coil Peaking-II



$\zeta = 1/\sqrt{2}$ $k = -1/3$ → 2.83X

Asymmetric T-Coil Peaking - 1

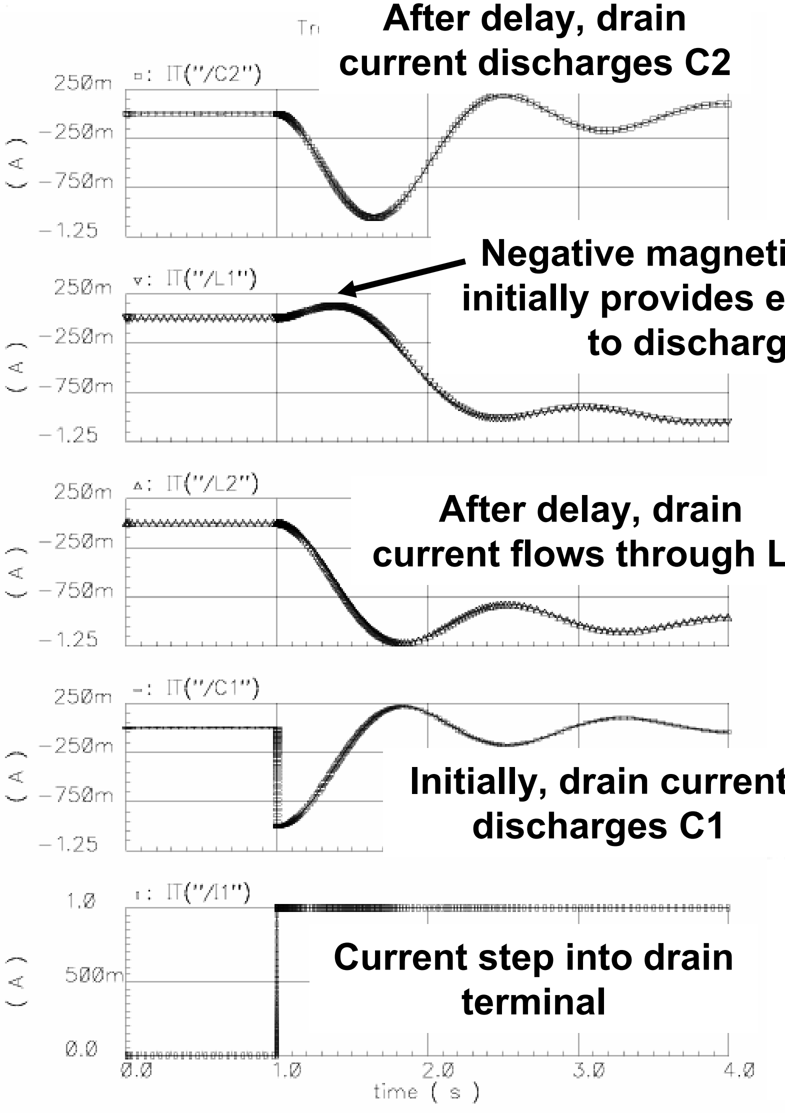


$$k_C = \frac{C_1}{C}$$

$$\boldsymbol{k_m = M / \sqrt{L_1 L_2}}$$

$$Z_N(s) = \frac{1 + \left(\dfrac{1}{m_1} + \dfrac{k_m}{\sqrt{m_1 m_2}}\right)\dfrac{s}{\omega_0}}{1 + \dfrac{s}{\omega_0} + \left(\dfrac{1}{m_1} + \dfrac{k_C}{m_2} + \dfrac{2k_C k_m}{\sqrt{m_1 m_2}}\right)\dfrac{s^2}{\omega_0^2} + \left(\dfrac{k_C(1-k_C)}{m_2}\right)\dfrac{s^3}{\omega_0^3} + \left(\dfrac{k_C(1-k_C)(1-k_m^2)}{m_1 m_2}\right)\dfrac{s^4}{\omega_0^4}}$$

Asymmetric T-Coil Peaking - 2



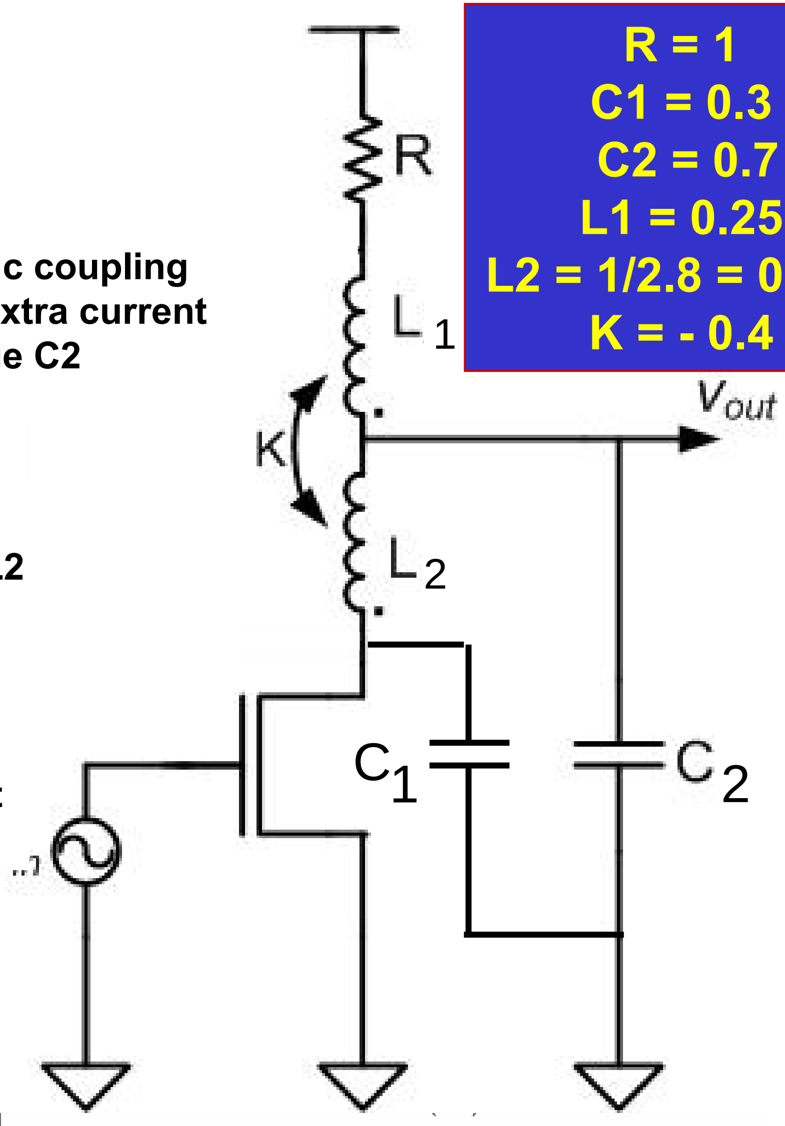
After delay, drain current discharges C2

Negative magnetic coupling initially provides extra current to discharge C2

After delay, drain current flows through L2

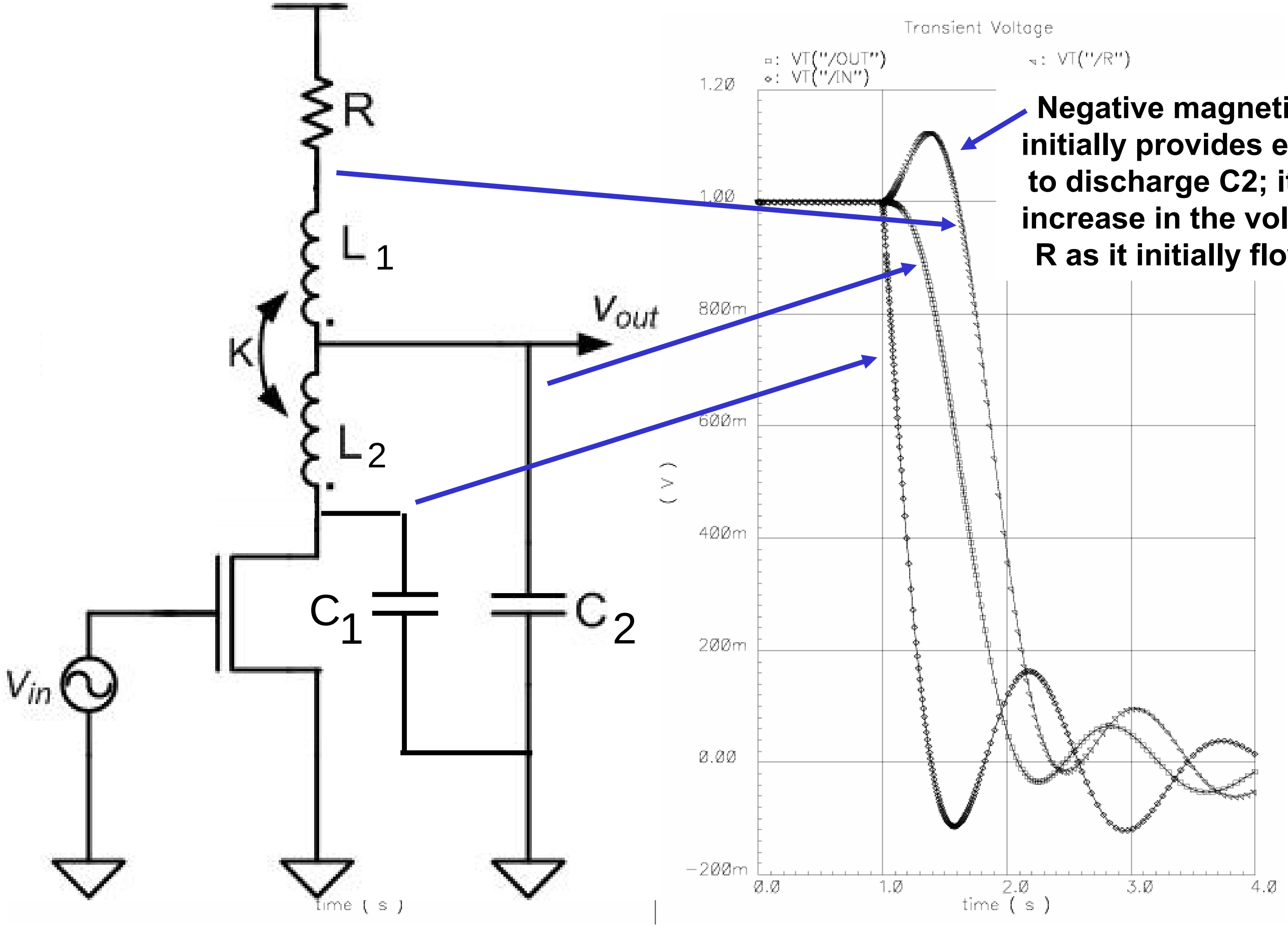
Initially, drain current discharges C1

Current step into drain terminal



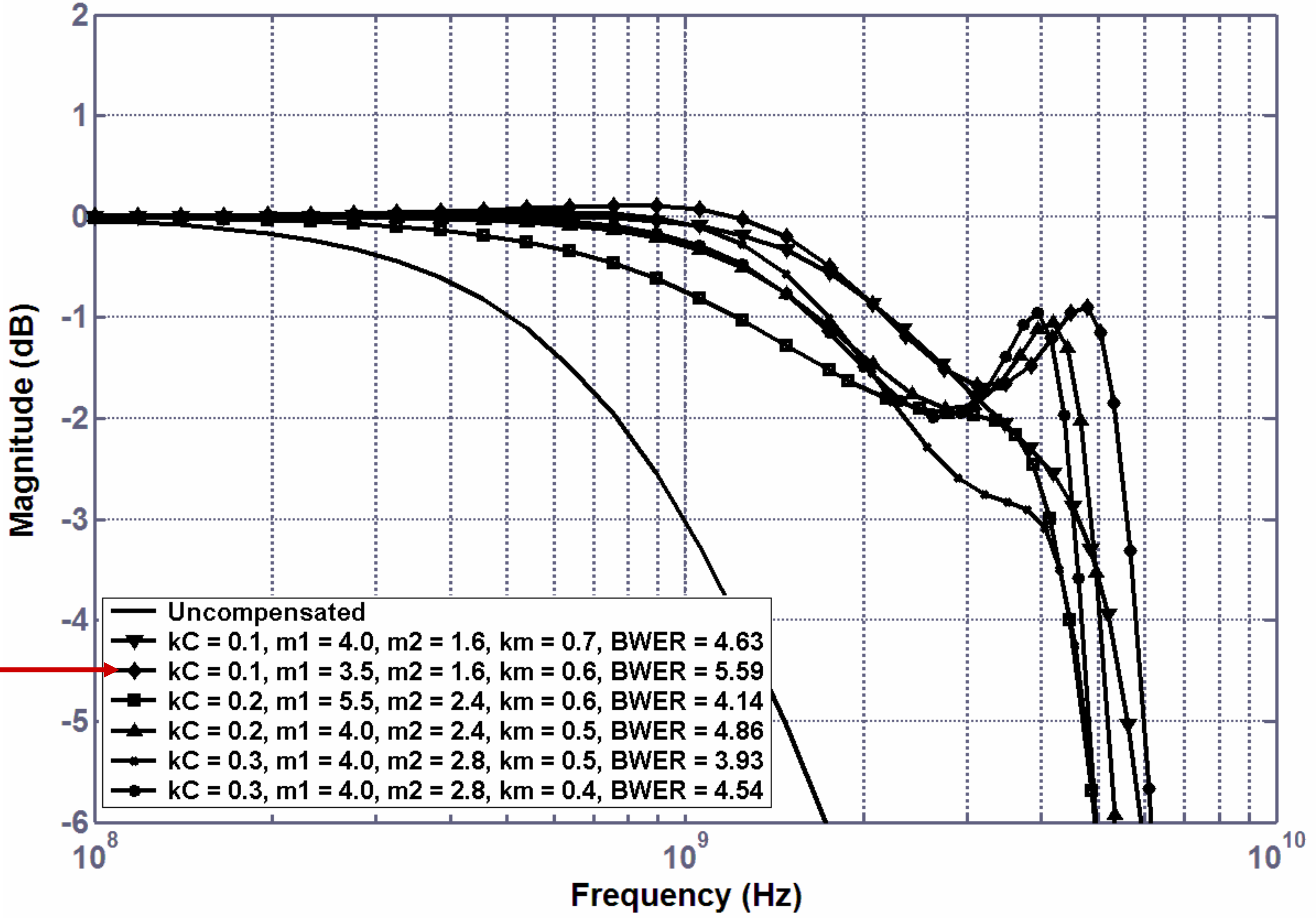
R = 1
C1 = 0.3
C2 = 0.7
L1 = 0.25
L2 = 1/2.8 = 0.357
K = - 0.4

Asymmetric T-Coil Peaking - 3



Negative magnetic coupling initially provides extra current to discharge C2; it causes an increase in the voltage across R as it initially flows upward

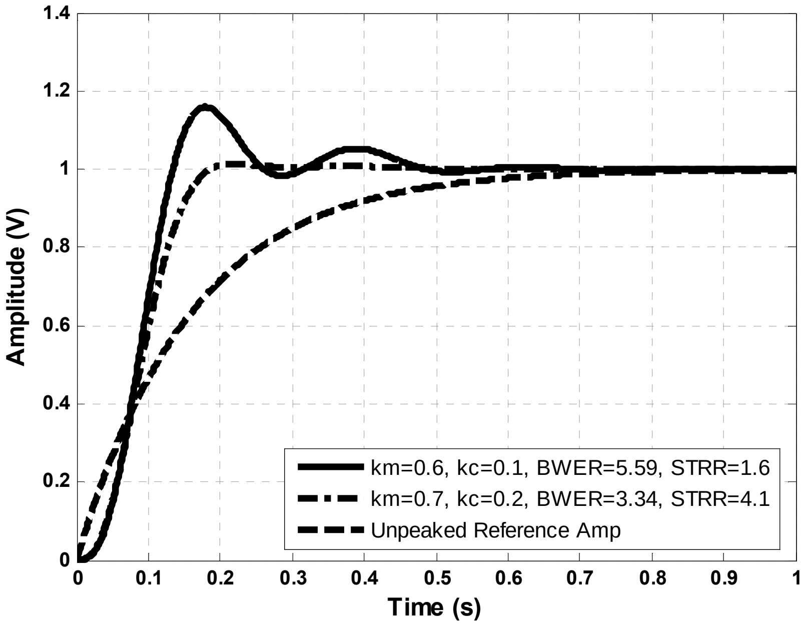
Asymmetric T-Coil Peaking - 4



Asymmetric T-Coil Summary - I

$k_C=C_1/C$	Peak (dB)	$m_1=R^2C/L_1$	$m_2=R^2C/L_2$	$k_m = M/\sqrt{L_1L_2}$	BWER
0.1	0	4	1.6	-0.7	4.63
	1	3.5	1.2	-0.6	4.92
	2	3.5	1.6	-0.6	5.59
0.2	0	5.5	2.4	-0.6	4.14
	1	3	2	-0.6	4.51
	2	4	2.4	-0.5	4.86
0.3	0	4	2.8	-0.5	3.93
	1	3.5	2	-0.4	3.98
	2	4	2.8	-0.4	4.54

Asymmetric T-Coil Summary - II

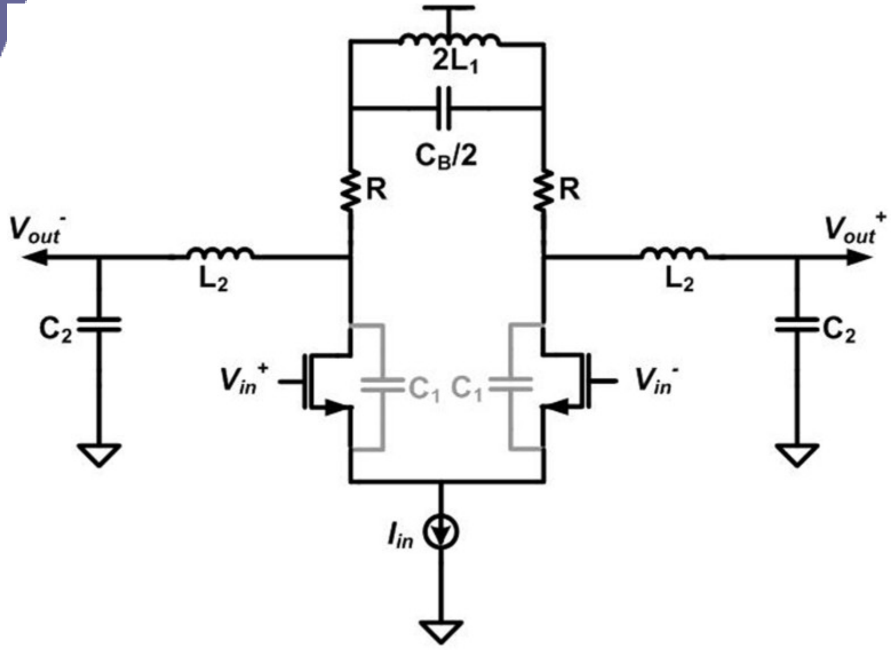


k_C	k_m	m_1	m_2	STRR	RTRR	BWER
0.1	0.7	4.0	1.6	1.90	4.20	4.63
	0.6	3.5	1.6	1.32	4.50	4.92
	0.6	3.5	1.2	1.57	4.43	5.59
	0.7	4.1	1.6	2.91	4.19	4.66
0.2	0.6	5.5	2.4	1.94	3.39	4.14
	0.6	3.0	2.0	1.23	3.91	4.51
	0.5	4.0	2.4	1.42	3.80	4.86
	0.7	4.6	2.2	4.11	3.35	3.34
0.3	0.5	4.0	2.8	1.54	3.40	3.93
	0.4	3.5	2.0	1.09	3.45	3.98
	0.4	4.0	2.8	1.10	3.52	4.54
	0.6	5.0	2.6	3.70	3.06	3.07

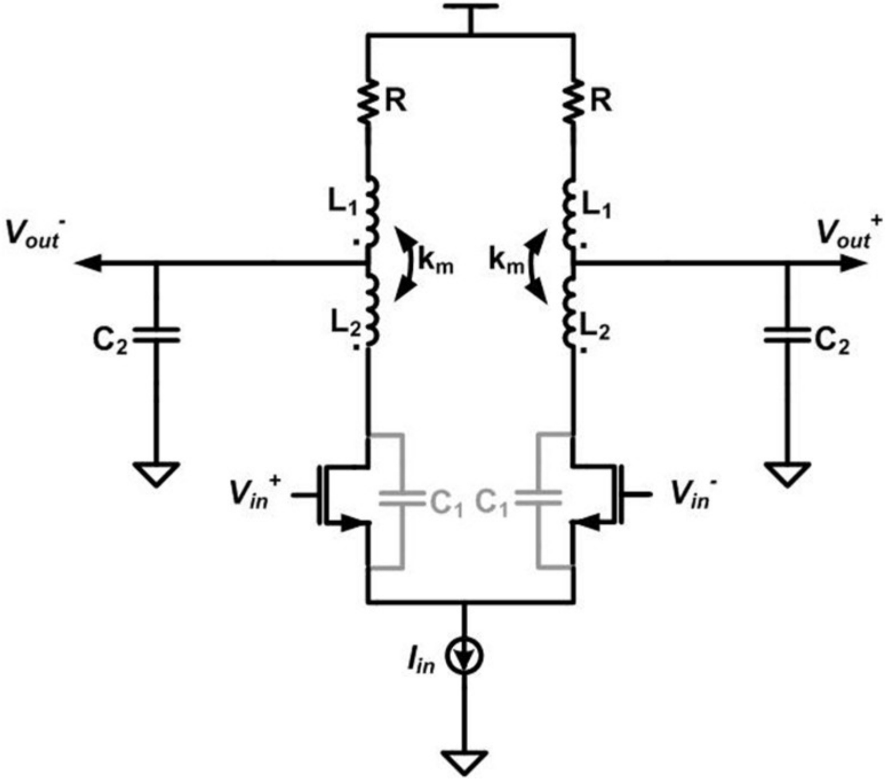
Peaking Techniques: Summary

k_C	Desired BWER	Desired STRR (1%)	Optimal Peaking Method
0.1-0.5	<1.83	<2.4	Bridged Shunt
0.1-0.4	3-5.59	<4.1	Asymmetric T-coil
0.4-0.5	3-4	<1.5	Bridged-Shunt-Series

Prototype Amplifiers



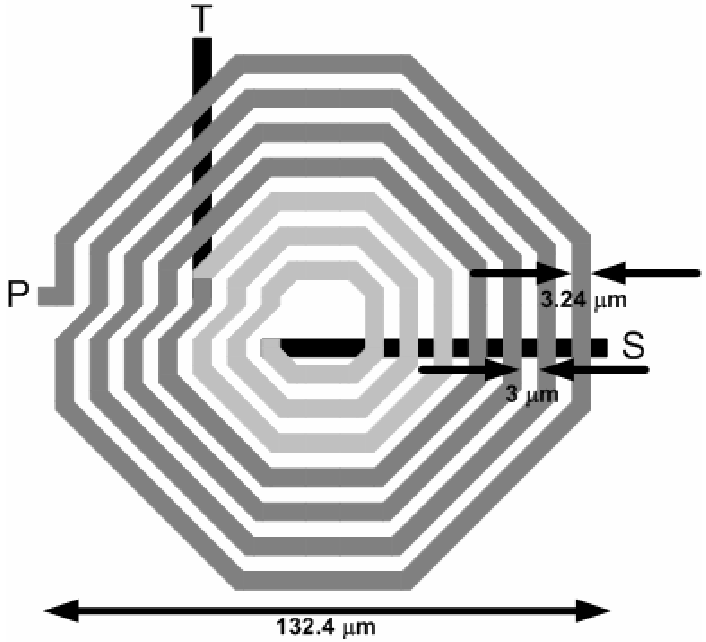
Bridged-Shunt-Series
$k_C = 0.4, 0.5$
Gain = 14dB
BW = 8GHz

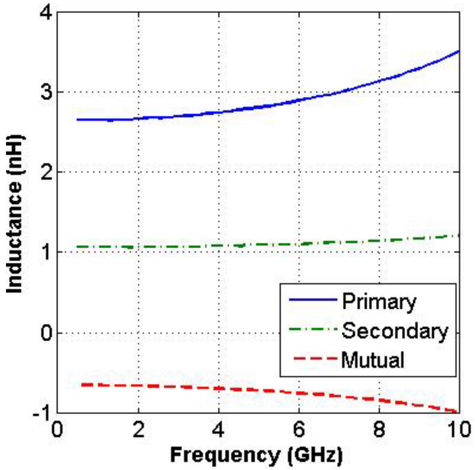


Asymmetric T-Coil
$k_C = 0.3$
Gain = 12dB
BW = 10.4GHz

Asymmetric T-coil

- T-coil needs weak-coupling
  → $k_m \sim 0.4$
- Simplicity, weak-coupling
  → concentric-windings
- Two-pronged design method
  → reduced design cycle
  1. Grover Calculations
  2. EM Simulation



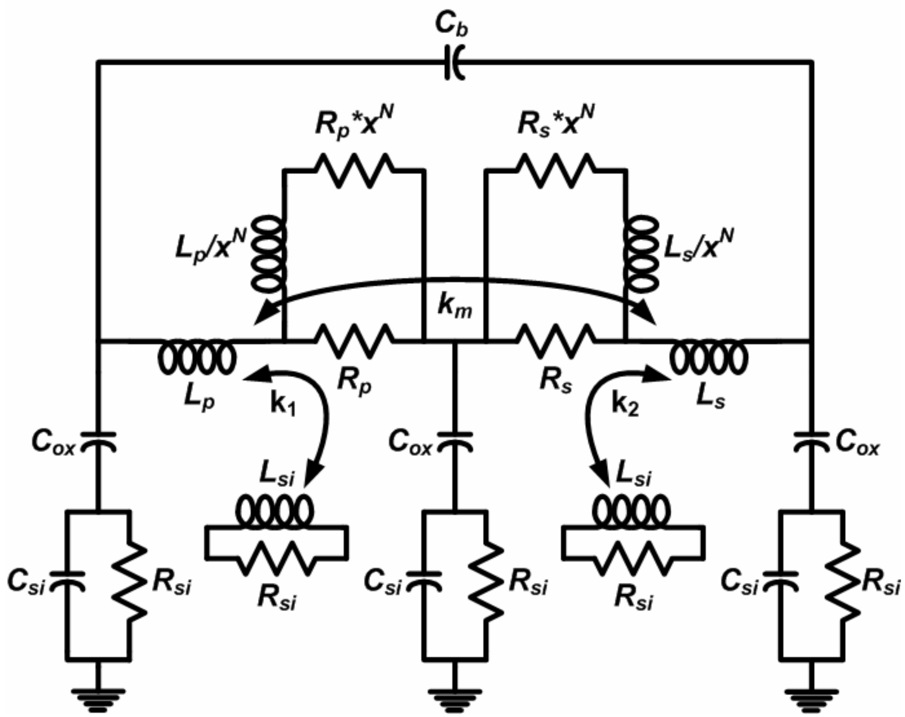


Spacing:	**3 µm**
Outer Diameter:	**132 µm**
Inner Diameter:	**51 µm**
Width:	**3.24 µm**
Top metal thickness:	**2 µm**

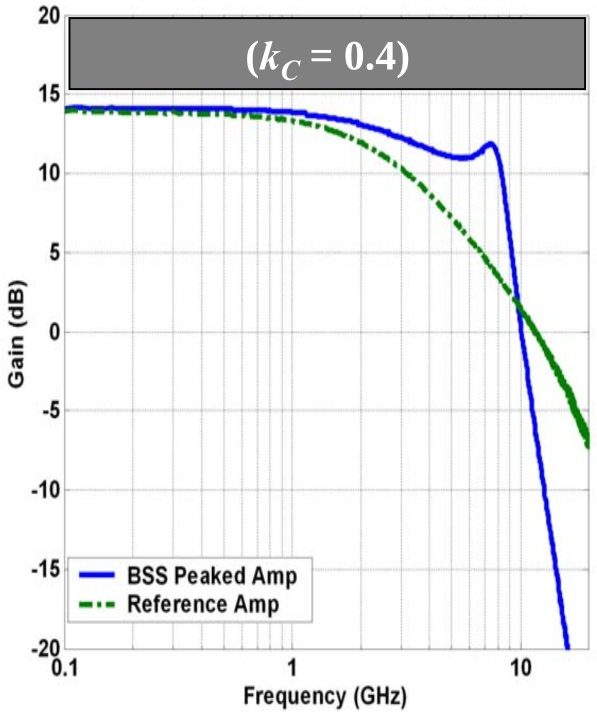
F. W. Grover, *Inductance Calculations: Working Formulas and Tables*. New York: D. Van Nostrand Company, Inc., 1946.

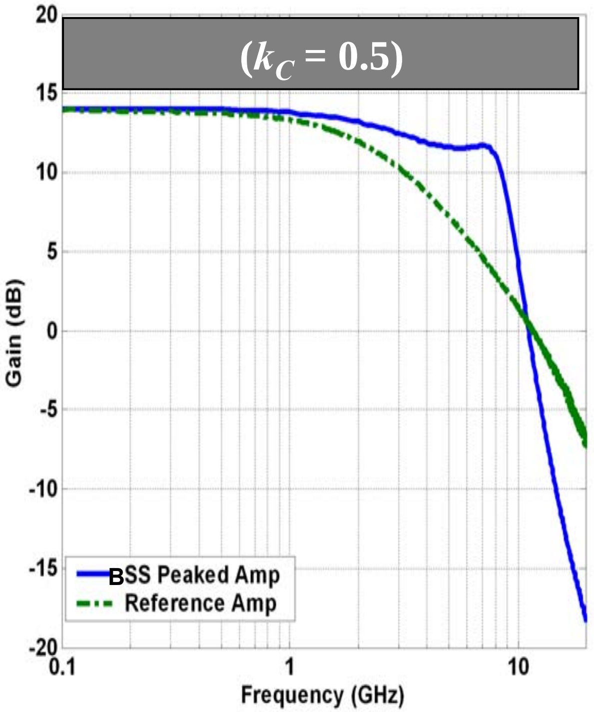
Asymmetric T-coil - II

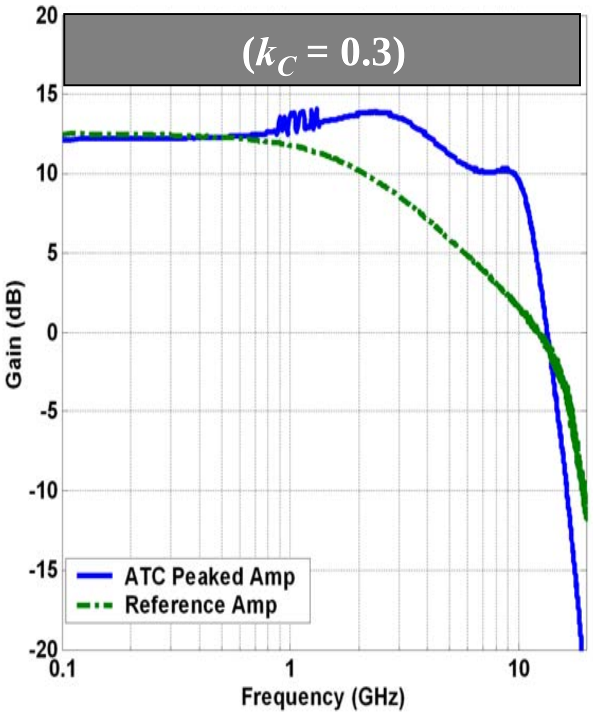
- T-coil EM simulation
  → freq. domain representation
- Transient simulation needs circuit model
- Proposed equivalent wideband circuit model
  → incorporates skin-effect, bulk-eddy currents
- Good to first self-resonance



Measurement Results







Bridge Shunt-Series
Gain = 14dB
BW = 8GHz
BWER = 3.0

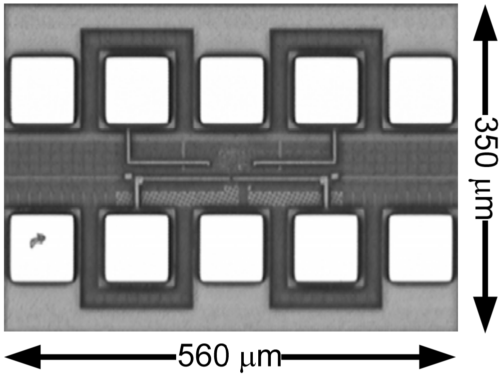
Asymmetric T-Coil
Gain = 12dB
BW = 10.4GHz
BWER = 4.1

Comparison

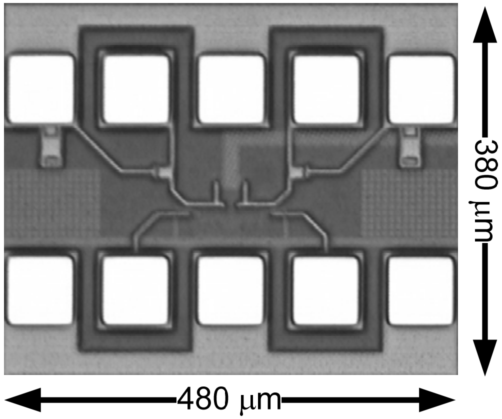
Reference	Bandwidth Extension Technique	CMOS Tech. (nm)	Single-stage		Multi-stage			
			Peaking (dB)	Single-stage BWER (Theory/Measured)	# Stages	Total Gain (dB)	Total Power (mW)	Total BW (GHz)
This work	Bridged-Shunt-Series	180	0.7	4.0/3.0	1	14.1	30	8
This work	Bridged-Shunt-Series	180	0.3	3.5/3.0	1	14.1	30	8
This work	Asymmetric T-coil with Negative Mutual Inductance	180	1.5	4.6/4.1	1	12.1	30	10.4
Galal, JSSC'04	Shunt-Series	180	1.8	3.5/NA	5	20.3	190	22
Kim, ISSCC'05	Asymmetric T-coil with Positive Mutual Inductance	130	0	3.23*/NA	-	-	-	42
Kanda, ISSCC'05	Shunt-Series	90	2.4	2/NA	2	-	21.6	20
Analui, ESSCIRC'02	Series Peaking	180	1.84-3	2.46/NA	3	56dBΩ	137.5 (single-ended)	9.2

* Simulated

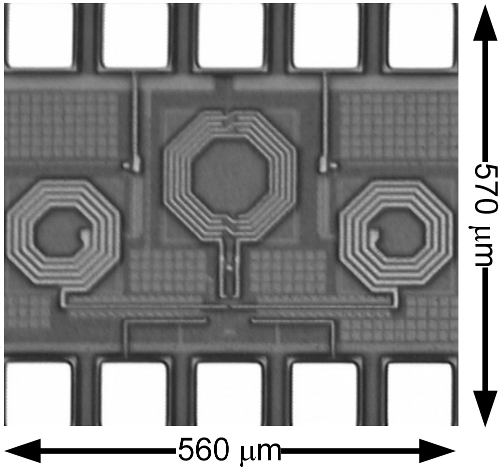
Die Micrographs in 0.18µm CMOS



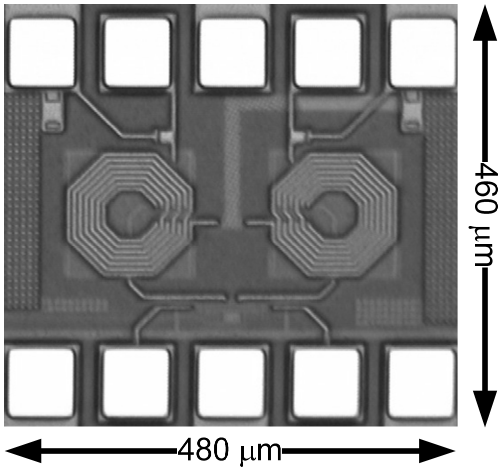
(a)



(b)



(c)

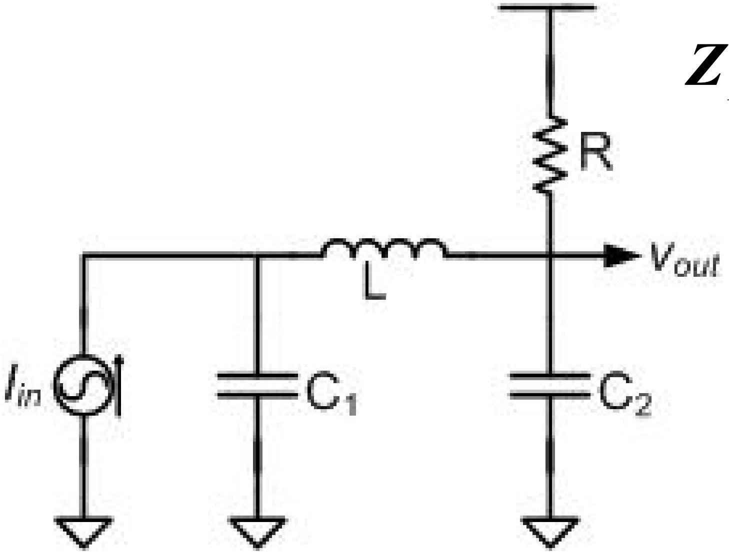


(d)

Conclusions

- Peaking techniques for larger BW extension
- Applicable to different k_C constraints
- Trade-off gain flatness for BW
- Amplifiers show large gain (>12dB) with largest BWER (4.1) reported.
- Wide bandwidth, high gain → fewer stages → power, area savings

Modified-Series Peaking

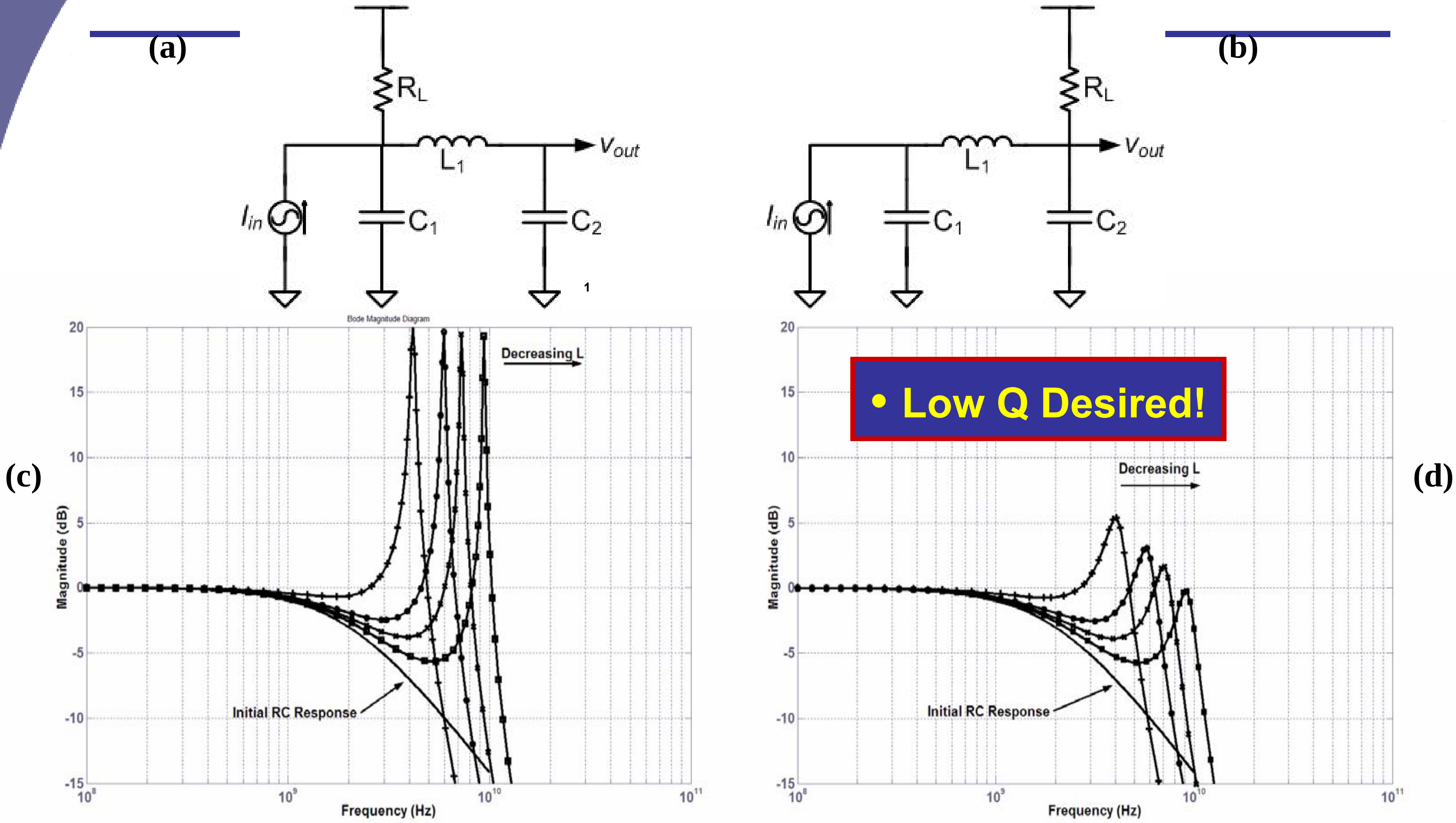


$$Z_N(s) = \frac{1}{1 + \frac{s}{\omega_0} + \left(\frac{k}{m}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k(1-k)}{m}\right)\frac{s^3}{\omega_0^3}}$$

- $C_1 \equiv$ Drain parasitics, etc.
- $C = C_1 + C_2$
- $C_1 = k_C C = kC$
- $m = R^2C/L$
- Note: *R* and *L* interchanged

Assuming k<<1, $Z_N(\omega) \approx \dfrac{1}{\left(1-\omega^2 LC_1\right)\left(1+j\omega RC_2\right)}$

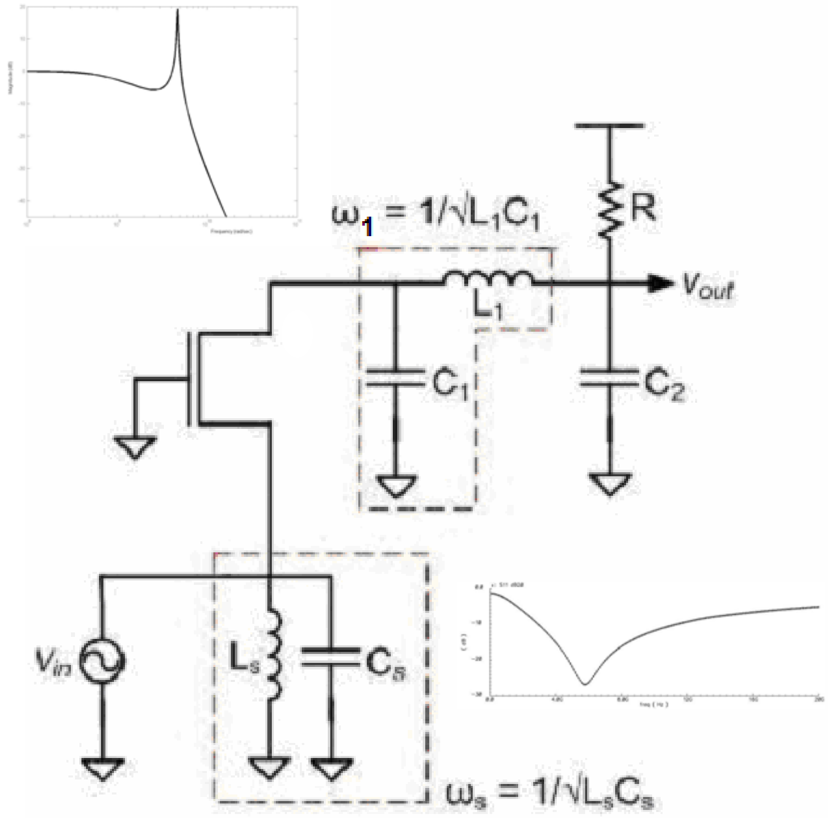
Peaking Response

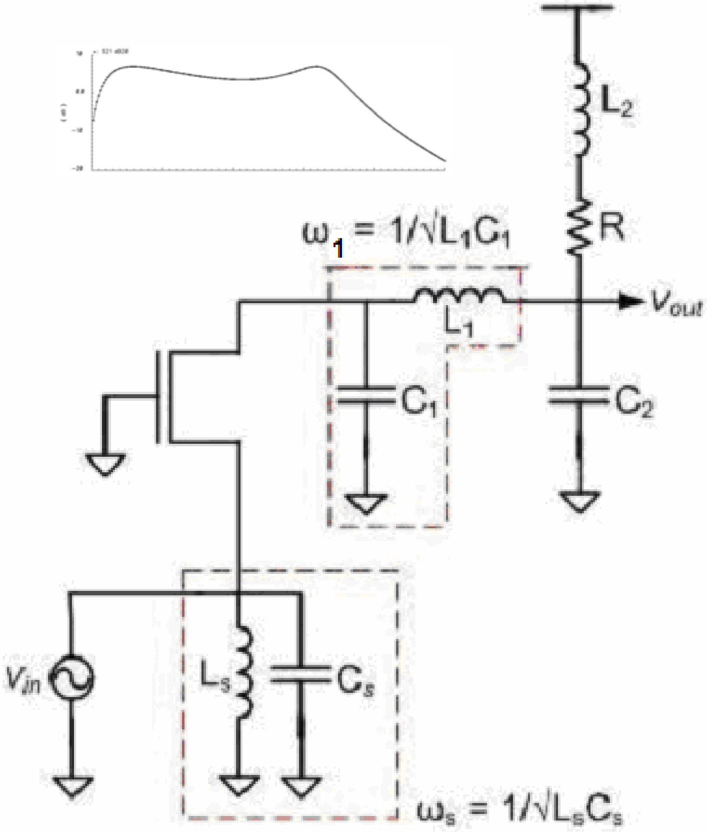


- **Low Q Desired!**

Simulated normalized responses of (b) with (c) L_1 ideal, and (d) L_1 with typical parasitics in a CMOS implementation (π-model)

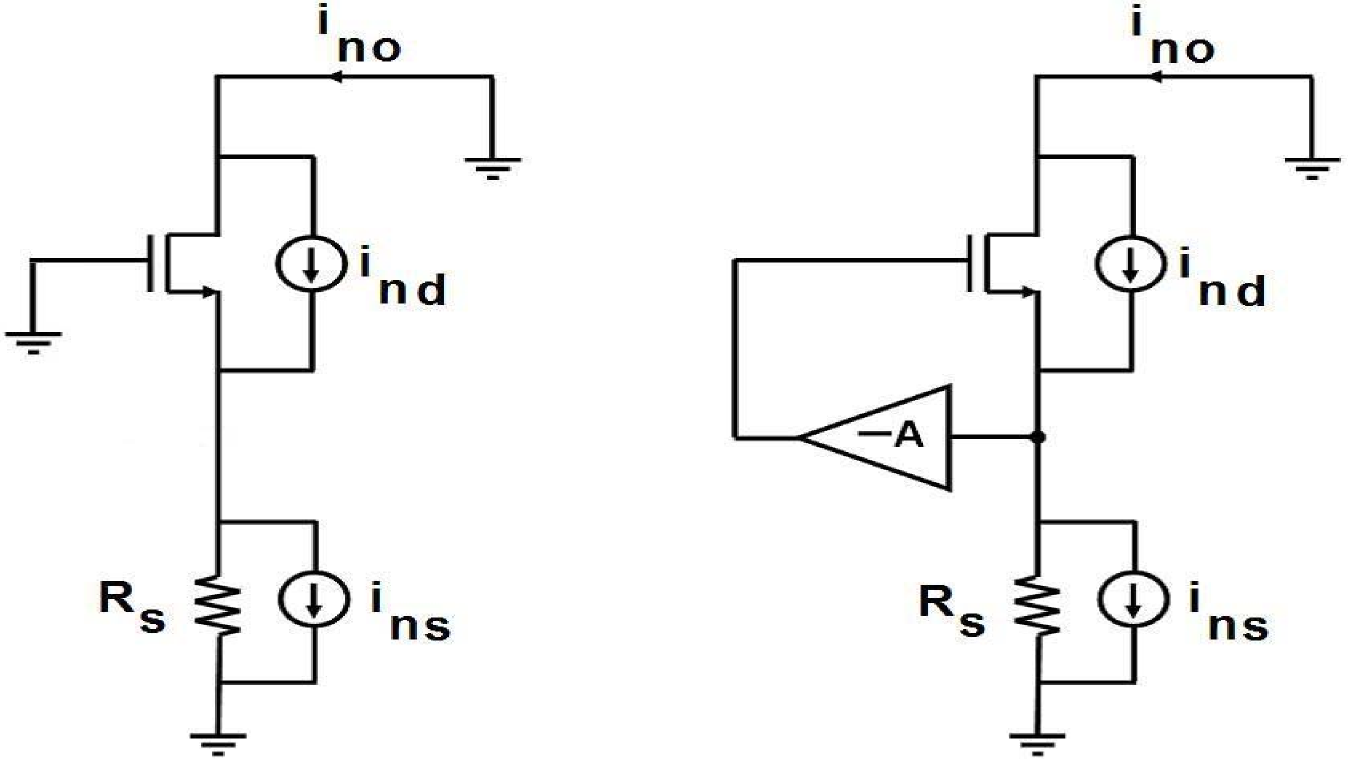
Anti-Staggered Series Peaking





- Similar to Pre-emphasis Idea
- Actually Tuning S_{11} (zero) and S_{21} (pole)
- Common-gate Amplifier!

g_m-Boosted CGLNA



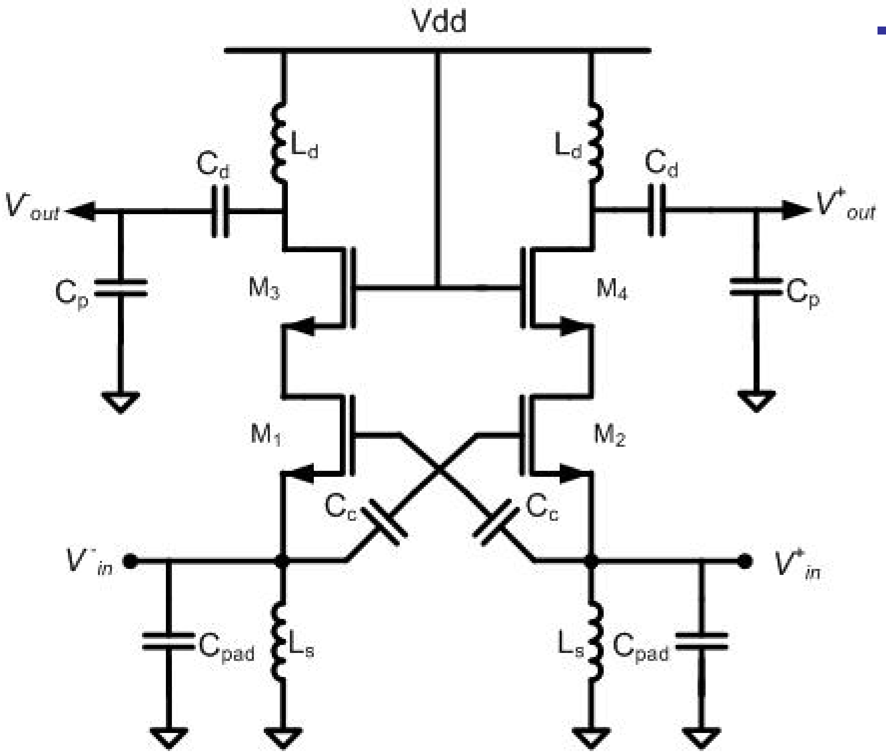
$$F \approx 1 + \frac{\gamma}{\alpha}$$

$$F \approx 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1+A}$$

**** X. Li, S. Shekhar and D.J. Allstot, “Low-power gm-boosted LNA and VCO circuits in 0.18um CMOS,” IEEE Intl. Solid-State Circuits Conference, Feb. 2005, pp. 534,535,615.*

**** X. Li, S. Shekhar and D.J. Allstot, “Gm-boosted LNA and VCO Circuits in 0.18um CMOS,” IEEE J. Solid-State Circuits, vol. 40, Dec. 2005.*

Capacitor Cross-Coupled-CGLNA



- **Lower Noise Figure**
- **Lower DC Current**

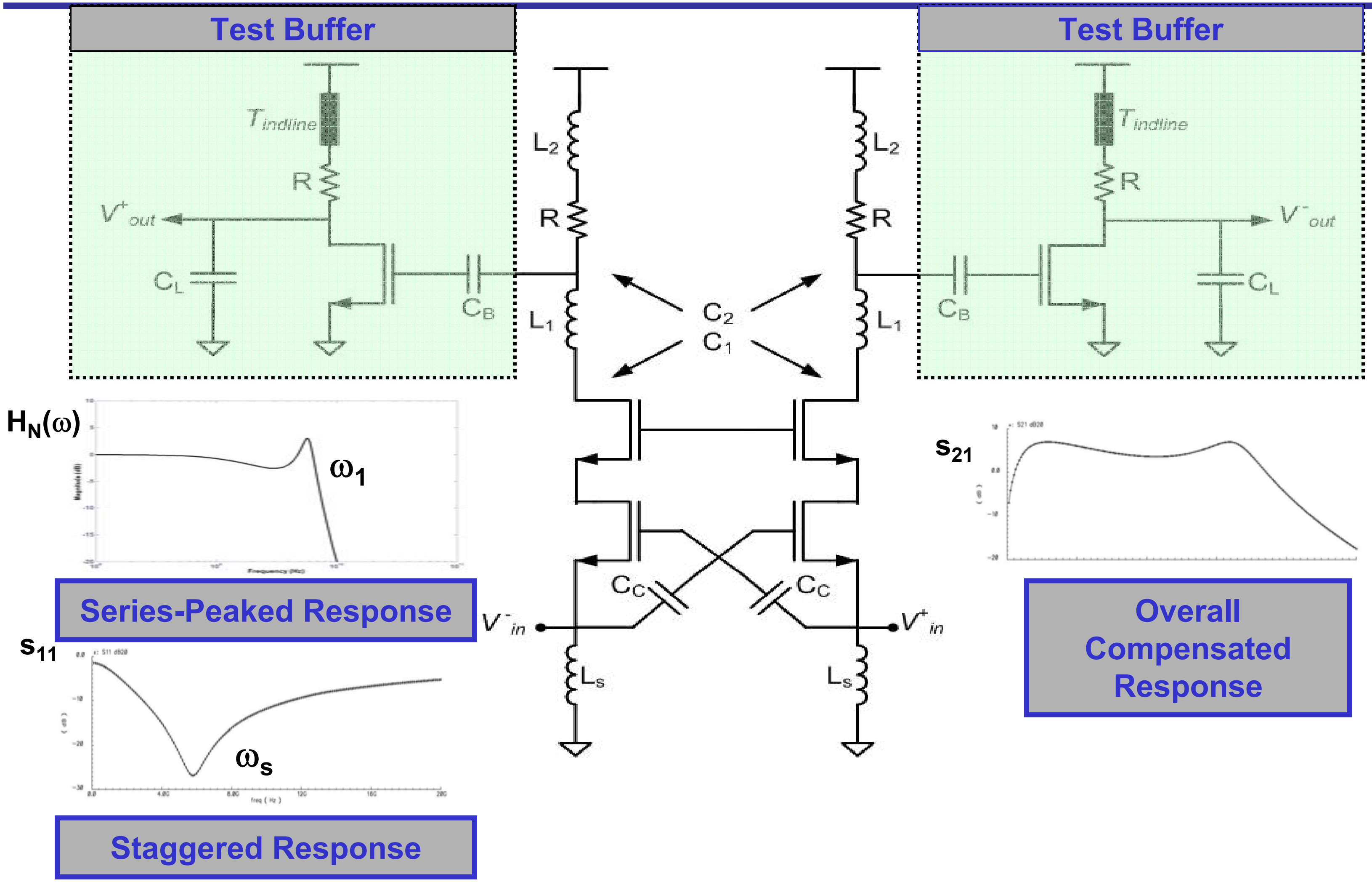
$$A = \frac{1}{1 + C_{gs}/C_c}$$

For $C_c >> C_{gs}$

- $G_m = 2g_m$
- $C_{in} = 4C_{gs}$
- $F \approx 1 + \frac{\gamma}{2\alpha}$

W. Zhuo, X. Li, S. Shekhar, S.H.K. Embabi, J. Pineda de Gyvez, D.J. Allstot and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low noise amplifier," IEEE Trans. on Circuits and Systems I: Express Briefs, vol. 52, 2005.

UWB CCCLNA



Series-Peaked Response

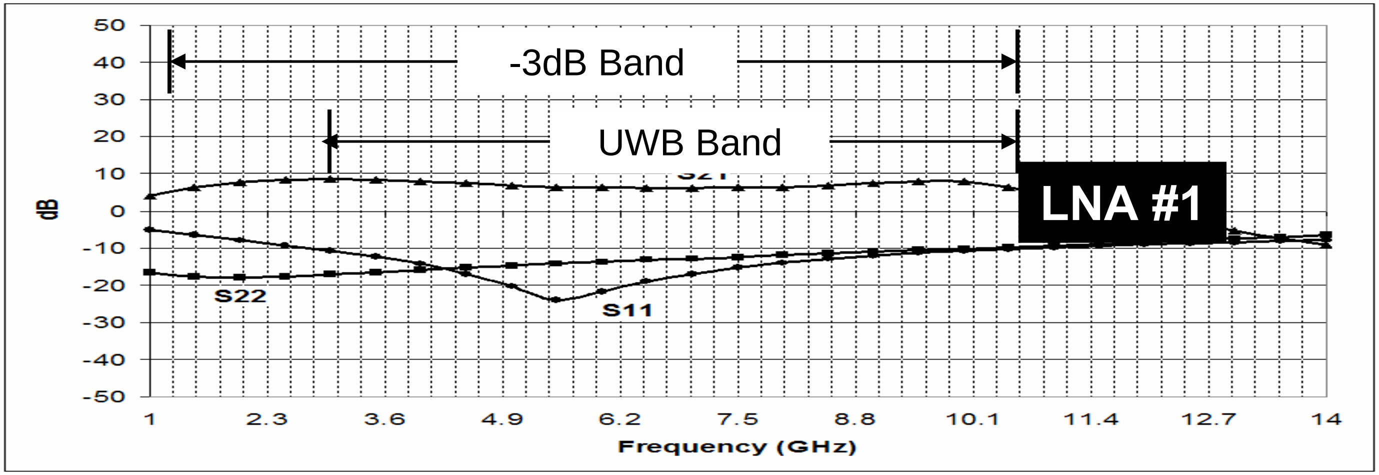
Staggered Response

Overall Compensated Response

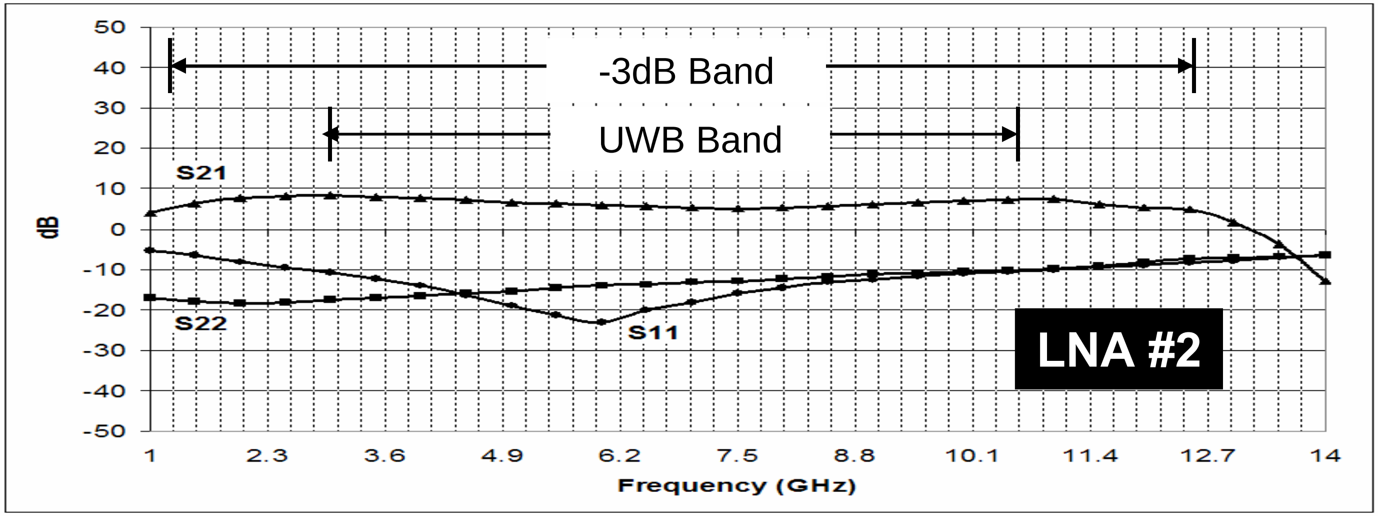
UWB LNA employing anti-stagger-compensated series peaking

Measurement Results

4.1X with 2.4dB Passband Ripple

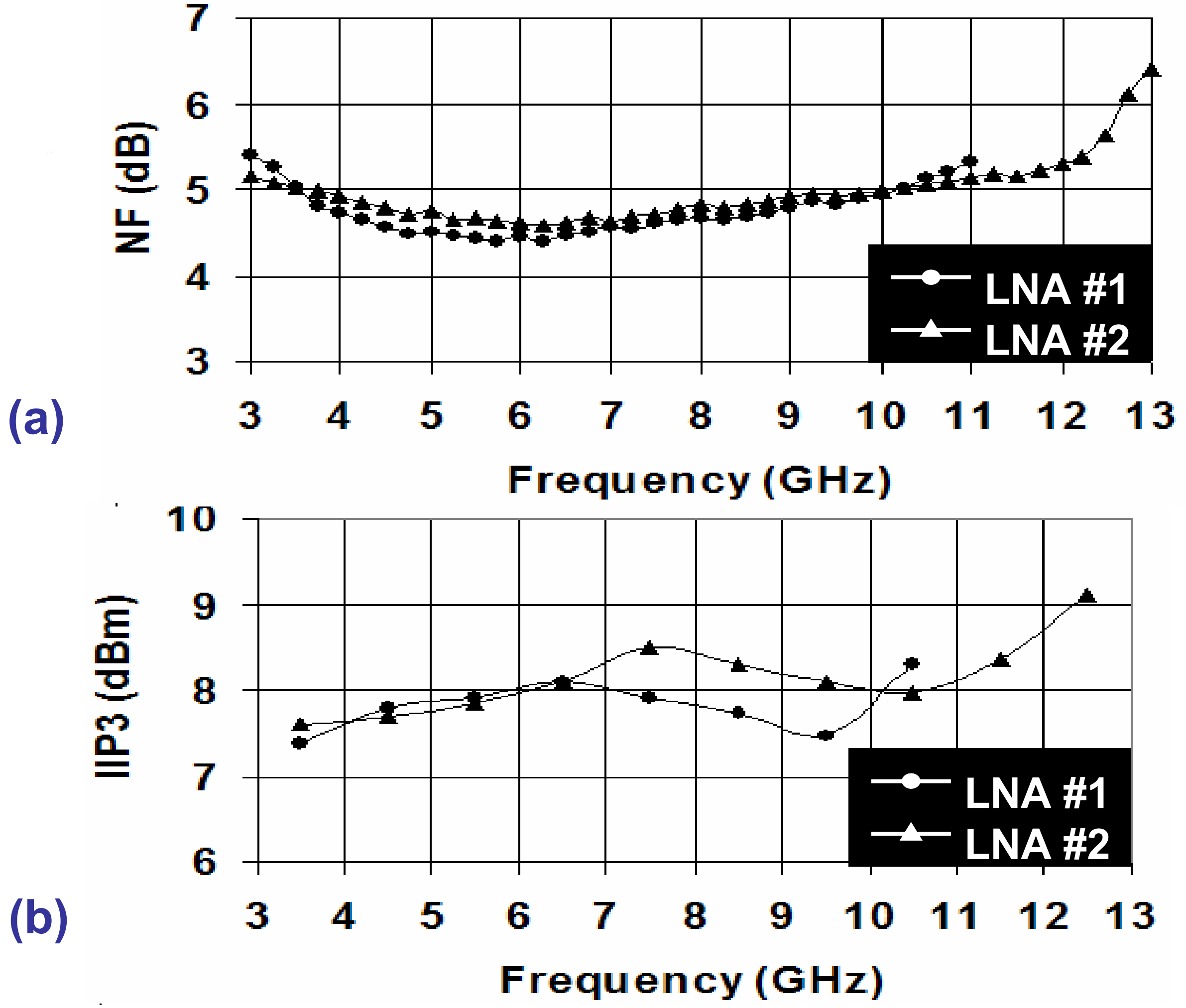


4.9X with 3.0dB Passband Ripple



Measured S-parameters of two versions of the UWB LNA

Measurement Results



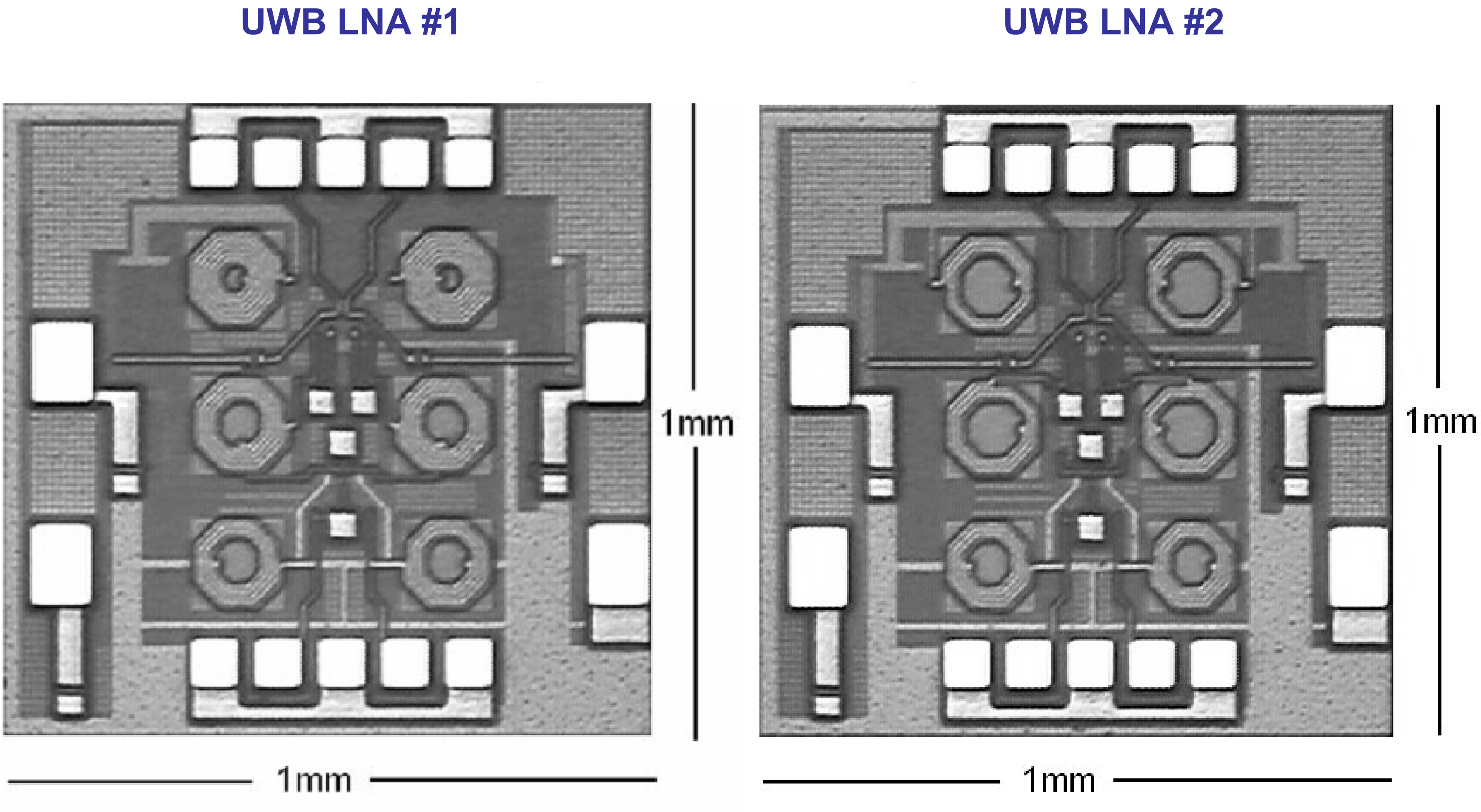
Measured (a) *NF*, and (b) *IIP3* values of two versions of the UWB LNA

Performance Comparison

Ref.	CMOS Tech. (nm)	-3dB BW (GHz)	Power (mW)	*NF* (dB)	Max.S_{21} (dB)	*IIP3* (dBm)	Area (mm^2)	FOM	
								$\frac{Gain_{abs} \cdot BW_{GHz}}{(F-1) \cdot P_{mW}}$	$\frac{Gain_{abs} \cdot IIP3_{mW} \cdot BW_{GHz}}{(F-1) \cdot P_{mW}}$
LNA #1	180	1.3 - 10.7	4.5	4.4 - 5.3	8.5	7.4 to 8.3	1.0	2.33 to 3.17	12.8 to 21.4
								(differential)	
LNA #2	180	1.3 - 12.3	4.5	4.6 - 5.5	8.2	7.6 to 9.1	1.0	2.69 to 3.64	15.5 to 29.6
								(differential)	
[1]	180	2.3 - 9.2	9	4.0 - 9.0	9.3	-8.2 to -5.6	1.1	0.32 to 1.48	0.05 to 0.41
								(single-ended)	
[2]	180	0.5 - 14	52	3.4 - 5.4	10.6	9.4	1.6	0.36 to 0.74	3.11 to 6.45
								(single-ended)	
[2]	180	0.6 - 22	52	4.3 - 6.1	7.3	8.7	1.35	0.31 to 0.56	2.3 to 4.18
								(single-ended)	
Heydari, RFIC05	180^{+}	0 - 12.6	19.8	2.9	9.6	-3.4	0.76	2.02	0.92
								(single-ended)	
Yazdi, Isscc05	180^{+}	0 - 25	54	4.8 - 7	9.1	4.7	1.32	0.33 to 0.65	0.97 to 1.93
								(differential)	

Wideband LNA Measured Performance Comparison

Chip Microphotographs



Chip Microphotographs; 0.18um RF CMOS

S. Shekhar, J.S. Walling and D.J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, Nov. 2006.

Conclusions

- Pros ☺
  - ➢ Large Bandwidth Extension
  - ➢ Low Power
  - ➢ Simple Input Match
  - ➢ Low Inductor Count
  - ➢ Flat Noise Figure
- Cons ☹
  - ➢ Low Gain
  - ➢ Bandwidth Extension Requires Two Stages/Nodes
  - ➢ 3dB Ripple Too Large for Some Applications
  - ➢ Sensitive Tuning