Challenges in Designing CMOS Wireless System-on-a-chip

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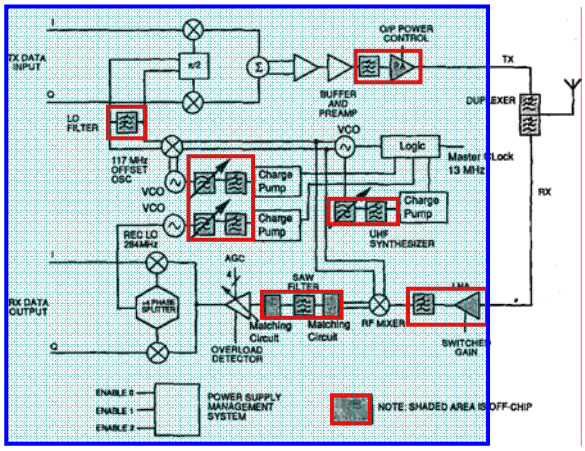
Outline

- Introduction
- Analog/RF:
  - CMOS Transceiver Building Blocks
- Digital:
  - System-on-a-chip Integration
- Conclusion

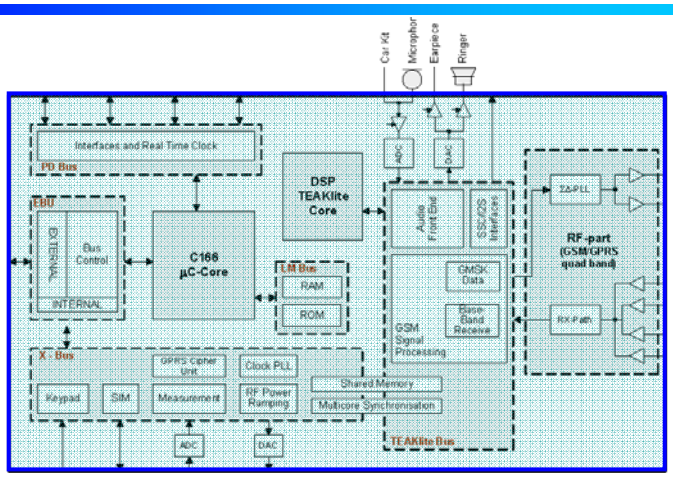
SoC Trends: GSM (1995)



Stetzler et al, ISSCC 95 (AT&T)

Integrated Transceiver with external components (e.g. filters)

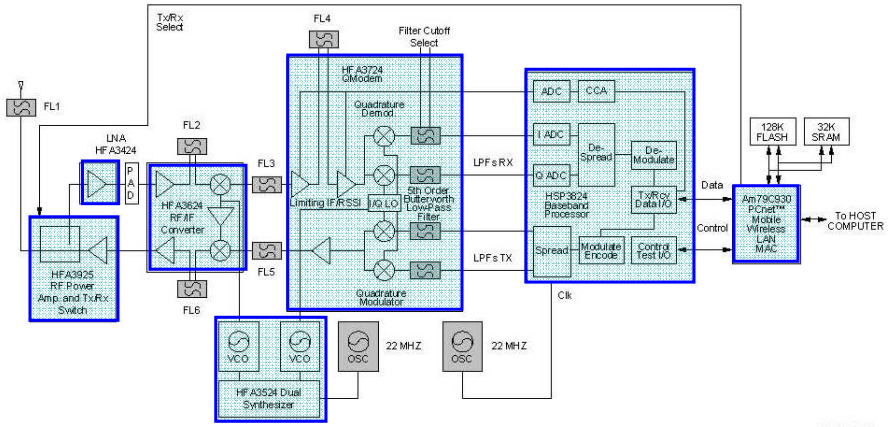
SoC Trends: GSM (2006)



Bonnaud et al, ISSCC 06 (Infineon)

SoC with integrated transceiver and CPU.

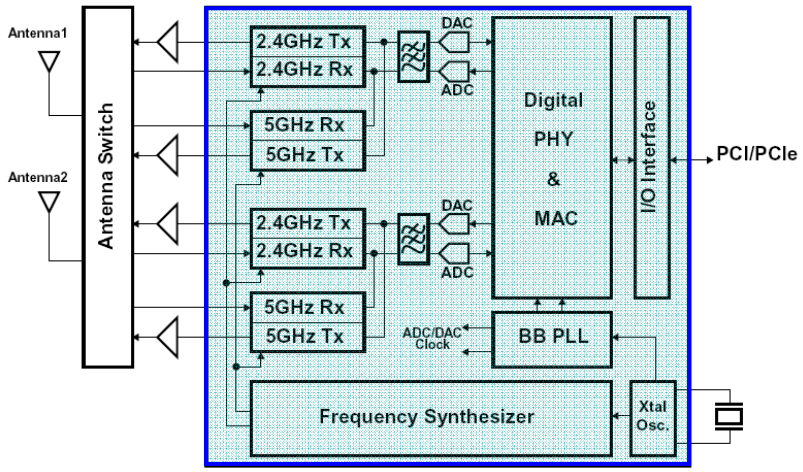
SoC Trends: WLAN (1996)



Multi-Chip 802.11b Transceiver

Prism WLAN chipset (Harris Semi) AMD App Note (www.amd.com)

SoC Trends: WLAN (2008)



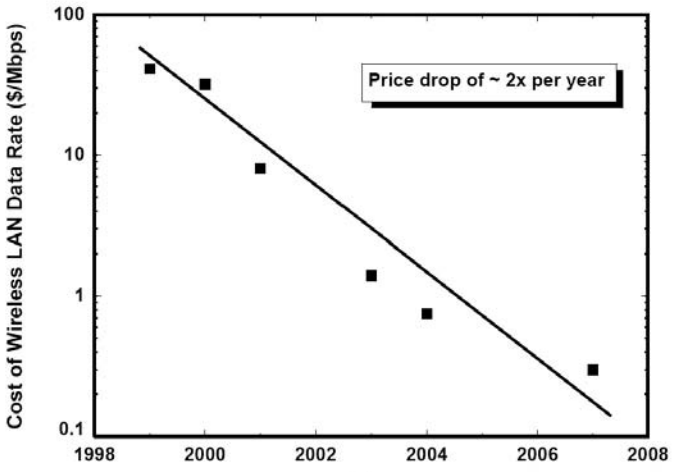
Nathawad et al, ISSCC 08 (Atheros)

11a/b/g/n (2x2 MIMO) Radio SoC

Advantages of SoC Integration

- Increased functionality
- Smaller Size / Form Factor
- Lower Power
  - On-chip interface
- Lower Cost
  - Single package
- Ease of use
  - Minimum RF board tuning
  - Reduced component count
    → Improved reliability

Cost of WLAN Data Throughput



Zargari, 2007 VLSI Symposium Short Course

CMOS RF Design

Advantages

- Low-cost, high-yield
- Multi-layer interconnect makes *decent* inductors
- High-level of integration supports sophisticated digital signal processing

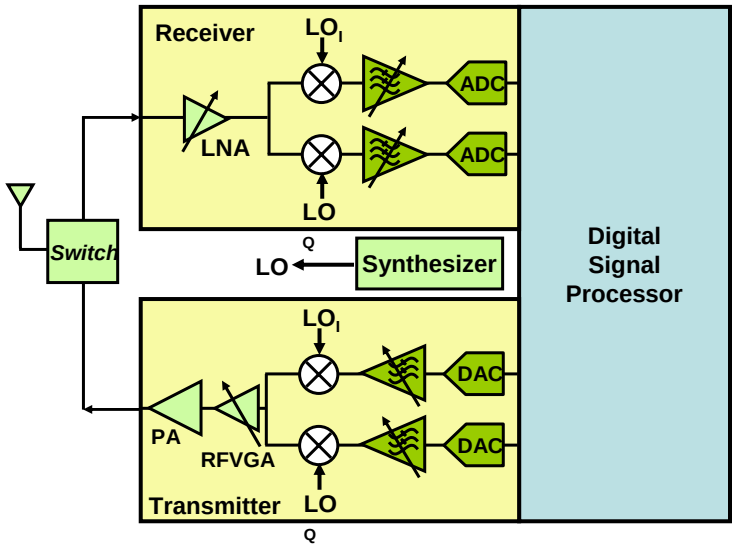
Challenges:

- Multi-GHz: narrowband design with inductors
- No high-Q BPF: architecture + dynamic range
- Process/Temp Variation: DSP algorithms
- Reduced supply headroom: IO devices
- Noise coupling: careful design & layout

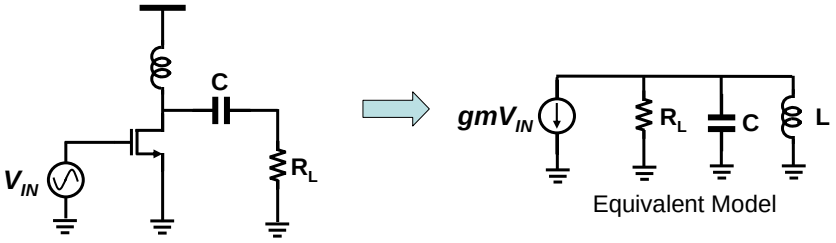
CMOS Transceiver Building Blocks

- ❑ Signal Amplification
- ❑ Frequency Translation
- ❑ Frequency Selectivity

Transceiver Block Diagram



Tuned CMOS RF Gain stage



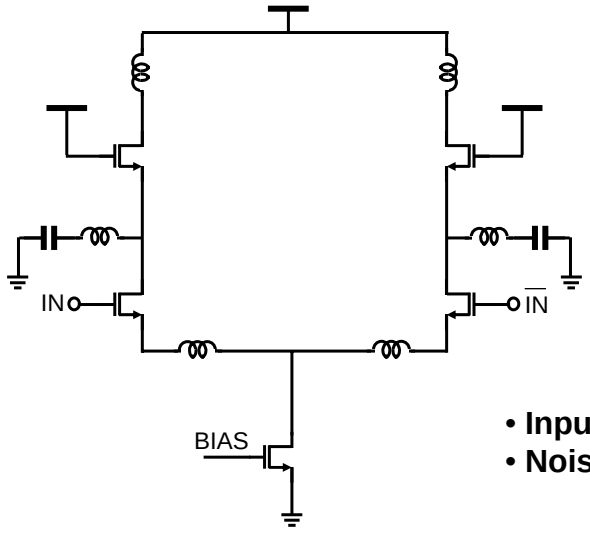
$$gm \quad R_X \approx \left[\frac{2I_D}{V_{GS}-V_T}\right]\frac{Q}{\omega_o C} = \left[\frac{2I_D}{V_{GS}-V_T}\right]Q\omega_o L$$

Low power design:
- **high Q**
- **smaller feature size technology: gm, V_{DD}**

LNA Design Goal

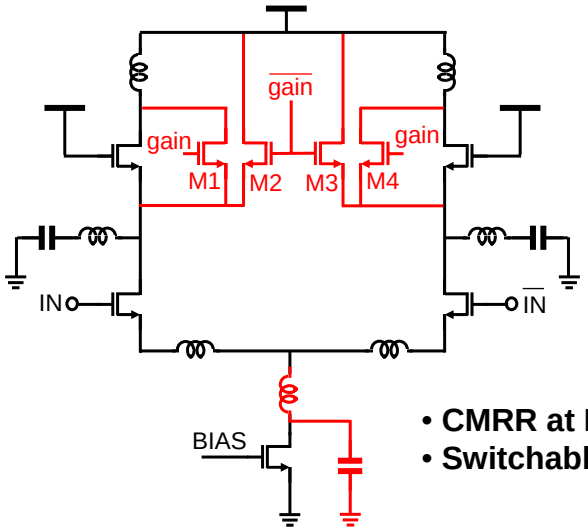
- Low Noise Figure
  - Sufficient gain
- Able to accommodate large blockers
  - Large Dynamic Range
  - Large Common-mode Rejection
  - High Linearity

LNA with Cascoded Diff Pair



- Input match
- Noise Figure

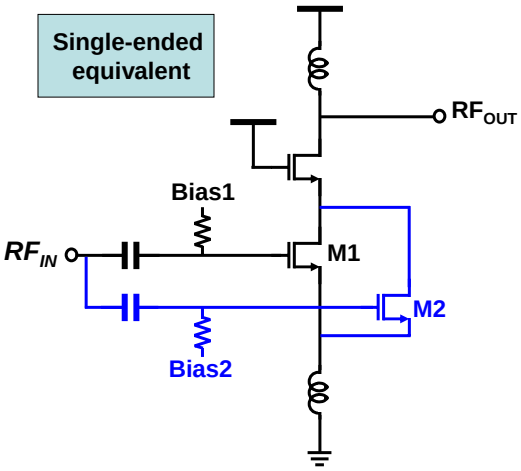
LNA with Switchable Gain



- CMRR at RF
- Switchable gain for high DR

Zargari et al, JSSC Dec 2004 (Atheros)

LNA with GM Linearization



Nonlinearity Compensation with two parallel transistors

Kim et al, JSSC Jan 2004 (KAIST)

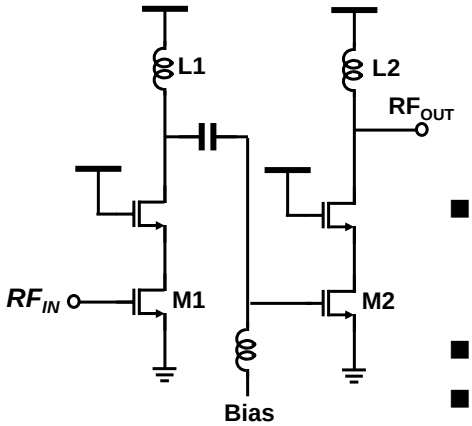
CMOS Power Amplifiers

- Output power (and efficiency) depends on V_{DD}

$$P_{out} \leq \frac{V_{DD}^{2}}{2R_L}$$

- Lower supply voltage reduces output power
  - → Cascoding (to support a higher V_{DD})
  - → Parallel Combining (of lower power PAs)

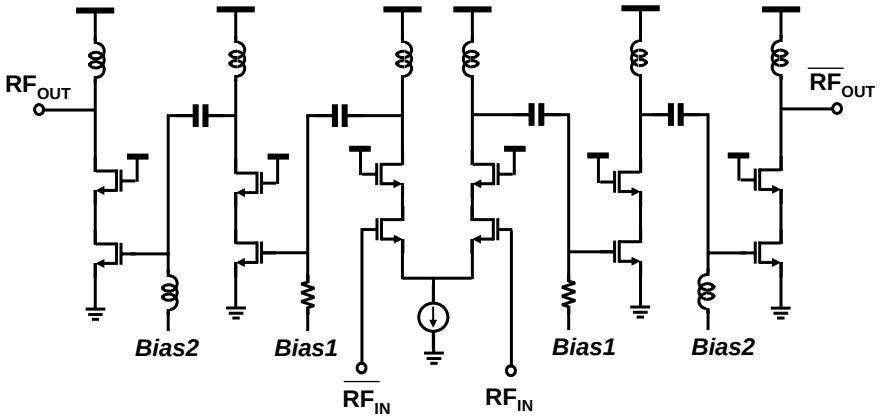
Cascoded Power Amplifier



Single-ended equivalent

- Cascoding advantages
  - 3.3V supply voltage
  - Stability
- Capacitive Level-shift
- Differential
  - Off-chip balun

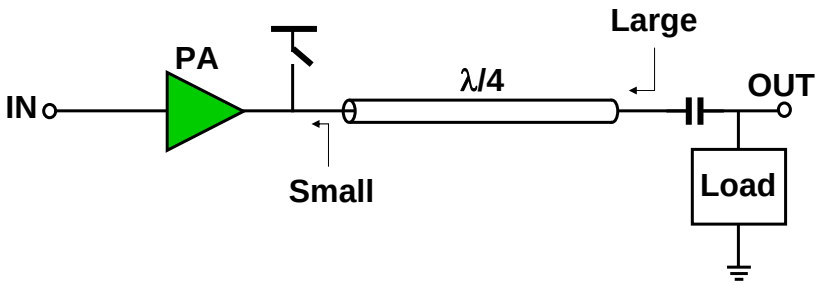
Cascoded Power Amplifiers



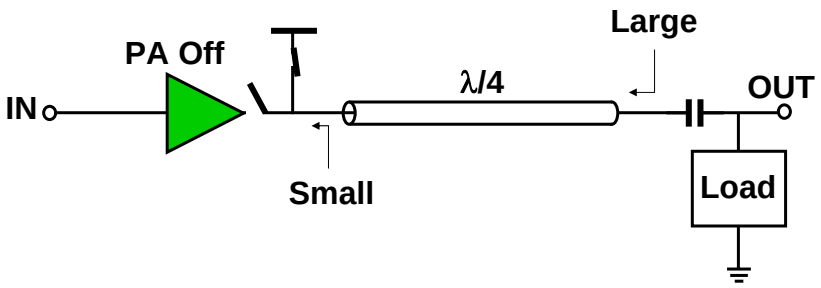
P_{MAX} = 22 dBm P_{OFDM} = 17.8 dBm (BPSK)

Zargari et al, JSSC Dec 2002 (Atheros)

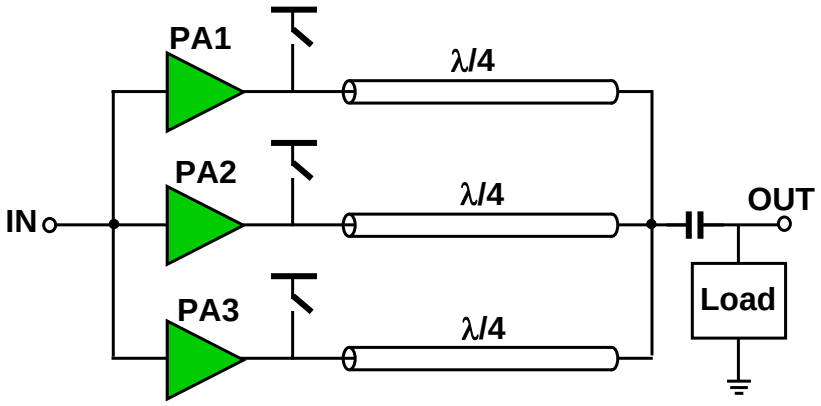
Power Amplifiers with Parallel Amplification



Power Amplifiers with Parallel Amplification

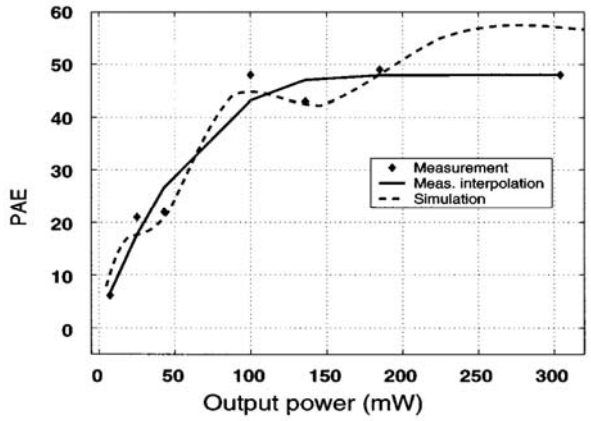


Power Amplifiers with Parallel Amplification



Shirvani et al, JSSC June 2002 (Stanford)

Power Amplifiers with Parallel Amplification



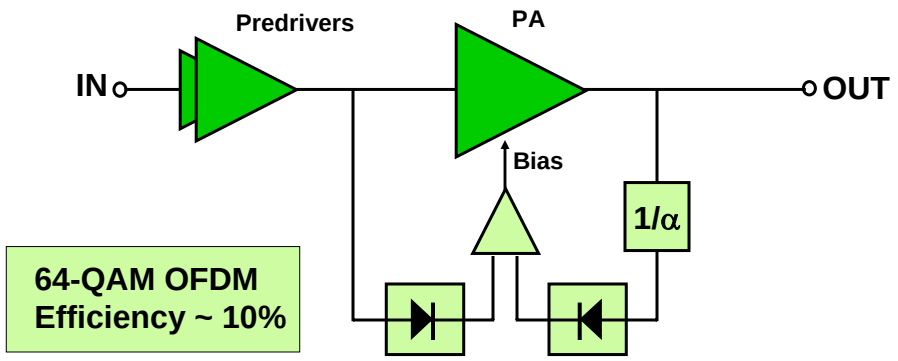
Shirvani et al, JSSC June 2002 (Stanford)

PA Peak to Average Ratio

- **Improved spectral efficiency (higher bits per Hz)**
  - **→ Large peak to average ratio**
  - **→ reduces power efficiency of the PA**
- **Example: 802.11a/g OFDM has PAR of 17dB**
  - **Class A efficiency of ~ 1%**
  - **Infrequent signal peaks**
    - **16-QAM OFDM, PAR of 6dB degrades SNR by only 0.25dB***
      - **→ Class A Efficiency ~ 12%**
    - **64-QAM OFDM, PAR of 12dB is needed**
      - **→ Class A Efficiency ~ 3%**

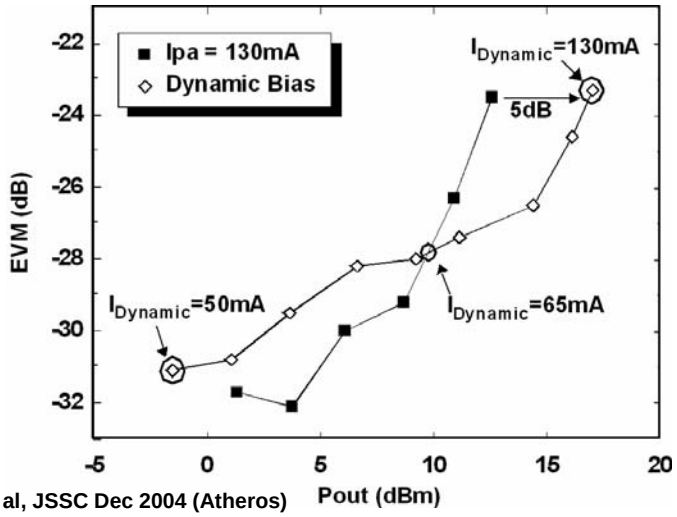
* Van Nee & Prasad, OFDM for Wireless Multimedia Communications, Artech House, 2000

Power Amplifiers with Dynamic Bias



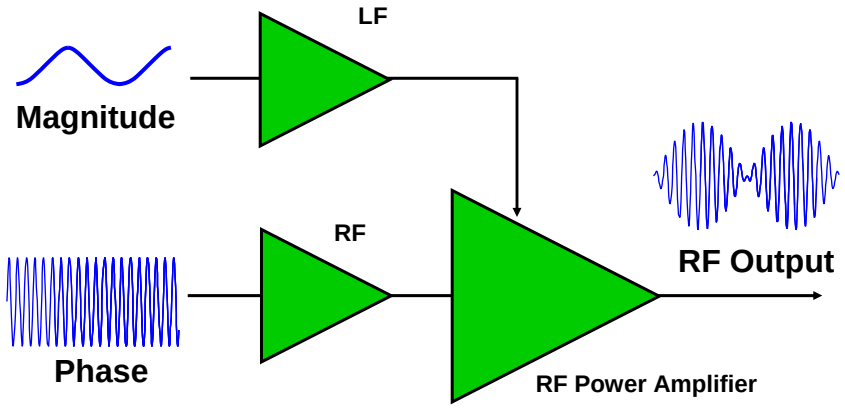
Zargari et al, JSSC Dec 2004 (Atheros)

Power Amplifiers with Dynamic Bias

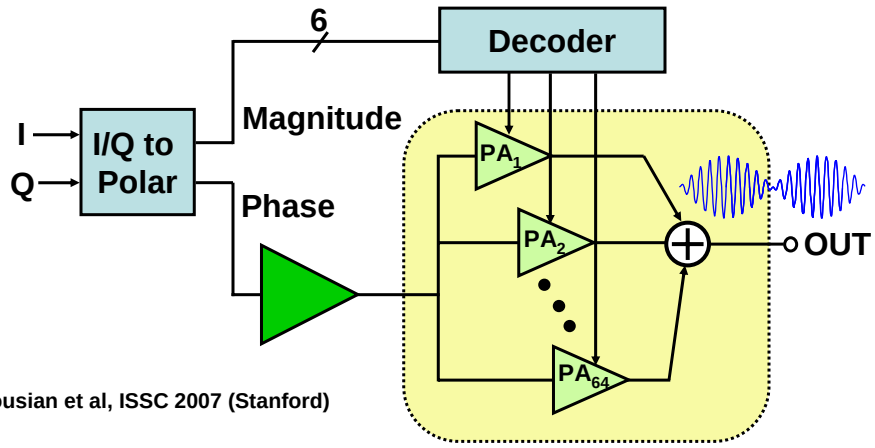


Zargari et al, JSSC Dec 2004 (Atheros)

Polar Modulated Power Amplifier

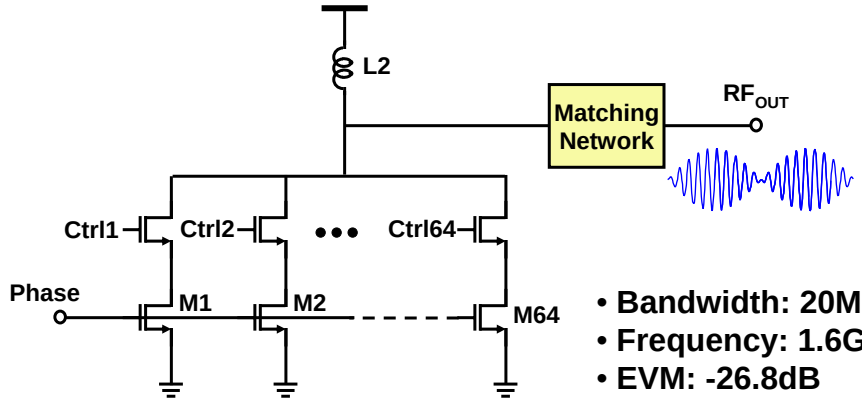


Digitally Modulated Polar Power Amplifier



Kavousian et al, ISSC 2007 (Stanford)

Digitally Modulated Polar Class-A Power Amplifier



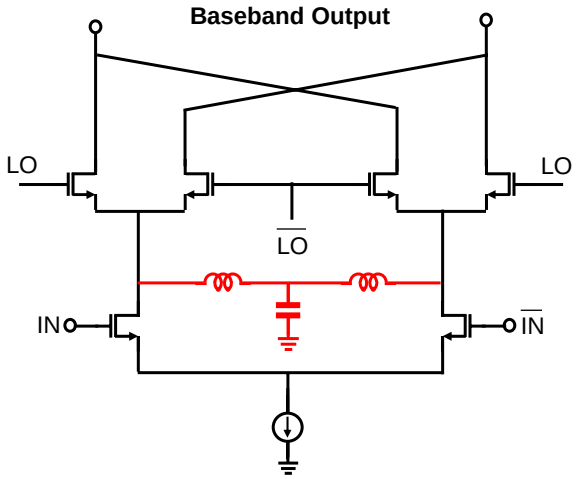
- Bandwidth: 20MHz
- Frequency: 1.6GHz
- EVM: -26.8dB
- Power: 13.6dBm

Kavousian et al, ISSC 2007 (Stanford)

Frequency Translation

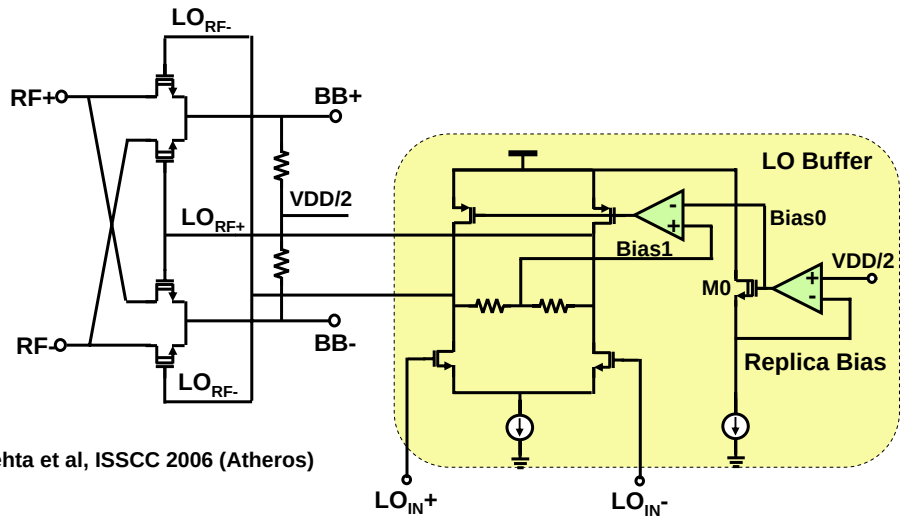
- RF ←→ Baseband
- Architecture:
  - Superhetrodyne
  - Sliding IF, low IF, Direct Conversion
- Components:
  - Mixers:
    - Active or Passive (lower power)
  - Local Oscillator:
    - Frequency Synthesizer

Active CMOS mixer



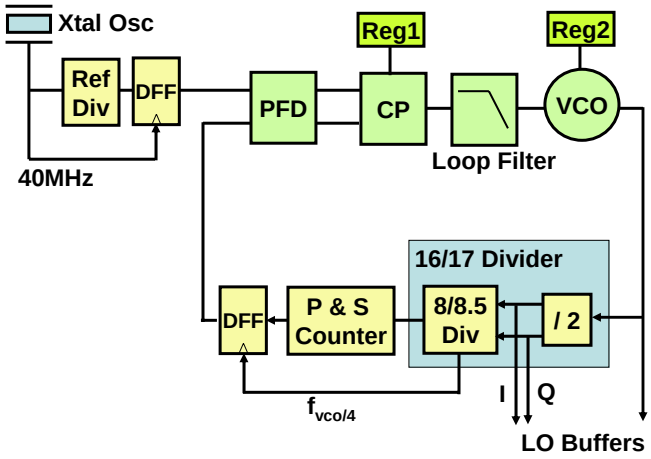
Brandolini et al, ISSCC 2005 (Univ of Pavia)

Passive CMOS Mixer



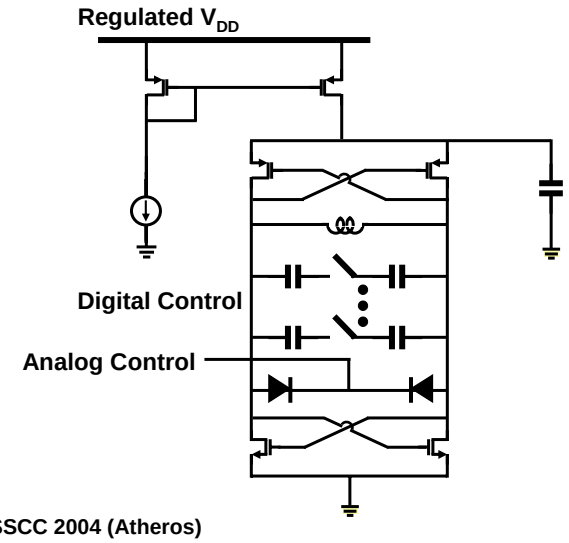
Mehta et al, ISSCC 2006 (Atheros)

Frequency Synthesizer



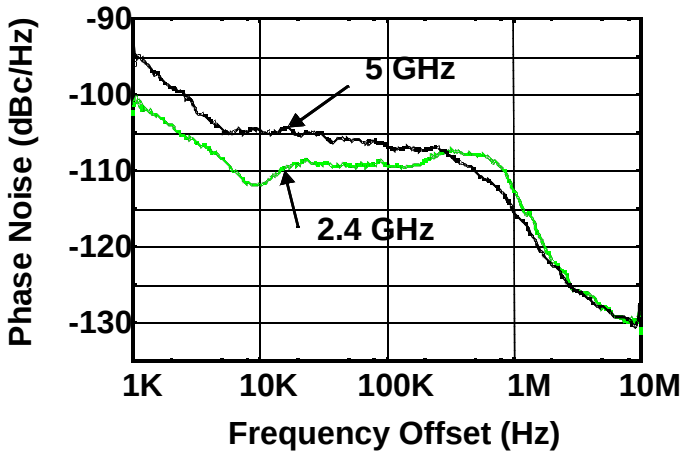
Terrovitis et al, ISSCC 2004 (Atheros)

Voltage Controlled Oscillator



Terrovitis et al, ISSCC 2004 (Atheros)

Measured Phase Noise

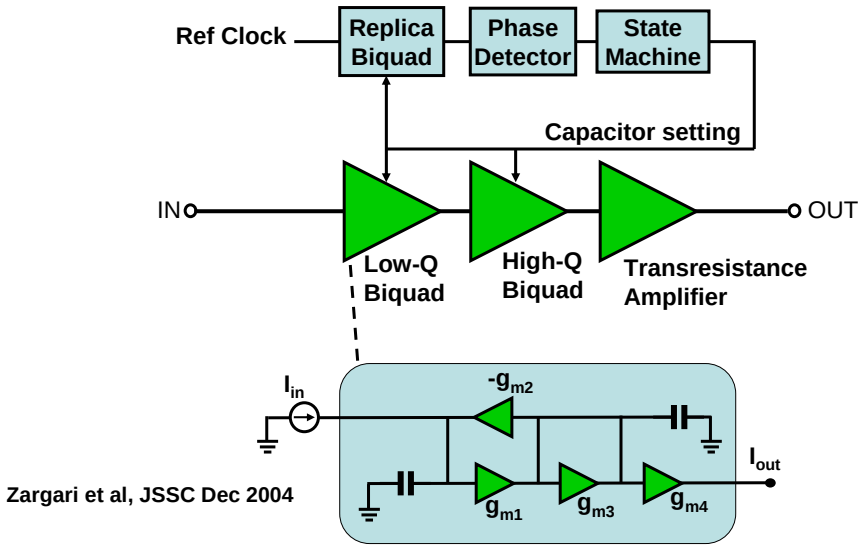


Terrovitis et al, ISSCC 2004 (Atheros)

Frequency Selectivity

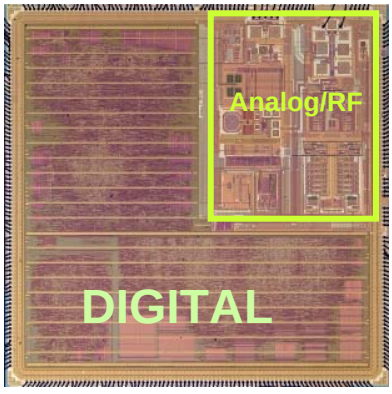
- Superhetrodyne conversion
  - IF filtering:
    - external SAW filter expensive
    - On-chip RF/IF high-Q filtering difficult
- Direct conversion
  - Baseband filtering:
    - Modest filtering to avoid anti-aliasing
    - Blocker filtering in digital domain

Anti-alias Low-pass gm-C Filter



Zargari et al, JSSC Dec 2004

System-on-a-Chip Integration



- Digital Power Consumption
- Digital Calibration techniques
- Noise Coupling

Digital Power Consumption

- Digital circuits (PHY, MAC, CPU, IO, memory) occupies most of the area of a wireless SoC:

- Reducing active digital power
  - Lower supply voltage
  - Lower interconnect capacitance
  - Small geometry CMOS
  - Clock gating of inactive digital logic

Digital Leakage Power

- Transistor leakage current has increased dramatically with technology scaling
- Leakage current reduction
  - Customized low-power (LP) process
  - Circuit techniques:
    - Transistor stacking
    - Multiple threshold voltages
    - Dynamically adjusted threshold (backgate bias)
    - Multiple supply voltages
    - Dynamically adjusted supply voltages

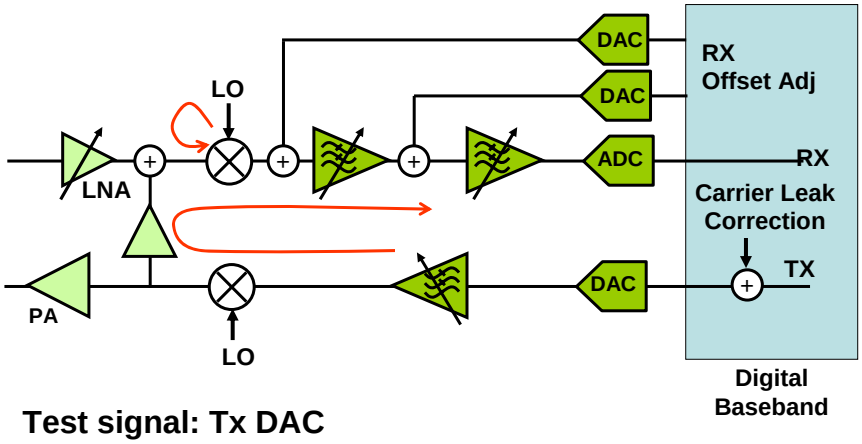
Digital Calibration Issues

- Digital logic to compensate/correct for imperfections of analog and RF circuits can enable:
  - Lower power, smaller area, improved reliability of analog/RF
- Desired properties of calibration:
  - Independent of temperature, aging, frequency
  - Inexpensive (in area and power) to implement
  - Do not interfere with system performance
- Wireless SoC advantage:
  - Calibration building blocks already exist on-chip: transmitter and receiver, data converters, and CPU
  - No package pin limitation

Calibration Techniques

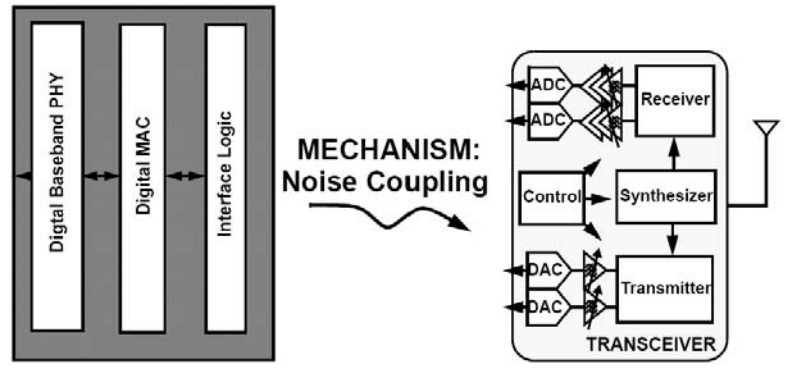
- Test Signal
  - Rx Gain: Thermal noise
  - Rx I/Q mismatch: Live Rx traffic
  - Tx carrier leak: Dedicated test signals from DAC
  - Receive filter bandwidth: RF loop back
- Observation Signal
  - ADC outputs
  - Comparator outputs
- Tuning Mechanism
  - Dedicated DAC
  - Selectable capacitors, resistors, transistors

Example: Tx Carrier Leak



- Test signal: Tx DAC
- Observation signal: RF loop back to Rx ADC
- Tuning: Carrier Leak Correction at Tx DAC input

Noise Coupling



SOURCE:
Noisy Digital Circuits

DESTINATION:
Sensitive Analog Circuits

Digital Noise Source

- Reduce noise by turning off unused digital logic
- Clock gating
- Avoid oversized digital buffers
- Stagger digital switching
  - Avoid large number of digital pads switching simultaneously
  - Avoid switching digital logic at the same sampling instance of sensitive analog

Noise Coupling Mechanism

- Supply noise coupling
  - Separate or star-connected power supplies
- Capacitive coupling to sensitive signals and bias voltages
  - Careful routing of signal traces to reduce parasitic capacitance
  - Use ground return-path shields
- Substrate coupling induced V_{TH} modulation
  - Low-impedance substrate connection
  - Guard rings
  - Physical separation
  - Deep Nwell

Noise Destination

- Increase immunity of sensitive analog and RF circuits
  - Fully differential topology
- Dedicated on-chip voltage regulators
- Avoid package coupling by keeping sensitive nodes on chip (Example: VCO control voltage)

Conclusions

- CMOS has become the technology of choice for integrated radio systems
- Integrating a radio in mixed-Signal System-on-a-Chip is no longer a dream but a reality
- Wireless SoC can provide significant advantages in size, power, and cost

Continuing Challenges

- Wireless SoCs with integrated radios will be as ubiquitous as today's mixed-signal SoCs with integrated ADC
- Multi-mode radios to support several wireless standards
- Challenge of radio designers will still be:
  - Power consumption / Battery life
  - Range
  - Data rate
  - Cost

Acknowledgments

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