Scaling of RF CMOS

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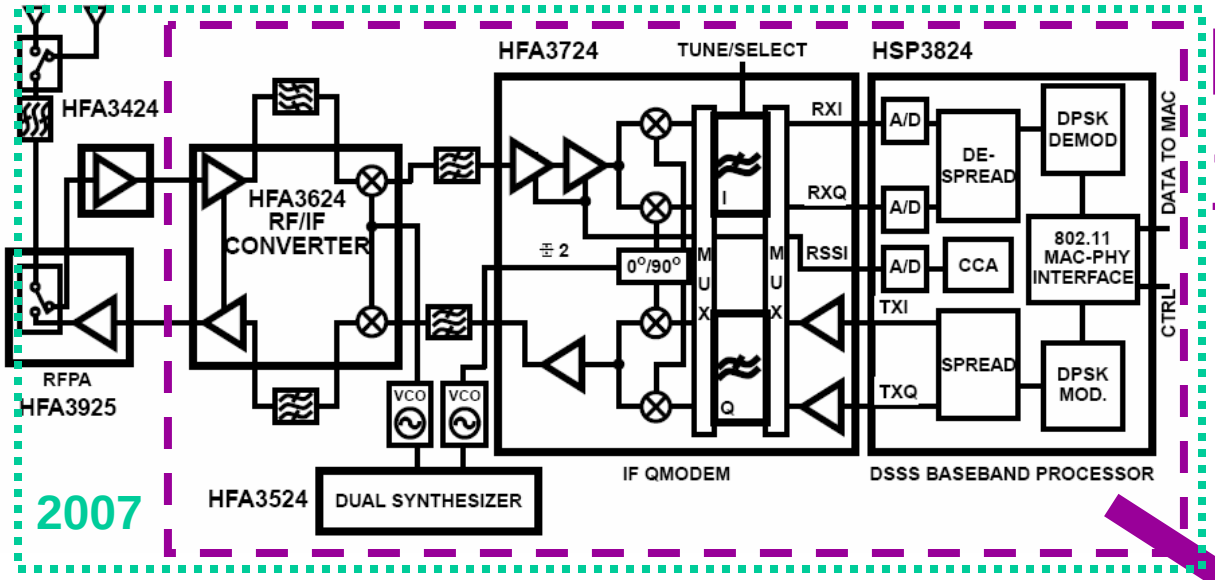
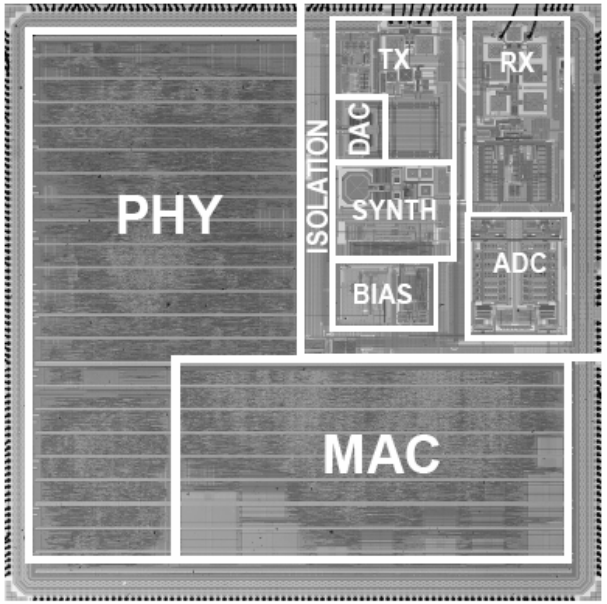
802.11 Evolution



Prism Chip Set
1998

Single Chip
180nm CMOS



Source : R. Chang, et al, "A Fully Integrated RF Front-End with Independent RX/TX Matching and +20dbm Output Power for WLAN Applications," *ISSCC*, p. 564, 2007.

Source : Mehta, et al., “An 802.11g WLAN SOC ," *ISSCC*, p. 94, 2005.

CMOS Scaling

- For Digital Applications

  Motivations – Faster; Lower cost/Hz-bit-function

- For RF Applications

  Spectra (1-6GHz) do not change; Are faster devices needed ?

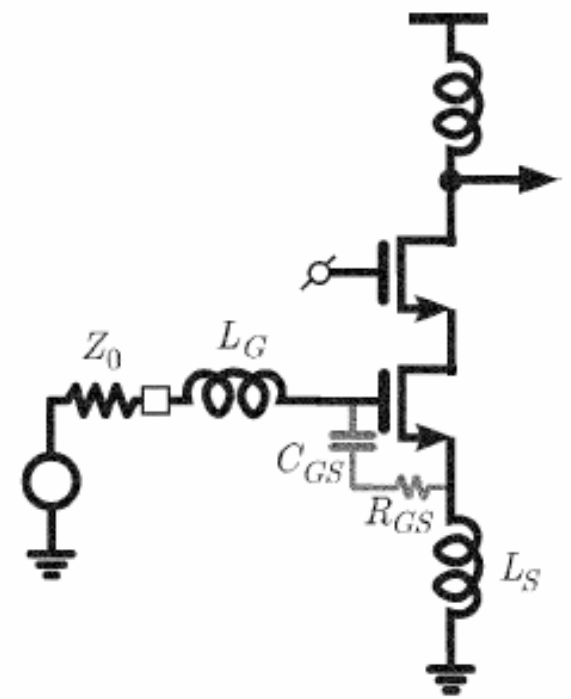
  Motivations – Smaller; Lower cost/function; Lower Power

Outline

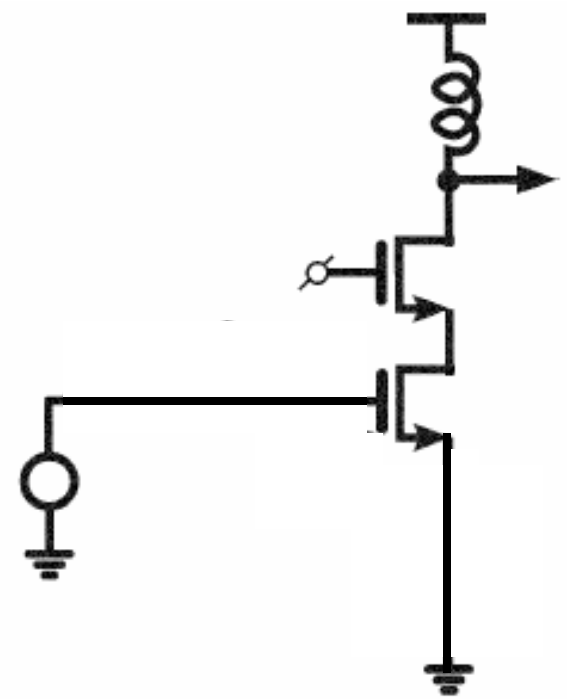
- Transistor Scaling
- Passive Components
- Future Integration Trends
- Conclusions

Sample RF Circuits

Low Noise Amplifier



Power Amplifier



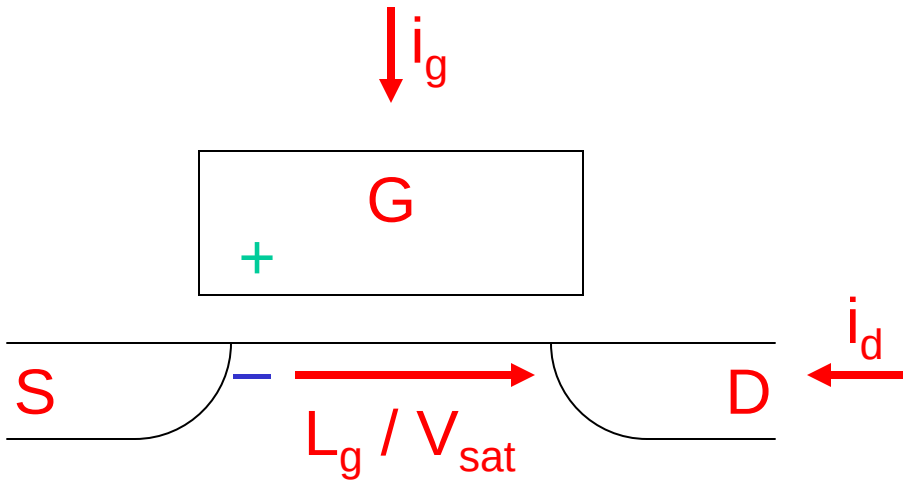
Extensive usage of inductor to tune out capacitance

MOSFET Frequency Response

$$f_t = \frac{1}{2\pi} \frac{g_m}{c_{gg} + c_{gso} + c_{gdo} + c_{par}} \rightarrow \frac{1}{2\pi} \frac{v_{sat}}{L_g}$$

$$f_{max} \approx \frac{f_t}{2\sqrt{(R_g + R_i)(g_{ds} + 2\pi f_t c_{gdo})}}$$

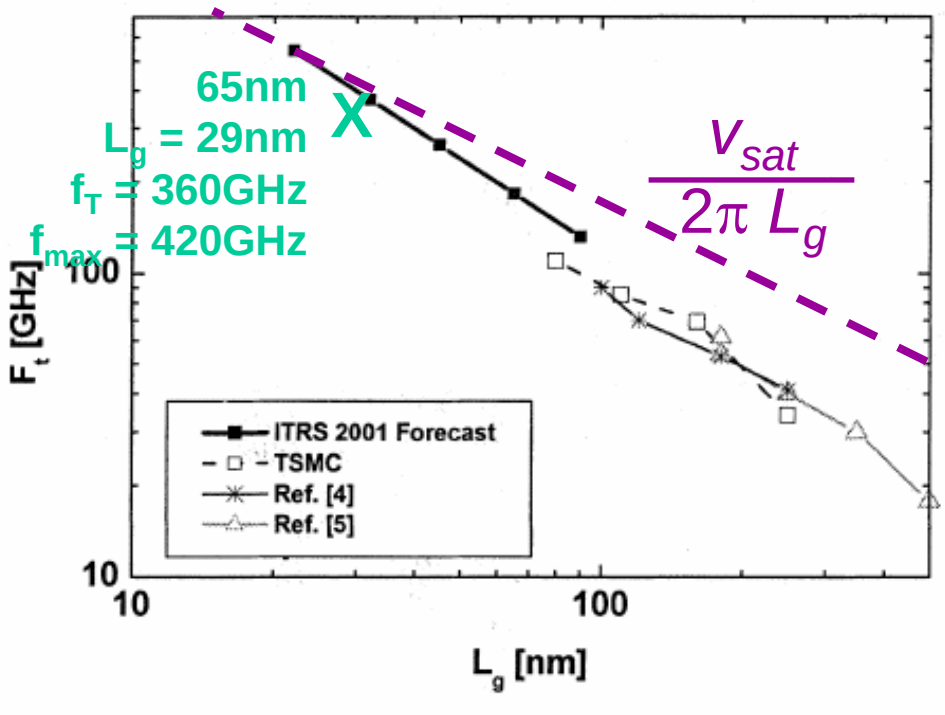
g_m = transconductance
C_{gg} = gate-channel capacitance
C_{gdo} = gate-drain overlap capacitance
C_{gso} = gate-source overlap capacitance
C_{par} = gate parasitic capacitance
V_{sat} = carrier saturation velocity
L_g = effective gate length
R_g = gate resistance
R_i = equivalent input resistance for non-quasi static effect
g_{ds} = output conductance

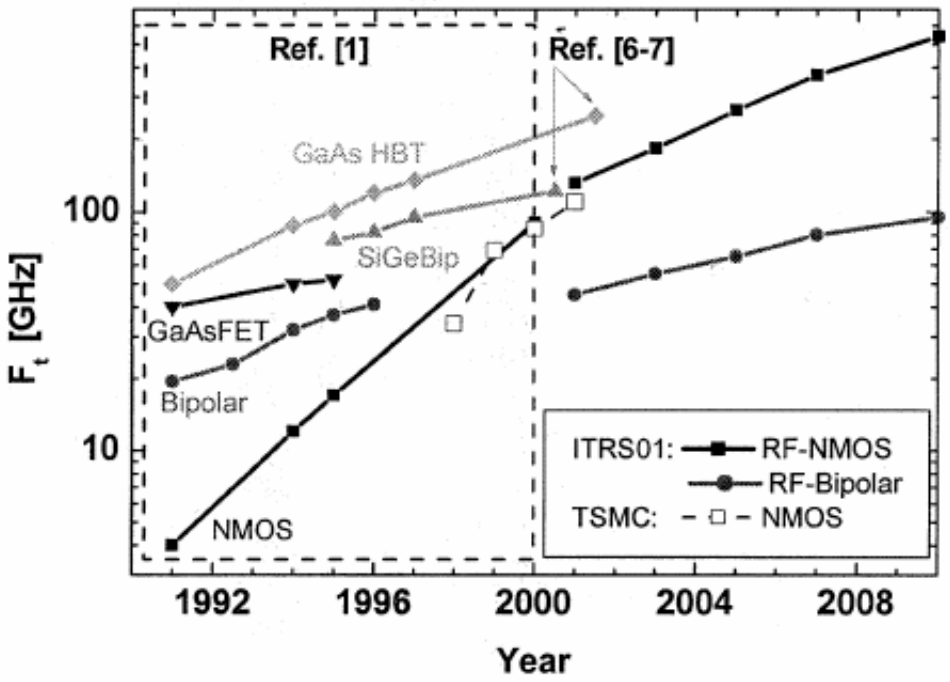


Theoretical Limit

L_g = 30 nm, f_t = 500 GHz

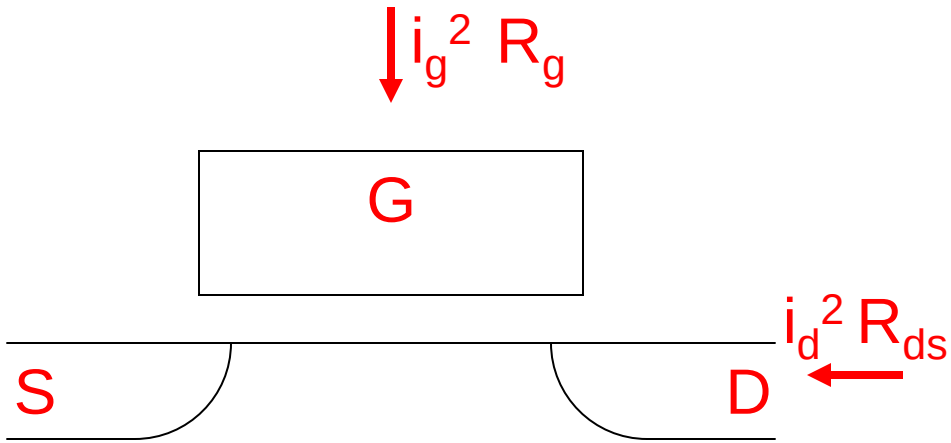
MOSFET f_T



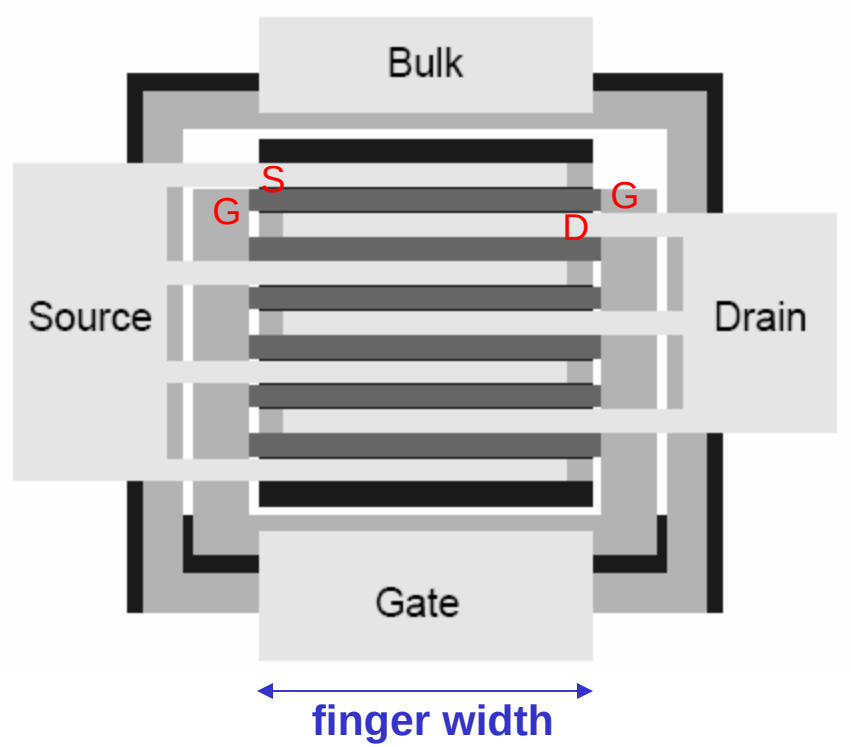


f_T >> typical RF spectra

Source : Diaz, et al., "CMOS Technology for MS/RF SoC," *IEEE TED*, 50, p. 557, 2003.


$i_g^2 R_g$
G
$i_d^2 R_{ds}$
S
D

Effect of Layout on f_T and f_{max}



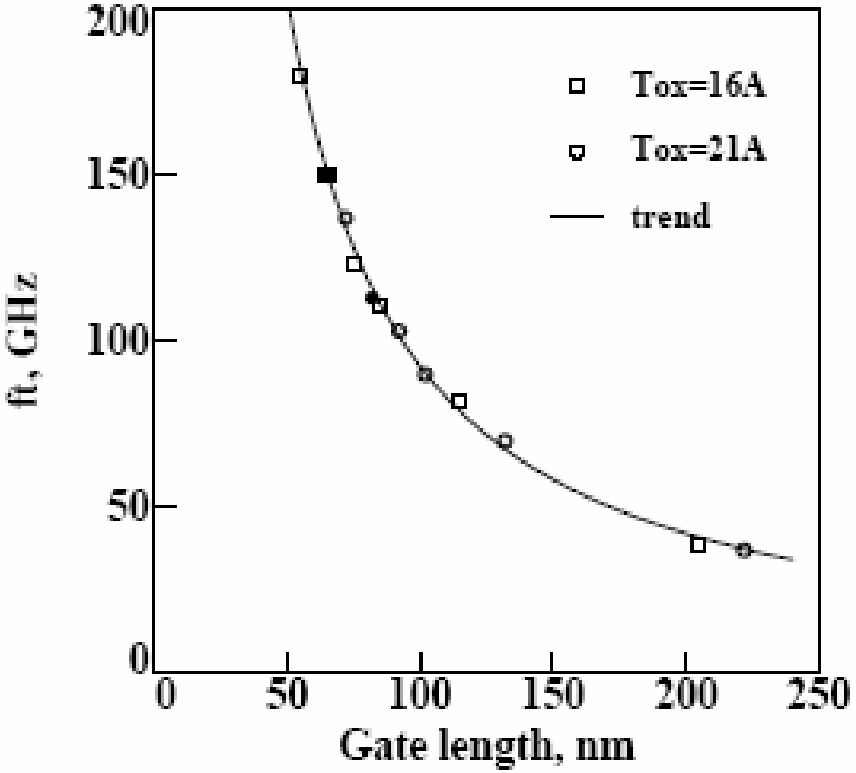
Parallel Rg improves f_{max}

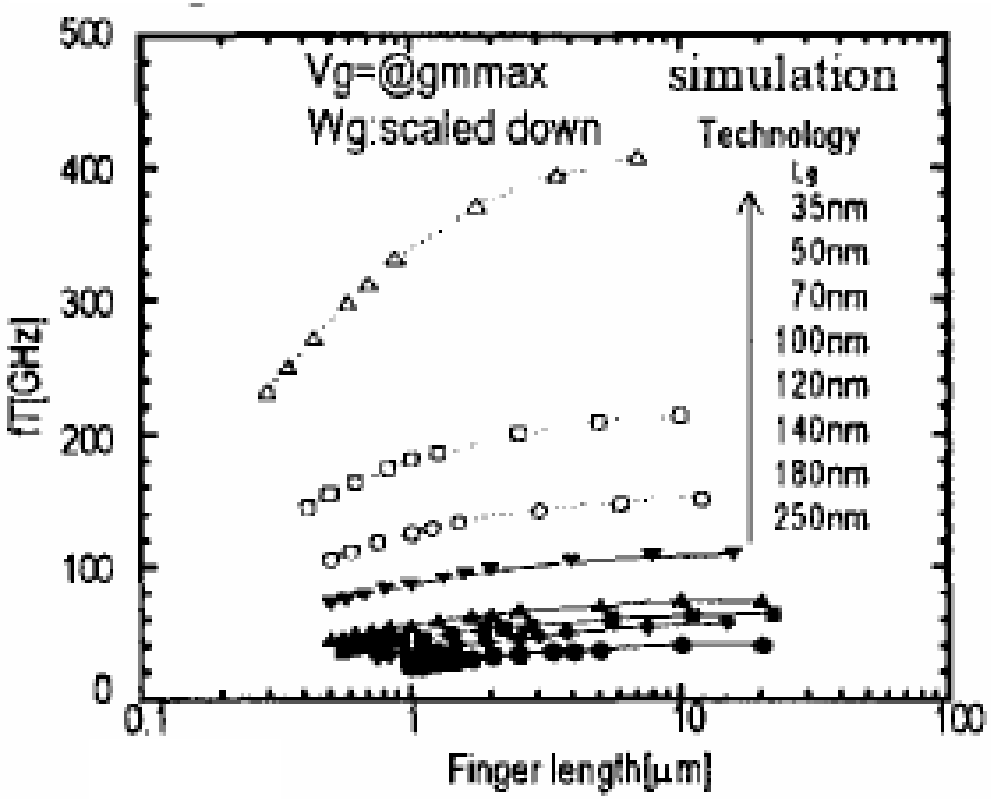
Gate connected at both ends

Source drain metals do not overlap

Bulk contacts surround device

Optimum Finger Width





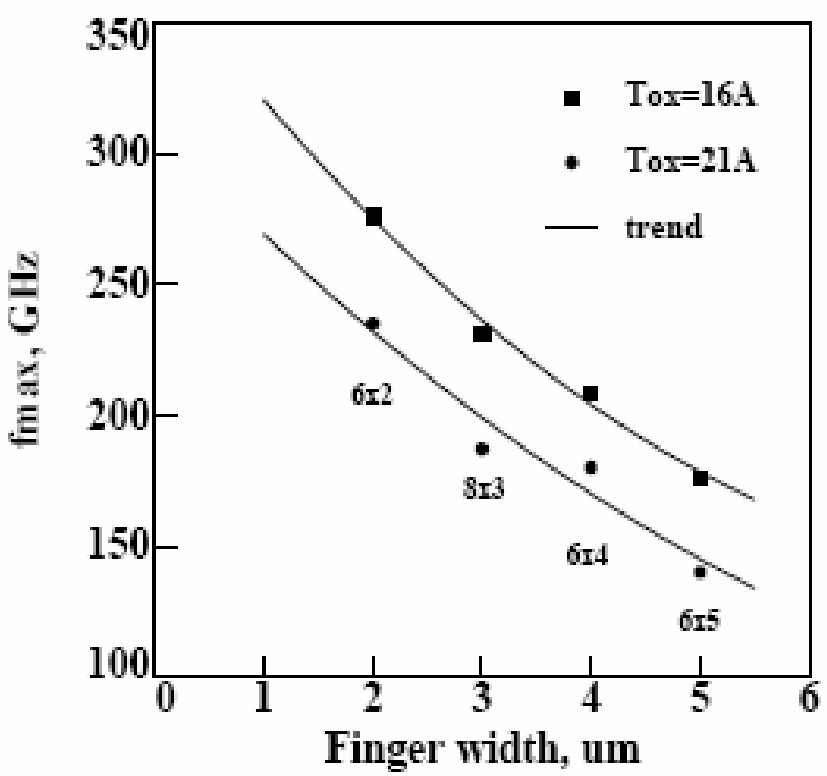
f_T scales with 1/L, independent of T_{ox}.

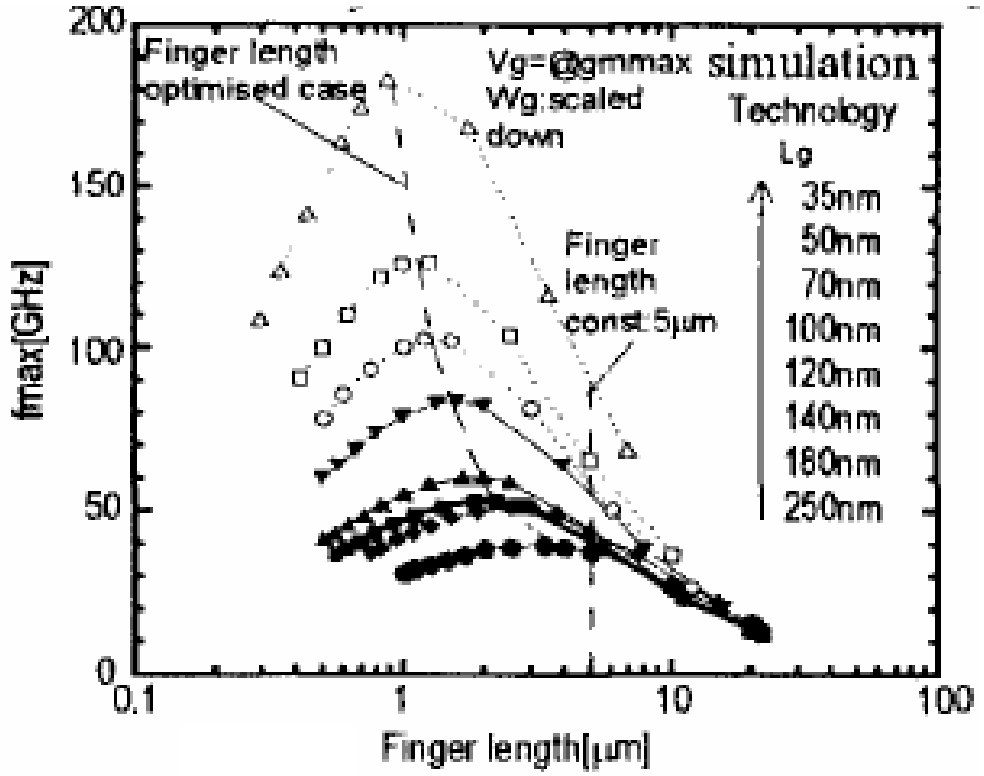
f_T depends weakly on finger width.

E. Morifuji, et al., “Future Perspective and Scaling Down Roadmap for RF CMOS," *Symposium on VLSI Technology Digest of Technical Paper*, pp. 163-164, 1999.

L. Tiemeijer, et al., "Record RF Performance of Standard 90 nm CMOS Technology," *IEEE International Electron Device Meeting*, pp. 441-444, 2004.

Optimum Finger Width





f_{max} depends on finger width.

E. Morifuji, et al., “Future Perspective and Scaling Down Roadmap for RF CMOS," *Symposium on VLSI Technology Digest of Technical Paper*, pp. 163-164, 1999.

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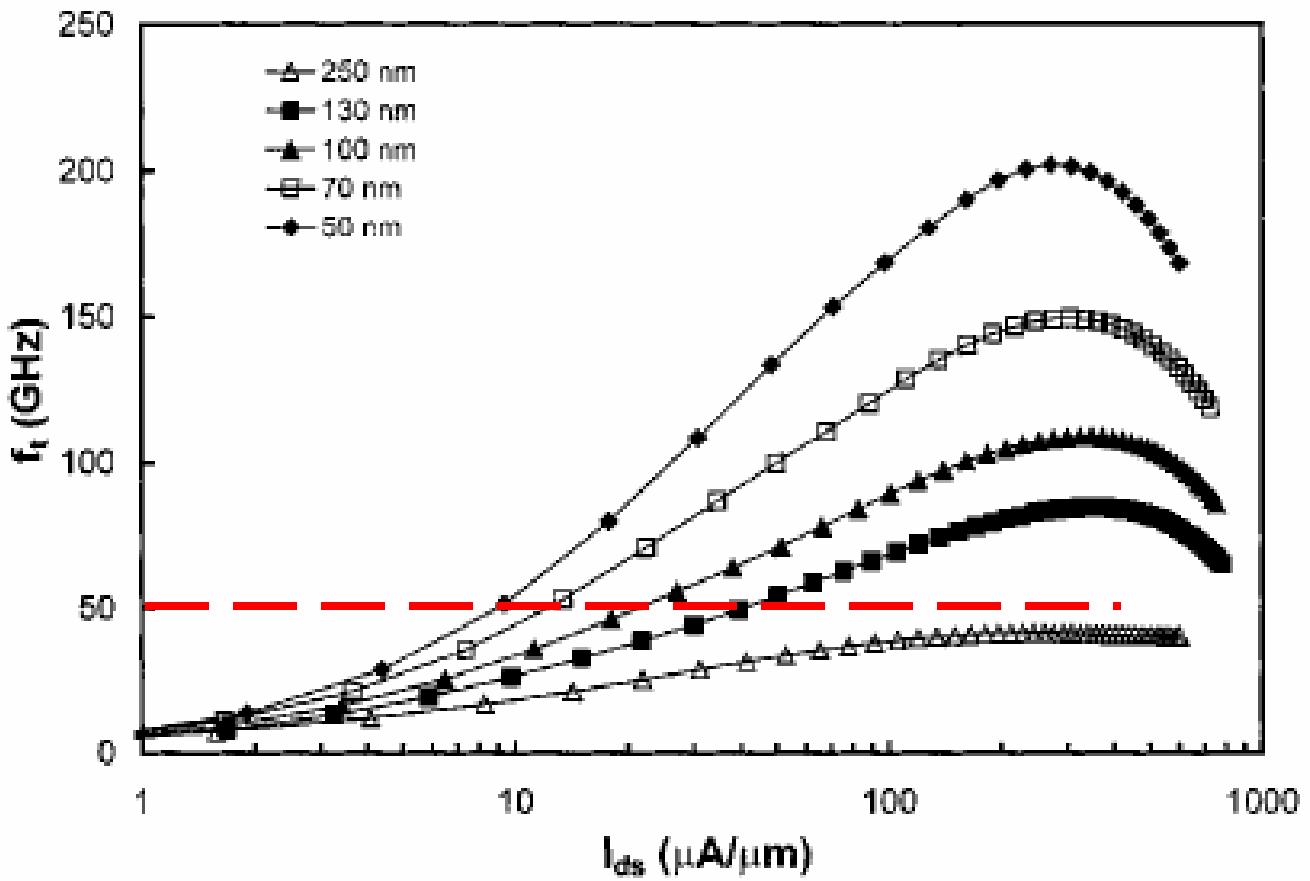
Dependence of f_T on Bias Current

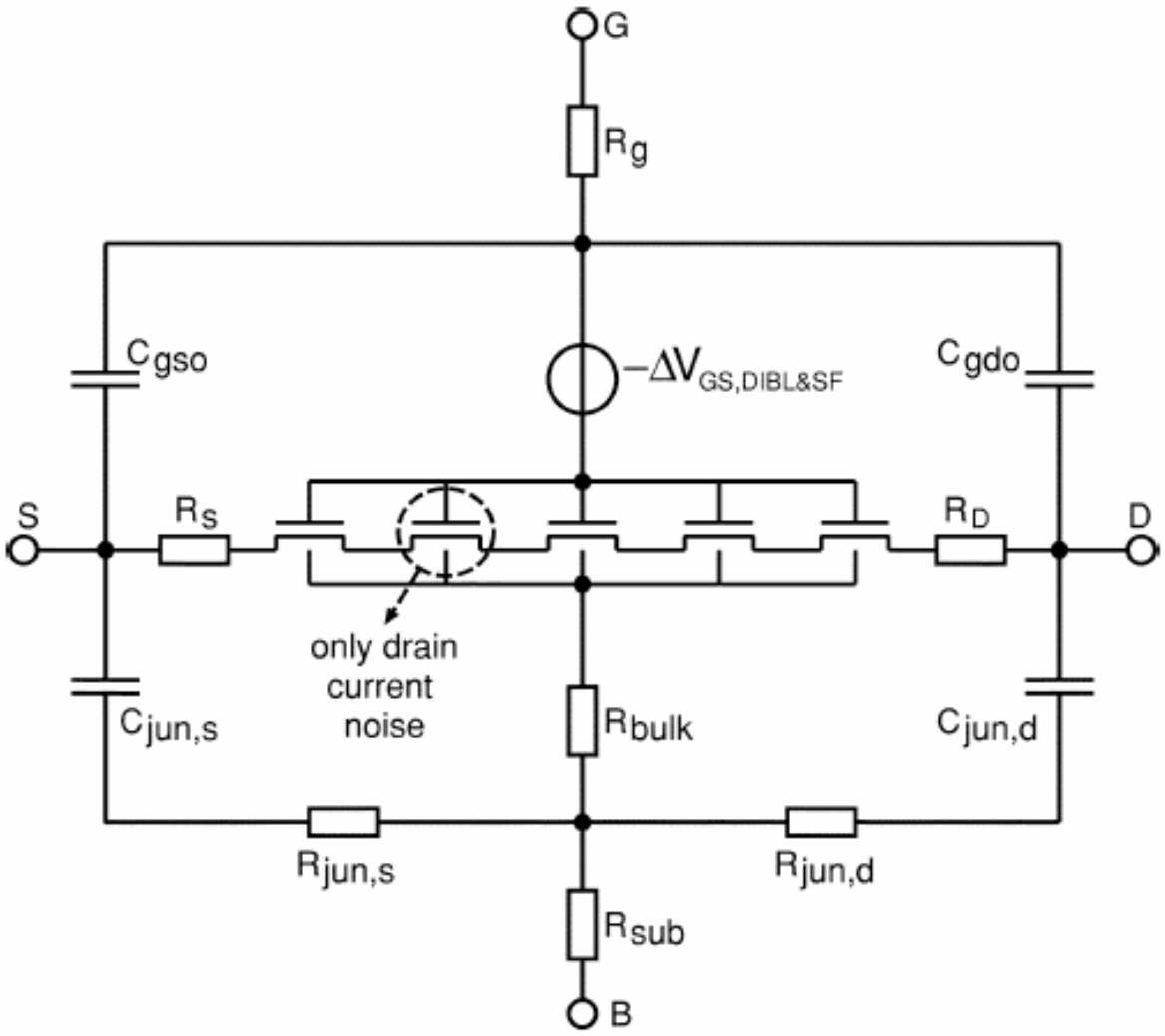


f_T depends on I_{DS}.

I_{DS} can be reduced for similar f_T with scaled technology.

P. Woerlee, et al., “RF CMOS Performance Trends," *IEEE Transactions on Electron Devices*, Vol. 48, pp. 1776-17 82, August 2001.

MOSFET Noise Model

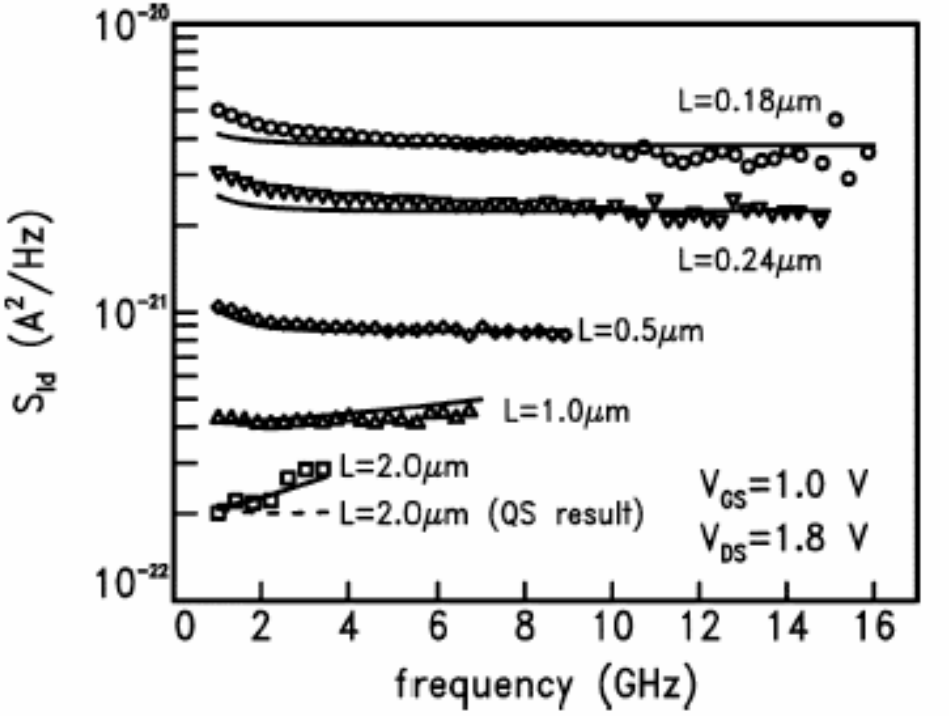


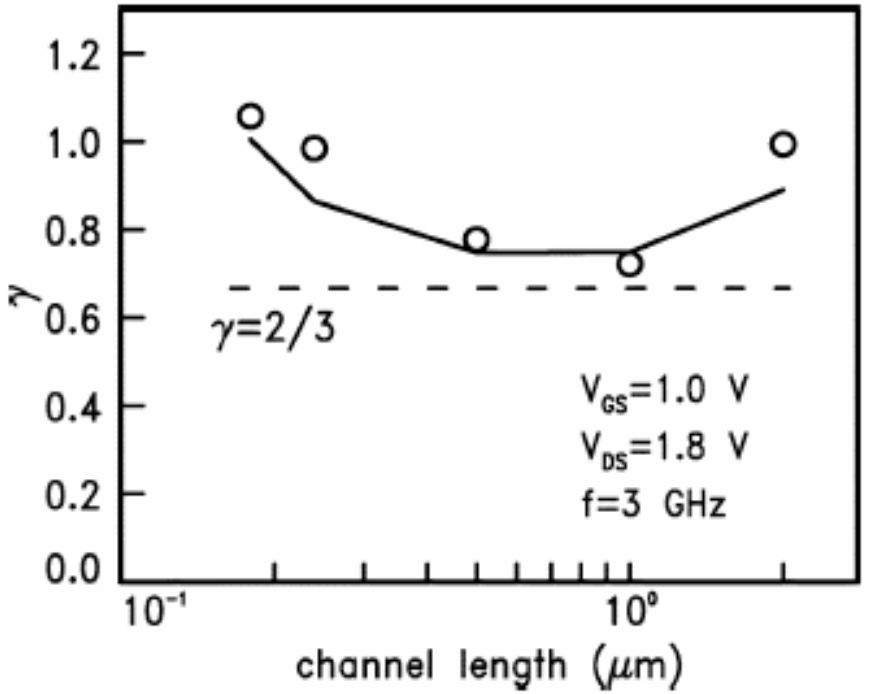
Source : A. Scholten, et al., "Noise Modeling for RF CMOS Circuit Simulation," *IEEE Transactions on Electron Devices*, Vol. 50, pp. 618-632, March 2003.

Drain Thermal Noise

Drain current noise is dominated by thermal noise at high f.
γ models the excessive noise observed in short L devices.
The excessive noise is believed to be due to substrate noise.

noise current source $S_{I_D} = 4k_B T g_{do} \gamma$ $e_n^2 = i_n^2 / g_{do}^2$

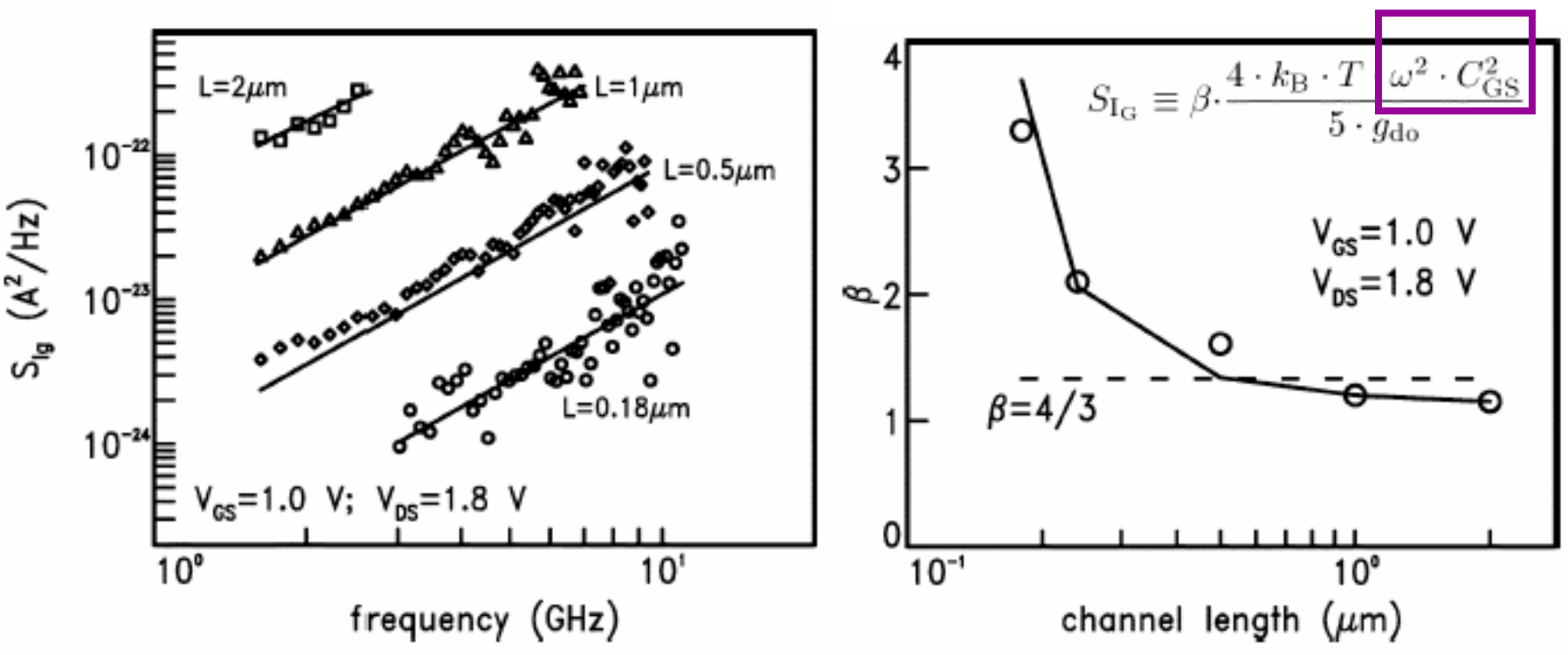




Induced Gate Noise

Gate noise induced by drain thermal noise is only a portion of the total noise.

β models the excessive noise observed in short L devices.



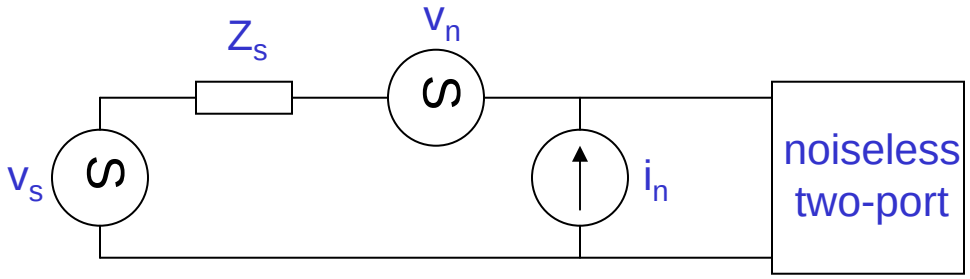
Noise Figure

- Noises due to parasitic resistances associated with drain, source, bulk and especially gate need to be accounted for.

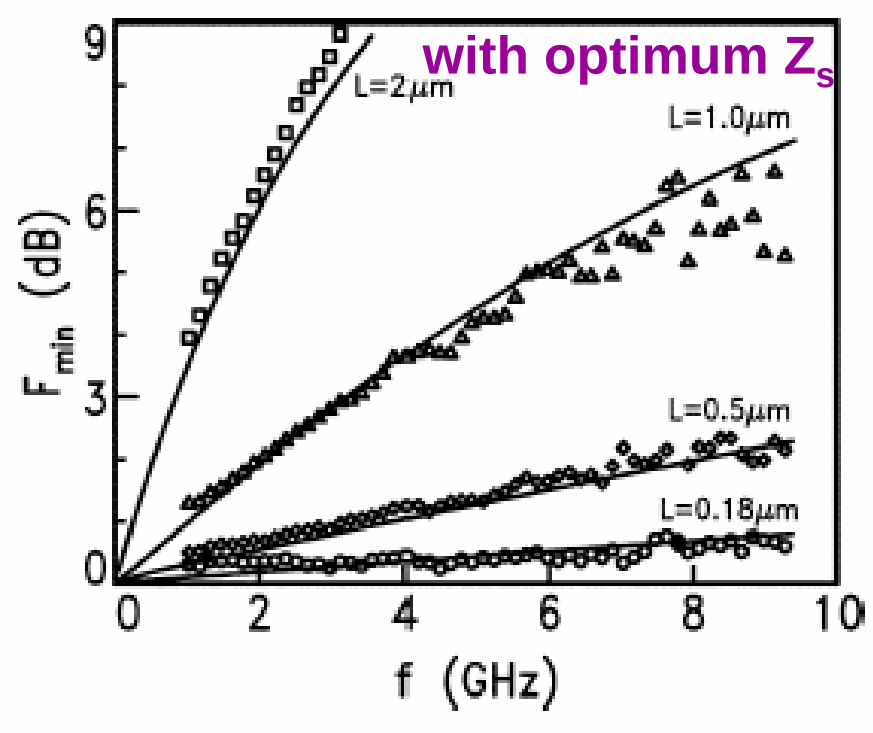
- Other noise sources, such as short noise due to gate leakage and avalanche noise at high V_{DS}, are usually insignificant.

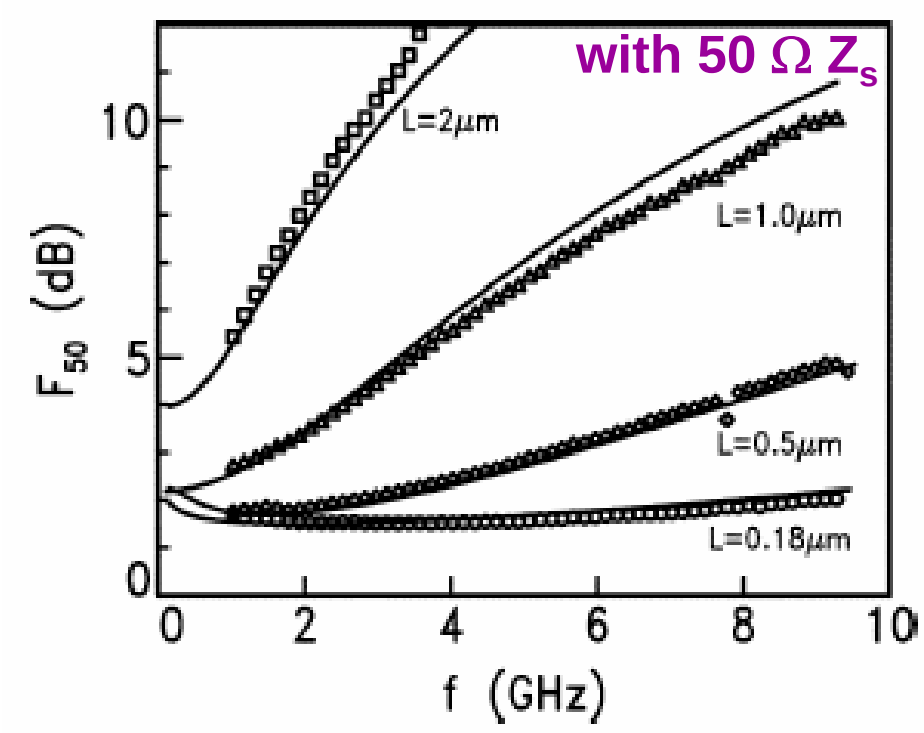
- Noise figure describes the noise performance of a circuit.

- Noise figure depends on the source impedance matching. When Z_s is low, v_n dominates. When Z_s is high, i_n dominates.



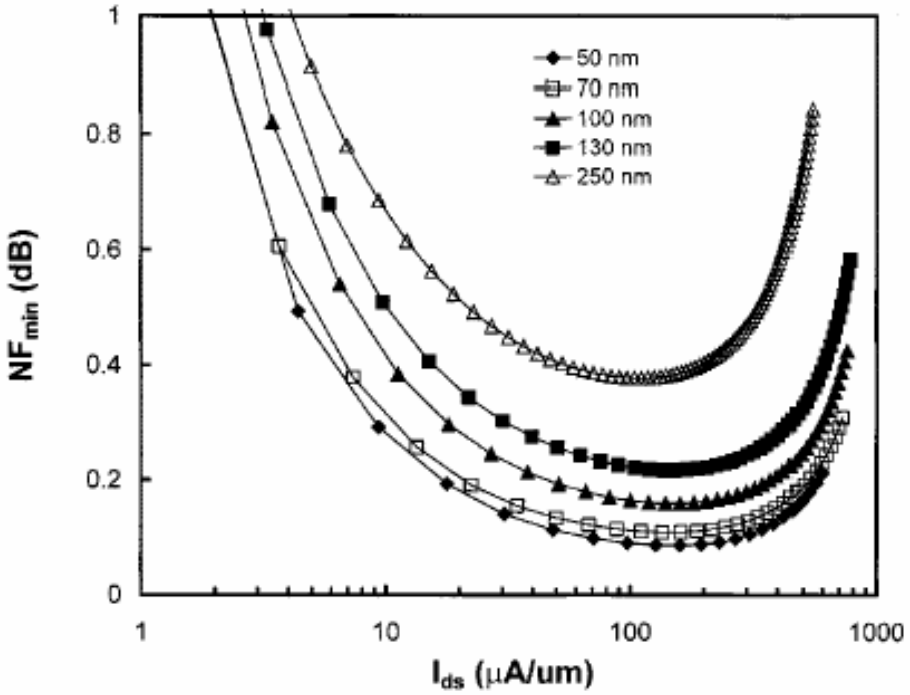
Noise Figure



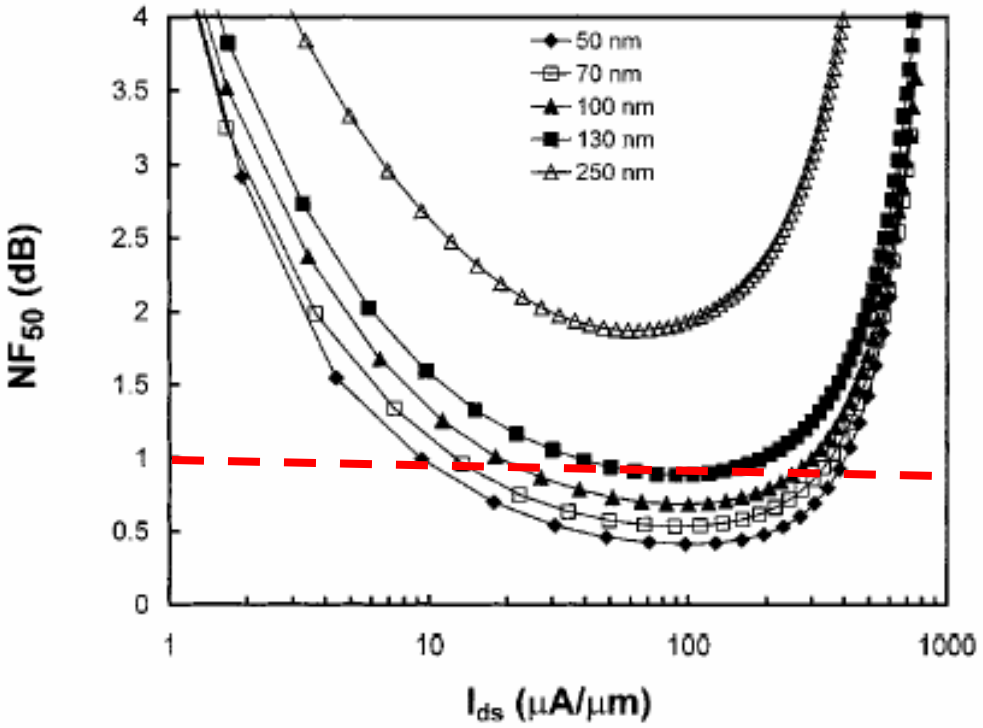


- For typical common source type LNA, NF ~ 1+ K f / f_T, NF improves with scaled technology.
- In practice, it is very difficulty to achieve the minimum NF because of other constraints.

Noise Figure versus Bias Current



with optimum Z_s

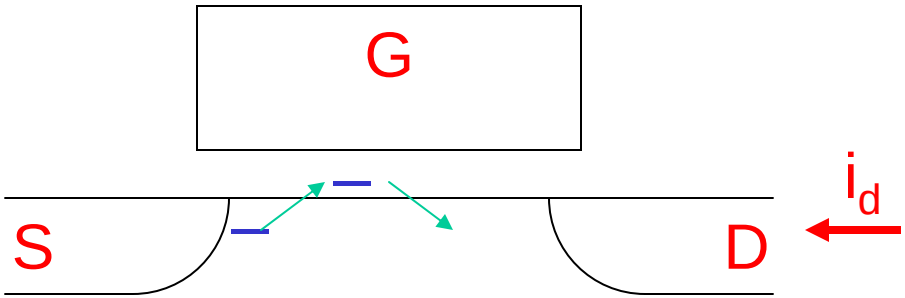


with 50 Ω Z_s

NF depends on f_T, and hence I_{DS}.
I_{DS} can be reduced for similar NF with scaled technology.

P. Woerlee, et al., “RF CMOS Performance Trends," *IEEE Transactions on Electron Devices*, Vol. 48, pp. 1776-17 82, August 2001.

Drain 1/f Noise

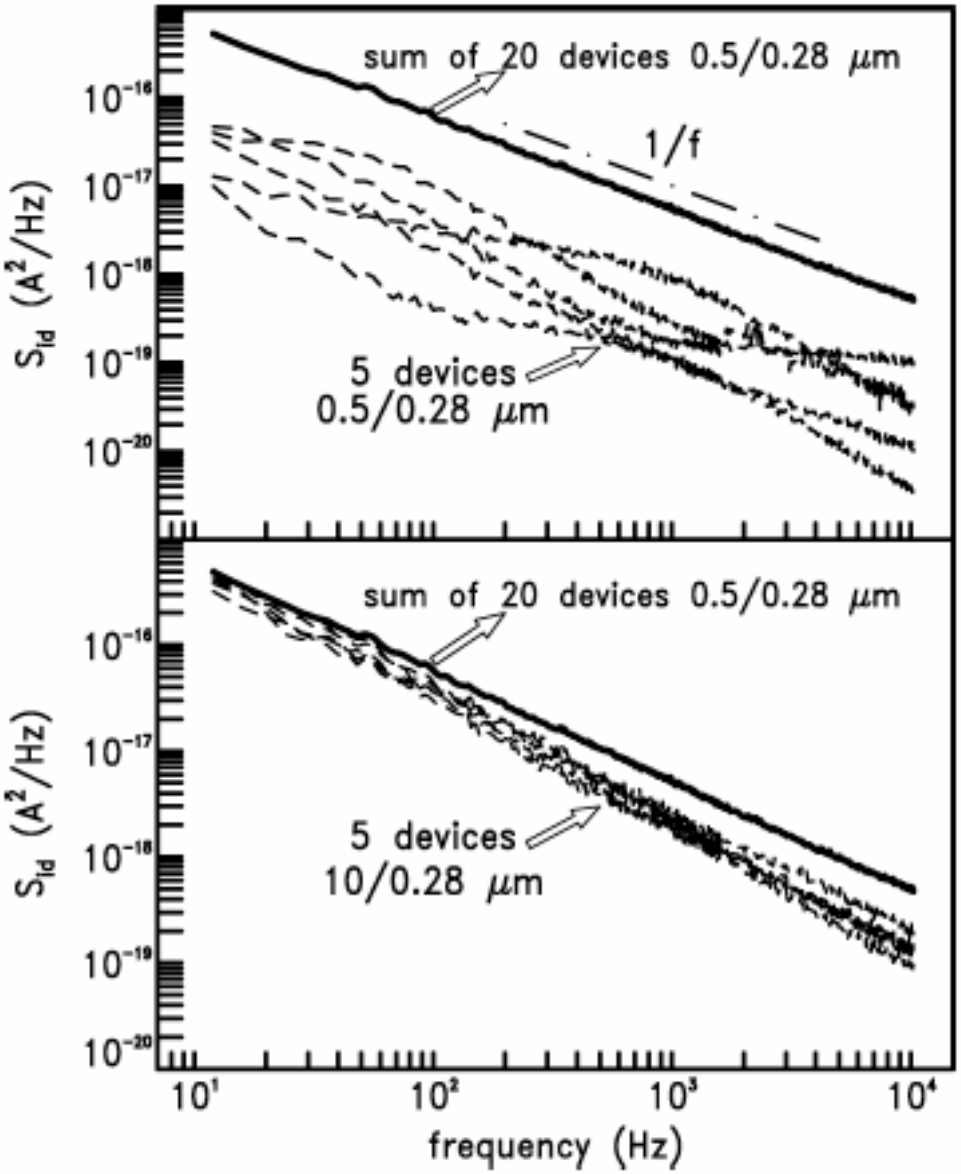


Drain 1/f Noise

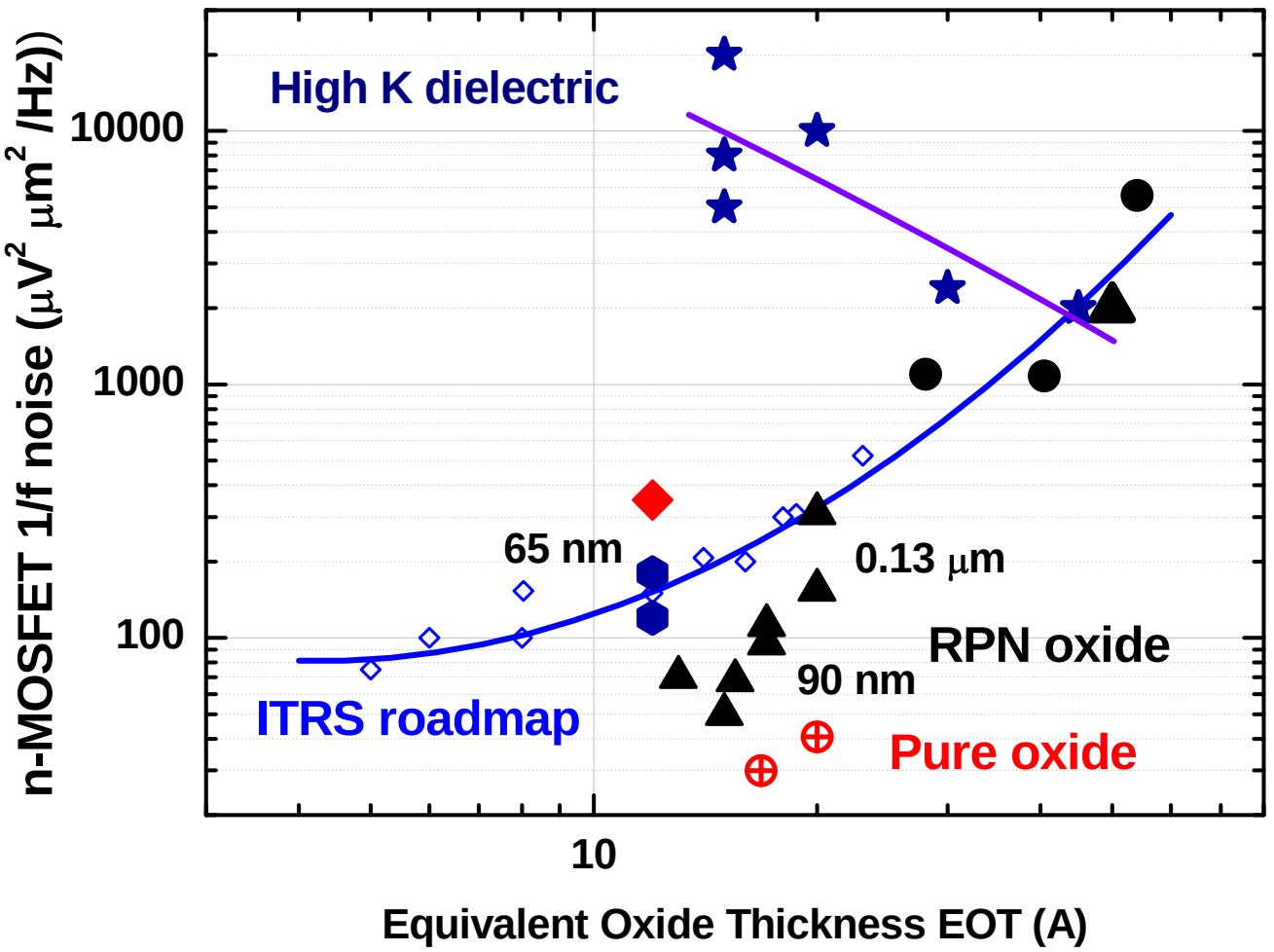
Drain current noise is dominated by1/f noise at low f.

Although not critical for LNA, very important for VCO, A/D

$$S_{id} = K\, gm^2 / \underline{W L C_{ox}^2}\, f$$



Degradation of 1/f Noise

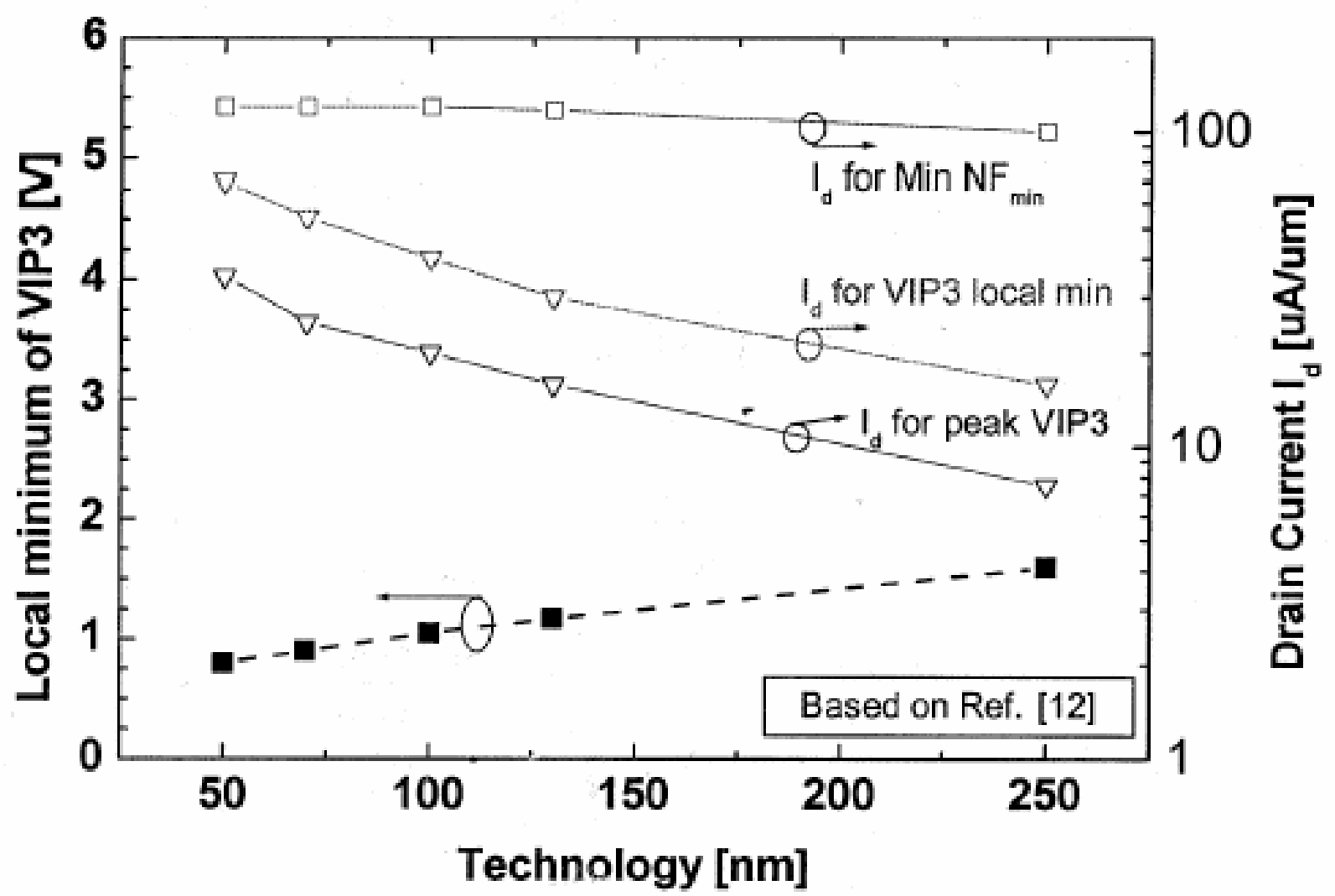


Source : Mercha, et al., “Impact of Scaling on Analog/RF CMOS Performance," *International Conference on Solid State and Integrated Circuits Technology Proceedings*, paper A3.2, 2004.

Characteristics of Scaled MOSFET

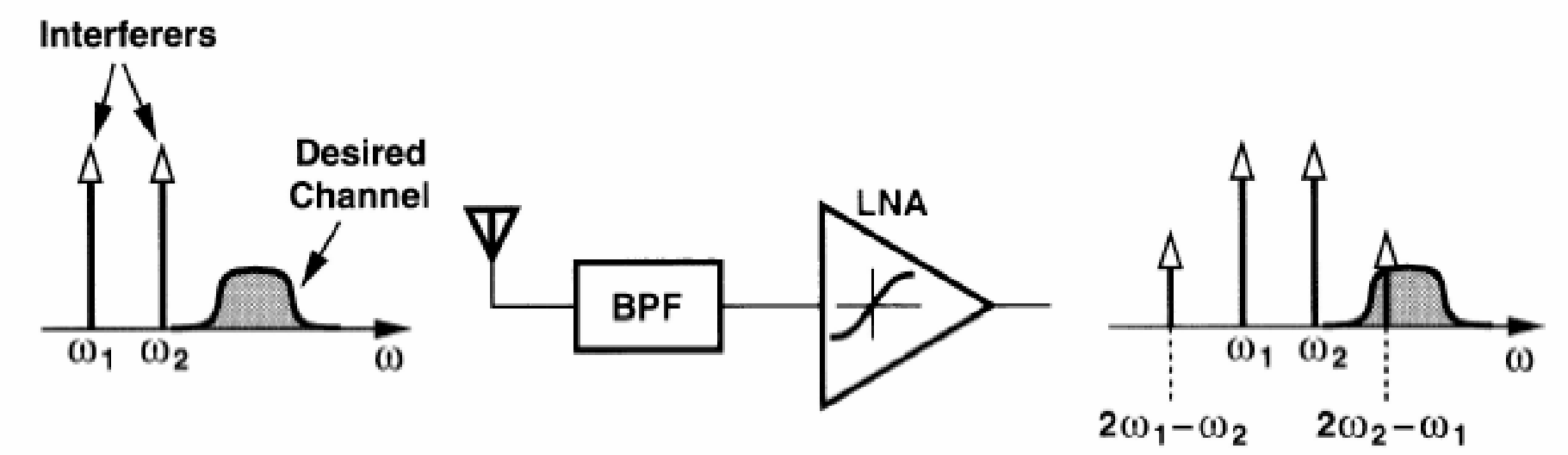
Process	0.25 μm ('98)	0.18 μm ('00)	0.13 μm ('02)	90 nm ('04)
V_{dd} (V)	2.5 (1x)	1.8 (0.7x)	1.2 (0.5x)	1.0 (0.4x)
I_{dsat} (μA/μm)	600 (1x)	600 (1x)	550 (1x)	850 (1.4x)
I_{off} (nA/μm)	0.01 (1x)	0.02 (2x)	0.32 (32x)	7 (700x)
I_{gate} (nA/μm)	2.5e-5 (1x)	1.8e-3 (100x)	0.65 (5e4)	6.3 (70000x)
I_{on}/I_{off} (10e6)	60 (1x)	30 (0.5x)	1.7 (0.03x)	0.12 (0.002x)
g_m (mS/μm)	0.3 (1x)	0.4 (1.3x)	0.6 (2x)	1.0 (3.3x)
g_{ds} (μS/μm)	7.7 (1x)	15 (2x)	42 (5.4x)	100 (13x)
g_m / g_{ds}	39 (1x)	27 (0.7x)	14 (0.36x)	10 (0.26x)
f_T (GHz)	30 (1x)	60 (2x)	80 (2.7x)	140 (4.7x)
Delay (ps/gate)	45 (1x)	30 (0.7x)	15 (0.3x)	11 (0.24x)
C_g (fF/gate)	0.47 (1x)	0.35 (0.7x)	0.25 (0.5x)	0.16 (0.34x)
C_j (fF/gate)	0.83 (1x)	0.80 (1x)	0.88 (1.1x)	0.66 (0.8x)

Linearity of MOSFET



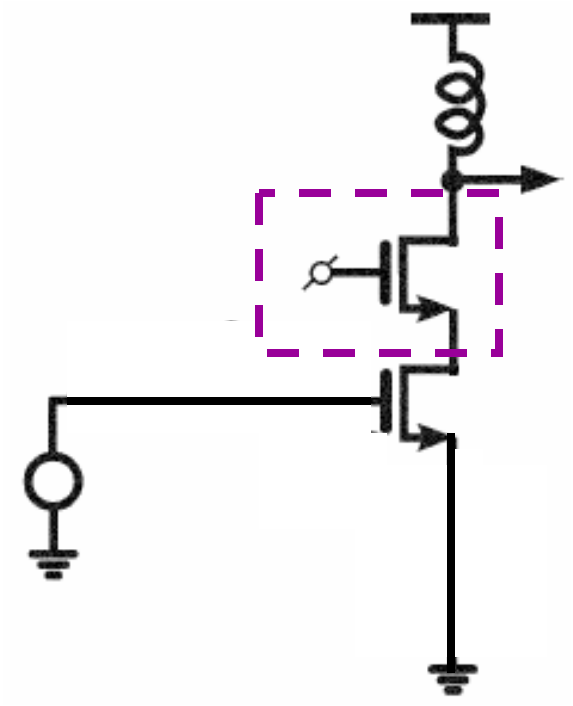
Source : C. Diaz, D, Tang and J. Sun, "CMOS Technology for MS/RF SoC," *IEEE Transactions on Electron Devices*, Vol. 50, pp. 557-566, March 2003.

Effect of Non-Linearity



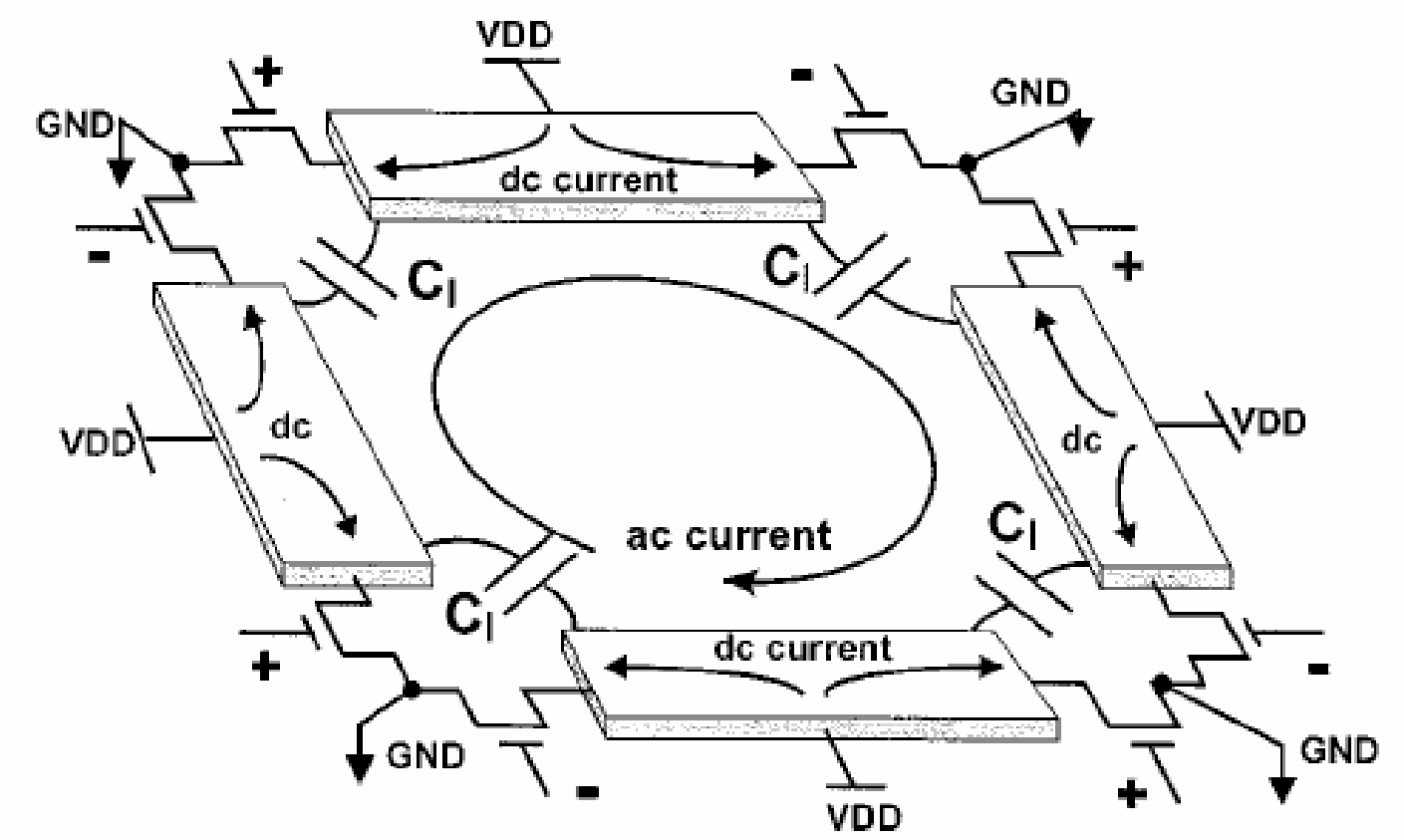
Sample RF Circuits

Power Amplifier



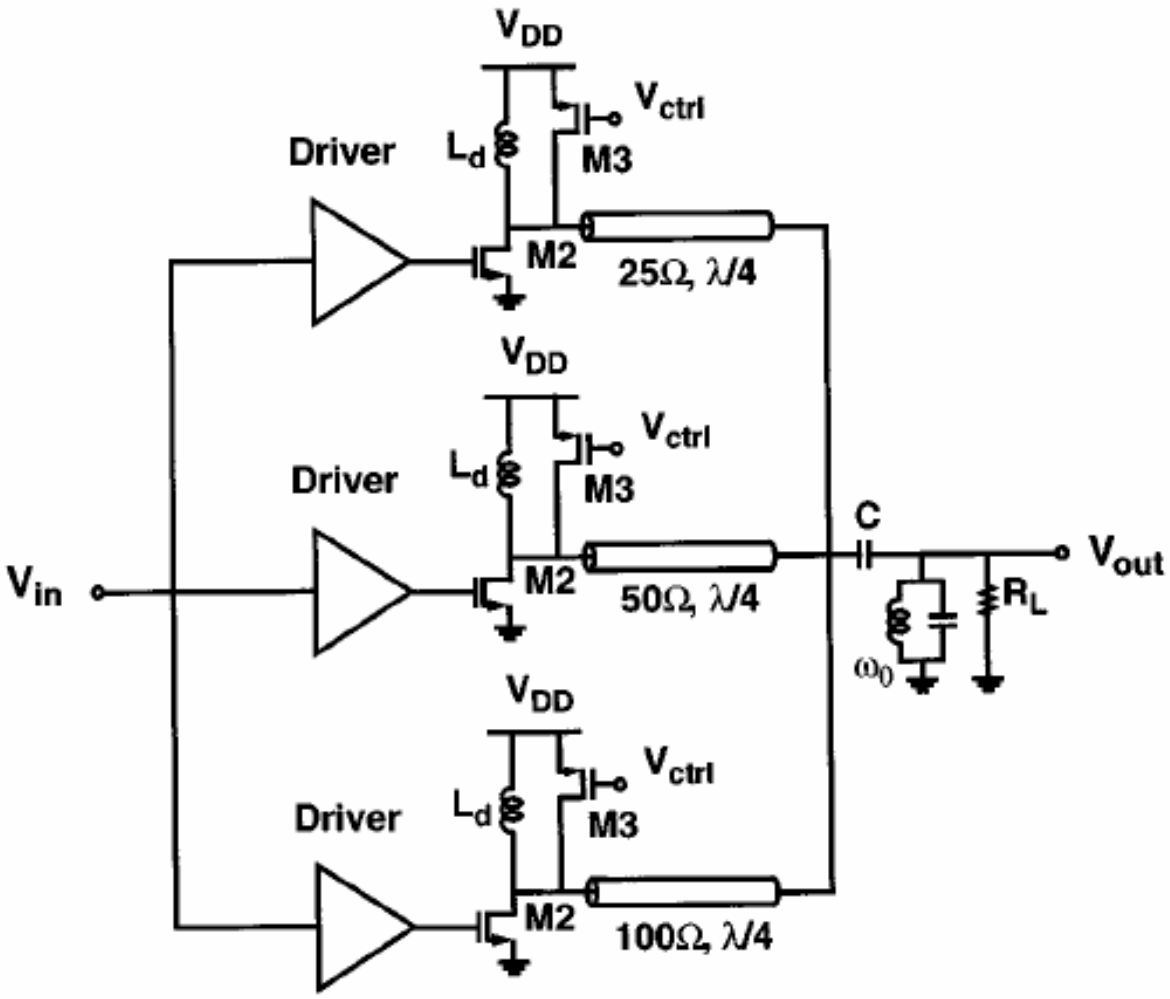
High voltage required for the cascode transistor.

Distributed Power Amplifier



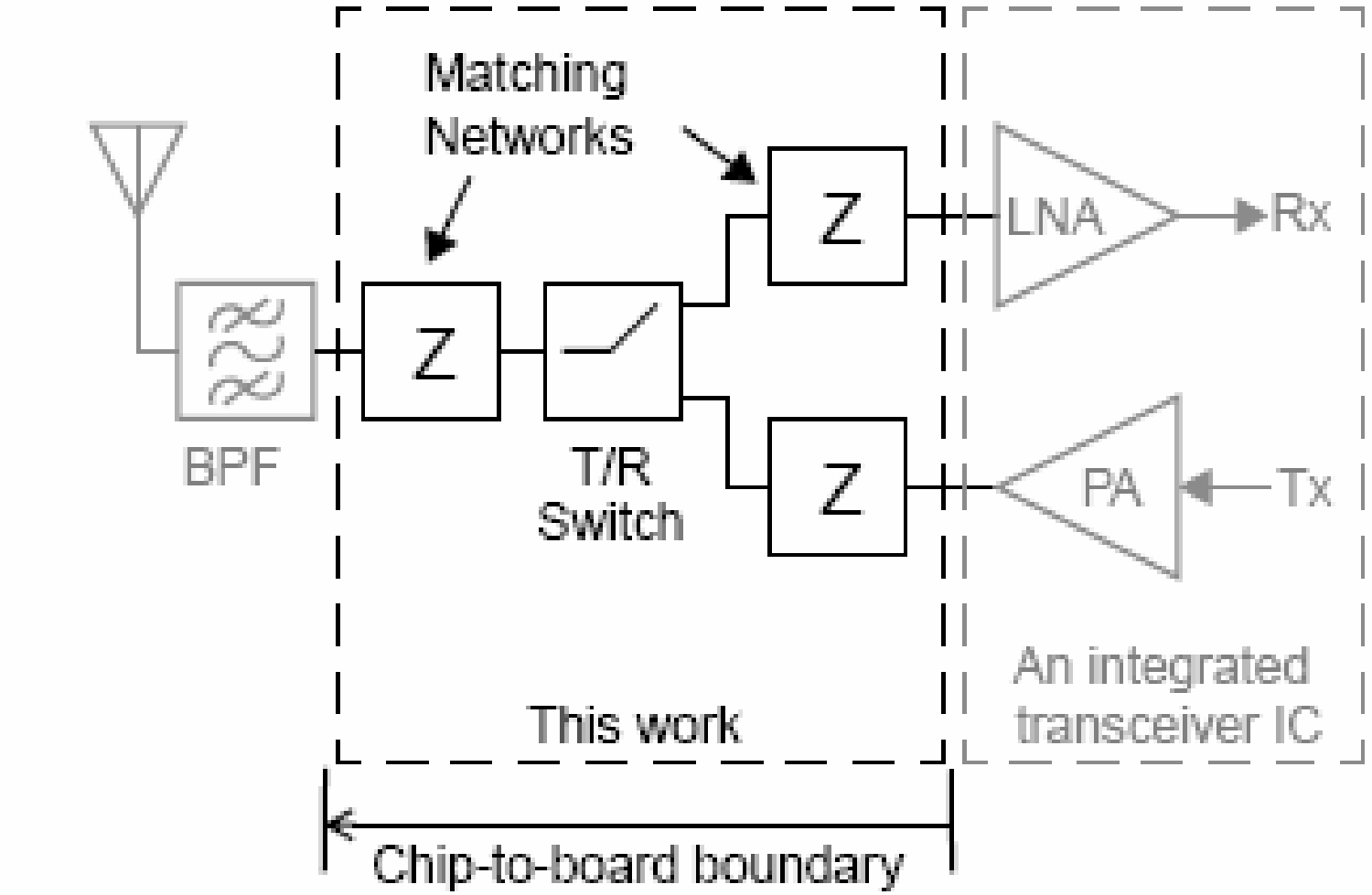
I. Aoki, et al., "Fully Integrated CMOS Power Amplifier Design Using the Distributed Active Transforme r Architecture," *IEEE Journal of Solid State Circuits*, Vol. 37, pp. 371 -383, March 2002.

Power Combining



A. Shirvani, et al., “A CMOS RF Amplifier with Parallel Amplification for Efficient Power Control," *IEEE Journal of Solid State Circuits*, Vol. 37, pp. 684 -693, June 2002.

Typical RF Transceiver



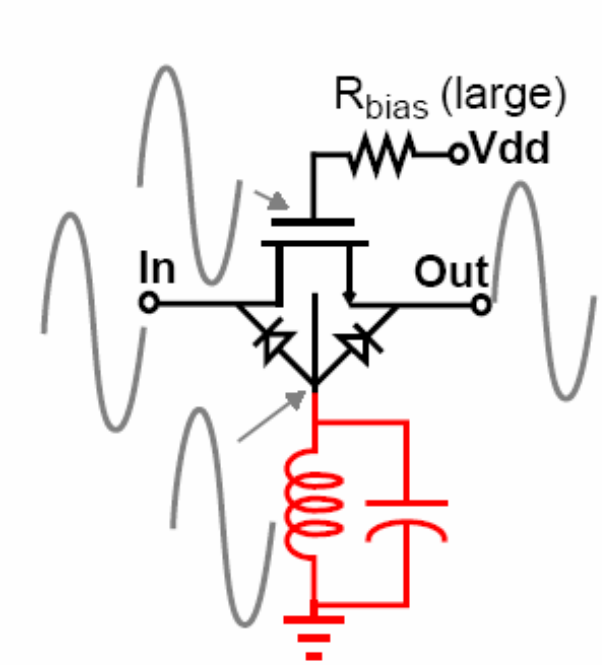
MOSFET-Based T/R Switch

Solution :

Bias the gate through a resistor – allows the gate to be bootstrapped with incoming signal – improve linearity

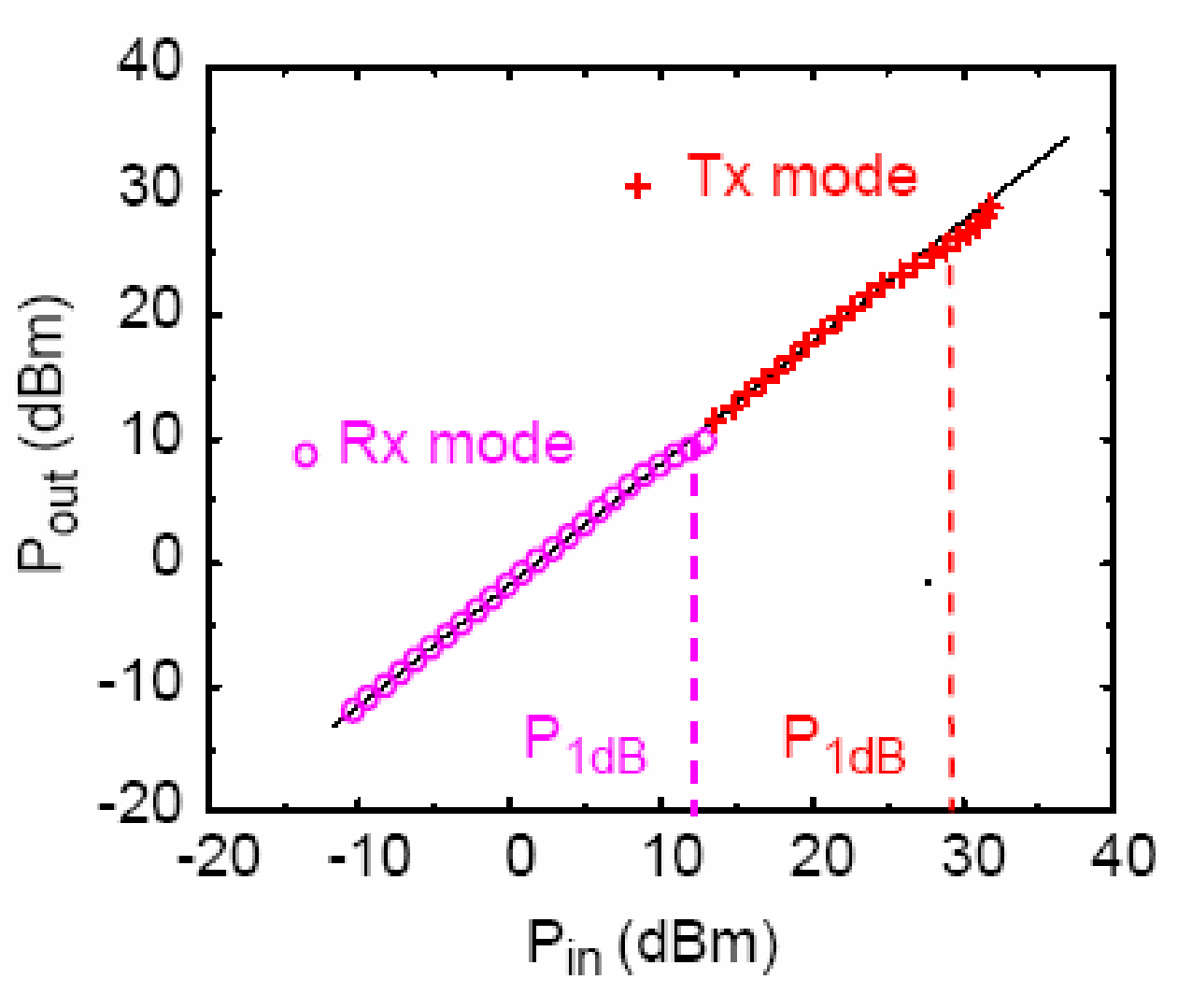
Bias the substrate through a L-C tank – allows the substrate to be bootstrapped with incoming signal,

Linearity is greatly improved.



N. Talwalkar, et al., "Integrated CMOS Transmit-Receive Switch Using L-C Tuned Substrate Bias for 2.4-GHz and 5.2-GHz Applications," *IEEE Journal of Solid State Circuits*, Vol. 39, pp. 863 -870, June 2004.

Switch Linearity



Outline

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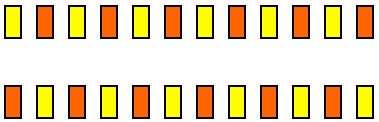
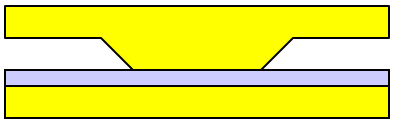
Capacitor Options

Inter-level Metal-Oxide-Metal (MOM)

Intra-level Metal-Oxide-Metal (MOM)

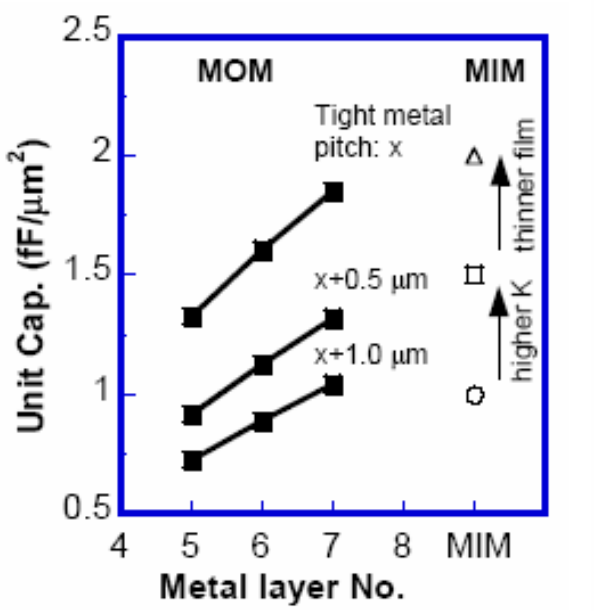


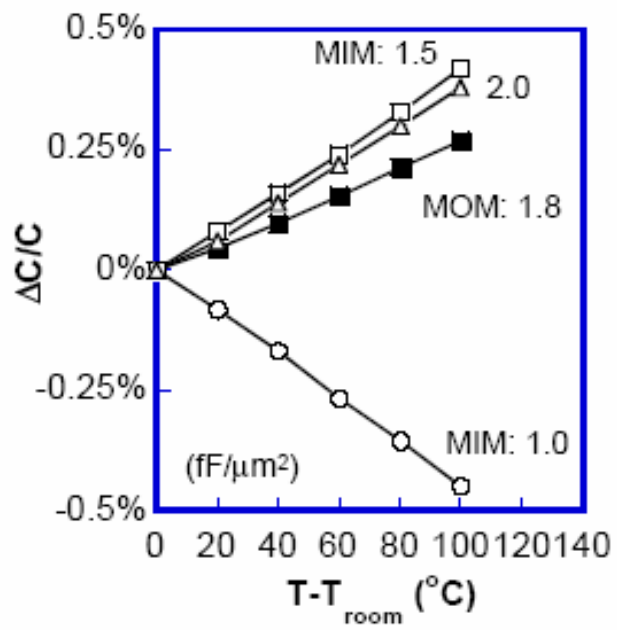
High K Metal-Insulator-Metal (MIM)

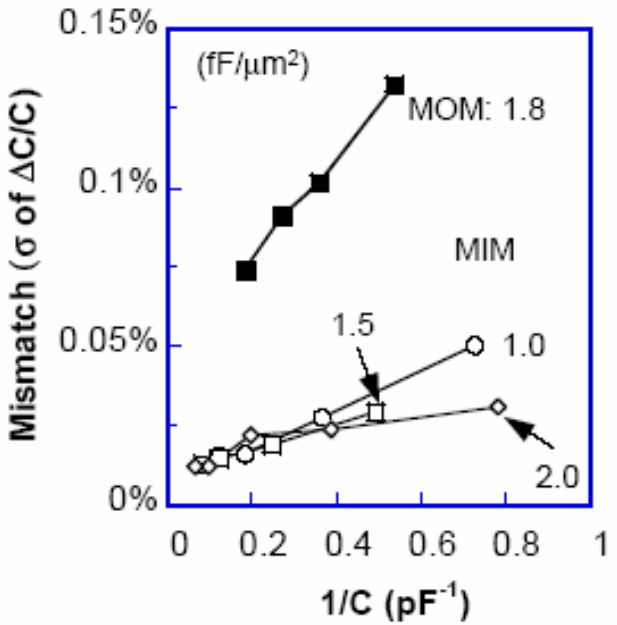


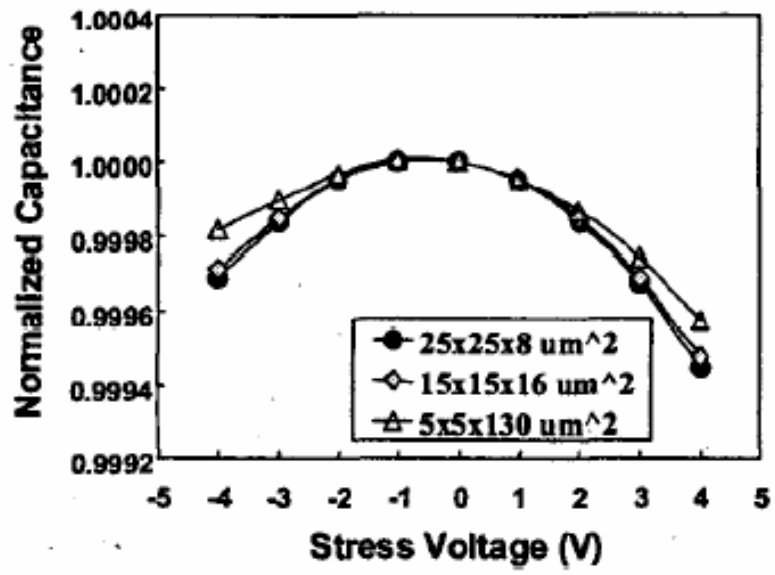
	Metal Thickness (μm)	Metal Space (μm)	Dielectric Thickness (μm)	Approx K
250 nm	0.6	0.4	1	4.1
180 nm	0.5	0.3	0.8	3.8
130 nm	0.4	0.2	0.5	3.8
90 nm	0.3	0.15	0.3	3.2

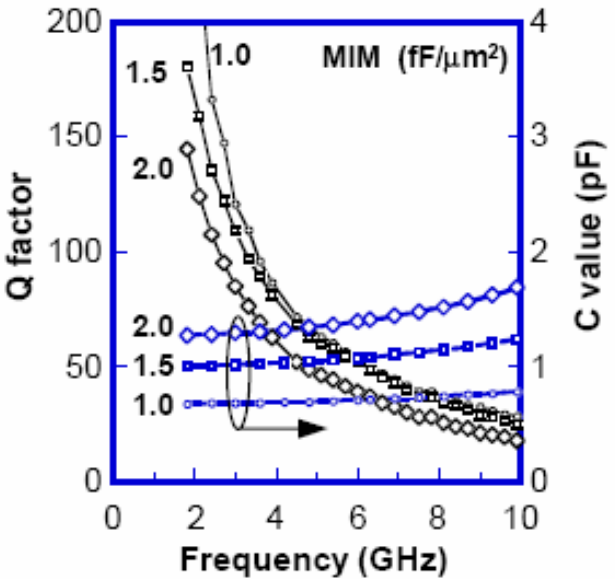
Capacitor Performance





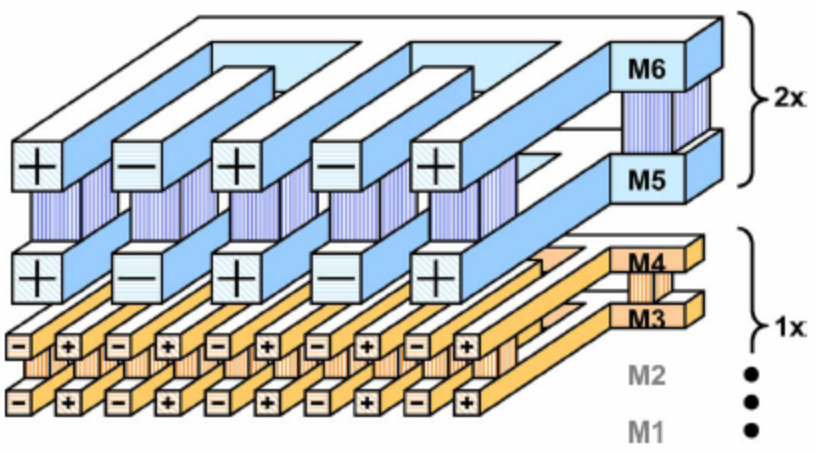


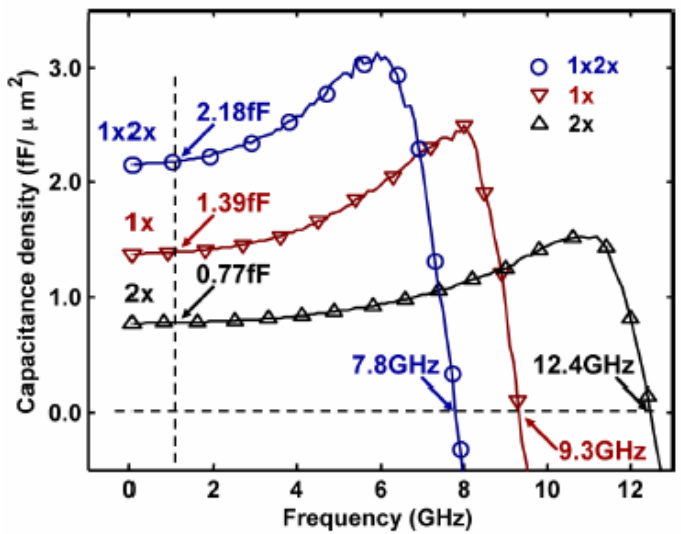


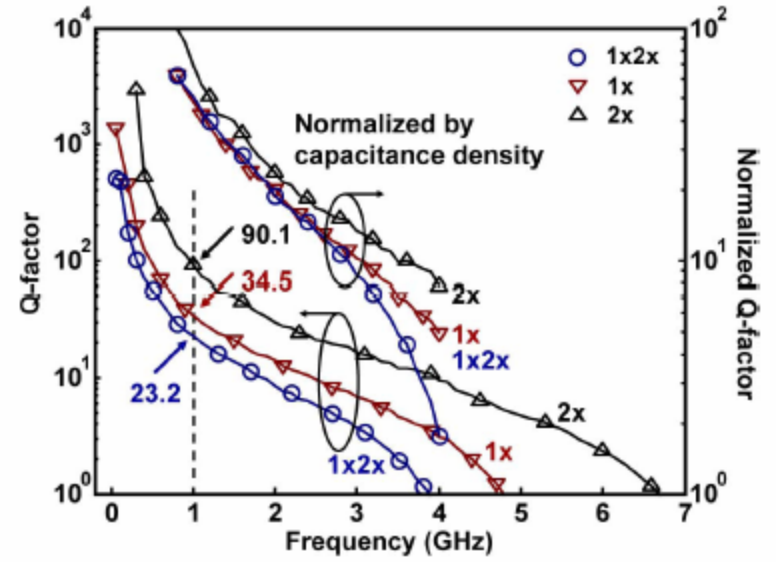


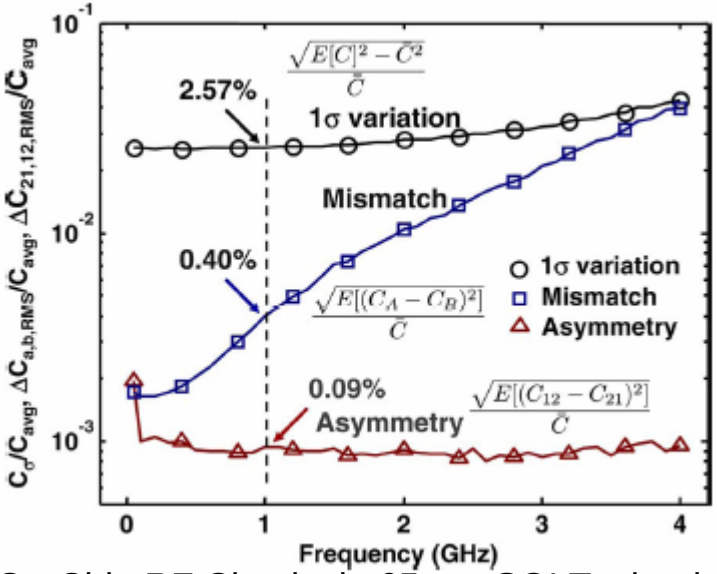
J. Lin, et al., "State-of-the-Art RF/Analog Foundry Technology," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 73-79, 2002. 39-42, 2003.

3D Capacitor



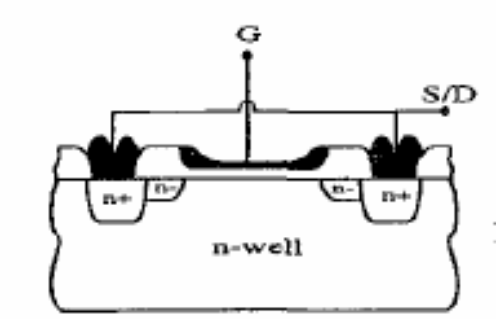


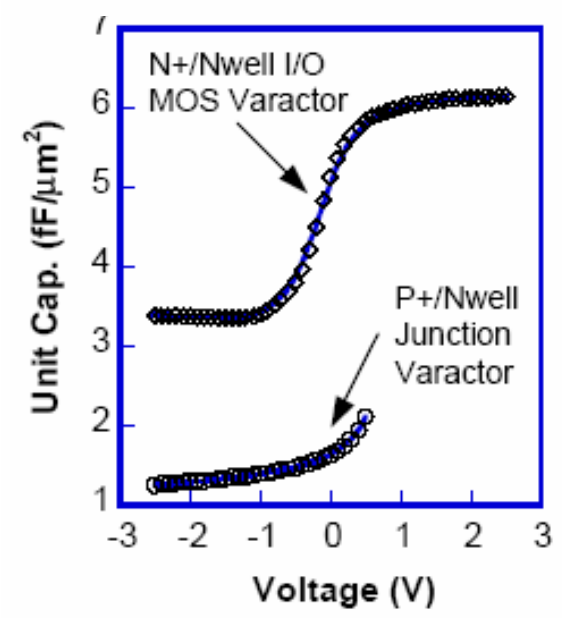


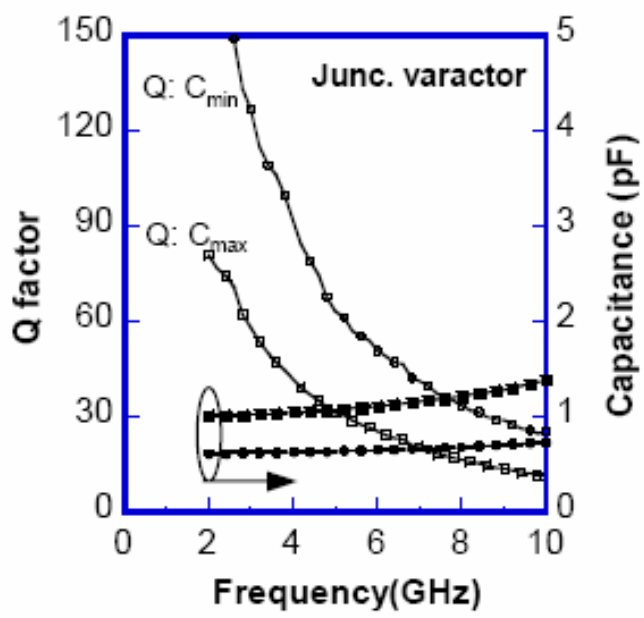


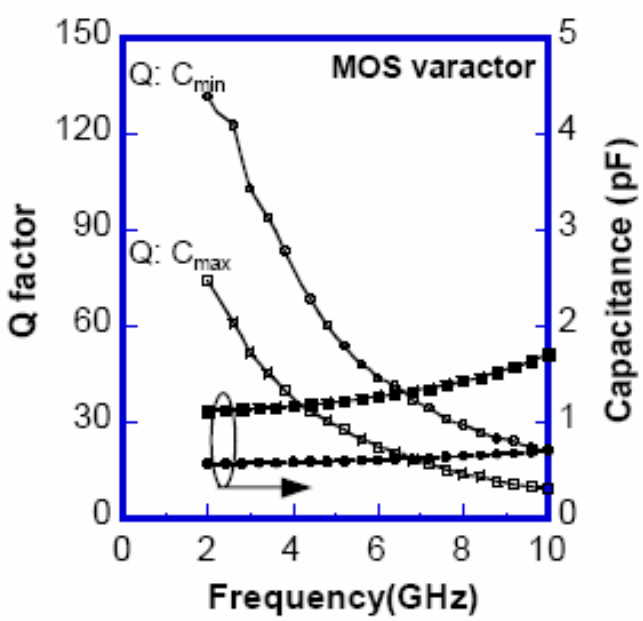
D. Kim, etal., “Symmetric Vertical Parallel Plate Capacitors for On-Chip RF Circuits in 65-nm SOI Technology," *IEEE Electron Device Letters*, pp. 616-618, July 2007.

Varactor Options





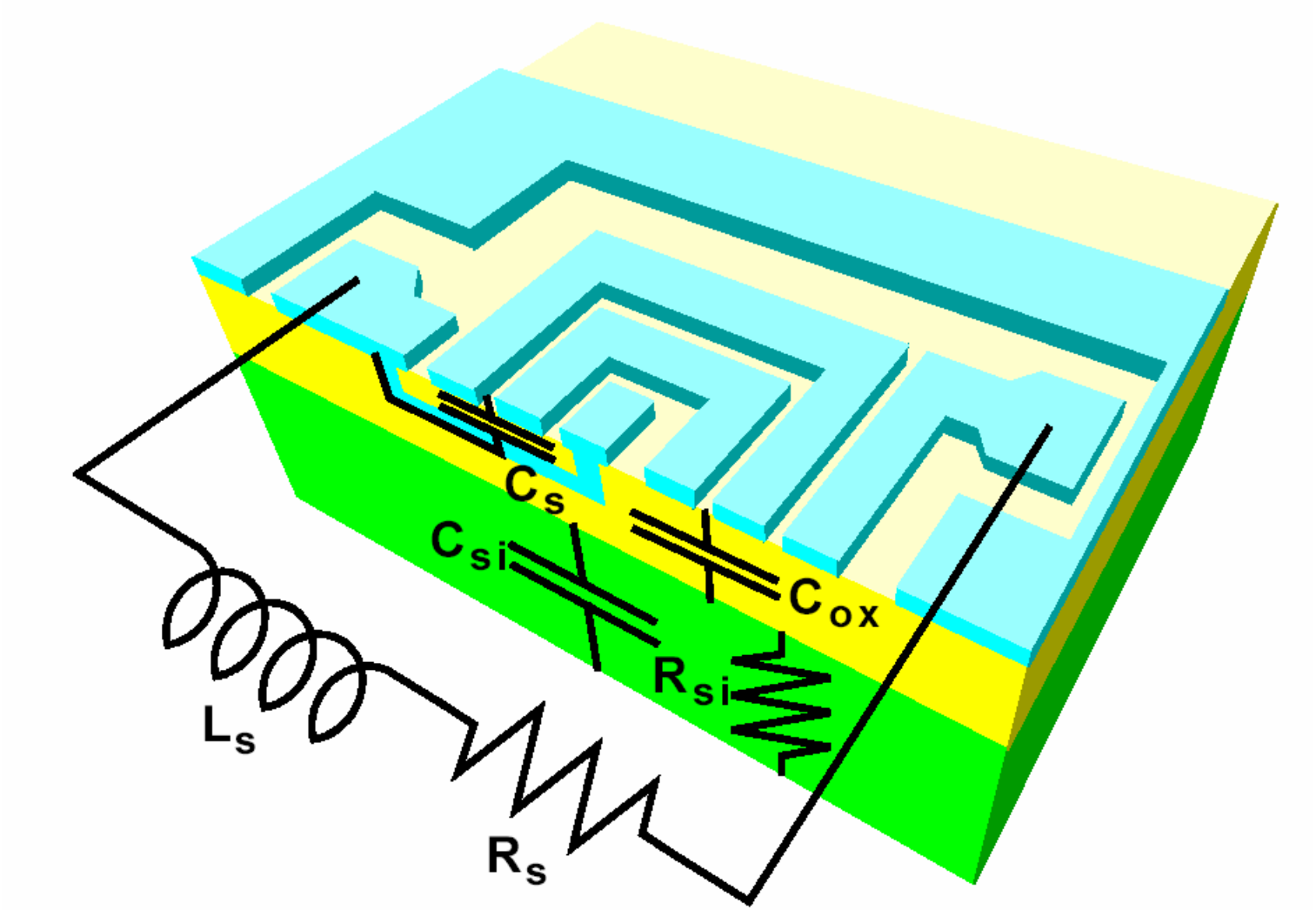




MOS accumulation mode varactor offers higher C/Area, more tuning range, comparable Q, and less temp sensitivity.

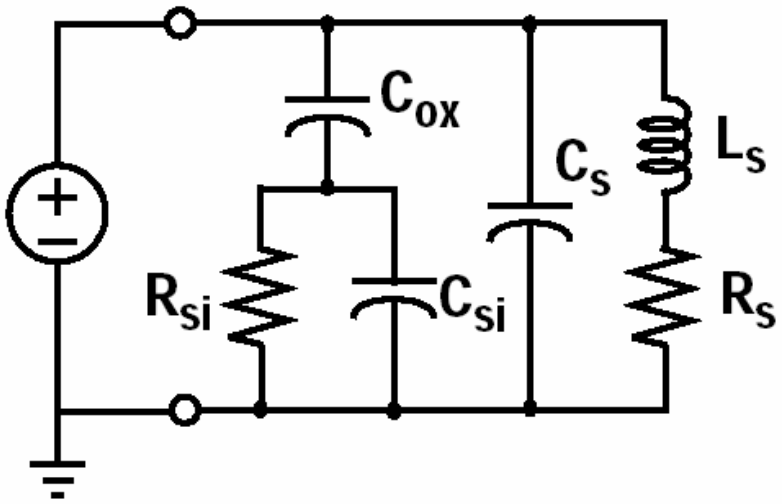
C. Chen, et al., "A 90nm CMOS MS/RF Based Foundry SOC Technology Comprising Superb 185 GHz fT RFMOS and Versatile, High-Q Passive Components for Cost/Performance Optimization," *IEEE International Electron Devices Meeting*, pp. 39-42, 2003.

On-Chip Spiral Inductor



C. Yue and S. Wong, "Physical Modeling of Spiral Inductors on Silicon," *IEEE Transactions on Electron Devices*, Vol. 47, pp. 560-568, March 2000.

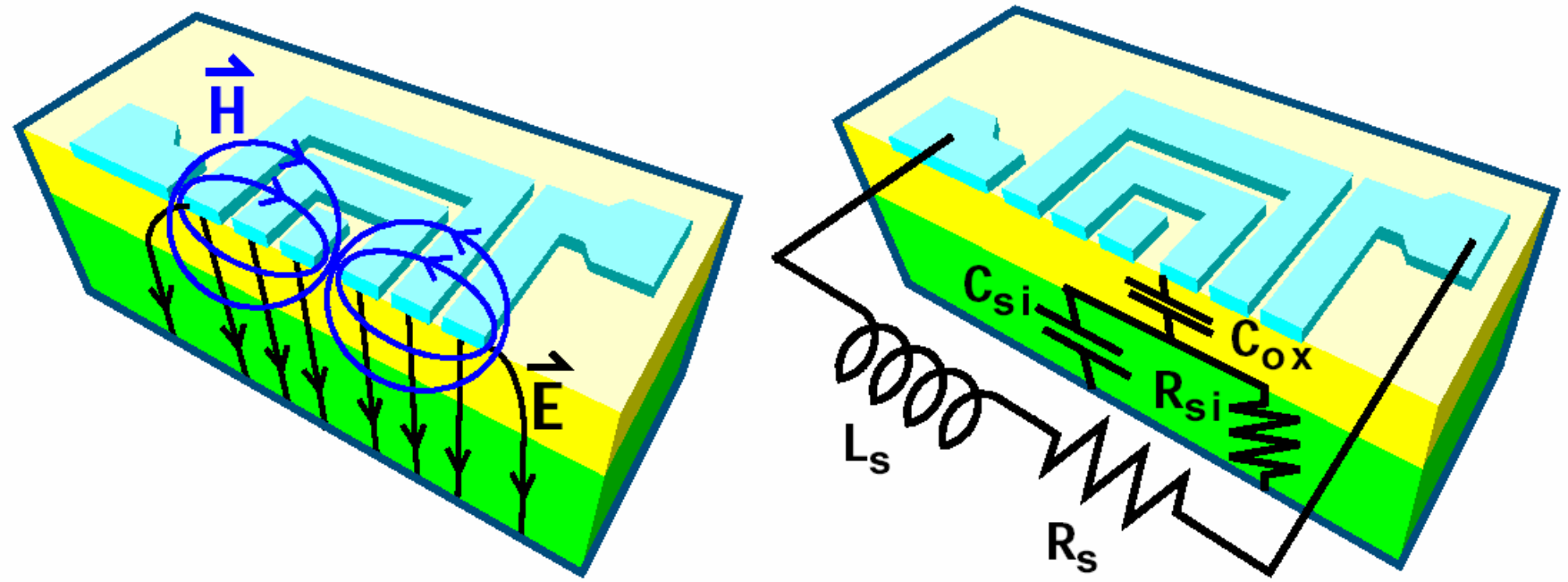
Quality Factor



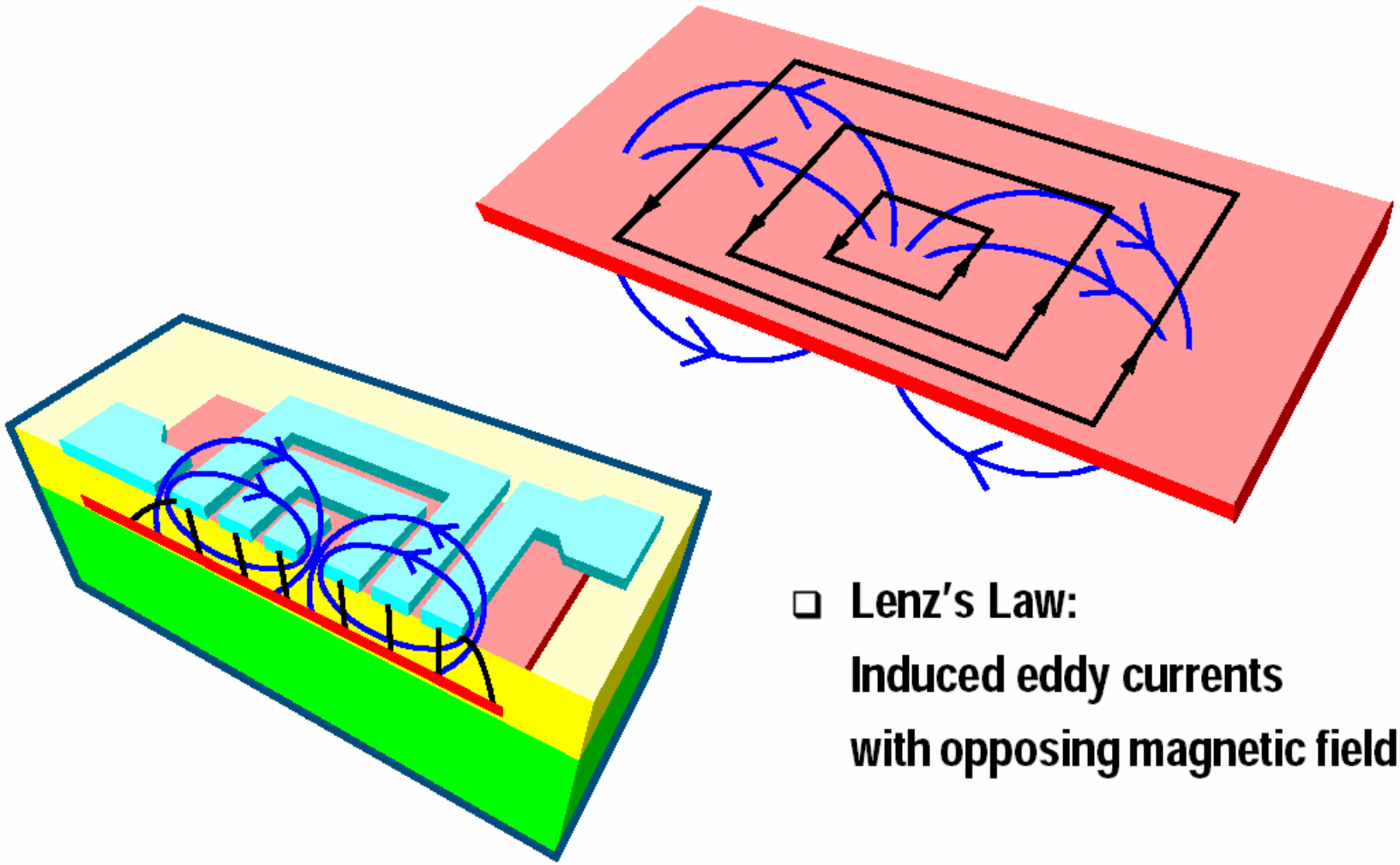
$$Q = 2\pi \frac{|\text{Peak Magnetic Energy} - \text{Peak Electric Energy}|}{\text{Energy Loss in One Oscillation Cycle}}$$

$$\frac{\omega L_s}{R_s} \times \underbrace{\frac{R_p}{R_p + [(\omega L_s / R_s)^2 + 1] \cdot R_s}}_{\text{Substrate Loss Factor}} \times \underbrace{\left(1 - \frac{R_s^2 (C_p + C_s)}{L_s} - \omega^2 L_s (C_p + C_s)\right)}_{\text{Self-Resonance Factor}}$$

Substrate Loss due to E-field Penetration

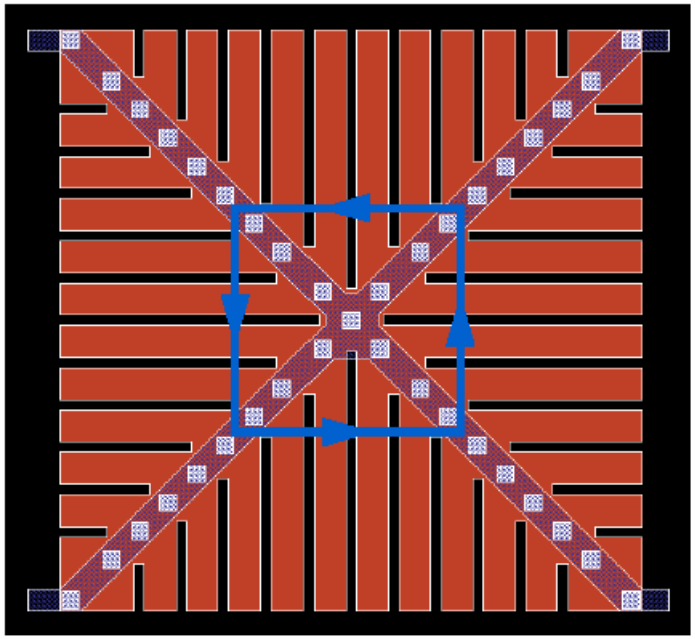


Ground Shield to Stop E-field Penetration



- Lenz's Law:
  Induced eddy currents
  with opposing magnetic field

Patterned Ground Shield



Silicided polysilicon

Induced loop current

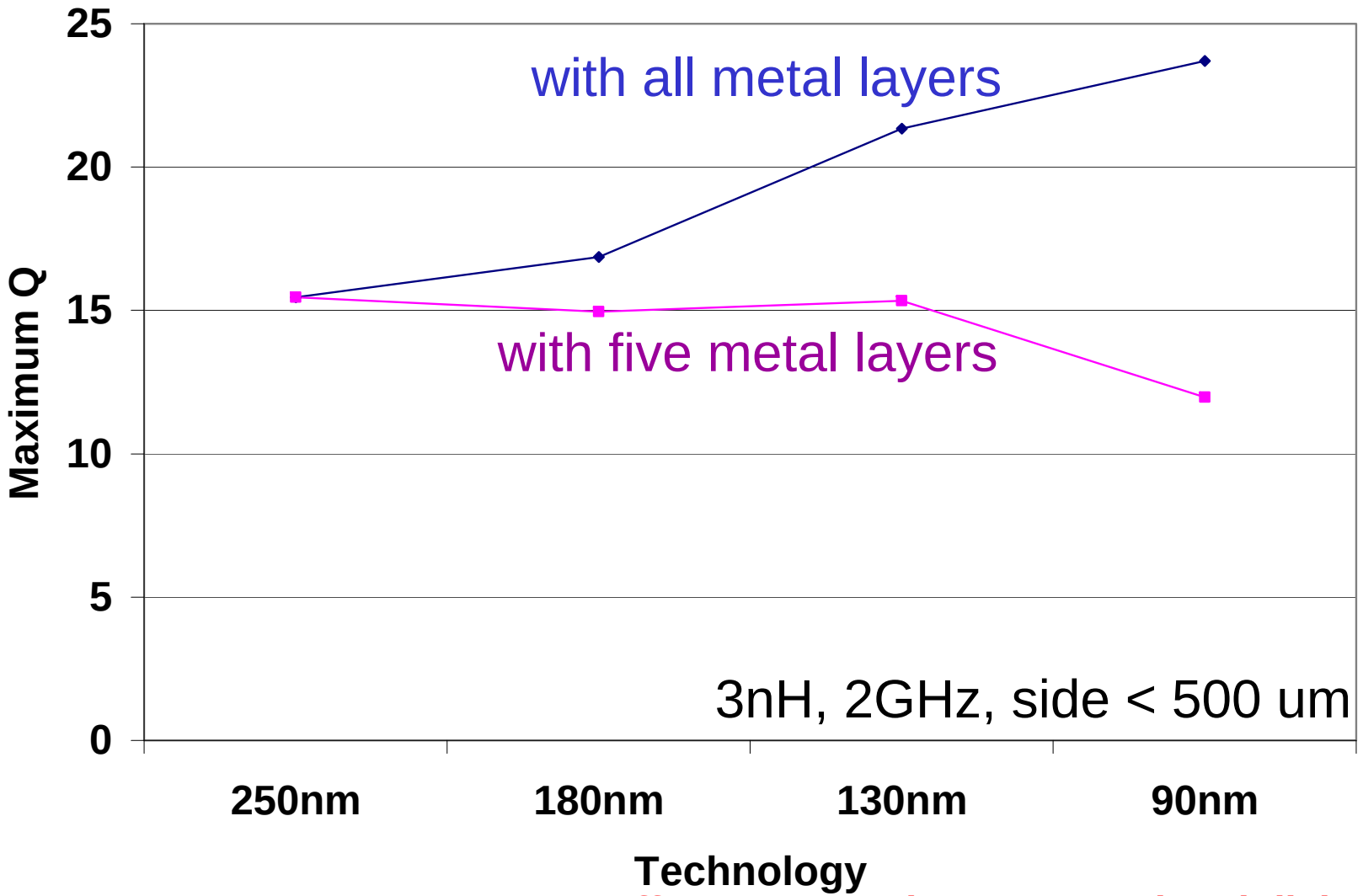
- Patterned Ground Shield
- Inserted between the inductor and substrate
- PGS fingers orthogonal to spiral for form a "star" shape
- No interference with the inductor magnetic field
- Use silicided polysilicon with Metal1 strap for low resistance path to ground.

C. Yue and S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE Journal of Solid State Circuits*, Vol. 33, pp. 743-752, May 1998.

Comparison of Back End Technology

	Metal Layers	Top Metal Thickness (μm)	Top Metal to Sub (μm)	M5 to Sub (μm)	Approx K
250 nm	5	1 Al	7.5	7.5	4
180 nm	6	1 Al	8	6.5	3.8
130 nm	8	0.9 Cu	7	4	3.8
90 nm	9	0.85 Cu	7	3	3.2

Optimized Inductor Q

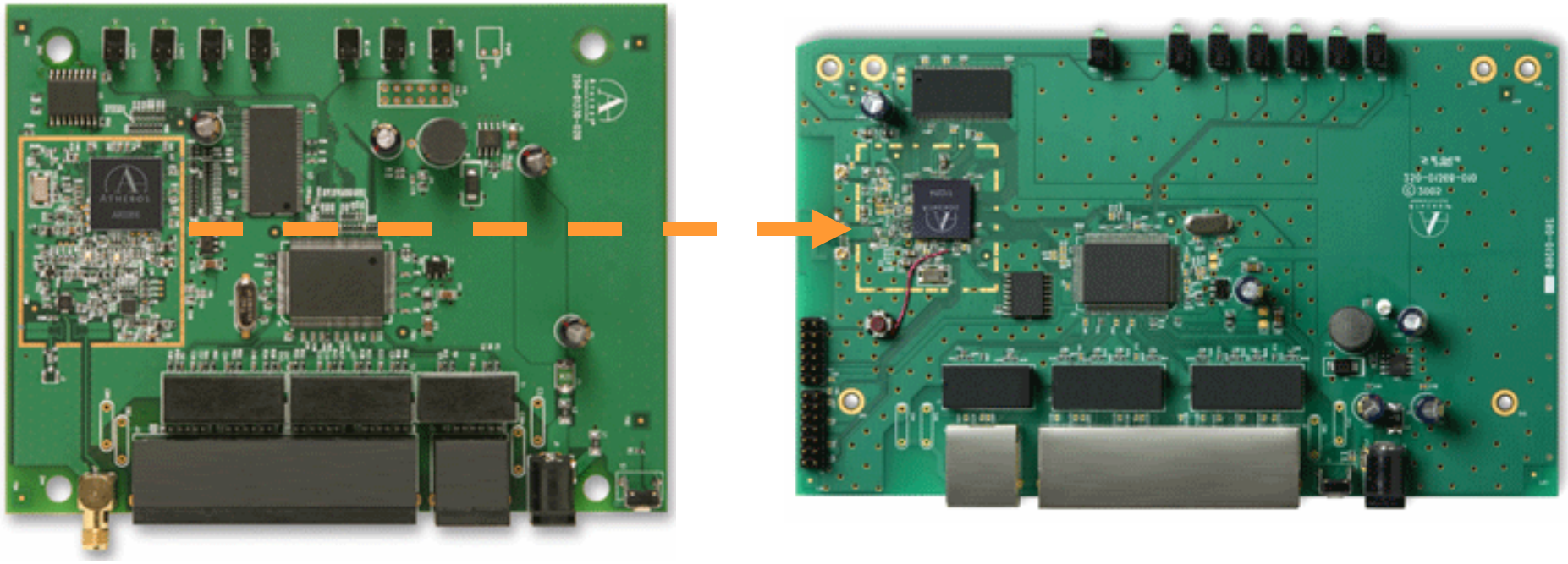


65nm offers more options on metal and dielectric, including multiple thick metal layers

Outline

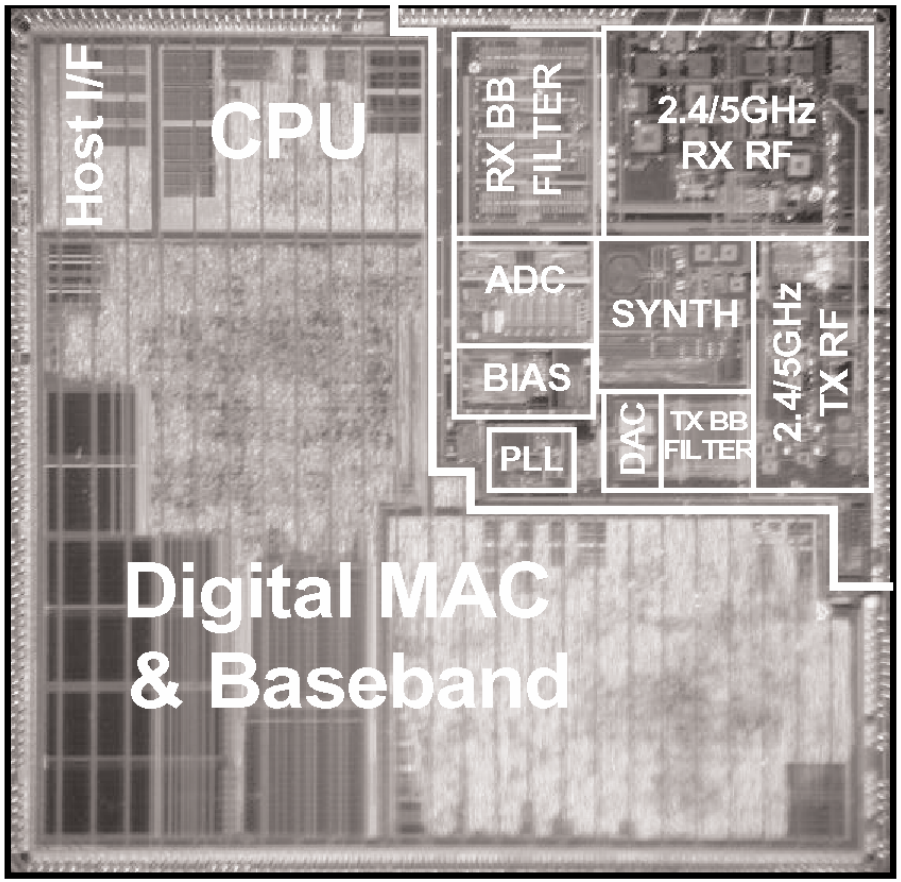
- Transistor Scaling
- Passive Components
- Future Integration Trends
- Conclusions

Integration of Off-Chip Components

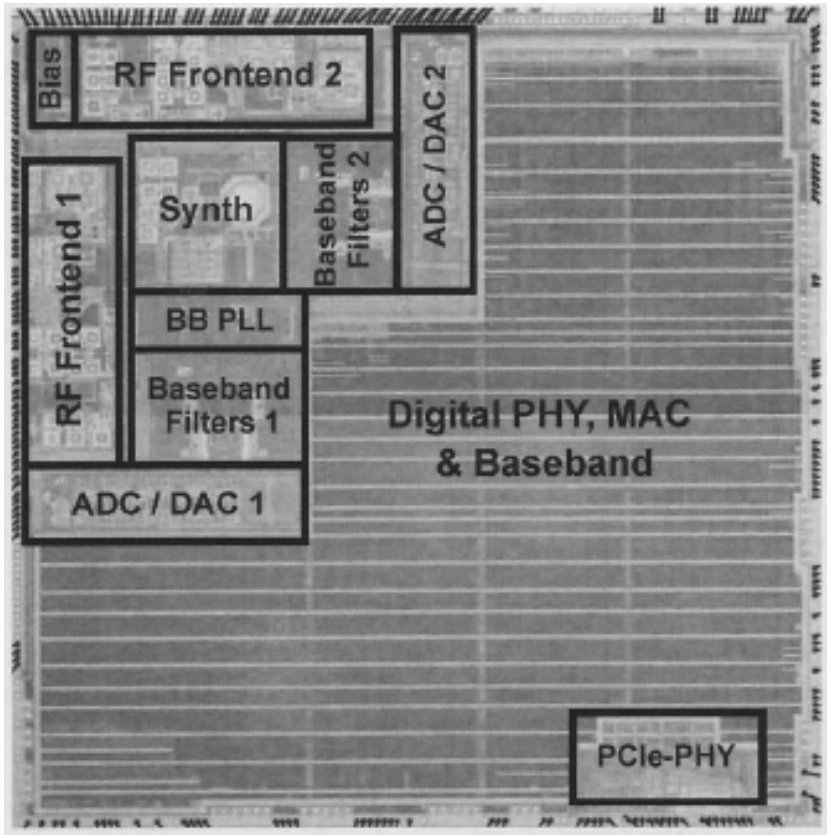


Significant reduction in system cost

Chip Comparison

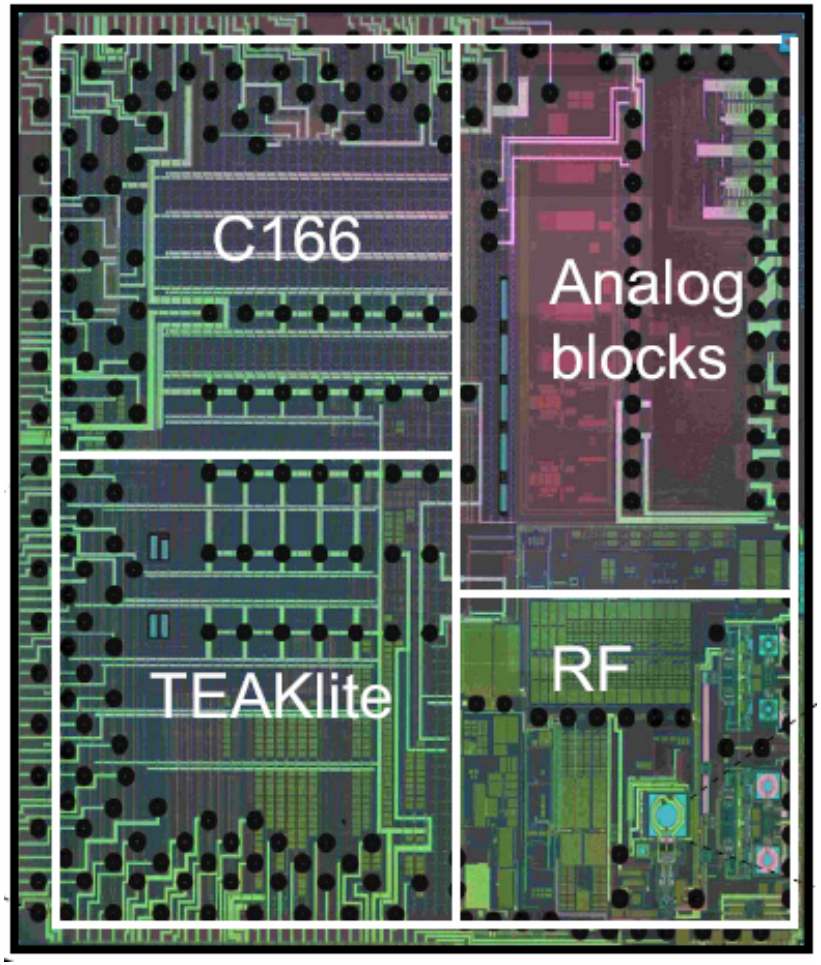


180nm 802.11abg

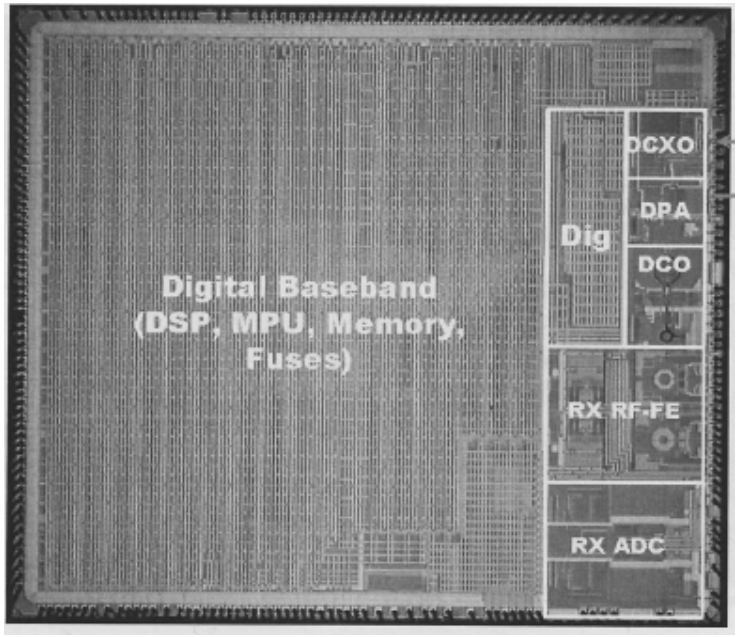


130nm 802.11n 2X2

Chip Comparison

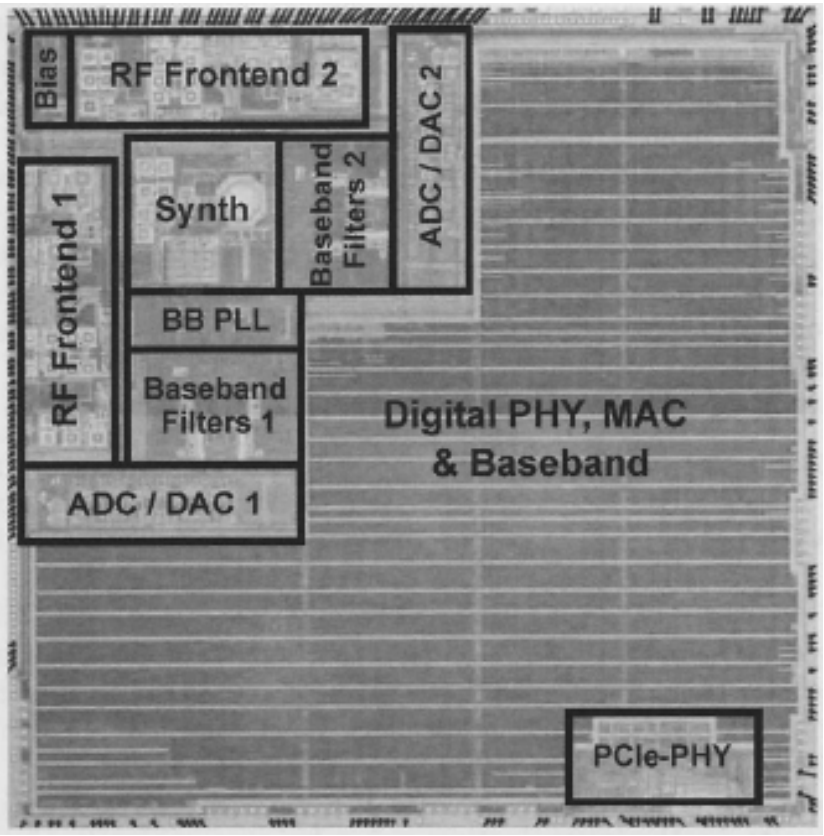


130nm GSM

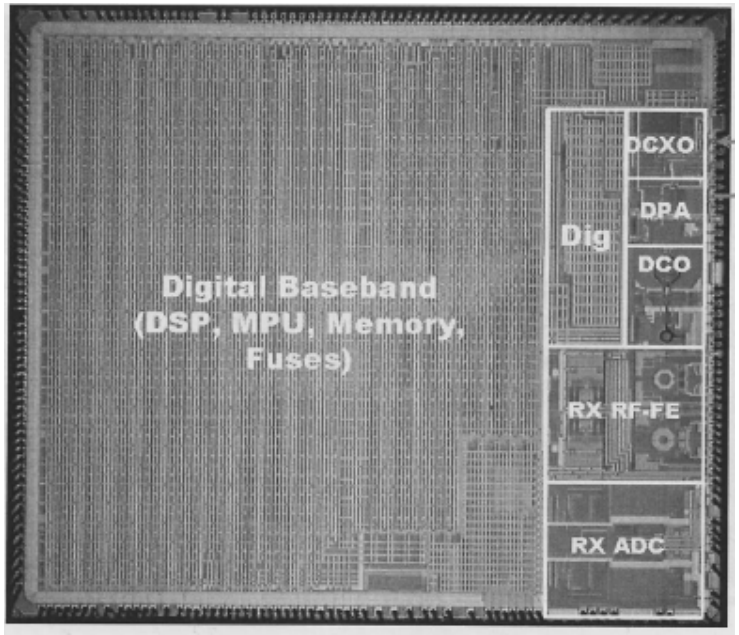


90nm GSM

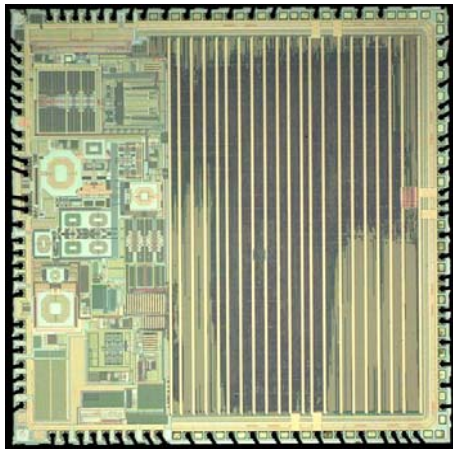
Chip Comparison



130nm WLAN 2X2 N

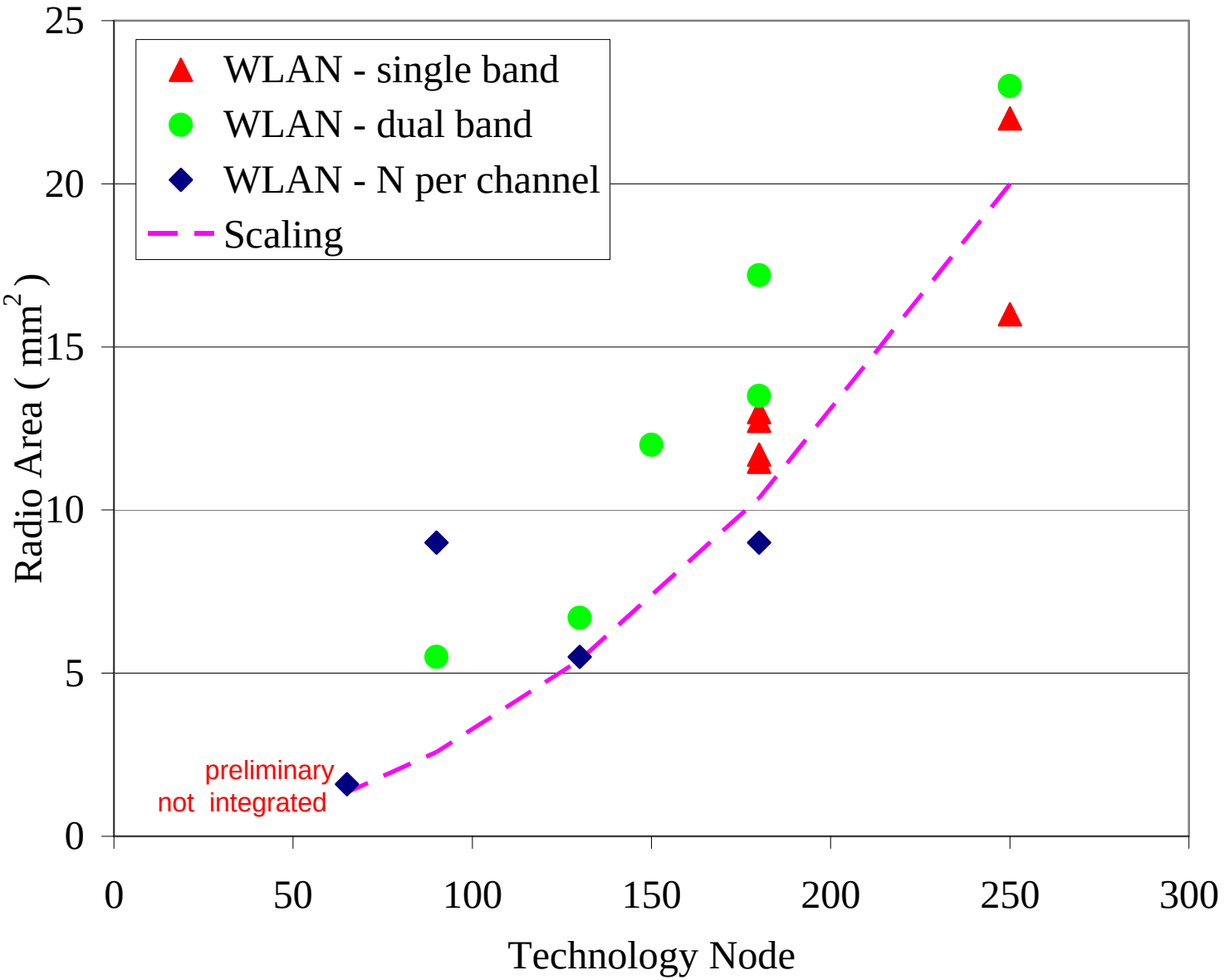


130nm GSM

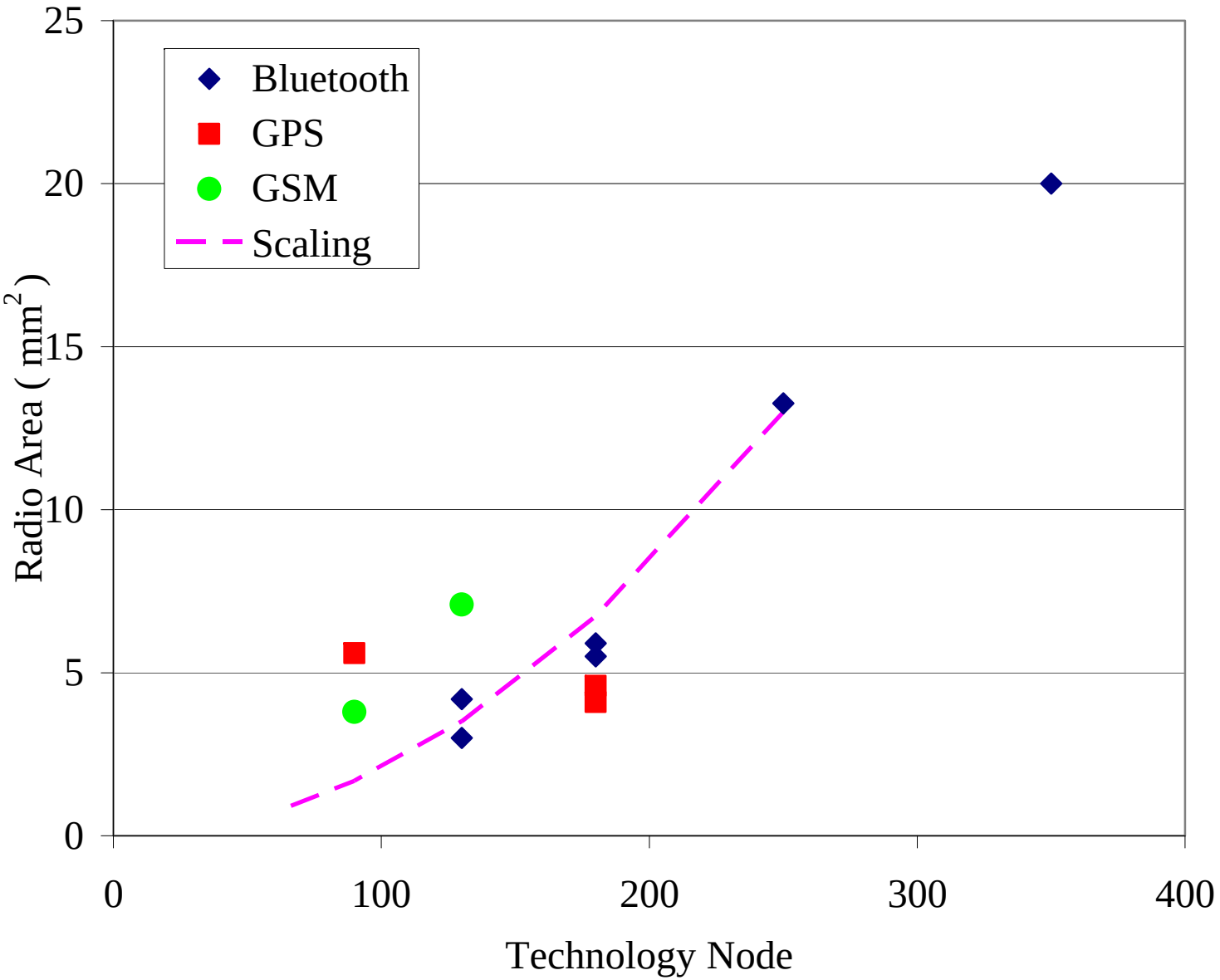


130nm Bluetooth

Radio Scaling



Radio Scaling



Conclusions

- **Scaled CMOS should improve NF and reduce power consumption; reduction in linearity and voltage capability complicates the design**
- **Advanced technology offers more options for passive components; quality of passive components may be compromised if not all metal layers are used**
- **Further Integration of off-chip components to reduce system cost**
- **Technology selection will depend on analog/digital mix**
- **Chip with mostly RF functions will scale moderately with technology**
- **Chip with largely digital functions will scale with technology**
- **Advanced technology my benefit the integration of multiple radios**