Compact Modeling and Simulation of PD-SOI MOSFETs: Current Status and Challenges

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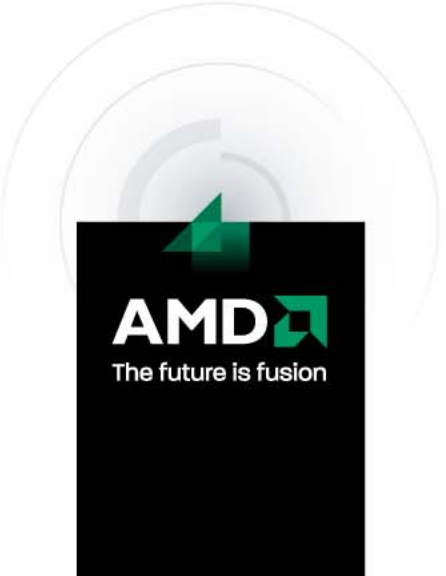


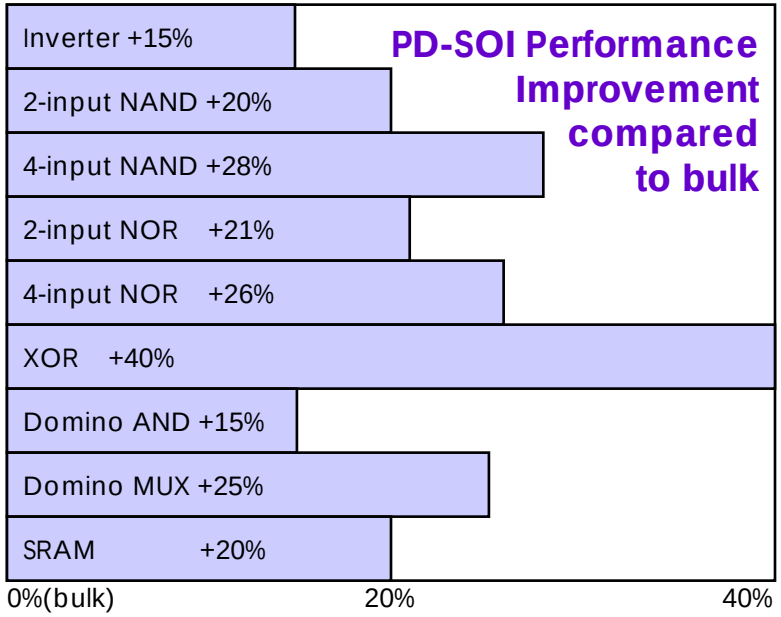
Outline

- Overview of the PD-SOI CMOS Technology
- Self-heating
- Model Parameter Calibration Flow
- Challenges in Measurement and Calibration
- Floating-Body Effects Modeling: History-Effect
- Body-Contacted Device Modeling
- Floating-Body Effects Simulation Issues
- Model Standardization
- Conclusion

History of Manufacturing PD-SOI

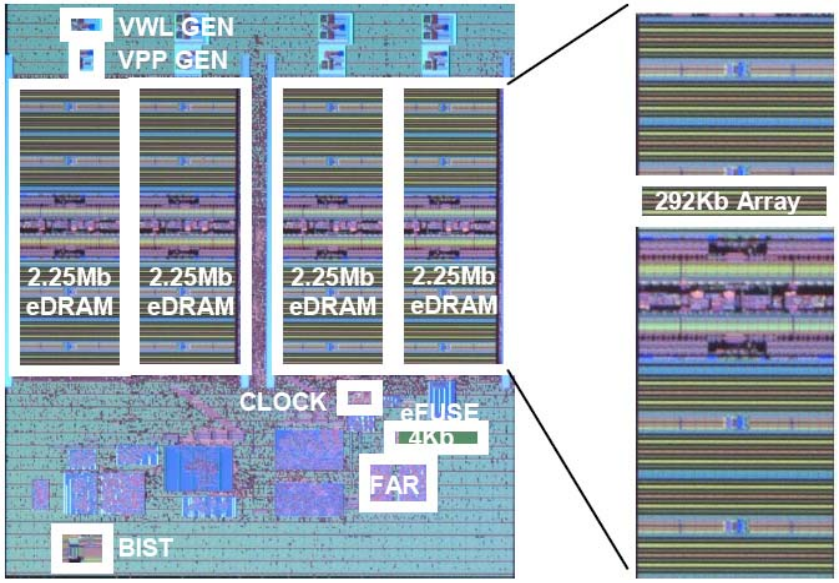
- Successfully manufactured in ULSI from the 225 nm through the 45 nm nodes

0.2um 64b PowerPC µProcessor



1999 ISSCC by D. H. Allen *et al.*

45 nm 2GHz eDRAM

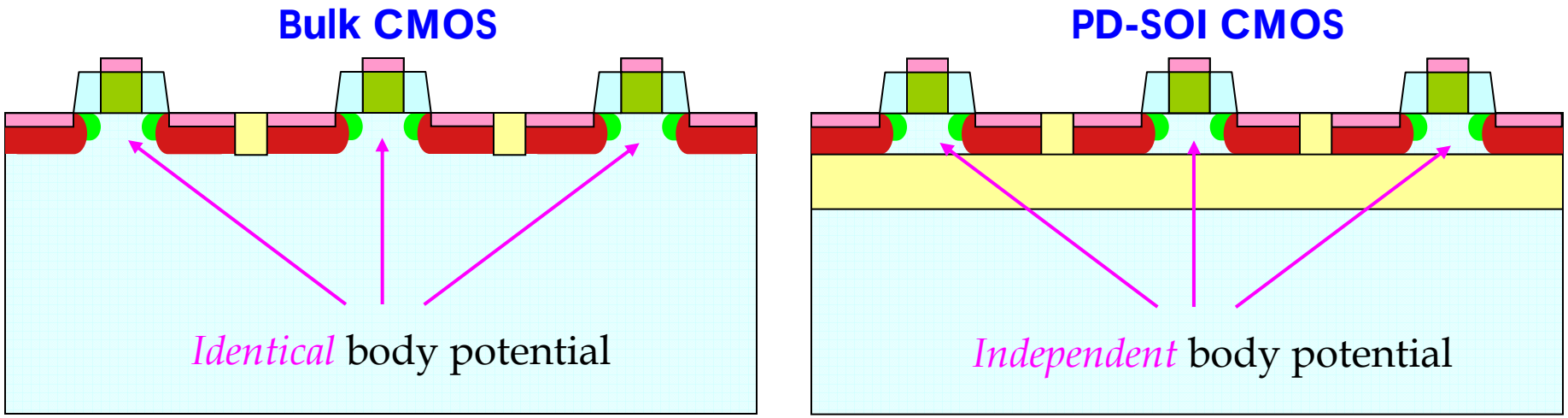


2008 VLSI Symp. by P. Klim *et al.*

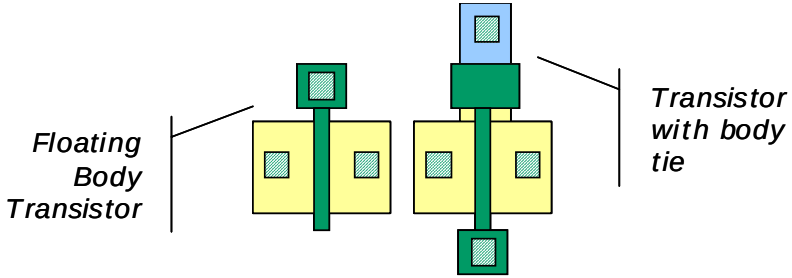
Benefits of PD-SOI CMOS

- Higher performance and lower power
  - Dynamic threshold (V_t) lowering
  - Reduced capacitive loading
  - Reduced body effects in stack transistor circuits
- Better control
  - Reduced V_t versus L_{gate} sensitivity
  - Elimination of well-implant proximity effects (WPE)
  - Natural isolation of auxiliary device elements (embedded DRAM, passives, high-voltage, and RF devices)
- Better reliability
  - Reduced soft-error rates
  - Elimination of latch-up

Bulk CMOS vs. PD-SOI CMOS

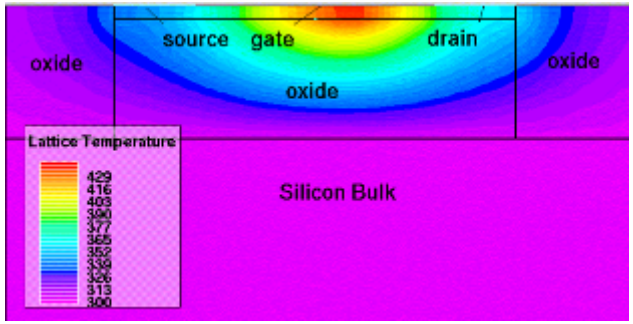


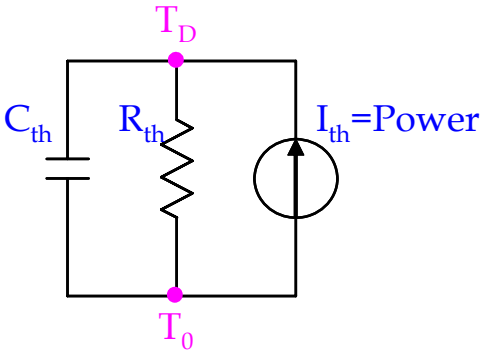
- The chief difference of the PD-SOI is that the body of each SOI transistor is an independent 4th terminal for the device
- When absolutely needed, the body can be fixed to a chosen potential with a body tie

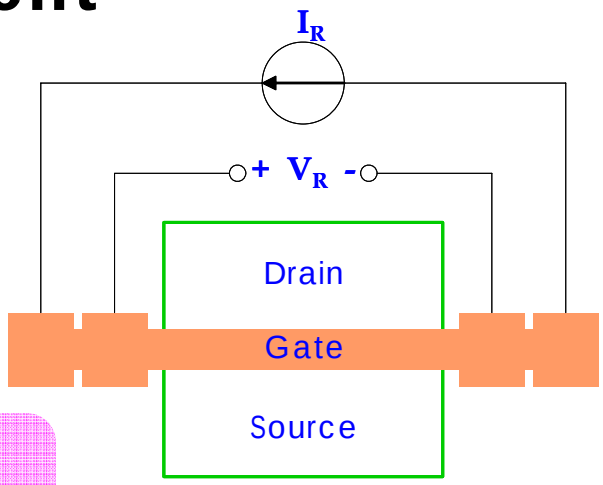


- However, in 99.9% of the chip, transistors will be operating as floating body devices

Self-Heating: DC R_{th} Measurement

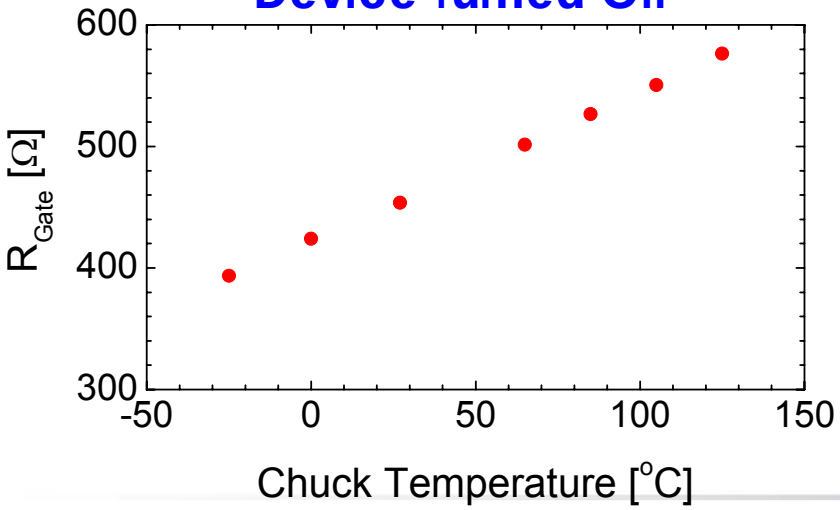




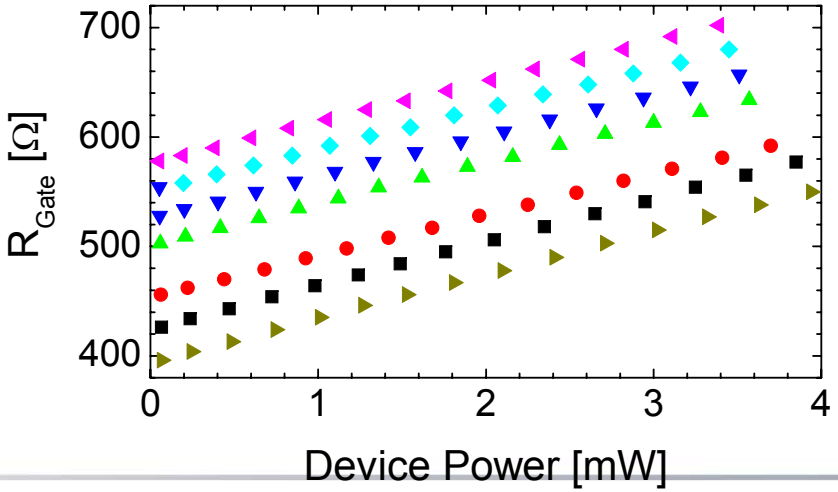


$$R_{th} = \frac{dT}{dPower} = \frac{dT}{dR_{Gate}} \times \frac{dR_{Gate}}{dPower}$$

Device Turned Off

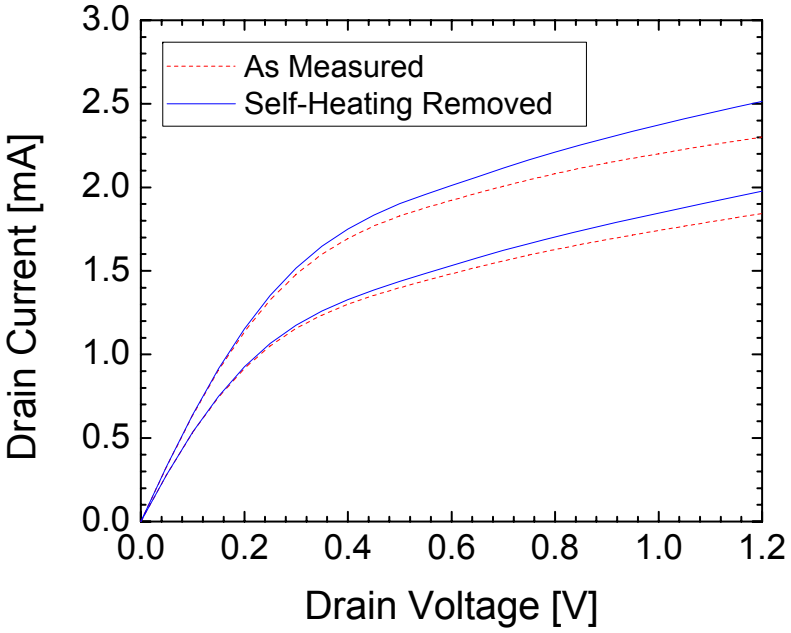


Device Turned On

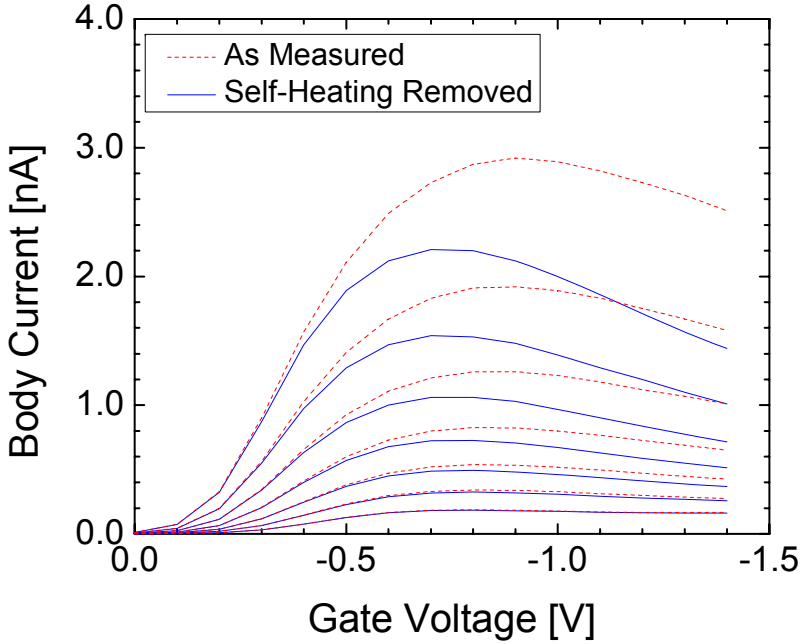


Self-Heating Removal

Channel Current

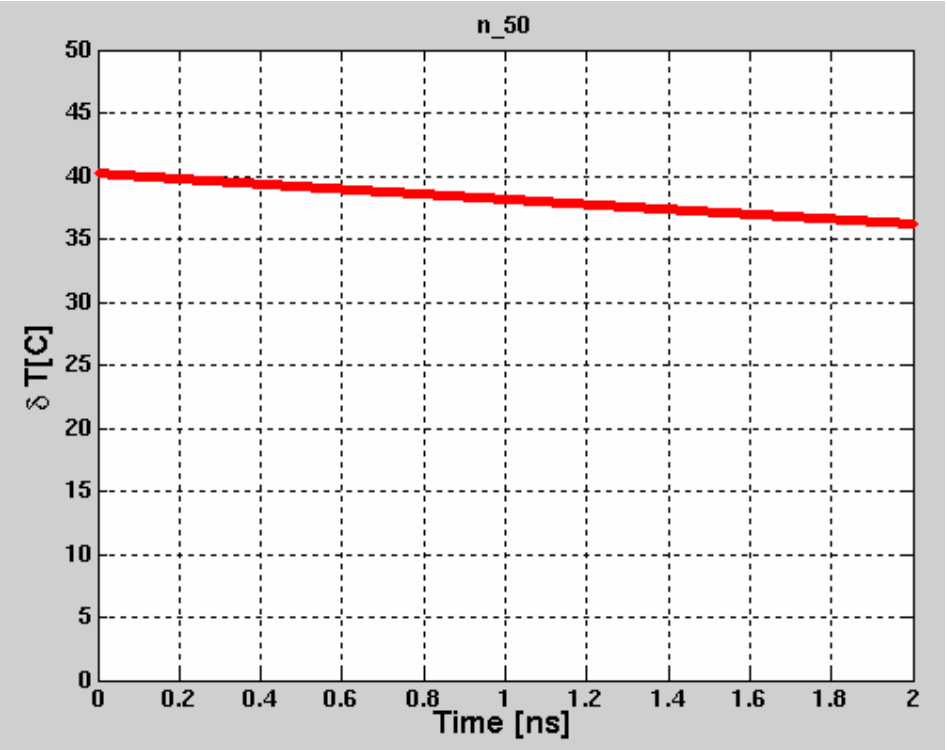


Parasitic Current



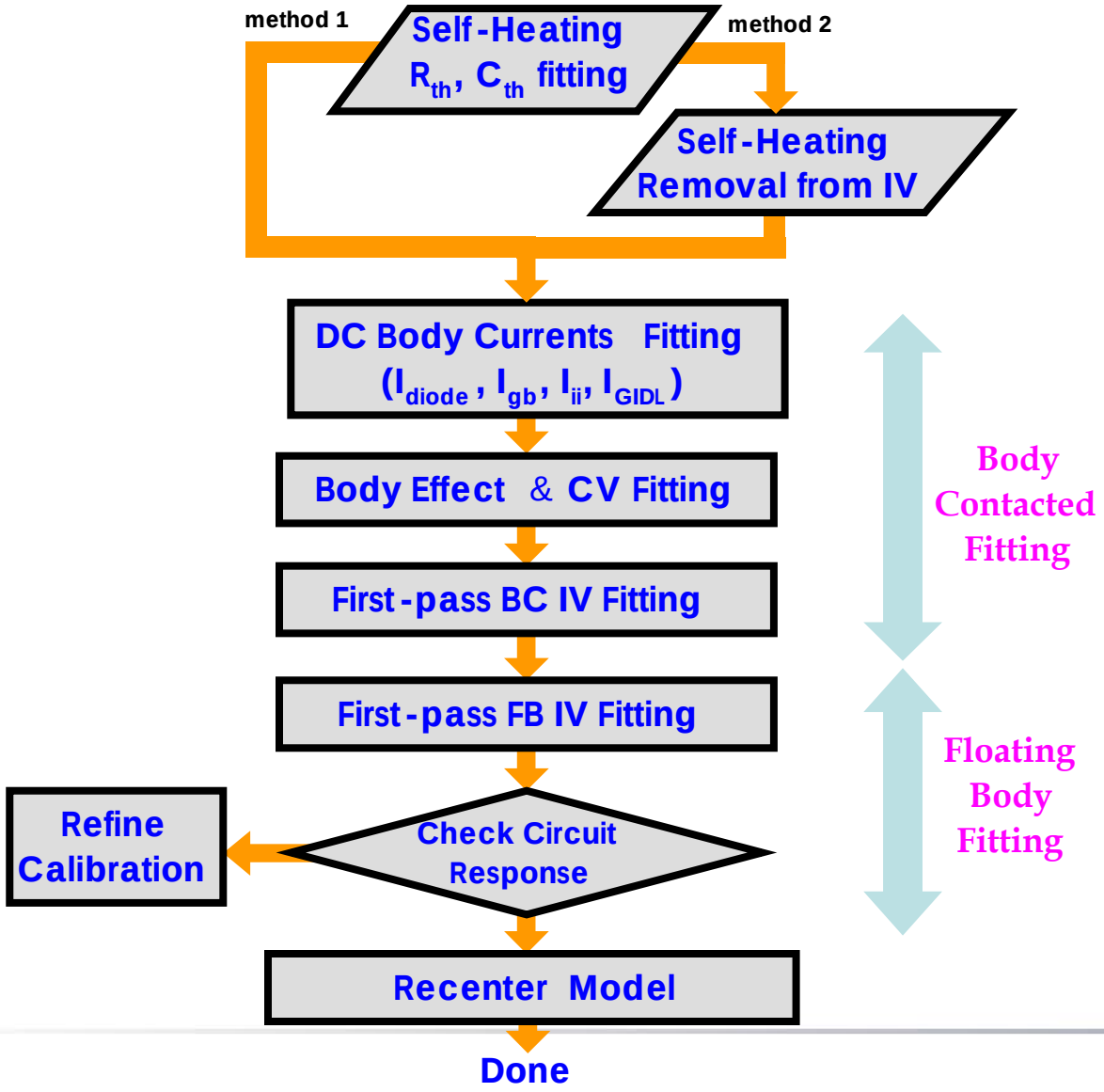
- Based on measured temperature dependence of the current
  - Linear
  - Quadratic
  - Exponential

Self-Heating during Simulation

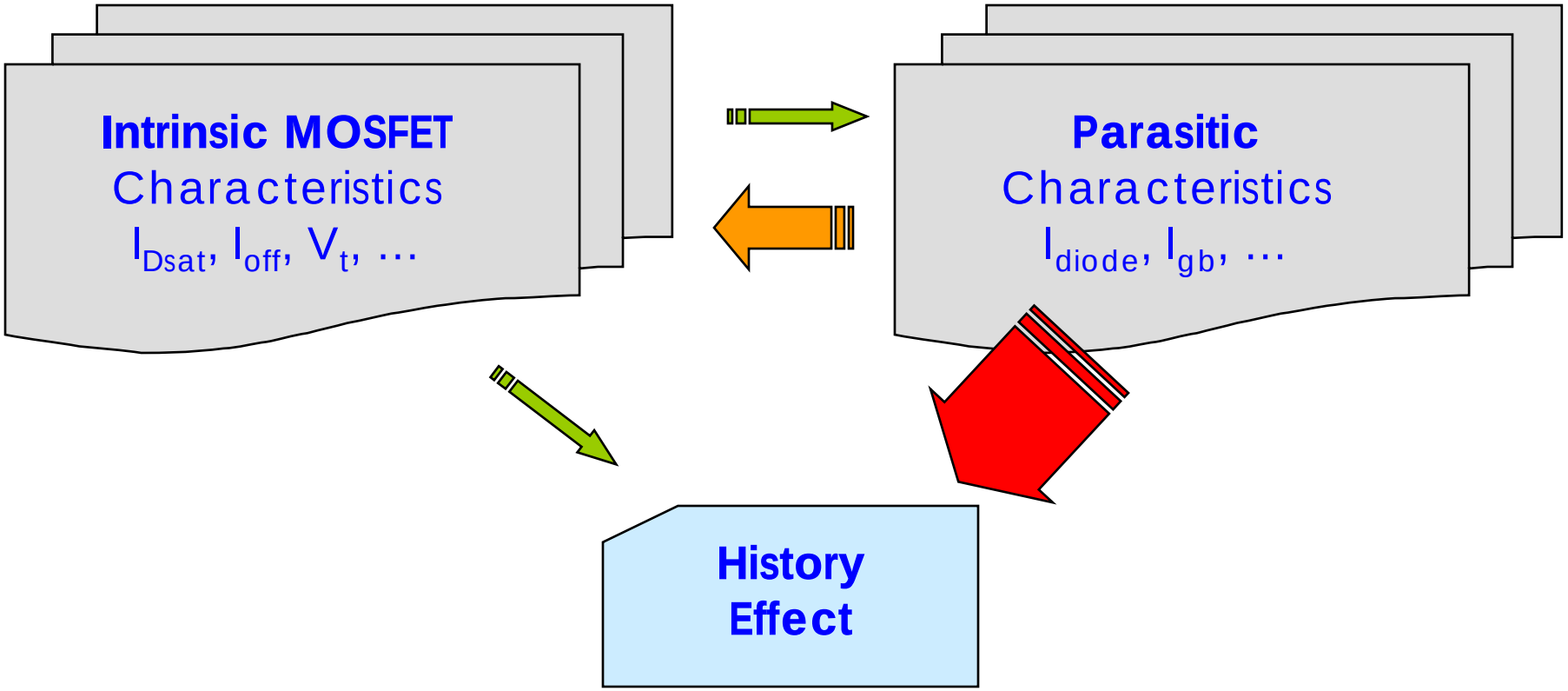


- Addition of temperature node leads to simulation time increase, and, possibly, convergence issue
- Can disable self-heating mode for many high-performance logic products
  - Switching time is much faster than the thermal time constant
  - Most analog blocks are operating at low enough bias range

PD-SOI Model Parameter Calibration

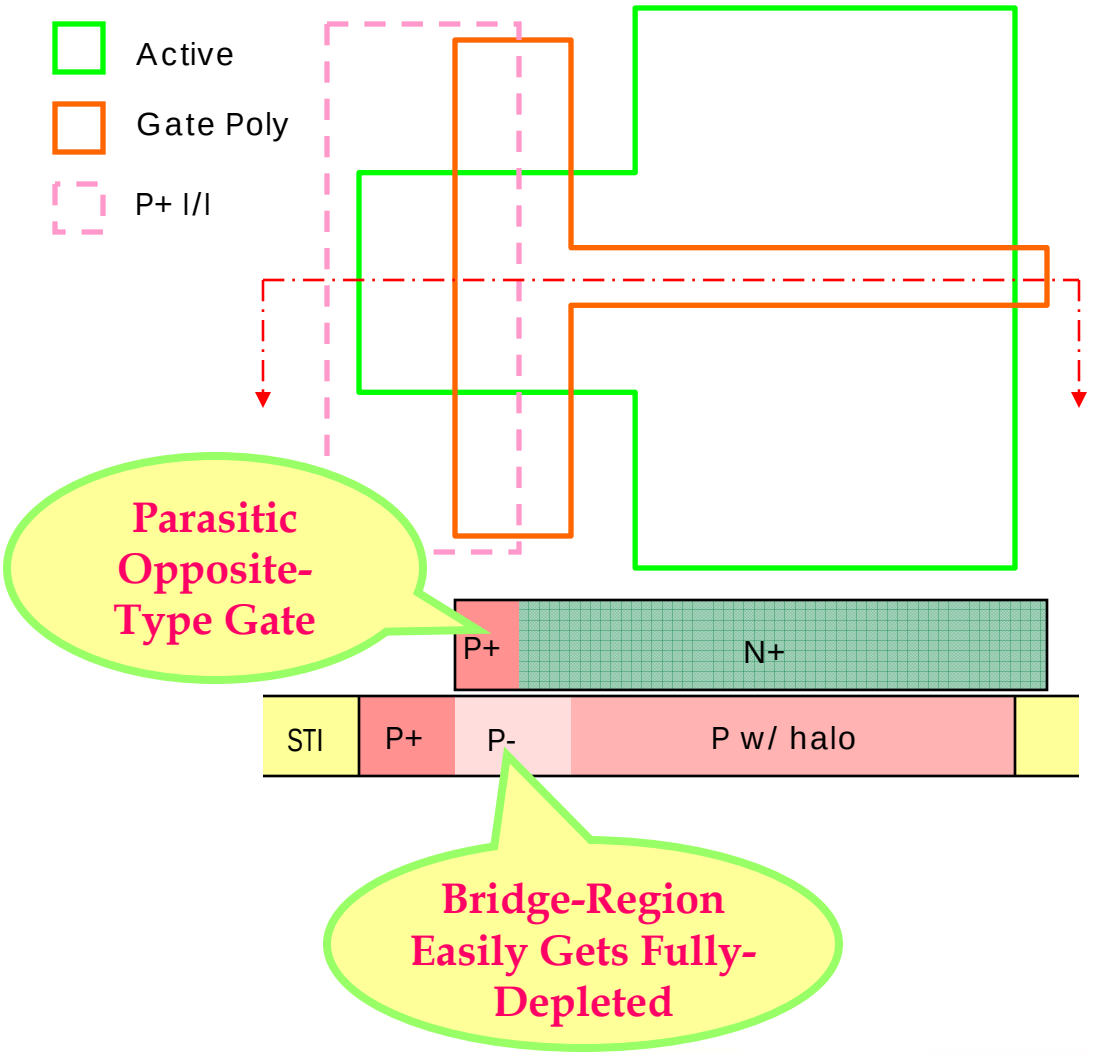


Do History-Effect Modeling First!

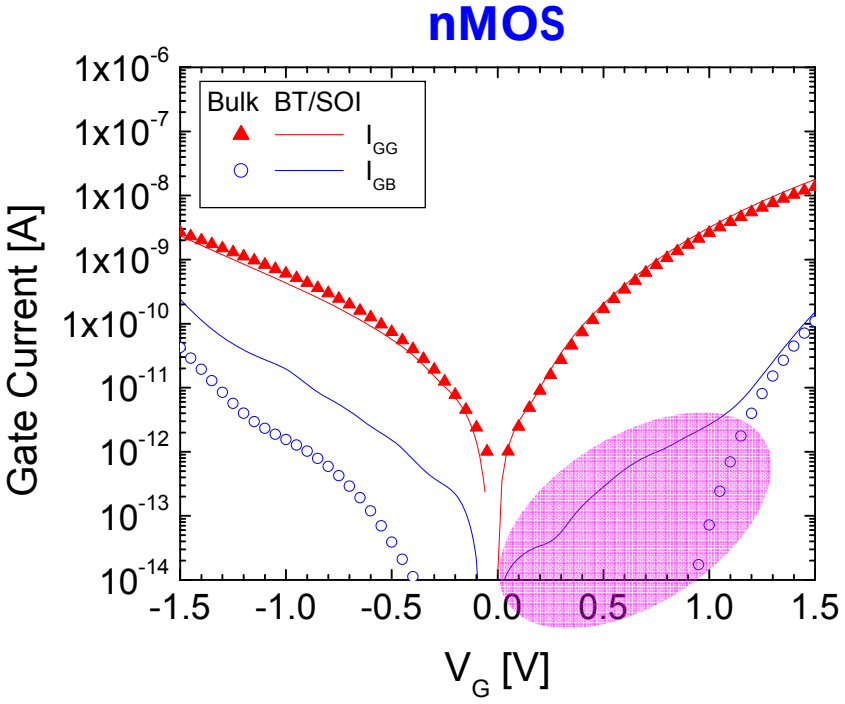


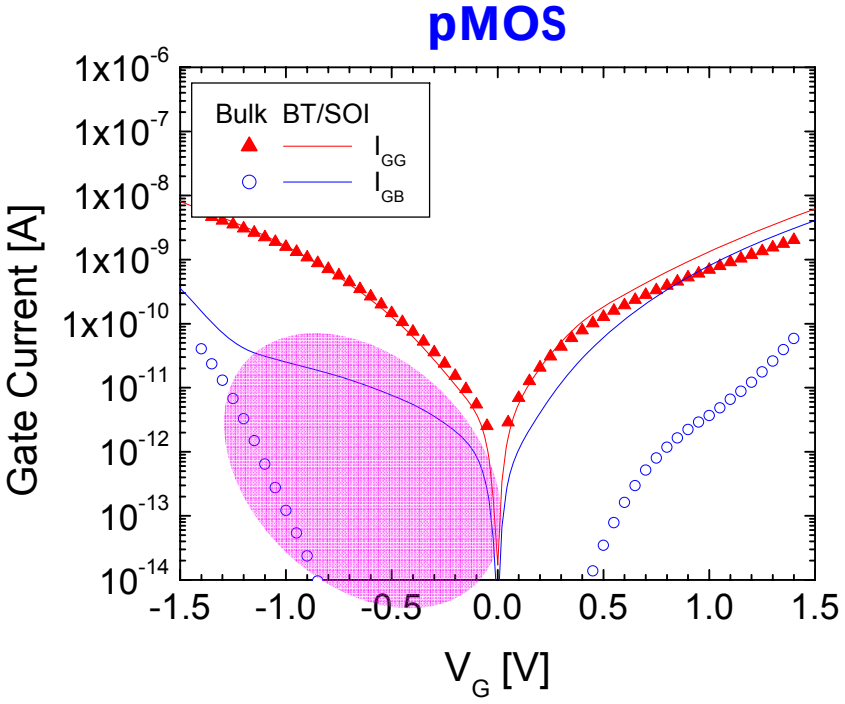
- Intrinsic MOSFET characteristics have only small impact on history effect
  - Except for the body-effect
- Adjusting parasitic characteristics have huge impact on history effect and cause noticeable change in channel current

Challenges in Measurement & Calibration



Parasitic Opposite-Type Gate

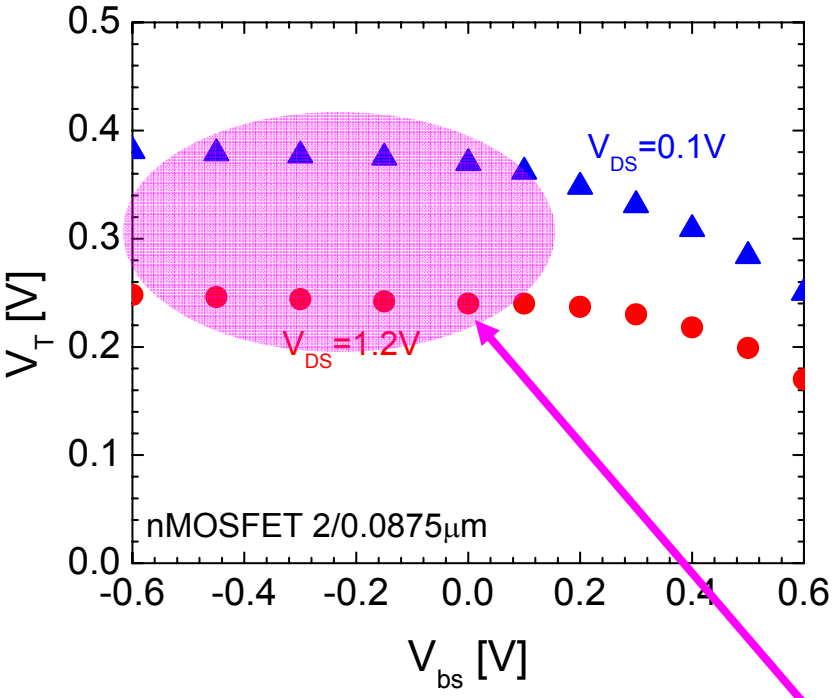




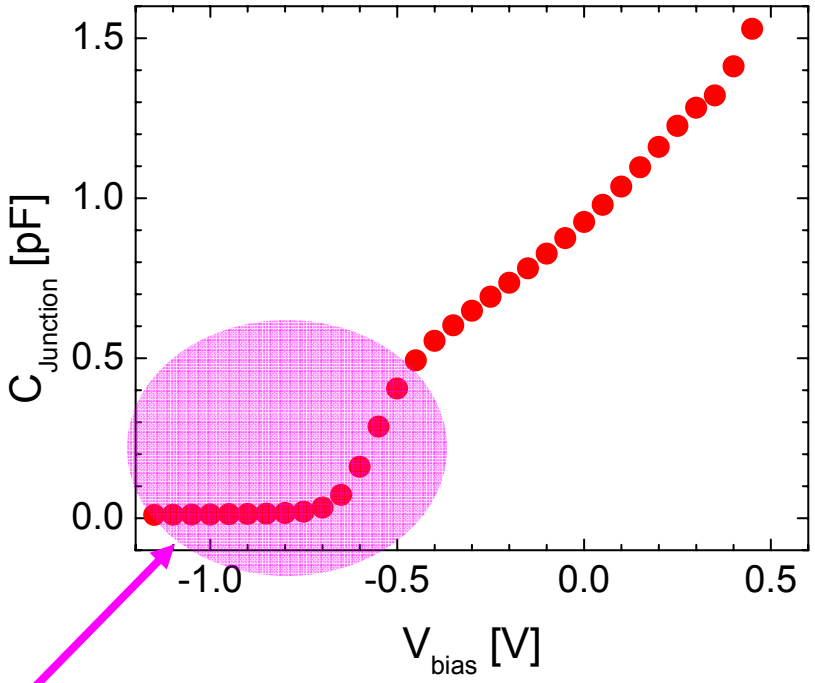
- Big discrepancy in I_{gb} characteristic due to the parasitic
  - Especially in inversion region
- Solutions:
  - Selectively use specific regions
  - Use bulk wafer

Fully Depleted Body

Body-Effect



Junction Capacitance

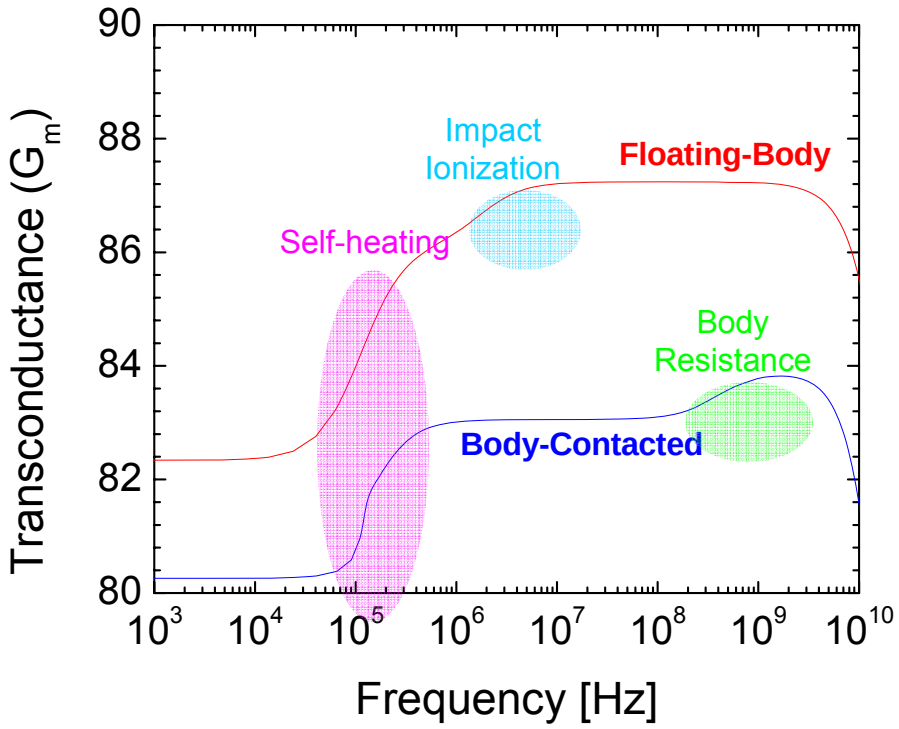


- Body bias can cause a fully-depleted body DBS1
- Low-doped bridge region can introduce artifacts in measured data
- Solutions:
  - Selectively use specific regions
  - Emphasize intrinsic response

Slide 13

DBS1 I cannot change this graphic image, but it should not be hyphenated because the ly in fully = the hyphen in this use
David B. Schlosser, 9/13/2008

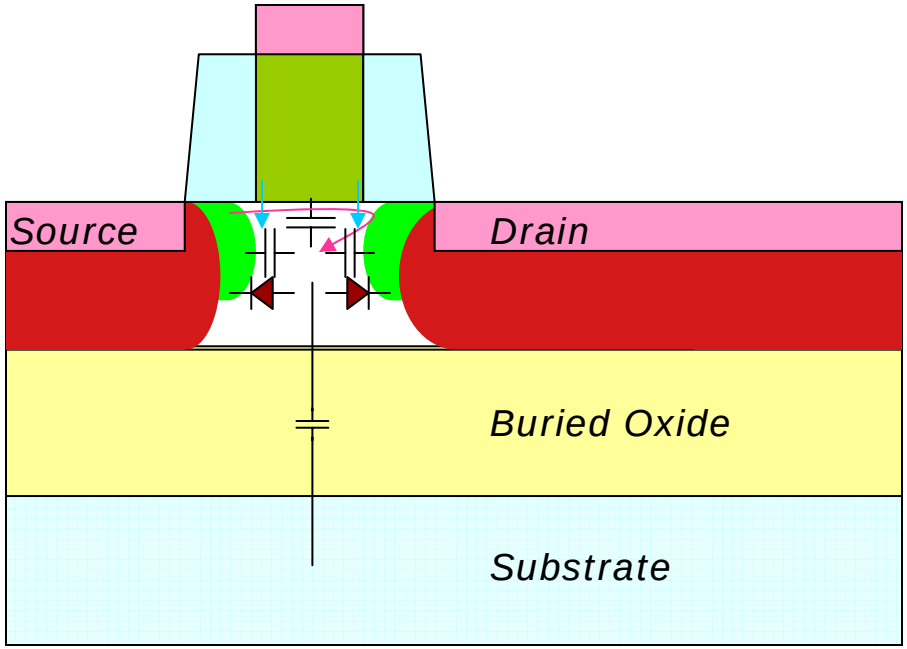
Implicit Calibration using RF Data



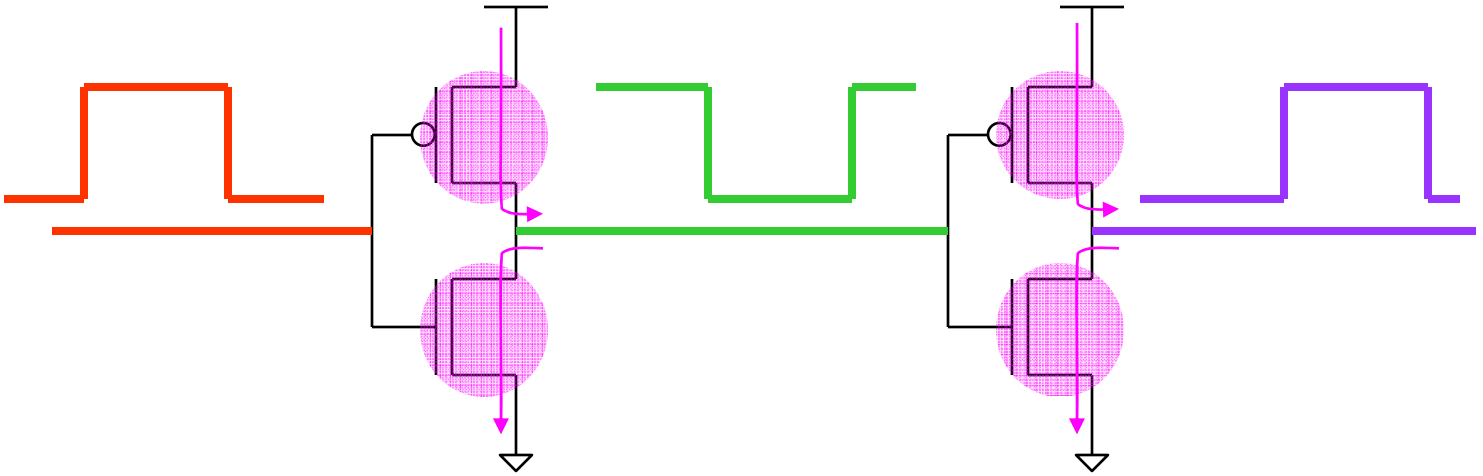
- RF measurement offers much implicit information:
  - Self-heating response time
  - Impact ionization
  - Body-contact time constant

What Causes Floating-Body Effect?

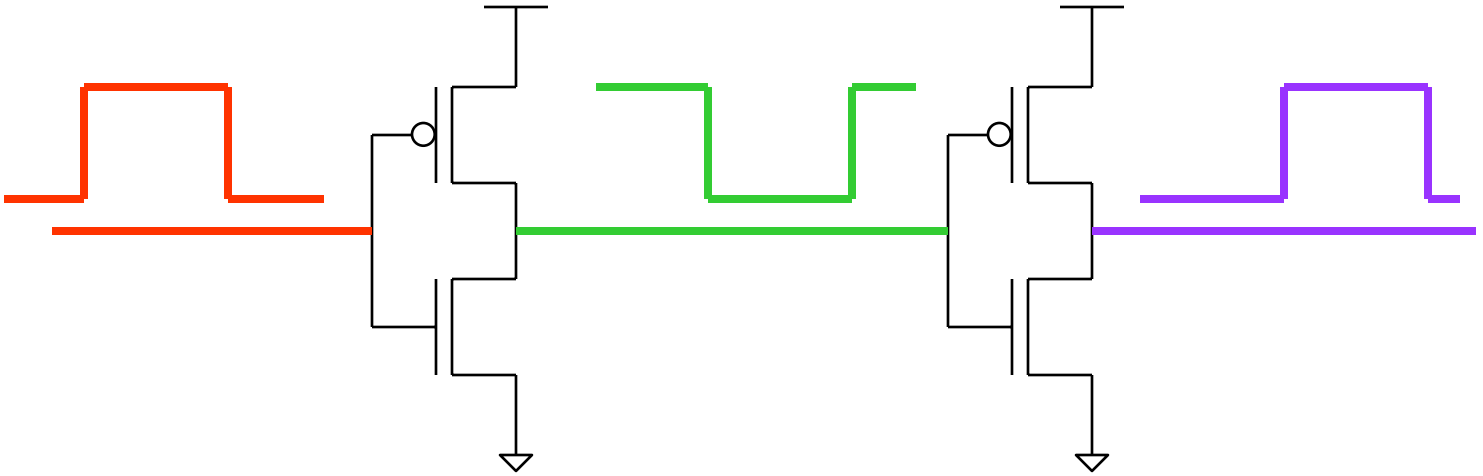
- Body potential is a function of:
  - Capacitive coupling to
    - Source
    - Drain
    - Gate
    - Substrate (small)
  - Diode leakages to
    - Source
    - Drain
  - Gate leakage
  - Impact ionization
- Also subject to the previous *switching history*



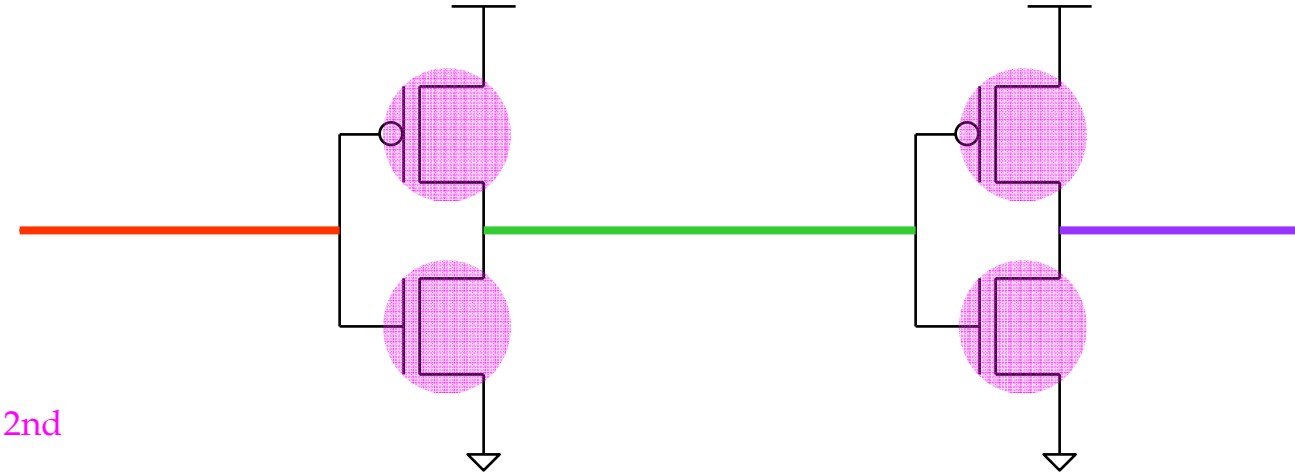
CMOS Inverter Operation

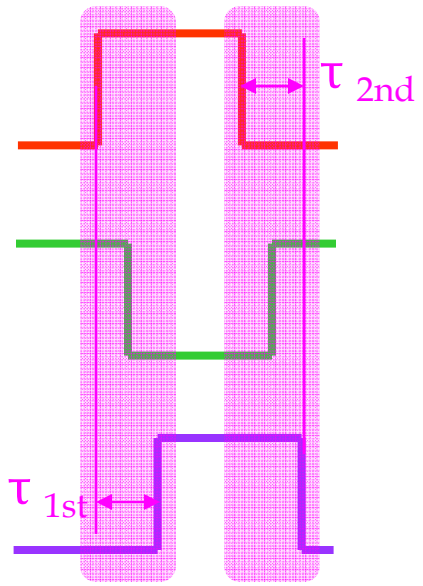


Definition of History-Effect



Definition of History-Effect





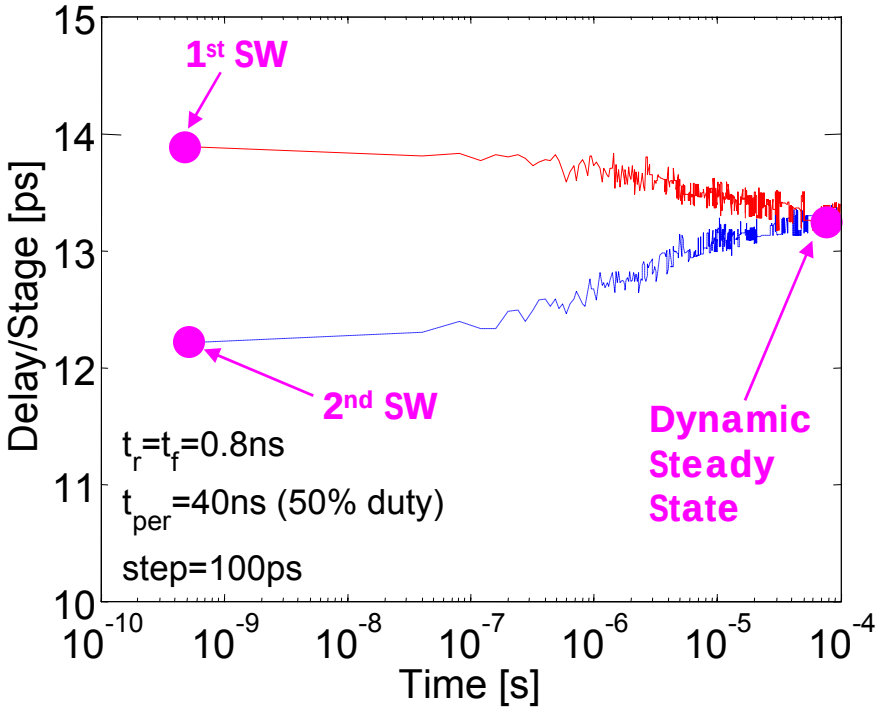
History-effect

$$H = (\tau_{1st} - \tau_{2nd}) / \tau_{2nd}$$

- 1st switch : input transition after being held constant for a long time
- 2nd switch: input transition short time after the 1st switch

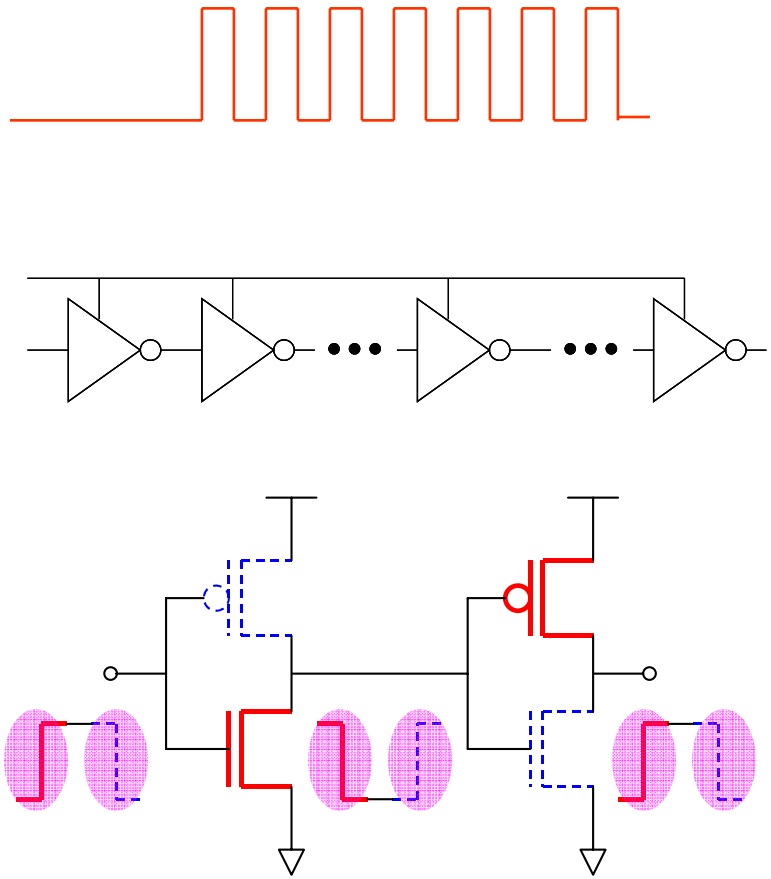
Typical History-Effect

Evolution of Switching Delay

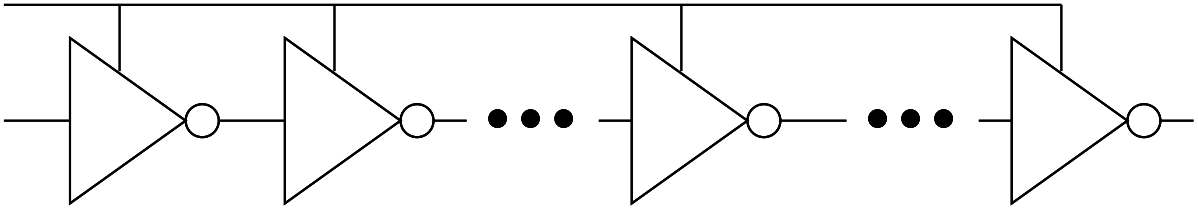


- Delay is subject to switching history of the logic gate

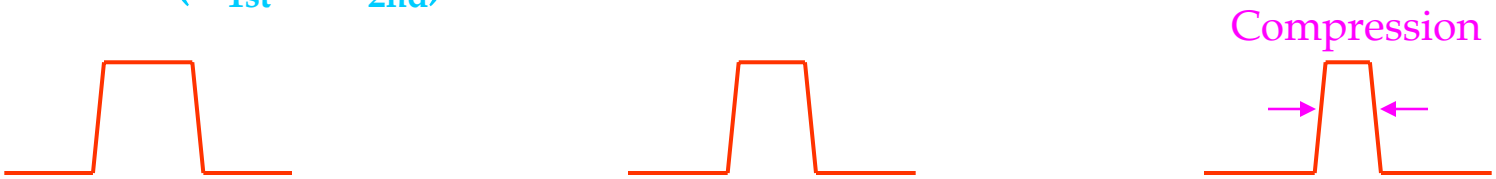
Input Clock Shape



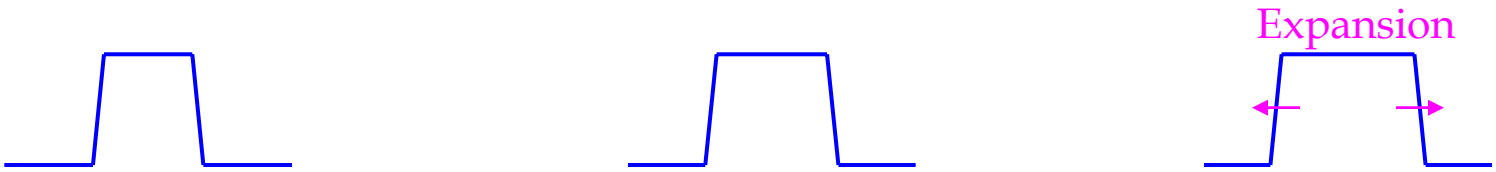
Pulse Compression vs. Expansion



Positive H ($\tau_{1st} > \tau_{2nd}$)

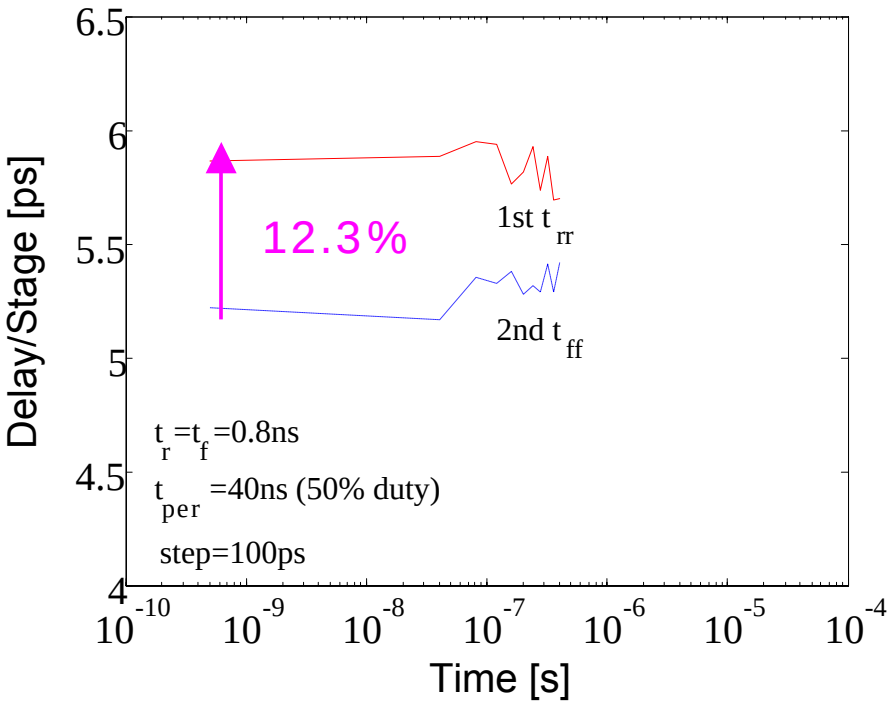


Negative H ($\tau_{1st} < \tau_{2nd}$)

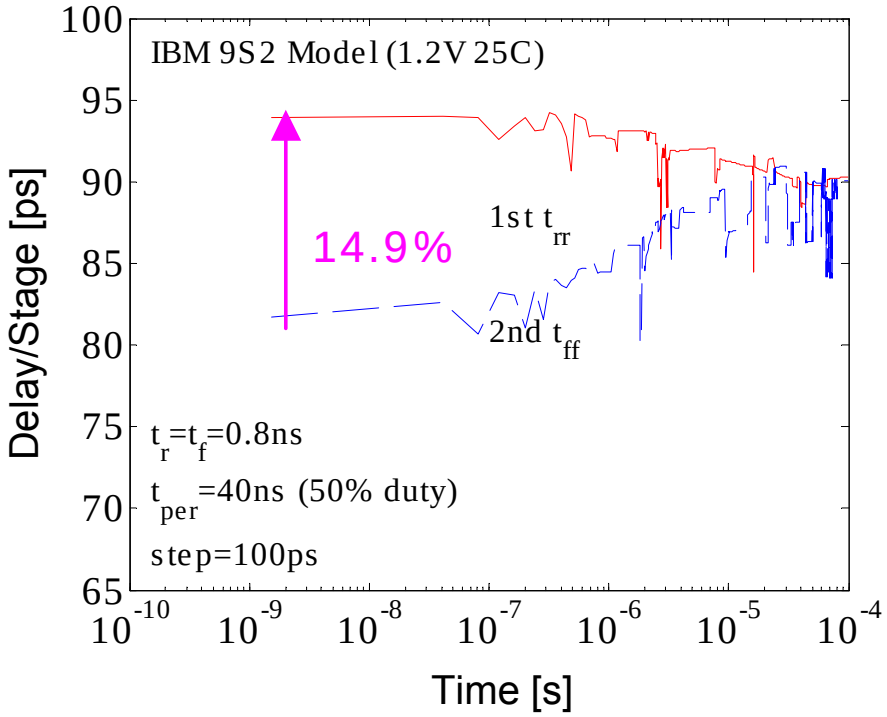


Impact of Loading on History-Effect

Unloaded

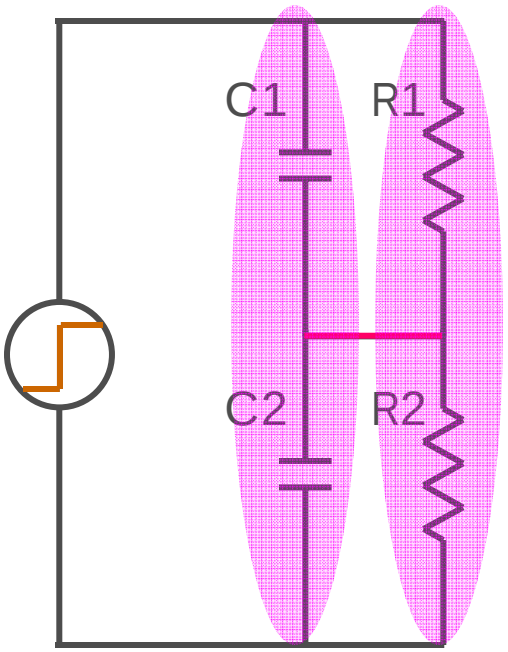


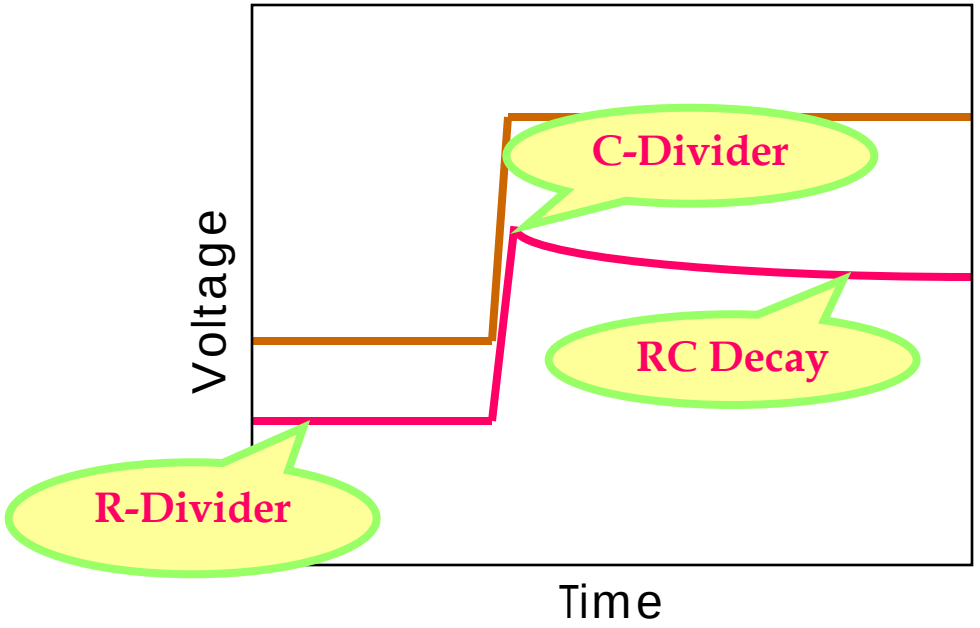
Heavily Loaded



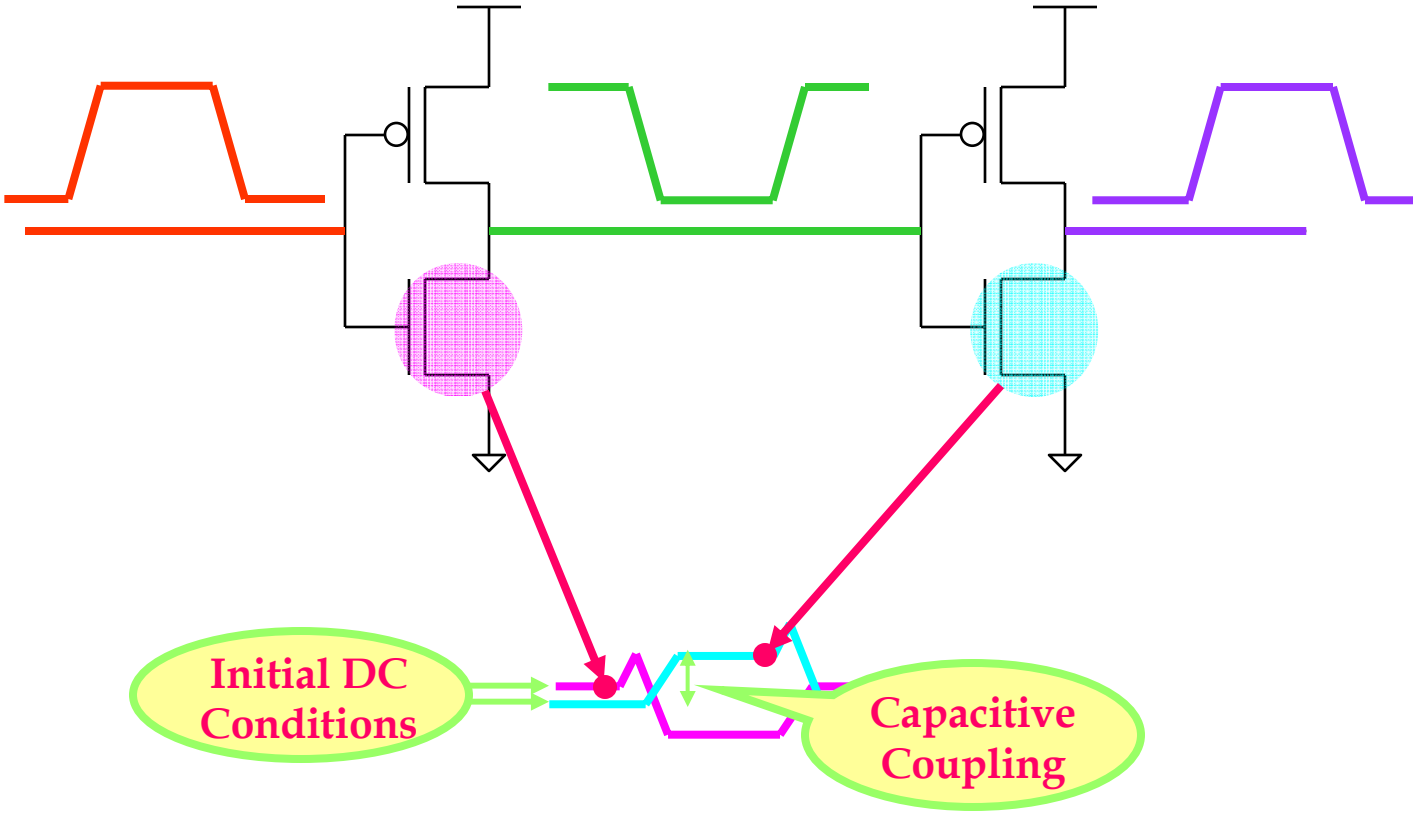
- Very limited impact of loading capacitance
  - Extremely large loading (100fF) -- changing switching delay by ~15X
  - Only changes ~2% in history-effect

Combined Capacitive/Resistive Network



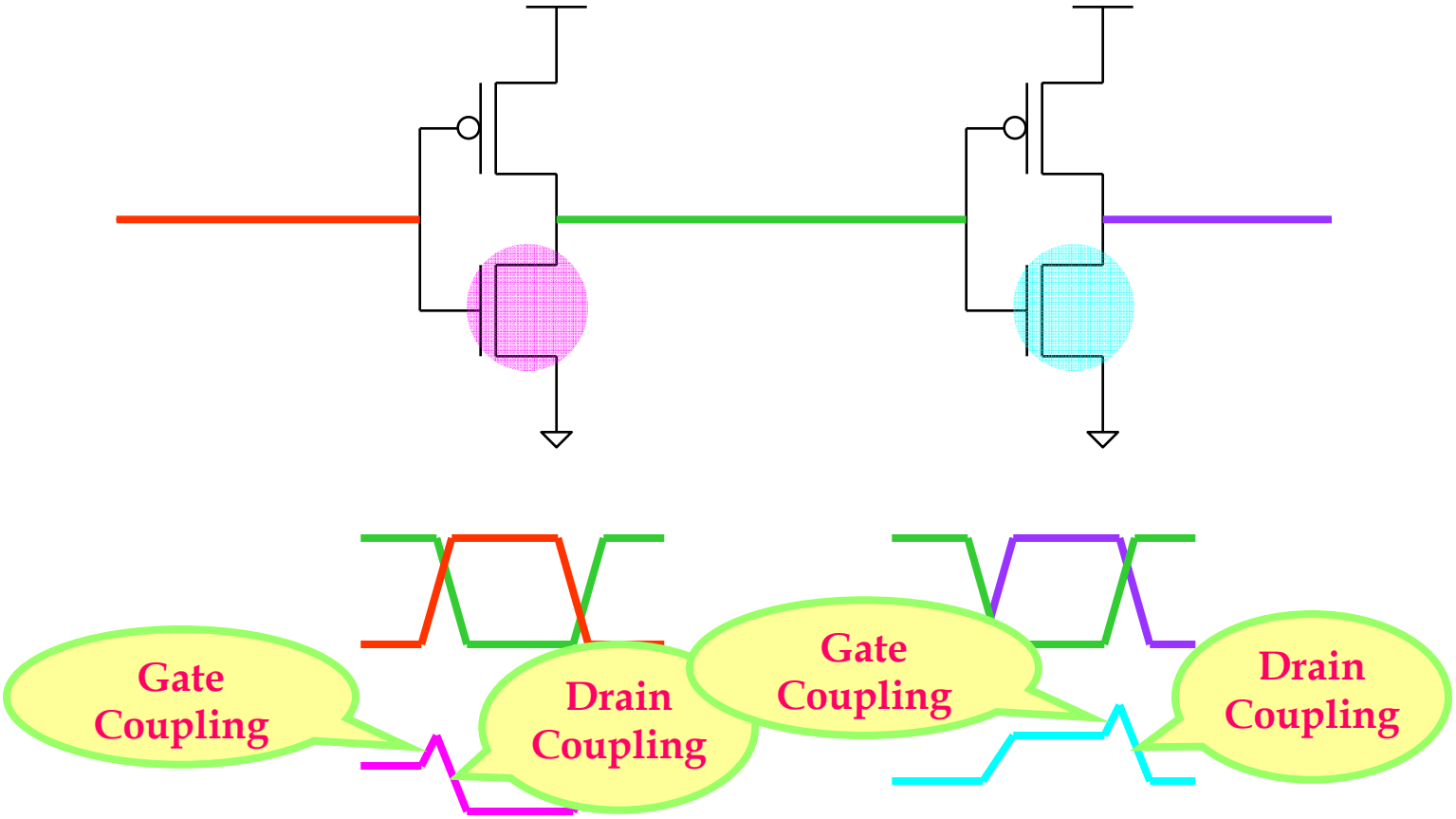


Time for Actual Contribution to Speed



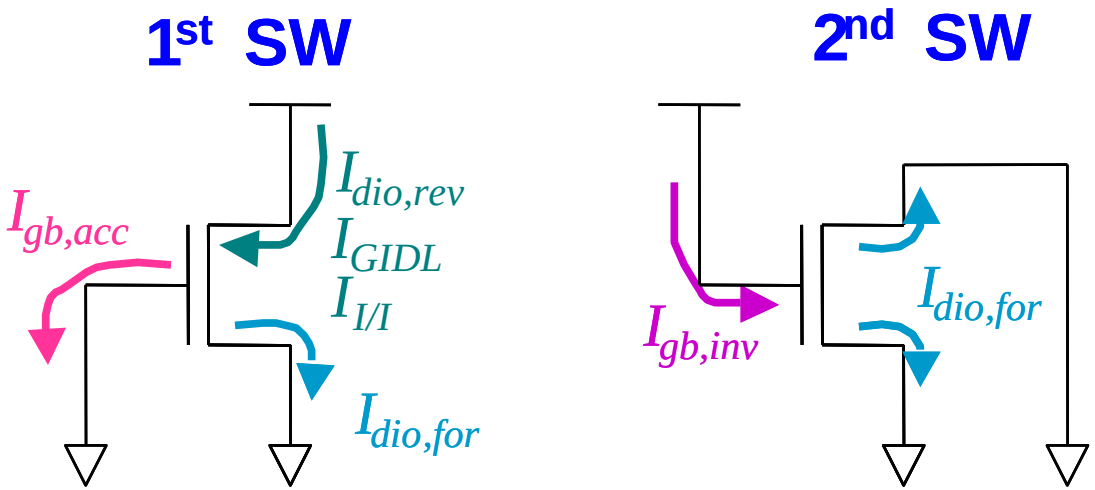
- 1st SW : Initial DC
- 2nd SW : Initial DC + Capacitive Coupling

Capacitive Coupling



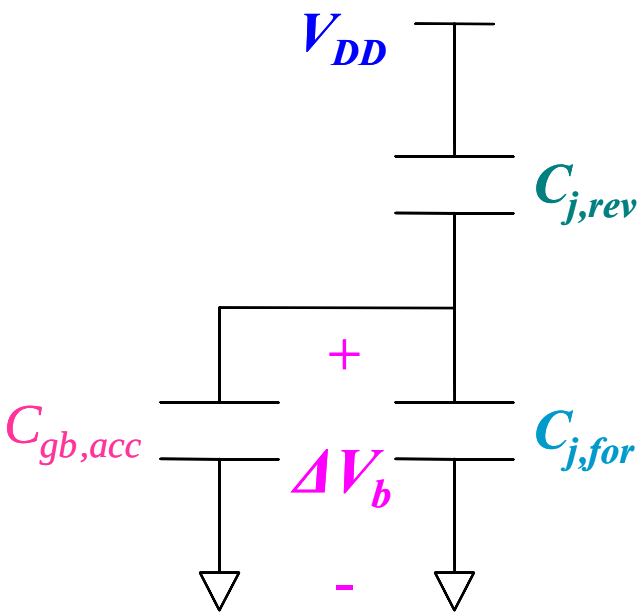
- Capacitive coupling is stronger to drain than to gate

Key Components (Initial DC Condition)



- 1st SW Initial
  - KCL balance between forward and (reverse I_{diode}+I_{GIDL}+$I_{I/I}$)
  - Accumulation I_{gb} is much smaller than forward I_{diode}
- 2nd SW Initial
  - KCL balance between forward I_{diode}*2 and inversion I_{gb}

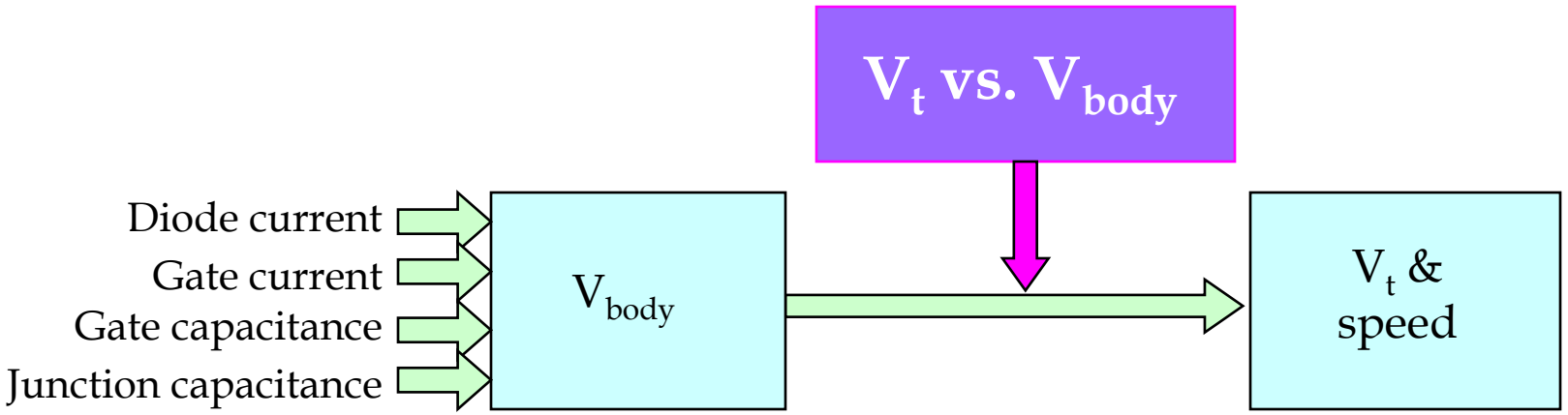
Key Components (Capacitive Coupling)



$$\Delta V_{bs} = V_{DD} \frac{C_{j,rev}}{C_{gb,acc} + C_{j,for} + C_{j,rev}}$$

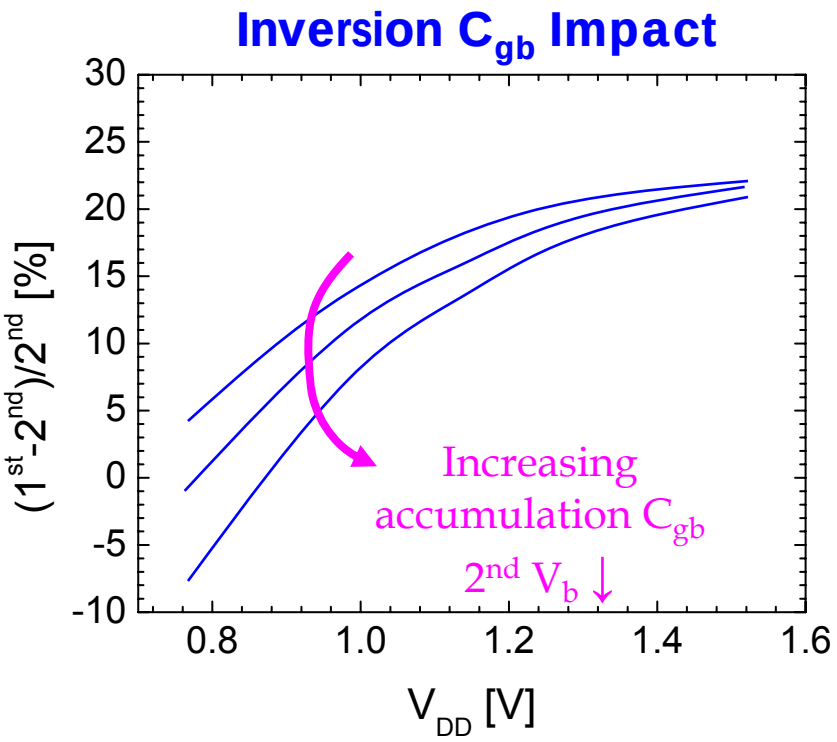
- Basically a voltage-divider that consists of
  - Gate-body capacitance, and
  - Junction capacitance

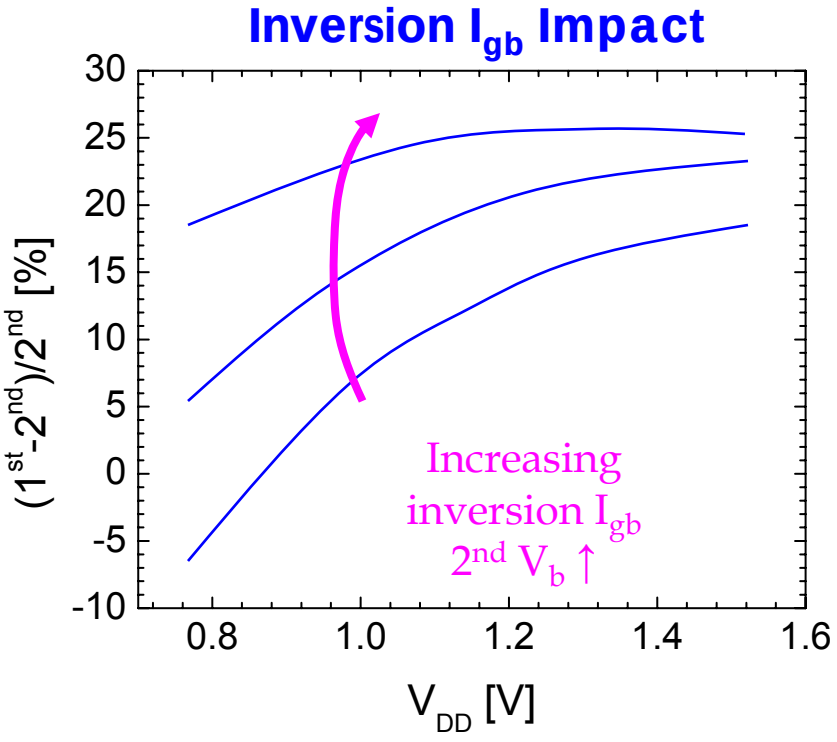
Key Components (Body-Effect)



- Body potential is established mostly by diode and gate characteristics (DC and AC)
- This body potential is translated into the actual switching performance by the body-effect (the main transfer function)

Impact of Gate Capacitance & Current

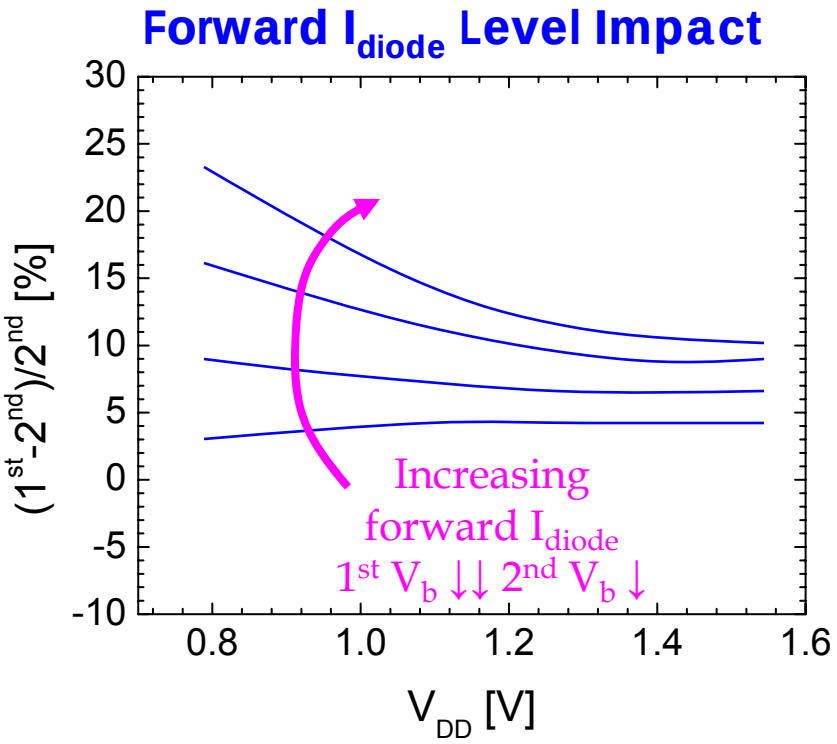


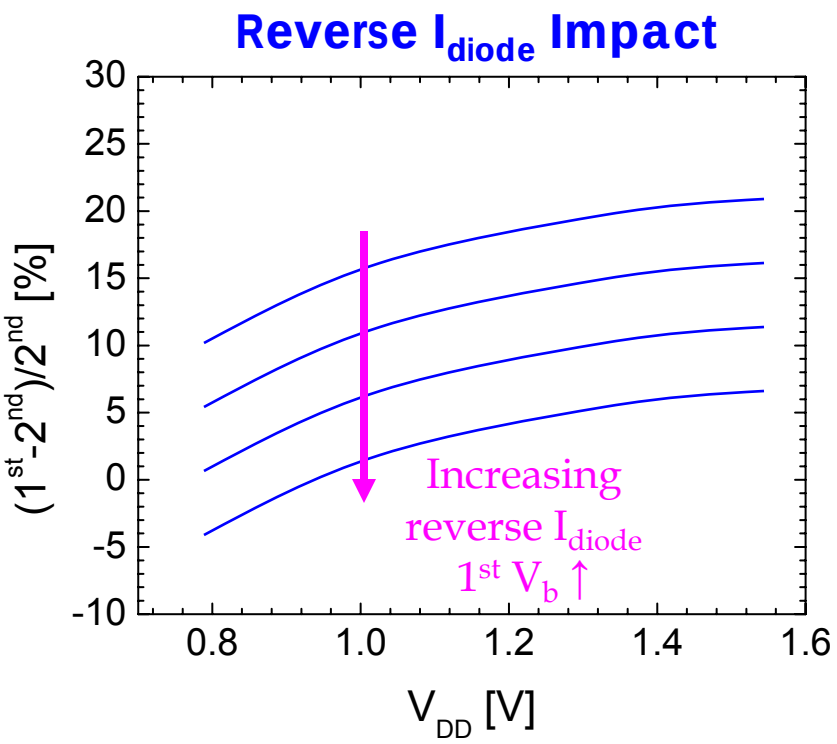


- C_{gb} is critical for V_{DD} dependence slope
- I_{gb} became a major factor from 90 nm technology onward

$$\downarrow \Delta V_{b,2nd} = V_{DD} \frac{C_{db}}{C_{gb} + C_{sb} + C_{db}} \uparrow$$

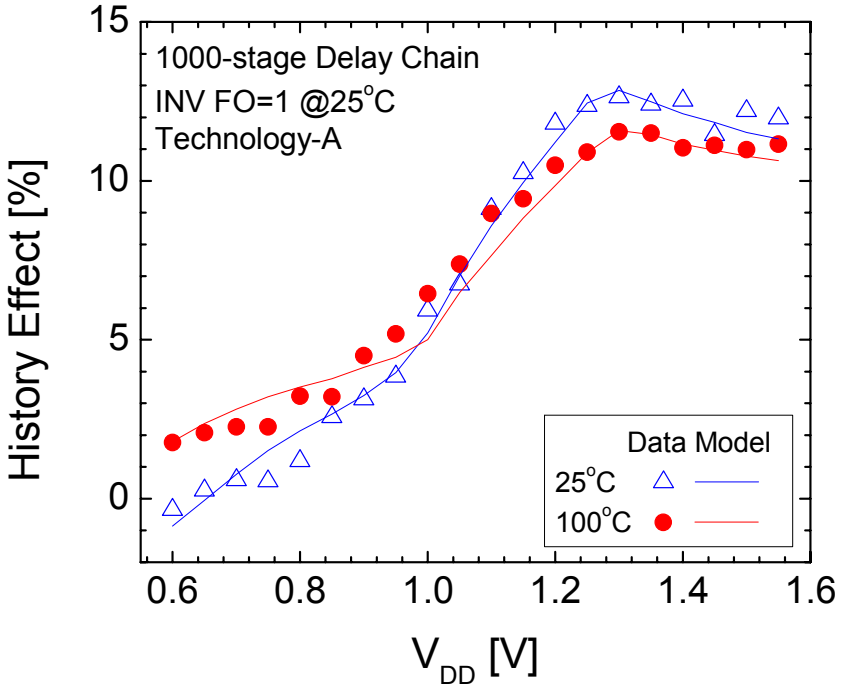
Impact of Diode Current





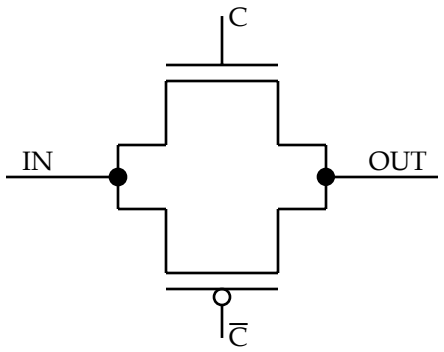
- The diode current characteristic is the key characteristic dominating the V_{DD} and temperature dependences of the history-effect
  - Proportional to forward I_{diode}
  - Inversely proportional to reverse I_{diode}

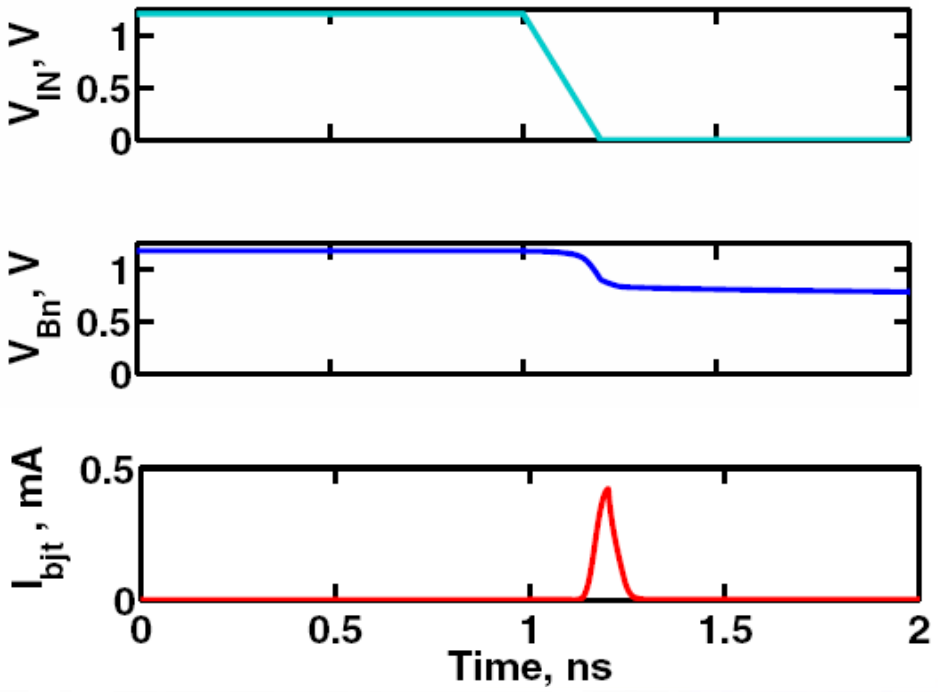
Final Reproduction of History-Effect



- The measured history-effect can be successfully reproduced across a wide range of conditions when all the key components are properly modeled

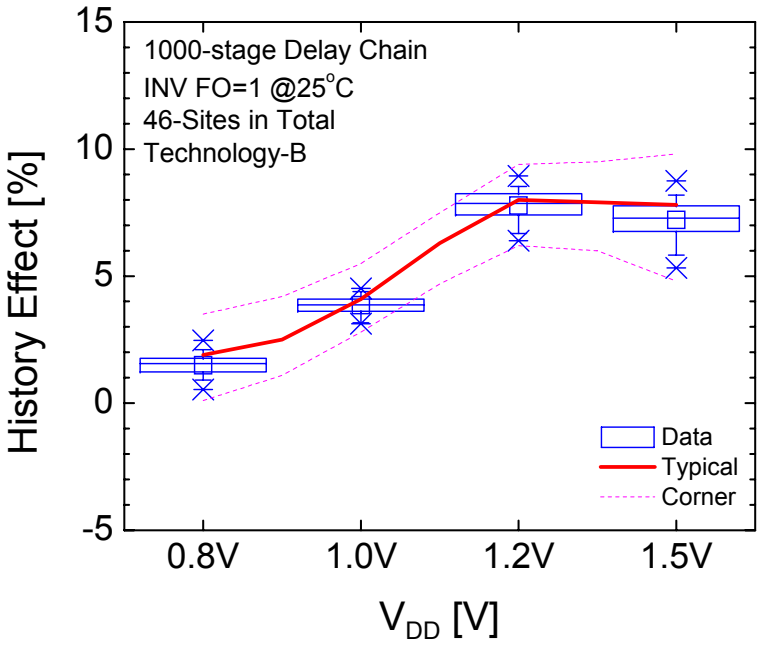
Other Floating Body Effects: Parasitic BJT





2007 CICC by W. Wu *et al.*

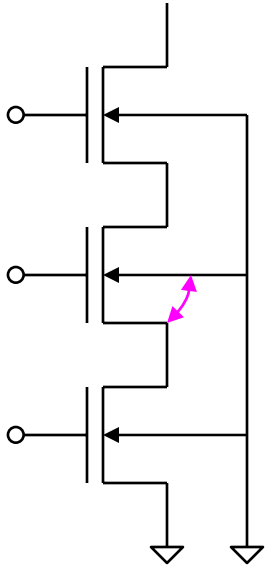
Challenges: Statistical Modeling

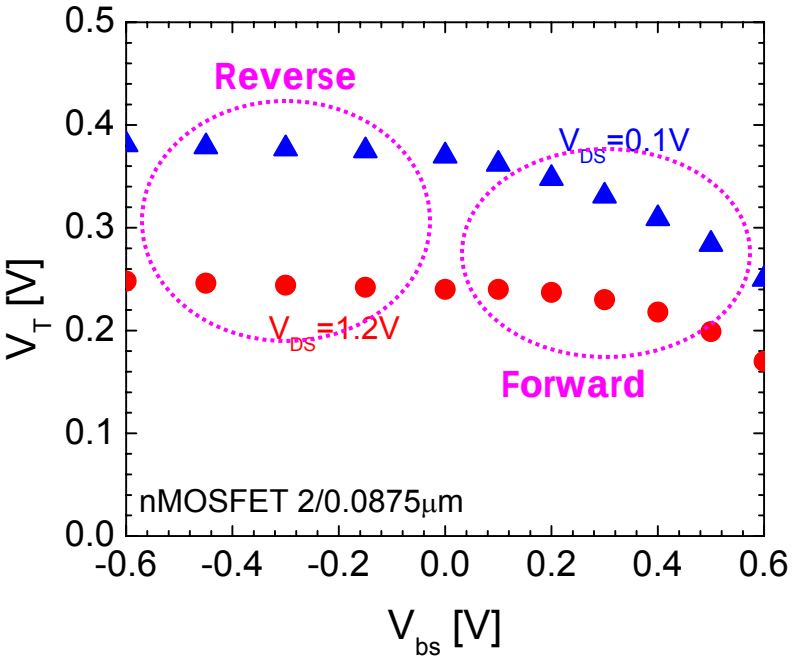


- Single-stage logic gate measurement
  - Requires very high-accuracy test equipment
  - Extremely low throughput
- Delay chain measurement
  - Averaged over all stages, loosing variation details
  - Large area
- In-line characterization
  - Approximate precision

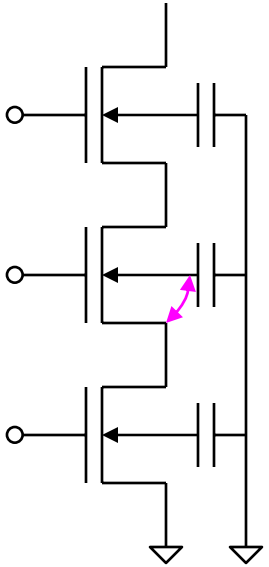
Back-Bias Range of Interest

Body-Contacted and Bulk



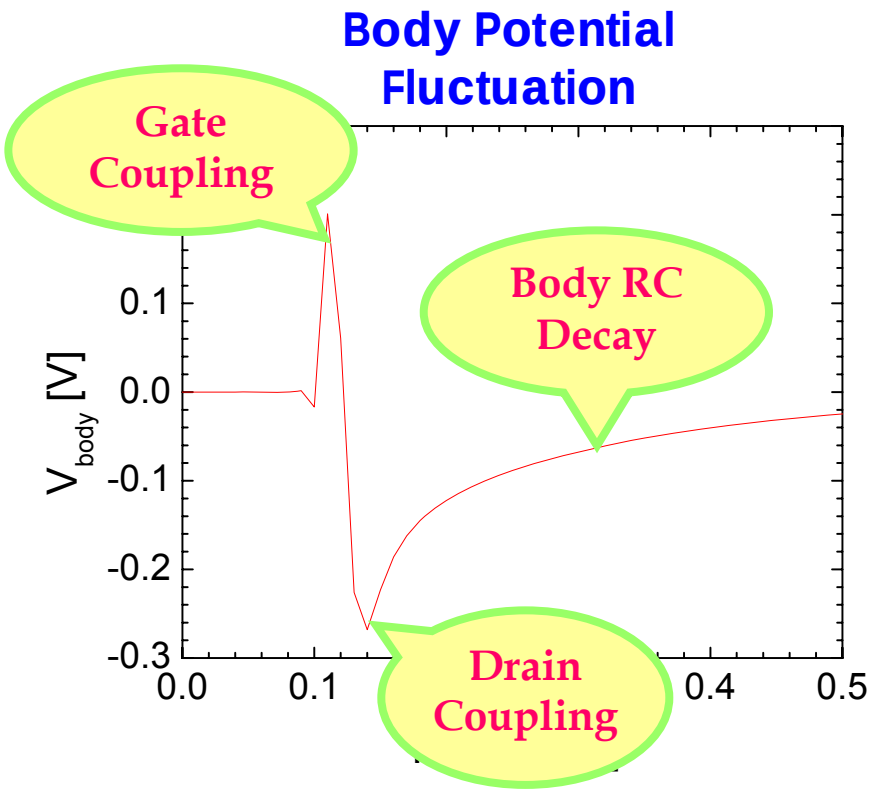


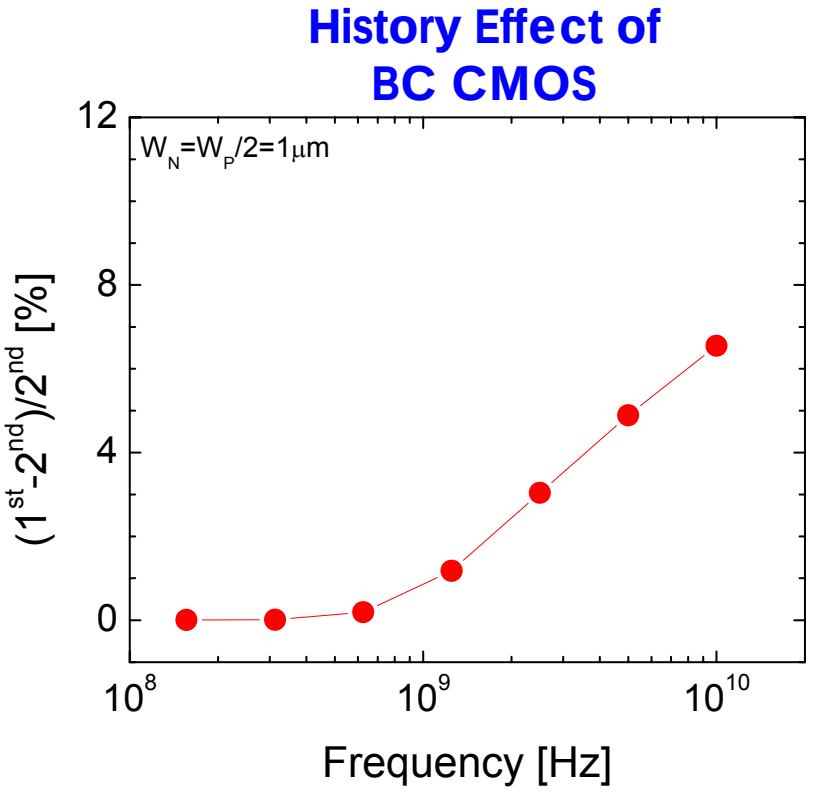
Floating Body



- Sometimes the body effect is not able to fit for the entire range
- Then some range should be compromised
- Separating body-contacted and floating-body models maybe more desirable

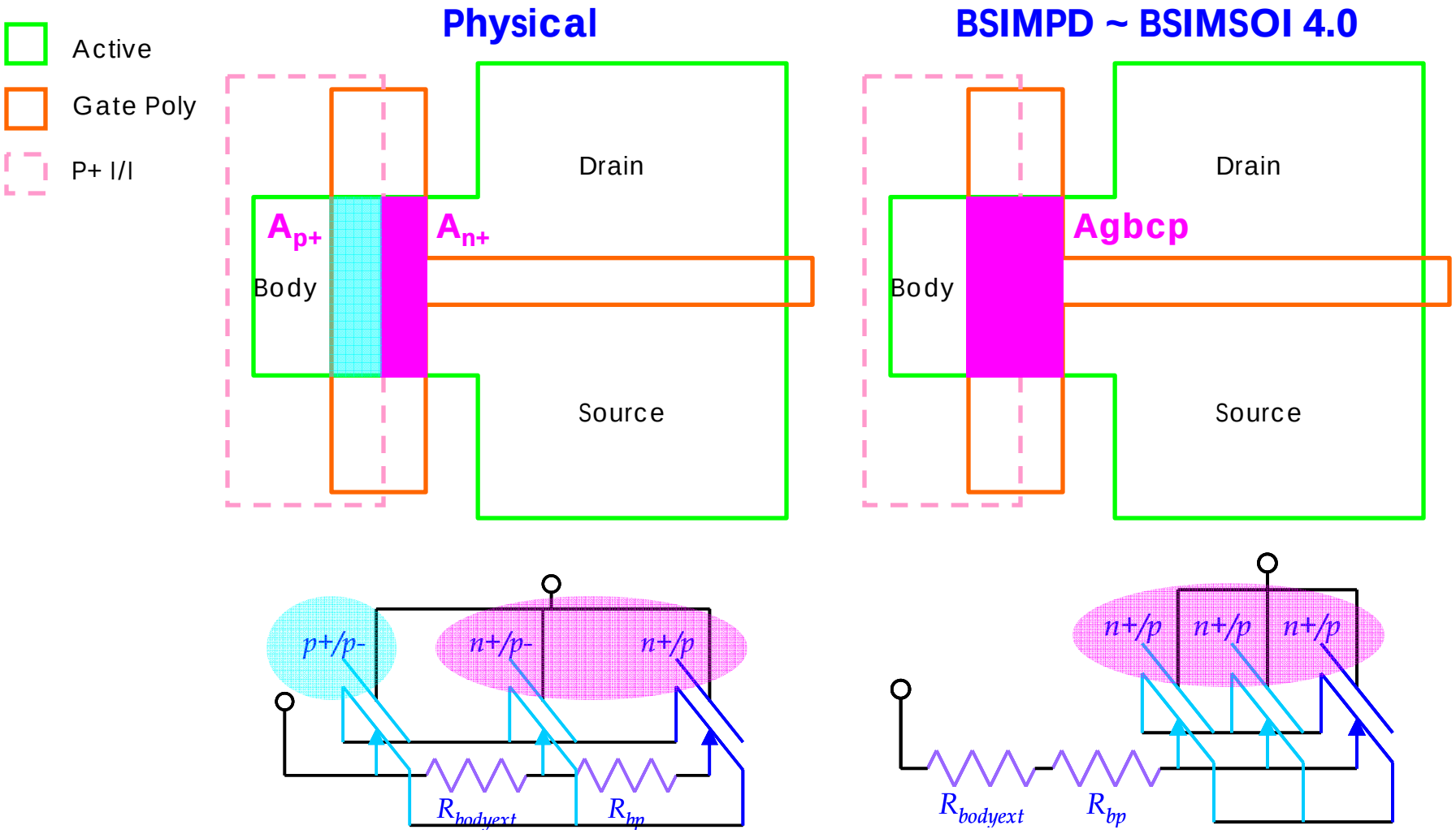
Can Body Be Really Tied?



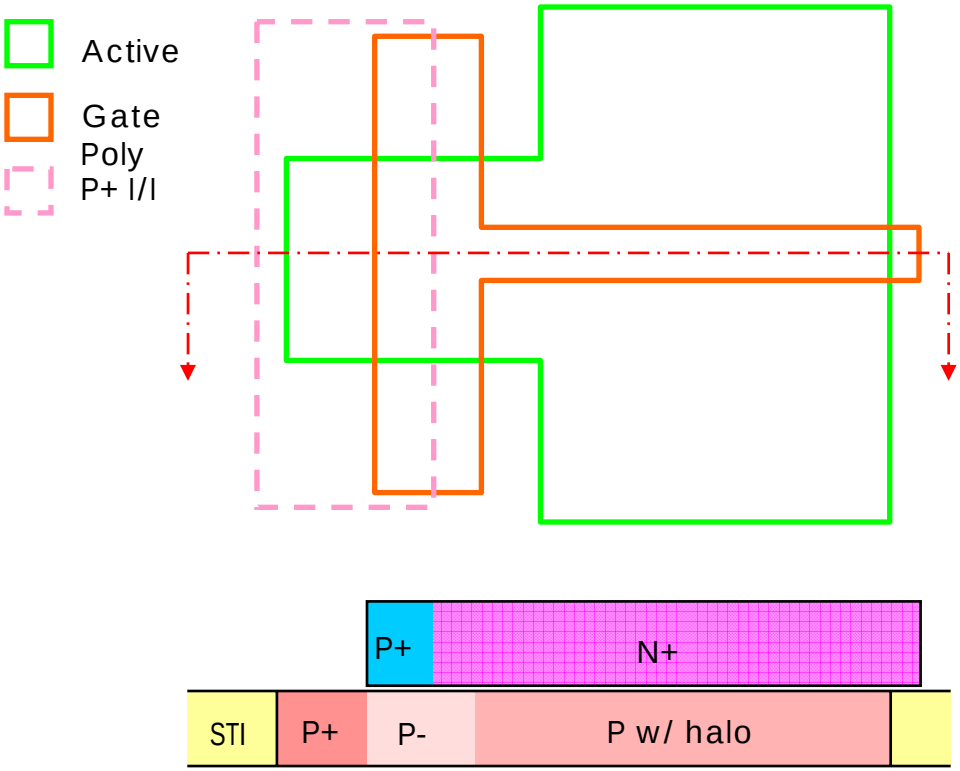


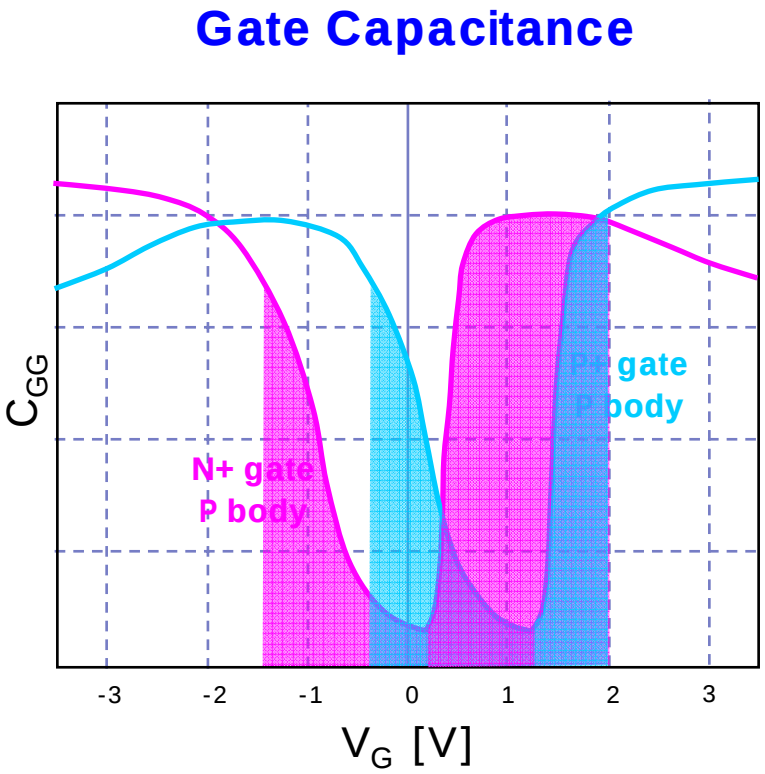
- Body-contacted PD-SOI circuit experiences the coupling effects exactly same as floating-body one
- Thus, it also exhibits history effect

Body-Contact: Gate Capacitance



Body-Contact: Gate Capacitance





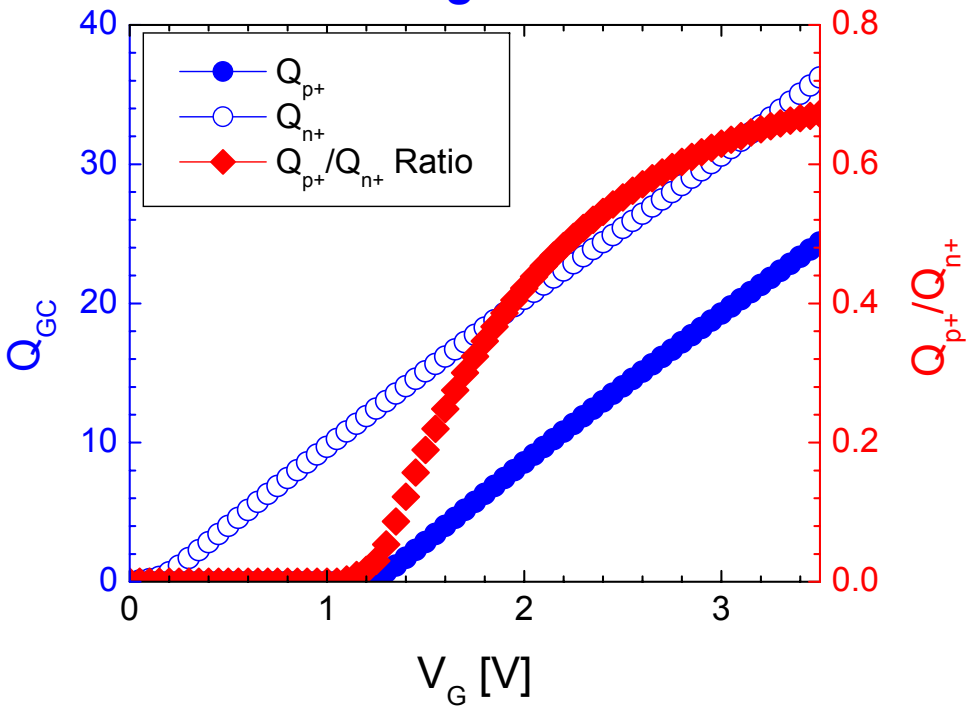
Over-Estimated

$$Q_{GB} \approx \int_{V_{FB}}^{V_T} C_G \cdot dV_{GS}$$

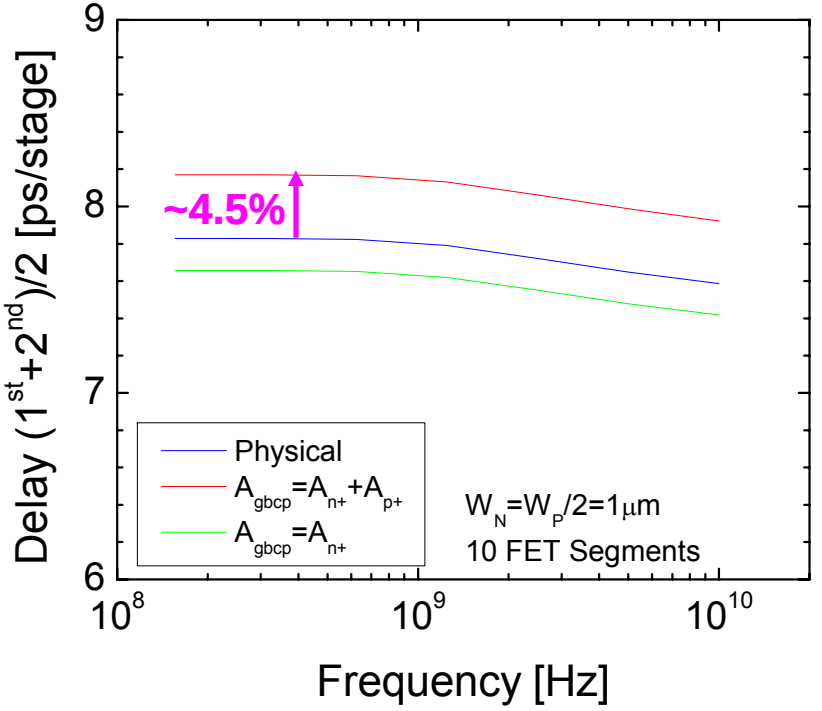
$$Q_{GC} \approx \int_{V_T}^{V_{DD}} C_G \cdot dV_{GS}$$

Body-Contact: Gate Capacitance

Charge Ratio

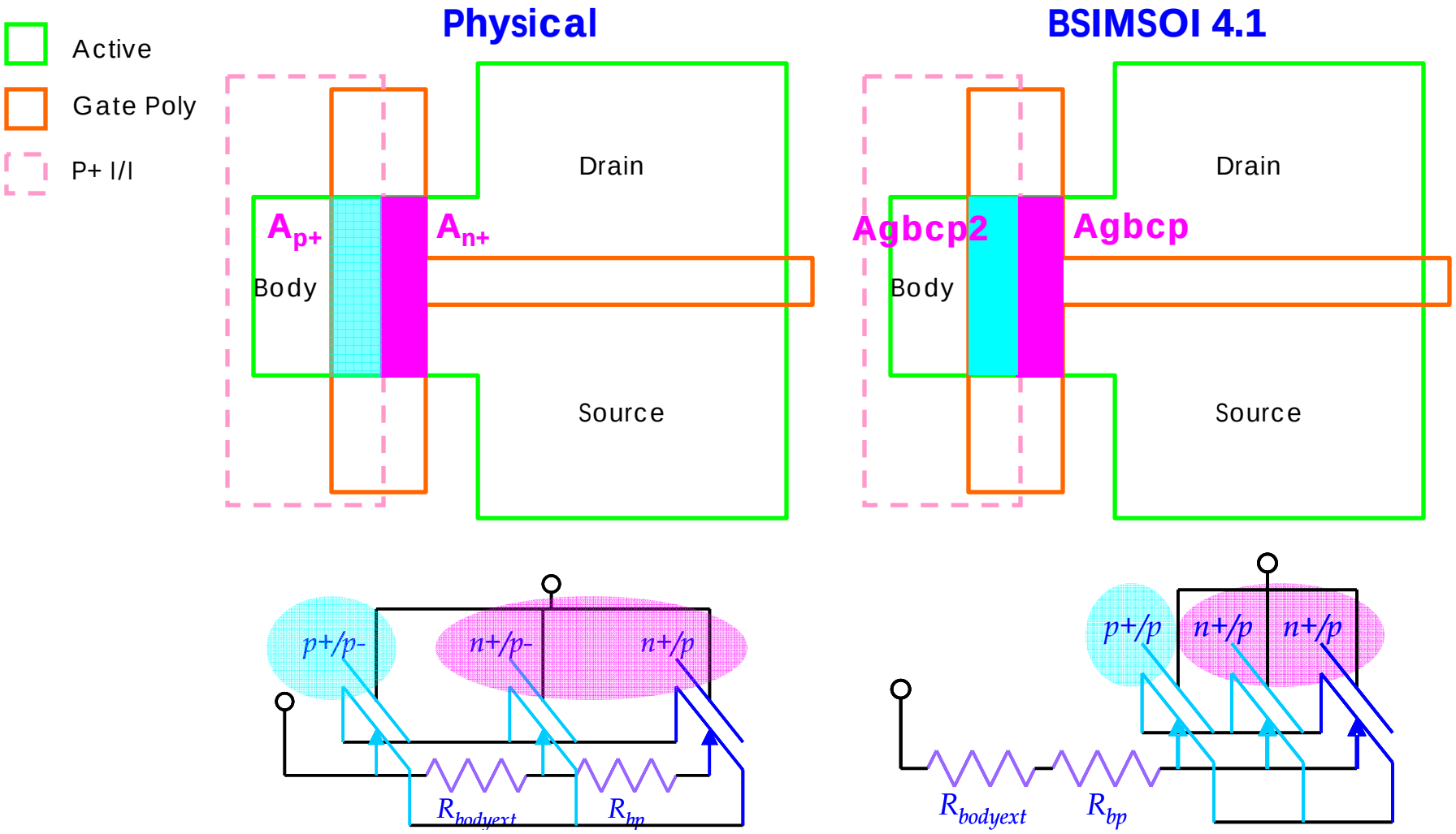


Impact on Switching Delay

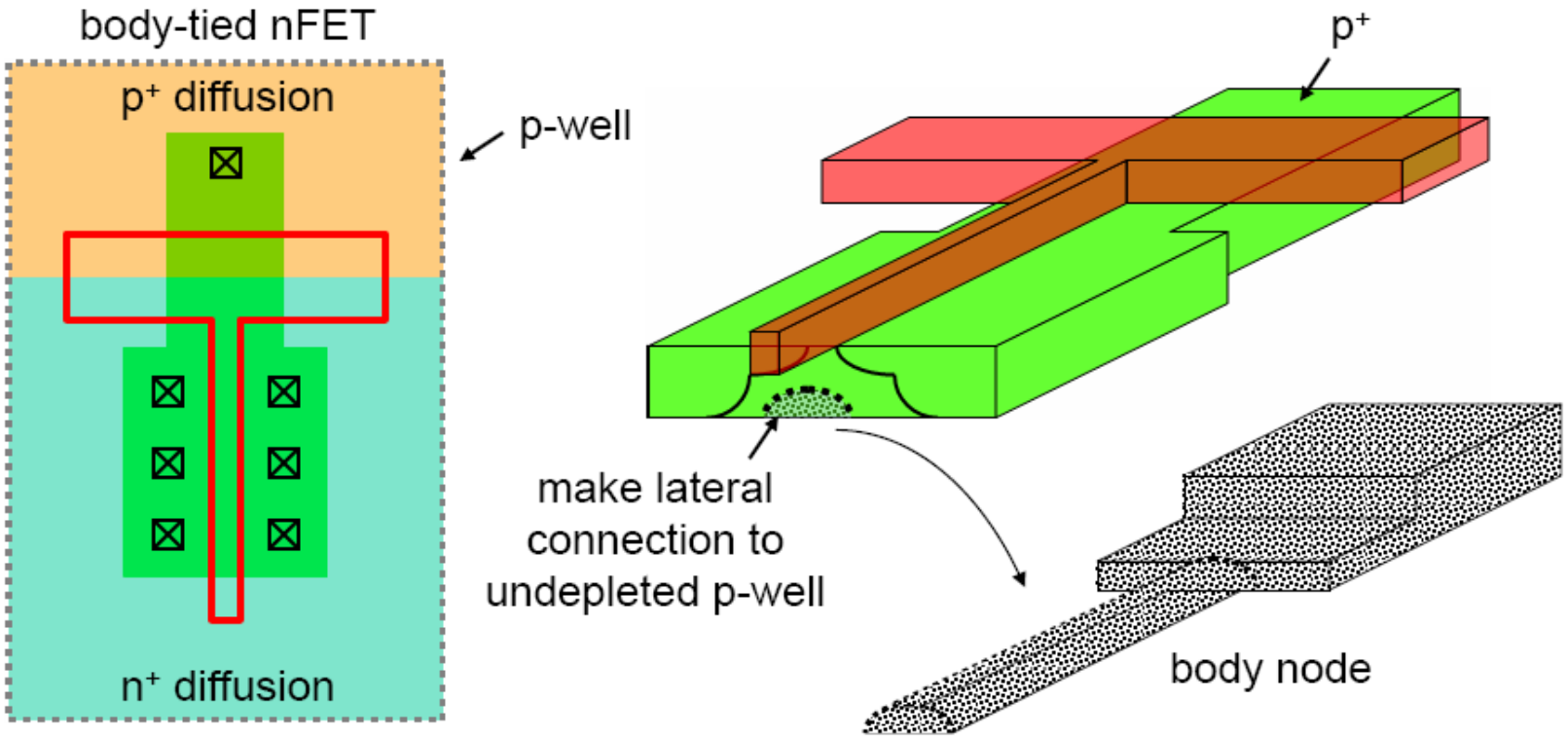


- The charge ratio is 0.2 ~ 0.5 within practical range
  - 2 ~ 5x overestimation
- Its impact of switching delay is not negligible

Body-Contact: Gate Capacitance



Bias Dependence of Body Resistance

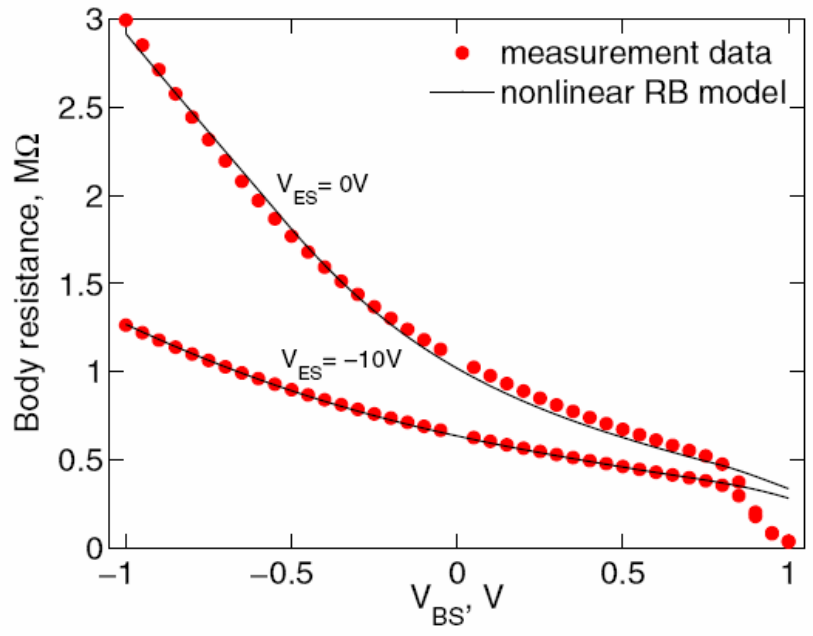


Courtesy of Alvin Loke *et al.*

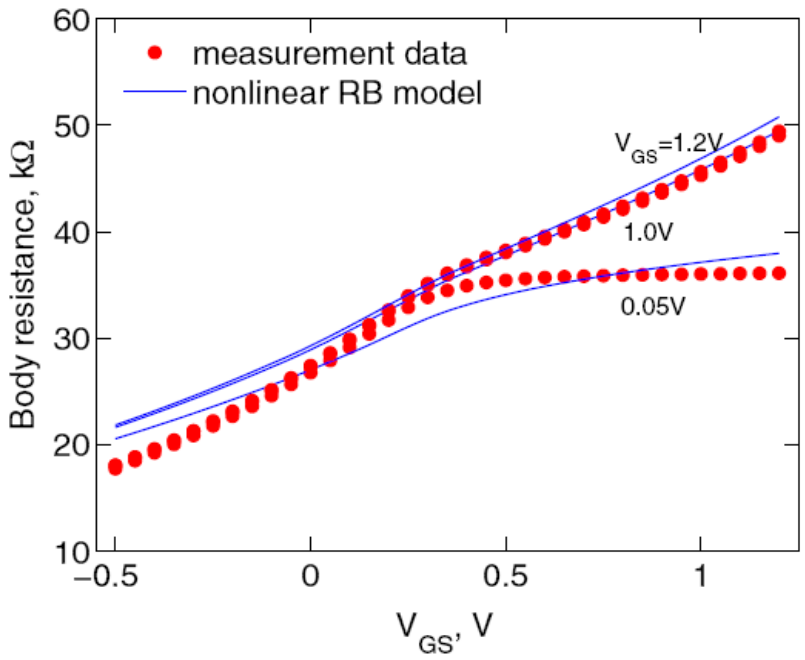
- Body resistance is determined by majority carriers in the neutral region

Bias Dependence of Body Resistance

Body Bias Dependence



Gate Bias Dependence

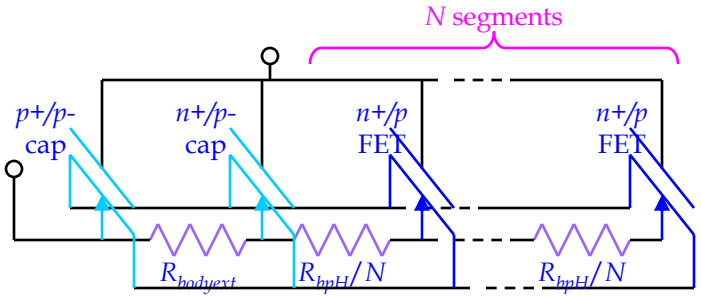


2007 CICC by W. Wu *et al.*

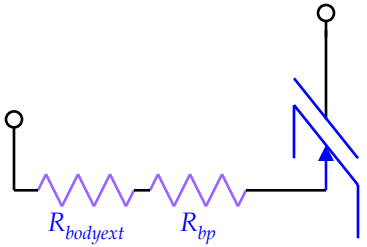
- Bias significantly modulates the depletion region; in turn, body resistance
  - Not captured in BSIMSOI
  - Well captured in PSP-SOI

Body-Contact: Distributed Body R

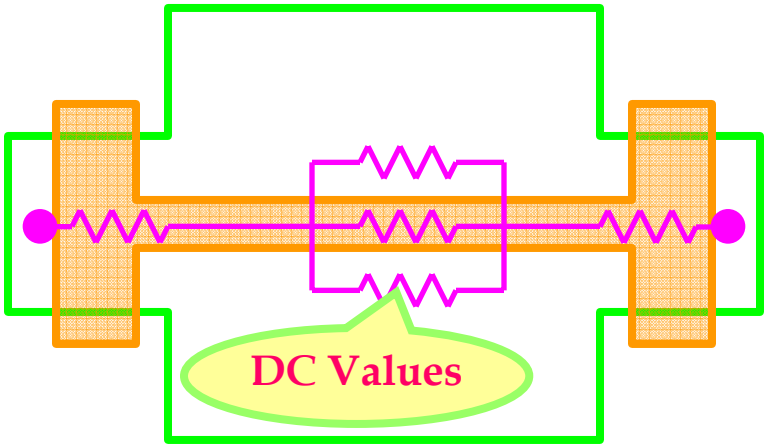
Distributed



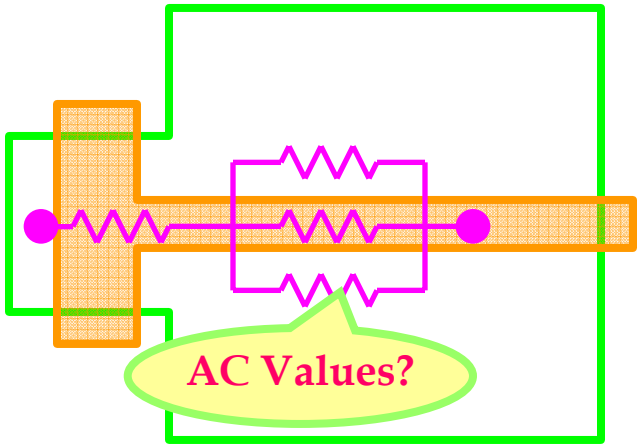
Single Lumped



Measurement



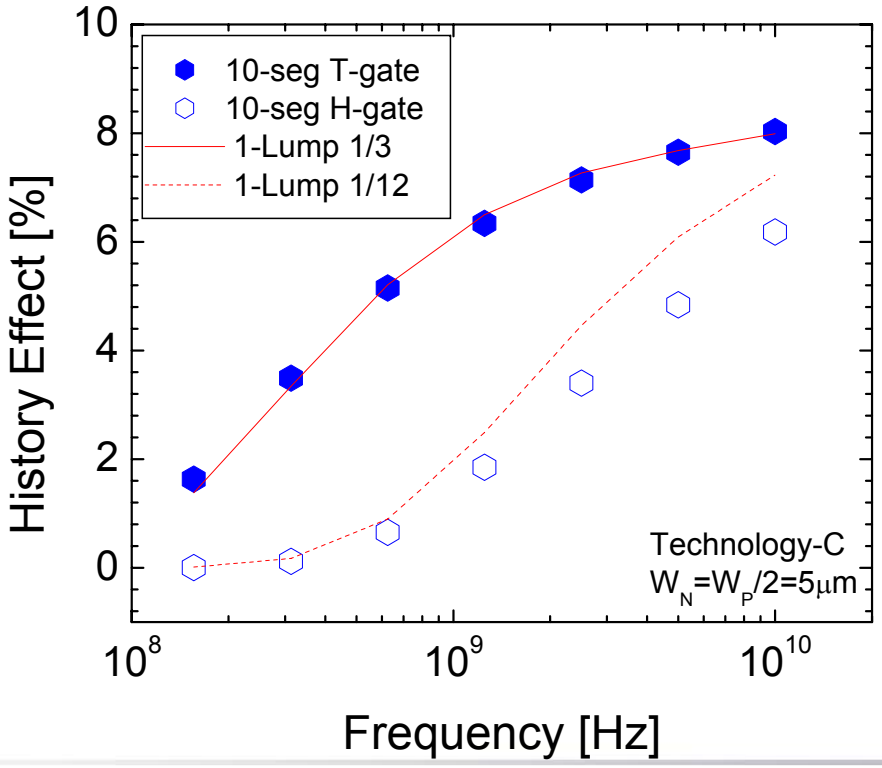
Model



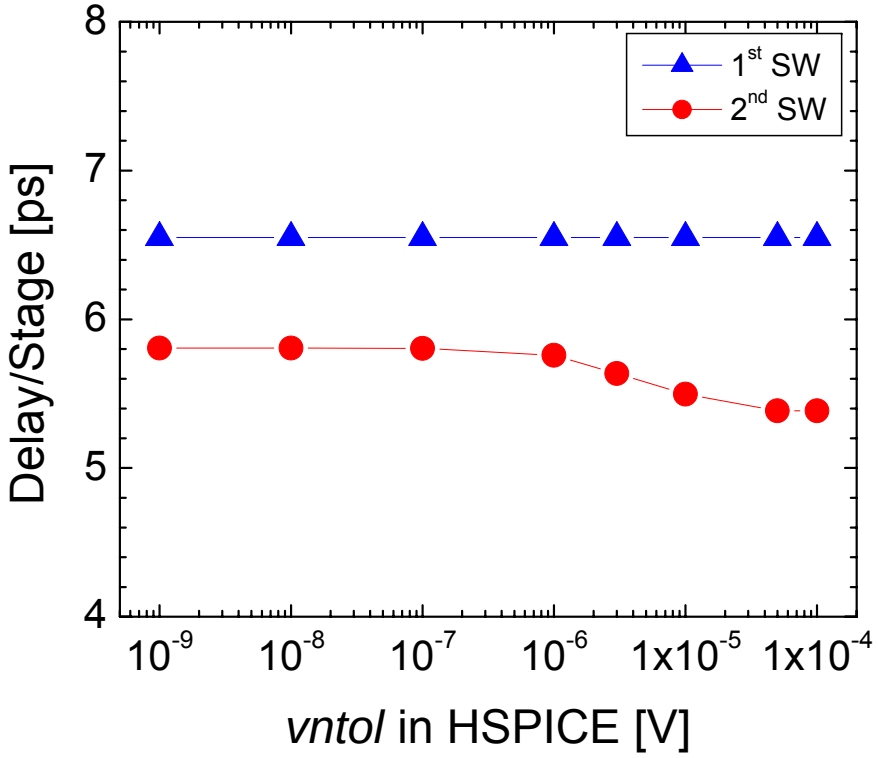
Body-Contact: Distributed Body R

Rule of Thumb

- Factor of 1/3 for single-side contact; 1/12 for double-side contact
- Mathematically derived for gate resistance noise
  - A. B. Philips, BJT Base Resistance (McGraw-Hill, 1962)
  - R. P. Jinal, MOSFET Gate Resistance (IEEE T-ED, pp. 1505-1509, October 1984)
- Applicable for other distributed resistance associated with active gain

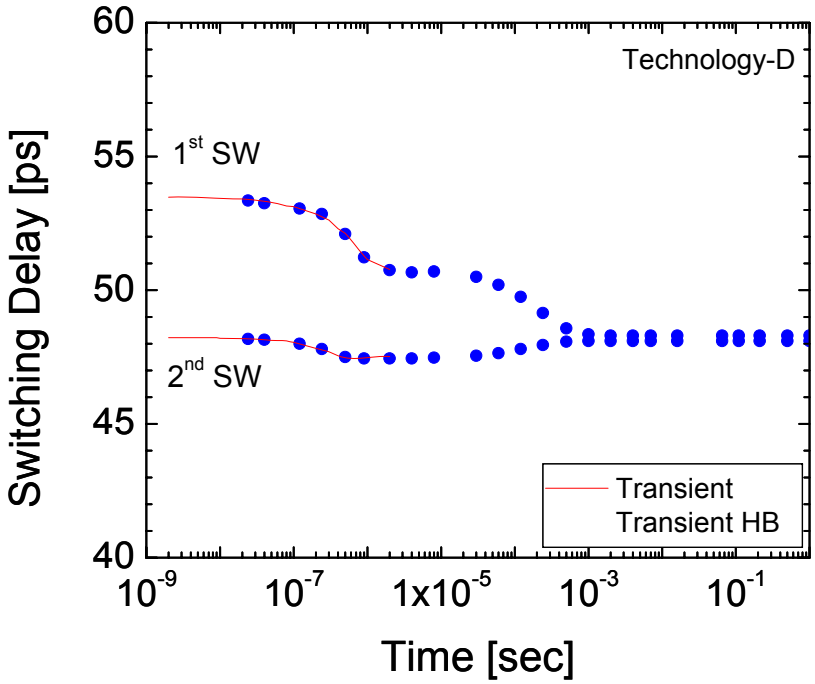


PD-SOI Circuit Simulation: Accuracy



- Accuracy options
  - $\Delta V_{body} << V_{DD}$ → needs higher accuracy in voltage convergence criteria (`vntol`, etc.)
  - $I_{body} << I_{DS}$ → needs tighter control on off-conductance of capacitors (`gmindc`)
  - Stronger sensitivity of diode currents at low temperature → needs special attention on numerical convergence criteria

PD-SOI Circuit Simulation: Time



- Harmonic balance
  - Solves Fourier series in *f*-domain
  - Requires over-sampling and sufficient harmonics
- Periodic steady state
  - Projects the evolution of the net body charges using the Newton method
- Indirect body initialization technique
  - .ic v(n)=V_{DD}/2
- Transient HB
  - Speed up by orders in magnitude

- Charging/discharging
  - Circuits in sleep and wake-up modes
- Steady-state
  - Critical for larger multi-input circuits, SRAMs, clock drivers, I/O, PLL, etc.
  - Takes μs~ms → impractically long

Model Standardization

- Compact Modeling Council (CMC)
  - Hosted by the Government Electronics and Information Association (GEIA)
  - Evaluates fundamental physics and numerical properties
    - Symmetry, continuity, convergence, and runtime
  - Publishes requirements and procedure
- Benefits
  - Consistency in implementation on user side
  - Recognition and funding to model developers
  - Improved model accuracy and features
    - Through detailed review during the standardization process
- CMC-Standard SOI Model
  - BSIMPD → BSIMSOI (University of California, Berkeley)
  - Next-generation SOI standardization was kicked off in 2006
  - Candidates
    - PD PSP-SOI PD, XSIM PD
    - DD (FD) PSP-SOI DD, HiSIM-SOI, ULTRA-SOI, XSIM DD

Conclusion

- Reviewed the current and future challenges in compact modeling, characterization, and circuit simulation of PD-SOI CMOS
- Floating-body effects
  - One of the main performance boosters
  - Main complexity in PD-SOI compact modeling
  - Measuring key components is challenging
  - Nevertheless, mechanisms are well understood; thus, can be reproduced
- Body-contacted device modeling
  - Parasitic gate capacitance and body resistance need to be accurate
  - Distributed effect of the body resistance can be simplified
- PD-SOI simulation requires tighter convergence criteria and novel simulation techniques, mainly due to the floating-body effects
- Model standardization promotes implementation consistency and improved accuracy and features.

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  - Technical contributions
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  - UFSOI Prof. Jerry G. Fossum (University of Florida, Gainesville)
  - HiSIM-SOI Prof. Mitiko Miura-Mattausch (Hiroshima University)
  - XSIM Prof. Xing Zhou (Nanyang Technological University)
  - ULTRA-SOI Prof. Jin He (Peking University)