Monolithic Phase-Locked Loops for Clocking Sub-Systems

Mehmet Soyuer
IBM T.J. Watson Research Center
Yorktown Heights, NY
soyuer@us.ibm.com

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Outline

• Introduction
• PLL Components
• PLL Modeling and Noise
• Design Examples
  – Clock Generation
  – Clock and Data Recovery
  – Frequency Synthesis
• Summary
Applications and Requirements

• Digital Systems
  – Used to generate a time reference for movement of data
  – Key PLL design considerations:
    • Wide tuning range
    • Low cycle-cycle and period jitter

• Wireline Communications
  – Used for clock generation and timing recovery
  – Key PLL design considerations:
    • Phase noise profile
    • Integrated jitter
    • Bandwidth control of clock generation and timing recovery loops

• Wireless Communications
  – Used for frequency synthesis
  – Key PLL design considerations:
    • Phase noise profile
    • Spur generation
    • Non-integer multiplication
Simple PLL Block Diagram

- Feedback control loop (watch out for stability, parasitic poles)
- $F_{out} = N \times f_{in}$
- Loop acts to align phases of input signal and the divided output clock
Analog and Digital PLL Architectures

Charge-Pump PLL

\[ \text{Fref} \rightarrow \text{PFD+CP} \rightarrow \text{LF} \rightarrow \text{VCO} \rightarrow \text{Fout} \]

- Linear PFD
- Continuously tuned VCO
- Continuous-time

Digital (Bang-Bang) PLL

\[ \text{Fref} \rightarrow \text{BB PFD} \rightarrow \text{LF} \rightarrow \text{DCO} \rightarrow \text{Fout} \]

- Bang-bang PFD
- Discrete DCO
- Discrete-time
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Design Considerations for Loop Components: CP-PLL Example

- Deadzone
- Speed
- Differential?
- ...
Phase/Frequency Detector (PFD)

- State machine
  - Extends linear range ($4\pi$)
  - Enables frequency acquisition
- In-phase when locked
- Cannot tolerate missing transitions (not suitable for CDR applications)
PFD Characteristic

- When PLL in lock-in range, PFD $\rightarrow$ PD
- When PLL is out-of-lock, PFD $\rightarrow$ FD
- Frequency limitations from reset path

Nonideal PFD: Deadzone

- Small phase error generates very narrow output pulse width.
  → Not enough to fully turn on CP current.
- PFD-induced deadzone
  - Due to capacitive loading at PFD output.
- CP-induced deadzone
  - Due to slow current switching at CP

For example, see: J.F. Ewen et al,"CMOS Circuits for Gb/s Serial Data Communication", IBM Jour. Research and Development, January/March, 1995
Minimizing Dead-Zone Effect

- Non-zero pulse width with zero phase error
  → Set minimum CP turn-on time
- Alternative method
  - Phase detection with non-zero static phase offset
Ideal Charge Pump

- Eliminates the need for active filter
  If $Z(s) = 1/sC$, then $V_z = I_{cp}/sC$
- Nonideal charge pump
  - Clock skew in digital clock generation
  - Reference spur in frequency synthesis
## Phase Detectors for CDR PLLs

<table>
<thead>
<tr>
<th>Phase Detector</th>
<th>Alexander</th>
<th>Eye Tracking</th>
<th>Hogge</th>
<th>LPD+$\Delta\Sigma$ Mod</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(ISSCC’07, pp. 228-229)</td>
<td>(ISSCC’08, pp. 98-99)</td>
<td>(JSSC’06, pp. 2566-76)</td>
<td>(ISSCC’09, pp. 186-187)</td>
</tr>
<tr>
<td><strong>Simplified Block Diagram</strong></td>
<td><img src="image1.png" alt="Simplified Block Diagram" /></td>
<td><img src="image2.png" alt="Simplified Block Diagram" /></td>
<td><img src="image3.png" alt="Simplified Block Diagram" /></td>
<td><img src="image4.png" alt="Simplified Block Diagram" /></td>
</tr>
<tr>
<td><strong>Type</strong></td>
<td>Bang-Bang</td>
<td>Bang-Bang</td>
<td>Linear</td>
<td>Linear</td>
</tr>
<tr>
<td></td>
<td>(Early/Late)</td>
<td>(Early/Late/Hold)</td>
<td>(PWM)</td>
<td>(PDM Encoded Binary Stream)</td>
</tr>
<tr>
<td><strong>Pros and Cons</strong></td>
<td>• simple circuit</td>
<td>• compatible w/ digital CDR</td>
<td>• simple circuit</td>
<td>• small quantization noise</td>
</tr>
<tr>
<td></td>
<td>• compatible w/ digital CDR</td>
<td>• medium quant. noise</td>
<td>• no quant. noise</td>
<td>• compatible w/ digital CDR</td>
</tr>
<tr>
<td></td>
<td>• large quant. noise</td>
<td>• less compatible w/ digital CDR</td>
<td>3-phase clock</td>
<td>requires ADC</td>
</tr>
</tbody>
</table>

After K. Fukuda et al, “10Gb/s Receiver with Track-and-Hold-Type Linear Phase Detector and Charge Distribution 1st Order $\Delta\Sigma$ Modulator,”” ISSCC, paper 10.4, Feb. 2009
Oscillators

• Resonator-based oscillator
  – LC VCO most popular as an integrated VCO

• Resonator-less oscillator
  – Ring VCO most popular as an integrated VCO
  – Relaxation VCO has wide tuning range but noisier

# LC or Ring?

<table>
<thead>
<tr>
<th></th>
<th>LC</th>
<th>Ring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. frequency</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Power (high f)</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Tuning range</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Cost</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Multiphase</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Flexibility</td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
LC VCO

- Use variable capacitance to tune output frequency
- Good phase noise but narrow tuning range

\[
\omega_o = \frac{1}{\sqrt{LC}}
\]

\[
\frac{1}{Q_{res}} = \frac{1}{Q_{ind}} + \frac{1}{Q_{var}}
\]
Band-Switching LC VCO

- Overcomes tuning range problem
- No calibration over temperature

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Typical PLL Linear Model

\[ \theta_i \xrightarrow{+} \sum \theta_e \xrightarrow{K_d} F(s) \xrightarrow{K_v/s} \theta_o \]

If \( \theta_e = c \), then \( \omega_o - \omega_i = \frac{d\theta_o}{dt} - \frac{d\theta_i}{dt} = \frac{d\theta_e}{dt} = 0 \)

- **Phase locked** means constant phase error, or actually “zero-frequency locked”
- **Is linear model good enough to analyze PLL?**
  - Yes, when we are interested in PLL within lock-in range
Loop Order and Types

\[ G(s) = K_d \cdot F(s) \cdot \frac{K_v}{s} \]

\[ H(s) = \frac{\theta_o}{\theta_i} = \frac{G(s)}{1+G(s)} = \frac{K_dK_vF(s)}{s + K_dK_vF(s)} \]

\[ E(s) = \frac{\theta_e}{\theta_i} = \frac{1}{1+G(s)} = \frac{s}{s + K_dK_vF(s)} \]

- **Order** - Number of poles of \( H(s) \)
- **Type** - Number of integrators within loop
Charge-Pump APLL vs BB-DPLL

- Linear PFD
- Continuously tuned VCO
- Continuous-time

- Bang-bang PFD
- Discrete DCO
- Discrete-time

\[
\frac{I_{CP}}{2\pi} \quad R + \frac{1}{C_S} \quad \frac{K_{VCO}}{s}\\
\]

PFD+CP  \(\rightarrow\)  LF  \(\rightarrow\)  VCO

- Fref
- Ffbk

\(\frac{1}{\sqrt{2\pi}} \frac{1}{\sigma}\)

\(K_{PFD} = \frac{1}{\sqrt{2\pi}} \frac{1}{\sigma}\)

\(\frac{1}{1 - z^{-1}}\)

\(K_P + K_I \frac{z^{-1}}{1 - z^{-1}}\)

\(\frac{1}{1 - z^{-1}}\)

\(\frac{K_{DCO}}{1 - z^{-1}}\)

BB PFD  \(\rightarrow\)  LF  \(\rightarrow\)  DCO

- Fref
- Ffbk

\(\frac{1}{N}\)
BB-PFD Linearization and Gain

Original non-linear transfer function:

\[ \Phi_{\text{REF}} - \Phi_{\text{FBK}} \]

Linearized transfer function:

\[ K_{PFD} = \frac{1}{\sqrt{2\pi} \sigma_{IN}} \]

- BB-PFD gain is inversely proportional to input jitter
- Low-noise BB-DPLL will have non-linear dynamics

J. Lee 2004
N. Da Dalt 2008
DPLL Bandwidth Control by Reference Dithering

A. Rylyakov et al, “Bang-Bang Digital PLLs at 11 GHz and 20 GHz with sub-200-fs Integrated Jitter for High-Speed Serial Communication Applications” ISSCC’09

- Measured phase noise plots shown for 11-GHz DPLL with LC-DCO
- Reference dithering does not degrade the rms jitter $\sigma$ (6.5 MHz to 5.5 GHz)
Noise Transfer Function

\[ G(s) = K_d \cdot F(s) \cdot \frac{K_v}{s} \]

\[ H_{n,i}(s) = \frac{\theta_o}{\theta_{n,i}} = \frac{G(s)}{1+G(s)} \]

\[ H_{n,f}(s) = \frac{\theta_o}{\theta_{n,f}} = \frac{K_v / s}{1+G(s)} \]

\[ H_{n,v}(s) = \frac{\theta_o}{\theta_{n,v}} = \frac{1}{1+G(s)} \]
Simulation: VCO Noise Suppression

- Low-frequency noise suppressed by open-loop gain

*After W. Rhee, ICSICT 2008 Short Course on Frequency Synthesizers and PLLs*
Noise Performance: LC vs. Ring

- Similar phase noise at 1MHz offset, but RJ is different
- Higher-gain ring VCO is more sensitive to substrate noise

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Clock Generation: Analog CP-PLL

Challenges
- Technology scaling
- Multiple data rates
- Large loop filter components
- Special analog devices
- Noise isolation, deterministic jitter
Can All-Digital PLL Help?

- Scales with technology node
  - Analog passive element is a bottleneck for area
    → Area/cost reduction with all-digital solution
  
- Programmable
  - Loop parameters can be accurately controlled
    → Advantageous when models are not mature

- Immune to leakage current
  - Large capacitor is not needed anymore
    → No need of thick-oxide transistor just for LPF
All gates are static CMOS (no CML, etc)

3 custom cells: 1 in the PFD, 1 in the DCO, plus voltage level shifter between the DCO and the logic power supplies

Highly modular design: loop filter (LF), multimodulus feedback divider (1/N) and both ΔΣ modulators use same adder
DPLL Example: Physical Design

A. Rylyakov et al, “A Wide Tuning Range, 1 GHz – 15 GHz Fractional-N All Digital PLL in 45nm SOI” CICC 08

- Technology: IBM 45nm SOI CMOS
- Transistor Count: ~25k
- Pd: 19mW, Jpp: 13ps @ 4GHz, 1V, 65°C
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PLL-Based Clock Recovery

- Requires frequency acquisition (e.g. quadri-correlator)
- Bang-bang loops preferred over traditional approaches
  - Narrow-band filtering approach requires non-linear processing of NRZ data spectrum
  - Binary quantized phase detectors maintain optimum sampling point over PVT => good for integration
Data Retiming with Recovered Clock

- Optimum sample time is at middle of bit window
e.g. Synchronizing at CLK rising edge & data slicing at falling edge
- Bit error when clock jitter > 0.5UI
- Data-retiming latch can be part of PD (e.g. Hogge and Early/Late PDs)

For more on bang-bang loop CDR design methodology: R. Walker, “Clock and Data Recovery for Serial Digital Communication”, ISSCC Short Course, February 2002
Jitter Transfer and Jitter Tolerance

- Extract clock information from noisy data and do retiming
  - Jitter transfer – Noise filtering performance of PLL
  - Jitter tolerance – Data tracking performance of PLL
Dual-Loop CDR: A 10-Gb/s Demonstrator

M. Meghelli et al, “A 10Gb/s 5-tap DFE / 4-Tap FFE Transceiver in 90nm CMOS Technology”, ISSCC’06

Goal:
• Minimize PLL/pin ratio in complex SoC ICs
• Reduce power and area
10-GHz PLL and 10Gb/s Receiver

Design Features:
- Digital CDR using phase interpolation*
- Half-rate clocking with 5-GHz PLL
- 130mW (with DFE & CDR logic)

**Key Features:**
- Fully-digital “bang-bang” loop
- Can handle up to +/- 4000ppm frequency offset
- Independent I,Q control
# 10-GHz PLL Characteristics

<table>
<thead>
<tr>
<th>PLL Performance</th>
<th>TxPLL</th>
<th>RxPLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min freq (GHz)</td>
<td>8.98</td>
<td>8.96</td>
</tr>
<tr>
<td>Max freq (GHz)</td>
<td>13.54</td>
<td>13.47</td>
</tr>
<tr>
<td>Mean freq (GHz)</td>
<td>11.26</td>
<td>11.22</td>
</tr>
<tr>
<td>Lock range (GHz)</td>
<td>4.56</td>
<td>4.52</td>
</tr>
<tr>
<td></td>
<td>+/-20.2%</td>
<td>+/-20.1%</td>
</tr>
<tr>
<td>Fine tune hold range</td>
<td>5.8%</td>
<td>5.8%</td>
</tr>
<tr>
<td>Phase noise @ 10MHz offset</td>
<td>-117.8</td>
<td>-117.7</td>
</tr>
<tr>
<td>(dBc/Hz, quarter rate clock)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jitter, 1MHz-100MHz (ps rms)</td>
<td>1.5</td>
<td>1.4</td>
</tr>
<tr>
<td>Jitter, fc/1667-100MHz (ps rms)</td>
<td>0.64</td>
<td>0.64</td>
</tr>
</tbody>
</table>

100mW power consumption
(with clock distribution)
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Frequency Synthesis by Phase Lock

\[
\frac{f_{\text{out}}}{f_{\text{ref}}} = \left( \frac{N}{M} \right) \cdot f_{\text{ref}}
\]

- Simple frequency synthesis by changing division ratio
- Frequency accuracy is as good as reference
- Longer settling time for larger \( N \)
20-GHz Frequency Synthesizer for mmWave Wireless

- Type-II, 4th order PLL
- Supports IEEE 802.15.3c 60-GHz frequency plan (with a tripler at the output)
- Half-integer divider allows finer resolution at higher ref-clock
- LC-VCO includes amplitude control loop
- Implemented in SiGe BiCMOS

<table>
<thead>
<tr>
<th>Power Consumption</th>
<th>144 mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Clock/Resolution</td>
<td>285.71 MHz / 500 MHz 308.57 MHz / 540 MHz</td>
</tr>
<tr>
<td>VCO Frequency</td>
<td>15.95-18.81 GHz (16.5%)</td>
</tr>
<tr>
<td>In-band Phase Noise @100kHz</td>
<td>-90 dBc/Hz</td>
</tr>
<tr>
<td>Phase Noise @10MHz</td>
<td>-126 to 123 dBc/Hz</td>
</tr>
<tr>
<td>Fractional Spur</td>
<td>-55 to -78 dBc</td>
</tr>
<tr>
<td>Reference Spur</td>
<td>-60 to -77 dBc</td>
</tr>
<tr>
<td>RMS Noise/Jitter (1MHz-1GHz integration)</td>
<td>0.5° to 1° 0.08 to 0.16ps</td>
</tr>
</tbody>
</table>

Fractional-$N$ with $\Delta\Sigma$ Modulation

- Randomized modulus control with noise shaping
- Arbitrarily fine resolution with digital word
- Fractional-$N$ PLL can also provide a solution for wireline by enabling multiple reference frequencies
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Active Research Topics

• Low-jitter dual-loop PLL/DLL CDRs for high-speed serial links
• All-digital PLLs
• Adaptive PLLs with self calibration
• On-chip testability and diagnosis (BIST)
  - Jitter monitor, supply voltage monitor
• Low-noise wide-range VCOs
• Clock generation with spread-spectrum for EMI reduction
• Wideband ΔΣ fractional-N PLLs for wireless/wireline links
  - Addressing nonlinear effects and quantization noise

→ More innovation required!
Summary

• PLL is a “simple and elegant” control system with a lot of complexity
• Both time and frequency domain techniques are required for leading-edge PLL design and analysis
• There is still room for creativity and innovation in PLL-based sub-system design!

Acknowledgements:
Many thanks to ex-IBM’er Prof. W. Rhee of Tsinghua University, for his 2008 ICSICT Short Course material on Frequency Synthesizers and PLLs. I am also grateful for the input from my colleagues, M. Meghelli, A. Rylyakov, D. Friedman and B. Floyd, at IBM.
More on Noise in Clock Subsystems

• Difficult to identify noise contribution from each source in time domain
• Use frequency and time domain analysis
Clock Noise

• Total jitter (TJ)
  = Random jitter (RJ) + Deterministic Jitter (DJ)
Random Jitter (RJ)
Conversion Between RMS and Peak-to-Peak Jitter at a Specified BER

- Gaussian distribution extends indefinitely beyond $\sigma$
- Need boundaries for communication link jitter budget
- Samples outside peak-to-peak range => BER as erfc(x)

<table>
<thead>
<tr>
<th>BER</th>
<th>RJ&lt;sub&gt;pp&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1.35 \times 10^{-3}$</td>
<td>6$\sigma$</td>
</tr>
<tr>
<td>$3.17 \times 10^{-5}$</td>
<td>8$\sigma$</td>
</tr>
<tr>
<td>$2.87 \times 10^{-7}$</td>
<td>10$\sigma$</td>
</tr>
<tr>
<td>$9.87 \times 10^{-10}$</td>
<td>12$\sigma$</td>
</tr>
<tr>
<td>$1.00 \times 10^{-12}$</td>
<td>14.069$\sigma$</td>
</tr>
</tbody>
</table>
Deterministic Jitter (DJ)

Time Domain

\[ RJ_{pk-pk} \text{ (e.g. } 14^*\sigma) \]

Frequency Domain

\[ DJ = 0.01 \text{ UI}_{pk-pk} \quad \leftrightarrow \quad P_{spur} = 10\log \left( \frac{\Delta f_{pk}}{2f_m} \right)^2 \approx -36\text{dBc} \]

\[ DJ_{pp} = \frac{2}{\pi} \cdot 10^{\frac{\Delta P}{20}} \text{ UI}_{pk-pk} \]