

Monolithic Phase-Locked Loops for Clocking Sub-Systems

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Outline

- Introduction
- PLL Components
- PLL Modeling and Noise
- Design Examples
 - Clock Generation
 - Clock and Data Recovery
 - Frequency Synthesis
- Summary

Applications and Requirements

- Digital Systems

- Used to generate a time reference for movement of data
- Key PLL design considerations:
 - Wide tuning range
 - Low cycle-cycle and period jitter

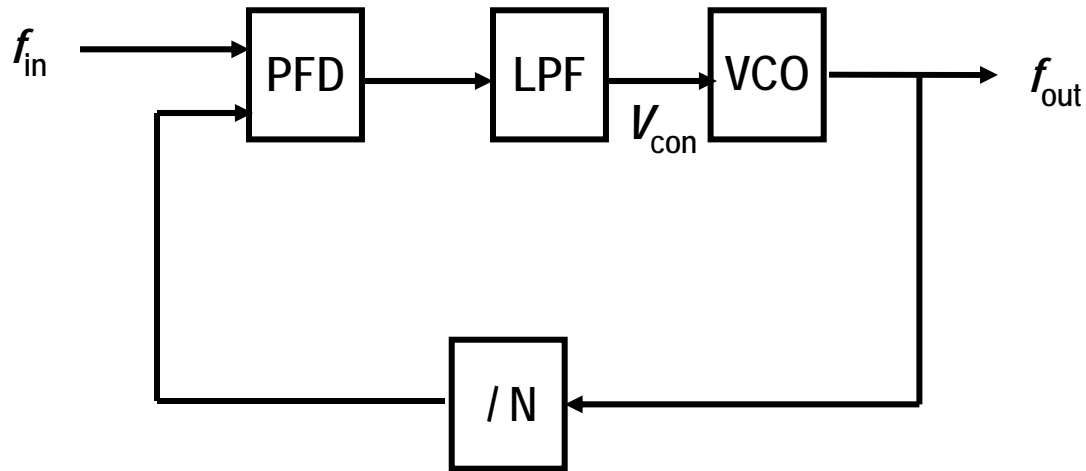
- Wireline Communications

- Used for clock generation and timing recovery
- Key PLL design considerations:
 - Phase noise profile
 - Integrated jitter
 - Bandwidth control of clock generation and timing recovery loops

- Wireless Communications

- Used for frequency synthesis
- Key PLL design considerations:
 - Phase noise profile
 - Spur generation
 - Non-integer multiplication

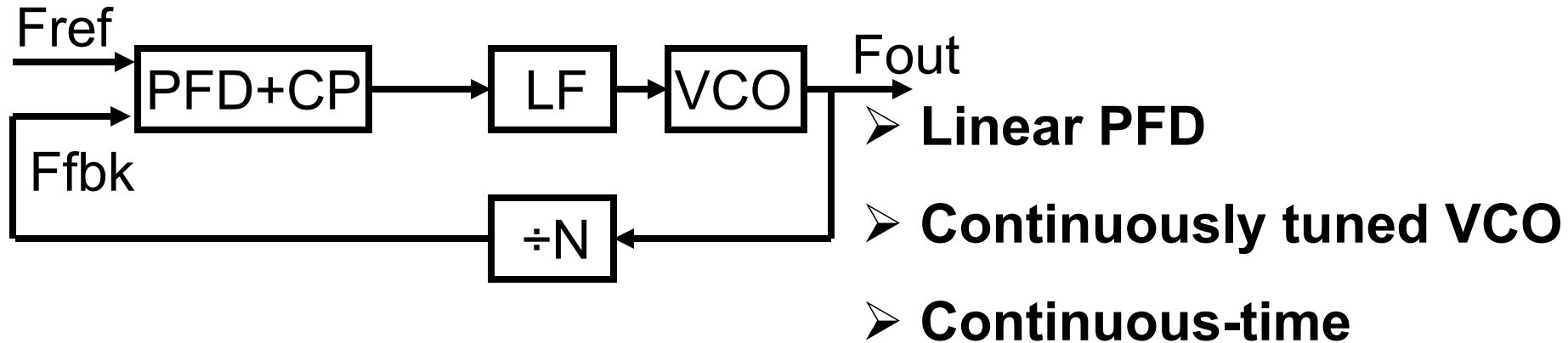
Simple PLL Block Diagram



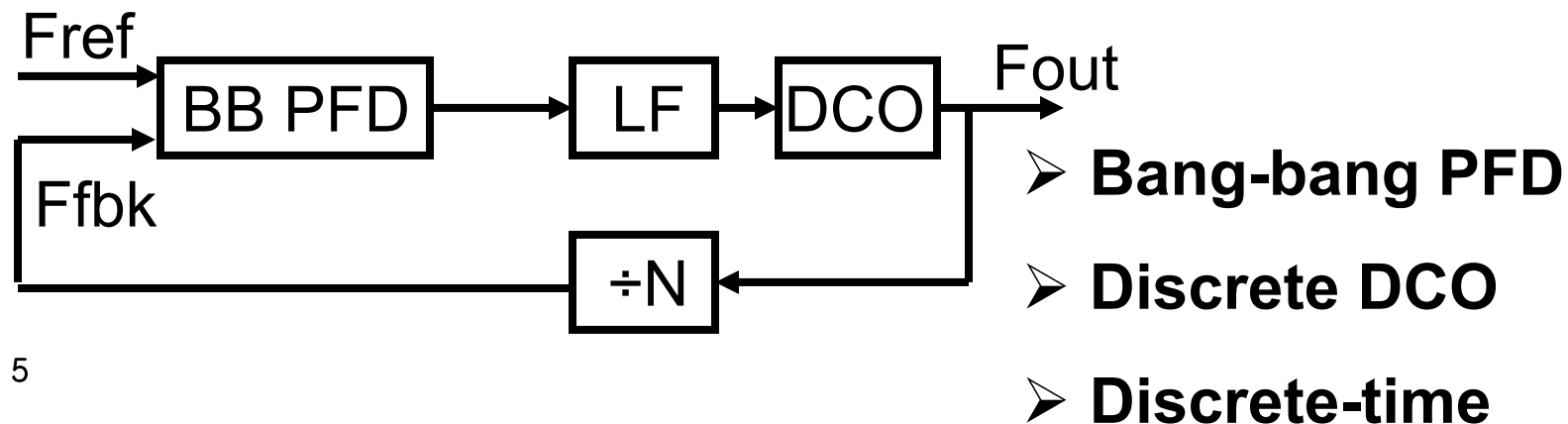
- Feedback control loop (watch out for stability, parasitic poles)
- $F_{out} = N * f_{in}$
- Loop acts to align phases of input signal and the divided output clock

Analog and Digital PLL Architectures

Charge-Pump PLL



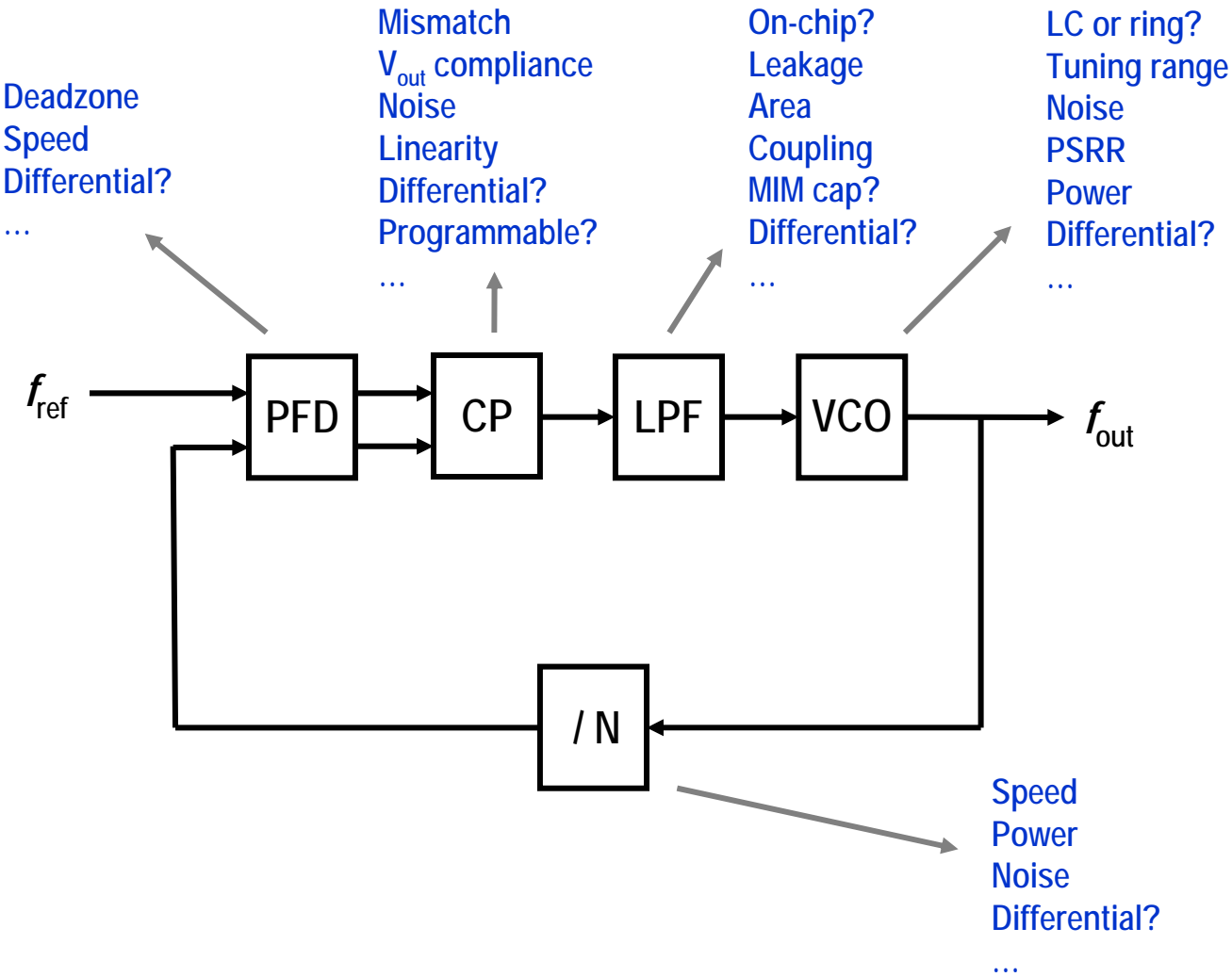
Digital (Bang-Bang) PLL



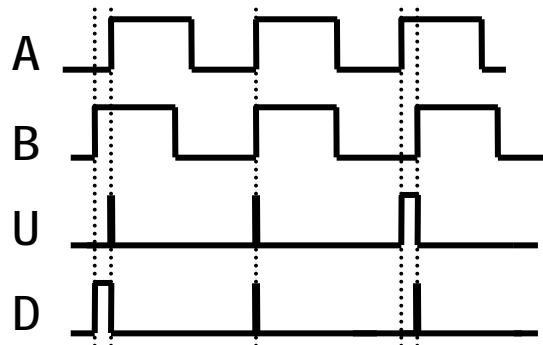
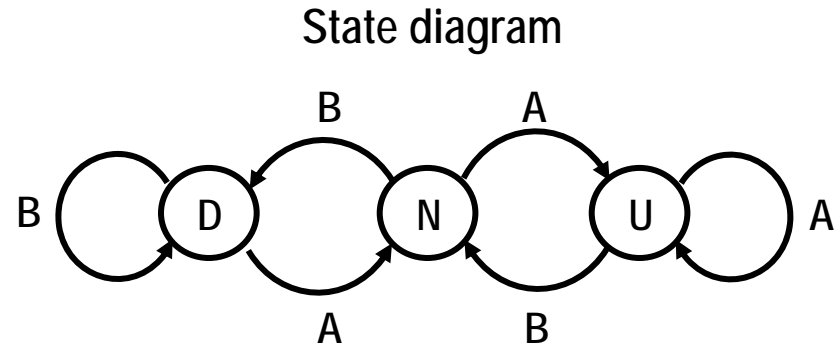
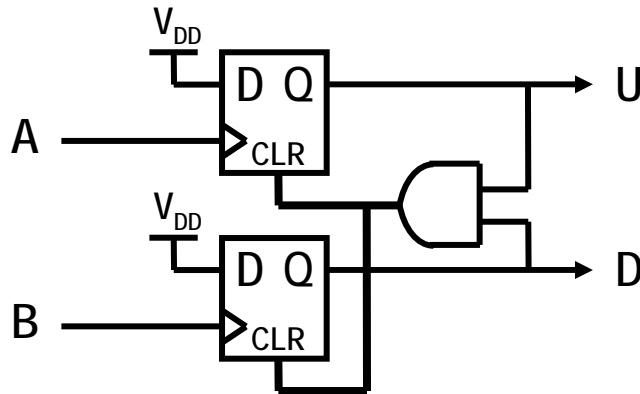
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Design Considerations for Loop Components: CP-PLL Example

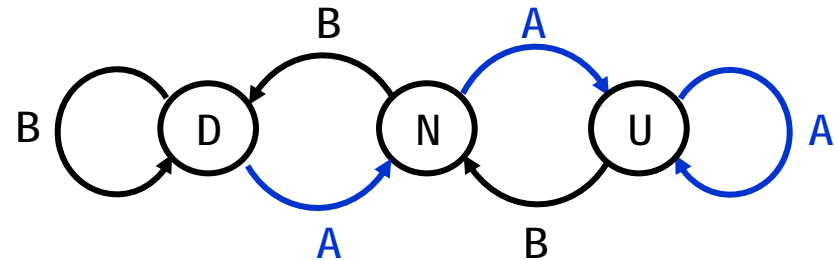
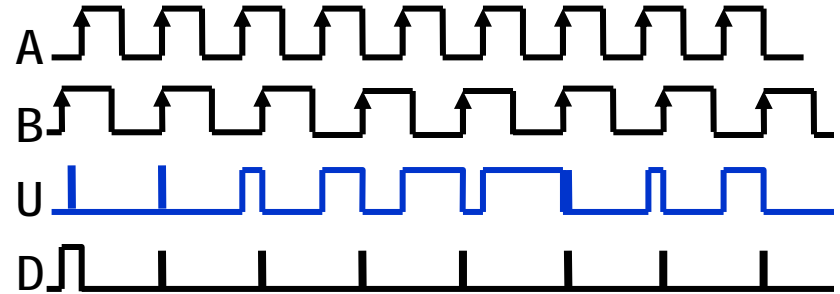
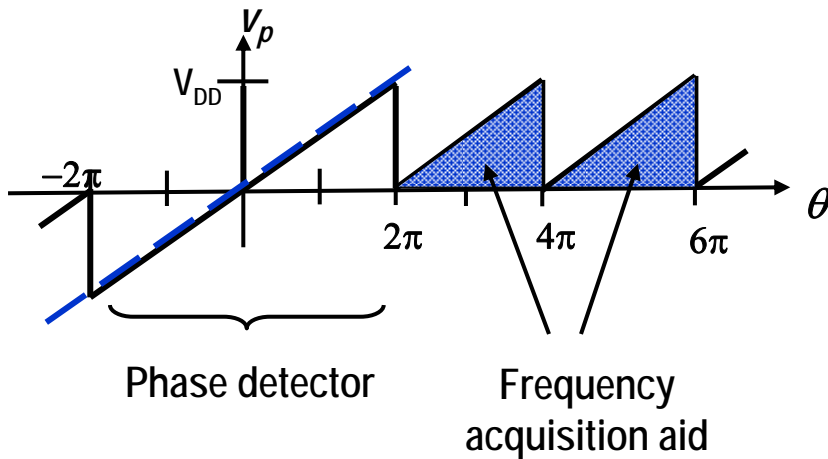


Phase/Frequency Detector (PFD)



- **State machine**
 - ✓ Extends linear range (4π)
 - ✓ Enables frequency acquisition
- **In-phase when locked**
- **Cannot tolerate missing transitions (not suitable for CDR applications)**

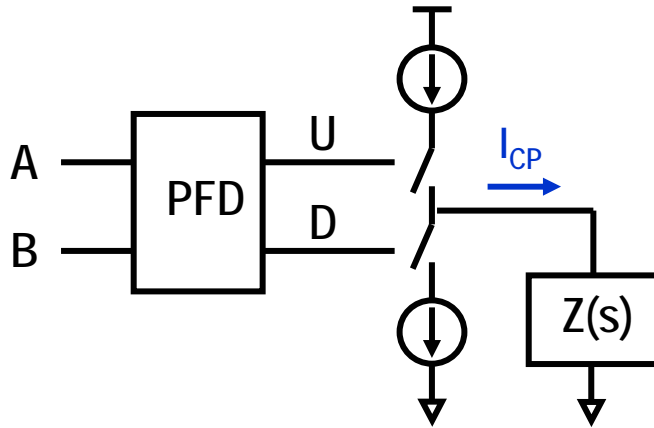
PFD Characteristic



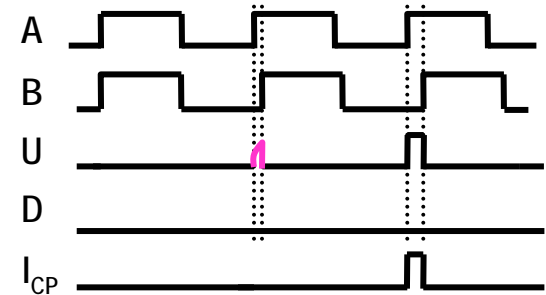
- When PLL in lock-in range, PFD \rightarrow PD
- When PLL is out-of-lock, PFD \rightarrow FD
- Frequency limitations from reset path

M. Soyuer and R. G. Meyer, "Frequency Limitations of a Conventional Phase-Frequency Detector" IEEE JSSC, August 1990

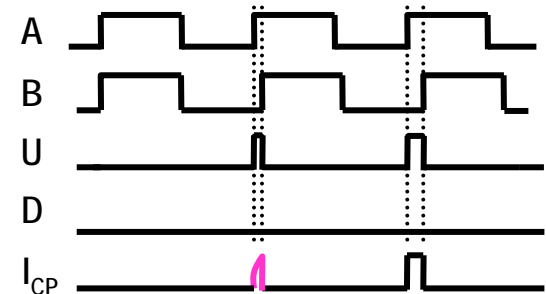
Nonideal PFD: Deadzone



PFD-induced deadzone



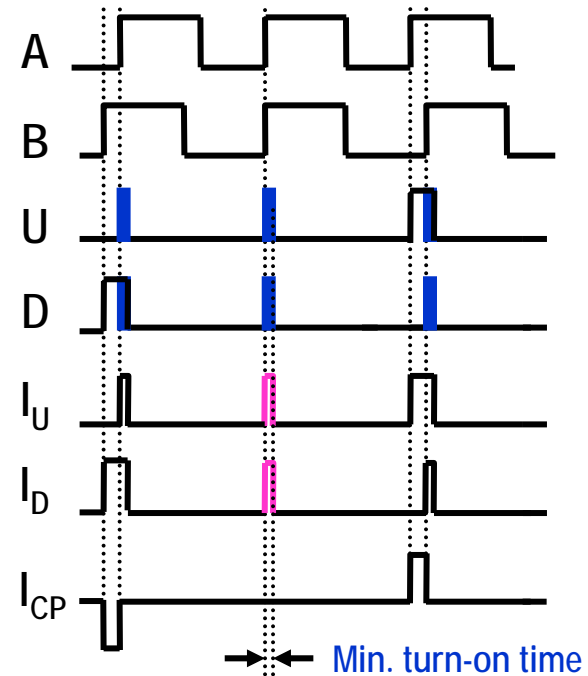
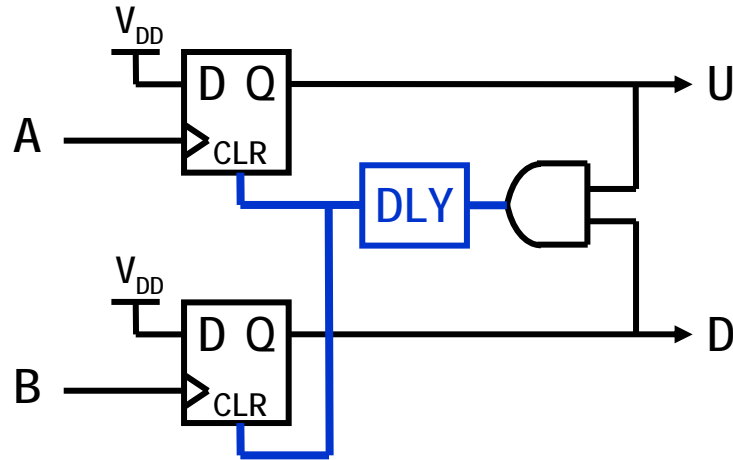
CP-induced deadzone



- **Small phase error generates very narrow output pulse width.**
 - Not enough to fully turn on CP current.
- **PFD-induced deadzone**
 - Due to capacitive loading at PFD output.
- **CP-induced deadzone**
 - Due to slow current switching at CP

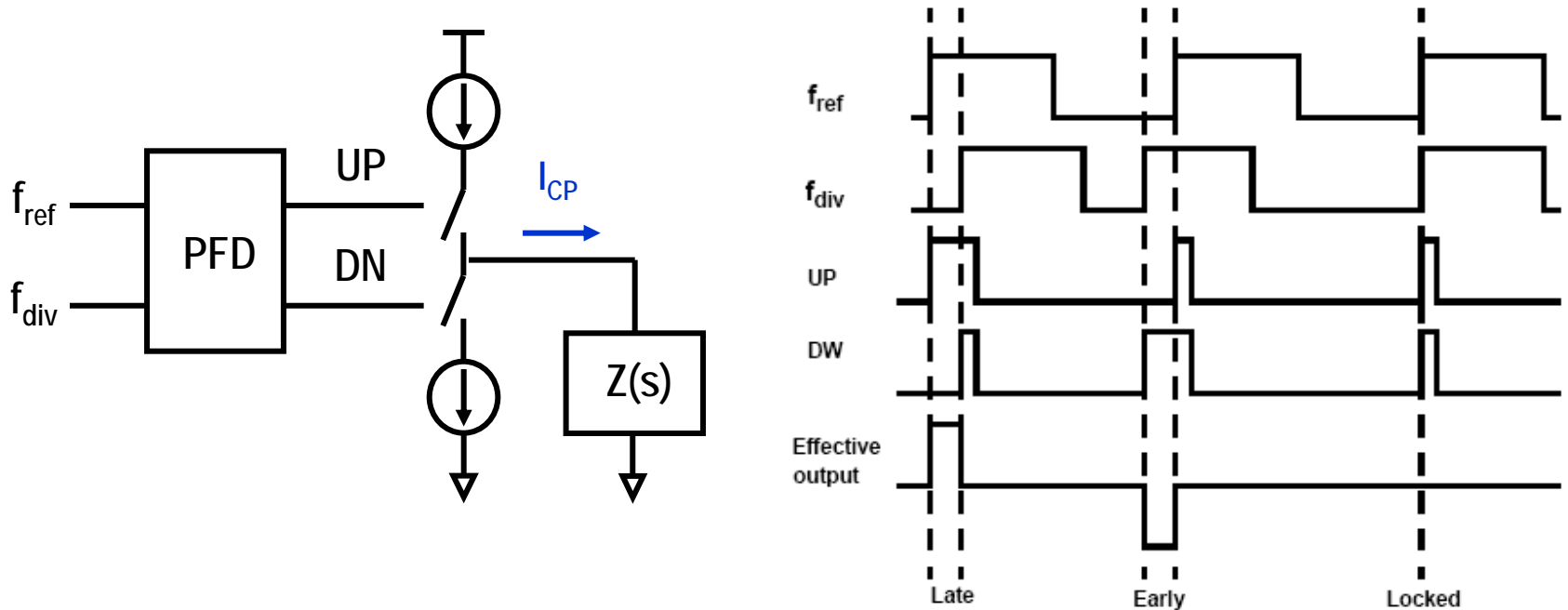
For example, see: J.F. Ewen et al, "CMOS Circuits for Gb/s Serial Data Communication",

Minimizing Dead-Zone Effect



- **Non-zero pulse width with zero phase error**
 - Set minimum CP turn-on time
- **Alternative method**
 - Phase detection with non-zero static phase offset

Ideal Charge Pump



- **Eliminates the need for active filter**
If $Z(s) = 1/sC$, then $V_z = I_{CP}/sC$
- **Nonideal charge pump**
 - Clock skew in digital clock generation
 - Reference spur in frequency synthesis

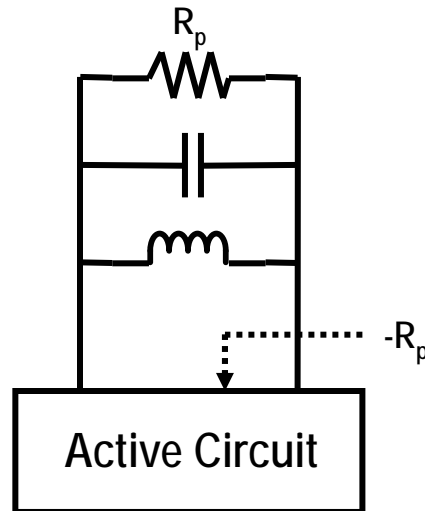
Phase Detectors for CDR PLLs

Phase Detector	Alexander (ISSCC'07, pp. 228-229)	Eye Tracking (ISSCC'08, pp. 98-99)	Hogge (JSSC'06, pp. 2566-76)	LPD+ $\Delta\Sigma$ Mod (ISSCC'09, pp. 186-187)
Simplified Block Diagram (Half-Rate)				
Type	Bang-Bang (Early/Late)	Bang-Bang (Early/Late/Hold)	Linear (PWM)	Linear (PDM Encoded Binary Stream)
Pros and Cons	<ul style="list-style-type: none"> • simple circuit • compatible w/ digital CDR • large quant. noise 	<ul style="list-style-type: none"> • compatible w/ digital CDR • medium quant. noise • 3-phase clock 	<ul style="list-style-type: none"> • simple circuit • no quant. noise • less compatible w/ digital CDR 	<ul style="list-style-type: none"> • small quantization noise • compatible w/ digital CDR • requires ADC

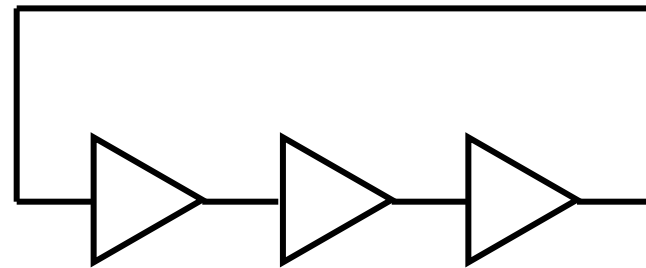
After K. Fukuda et al, "10Gb/s Receiver with Track-and-Hold-Type Linear Phase Detector and Charge Distribution 1st Order $\Delta\Sigma$ Modulator," ISSCC, paper 10.4, Feb. 2009

Oscillators

LC Oscillator



Ring Oscillator



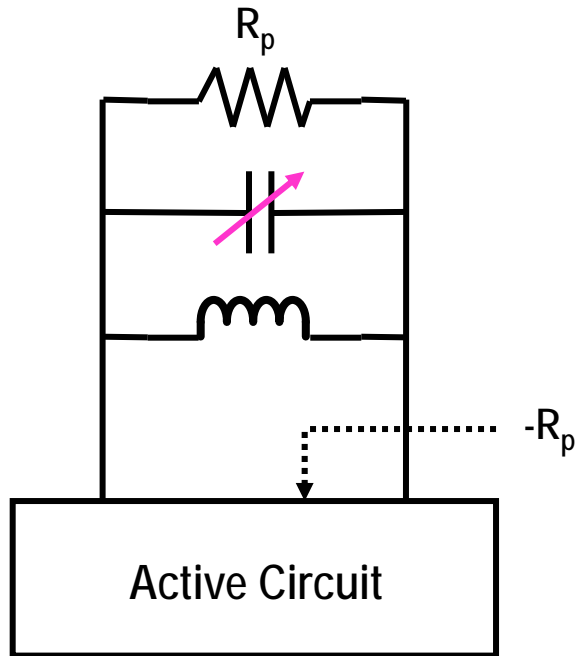
- **Resonator-based oscillator**
 - LC VCO most popular as an integrated VCO
- **Resonator-less oscillator**
 - Ring VCO most popular as an integrated VCO
 - Relaxation VCO has wide tuning range but noisier

For resonator-less CMOS VCOs: J.F. Ewen et al, "CMOS Circuits for Gb/s Serial Data Communication", IBM Jour. Research and Development, January/March, 1995

LC or Ring?

	LC	Ring
Max. frequency	✓	
Power (high f)	✓	
Tuning range		✓
Cost		✓
Noise	✓	
Multiphase		✓
Flexibility		✓

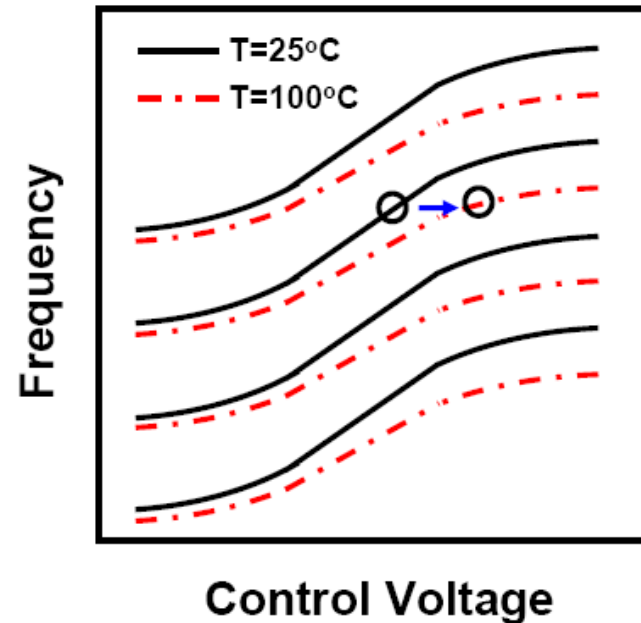
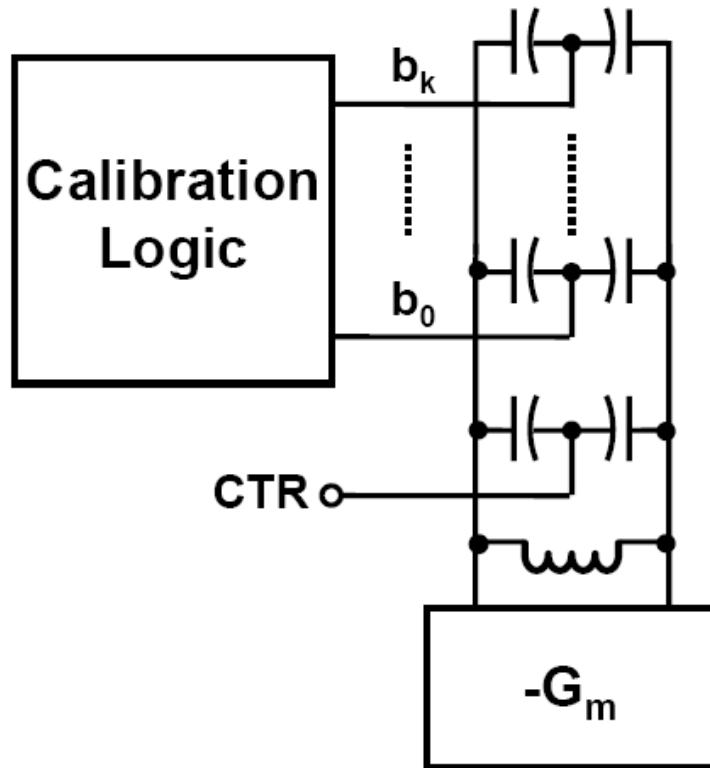
LC VCO



$$\omega_o = \frac{1}{\sqrt{LC}}$$
$$\frac{1}{Q_{res}} = \frac{1}{Q_{ind}} + \frac{1}{Q_{var}}$$

- Use variable capacitance to tune output frequency
- Good phase noise but narrow tuning range

Band-Switching LC VCO



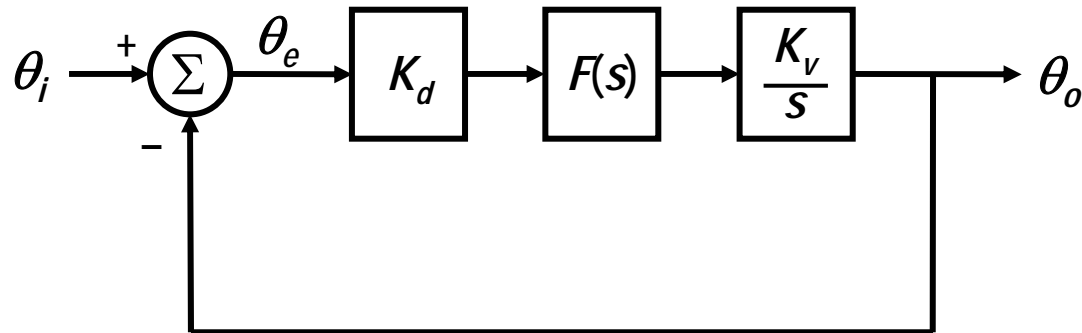
- Overcomes tuning range problem
- No calibration over temperature

After W. Rhee et al, "A Uniform Bandwidth PLL Using a Continuously Tunable Single-Input Dual-Path LC VCO for 5-Gb/s PCI Express Gen2 Applications", IEEE A-SSCS, Nov. 2007

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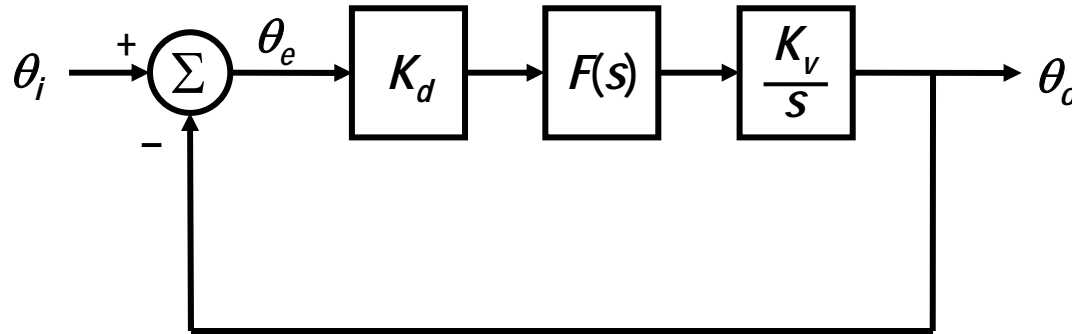
Typical PLL Linear Model



$$\text{If } \theta_e = c, \text{ then } \omega_o - \omega_i = \frac{d\theta_o}{dt} - \frac{d\theta_i}{dt} = \frac{d\theta_e}{dt} = 0$$

- *Phase locked means constant phase error, or actually “zero-frequency locked”*
- **Is linear model good enough to analyze PLL?**
 - Yes, when we are interested in PLL within lock-in range

Loop Order and Types



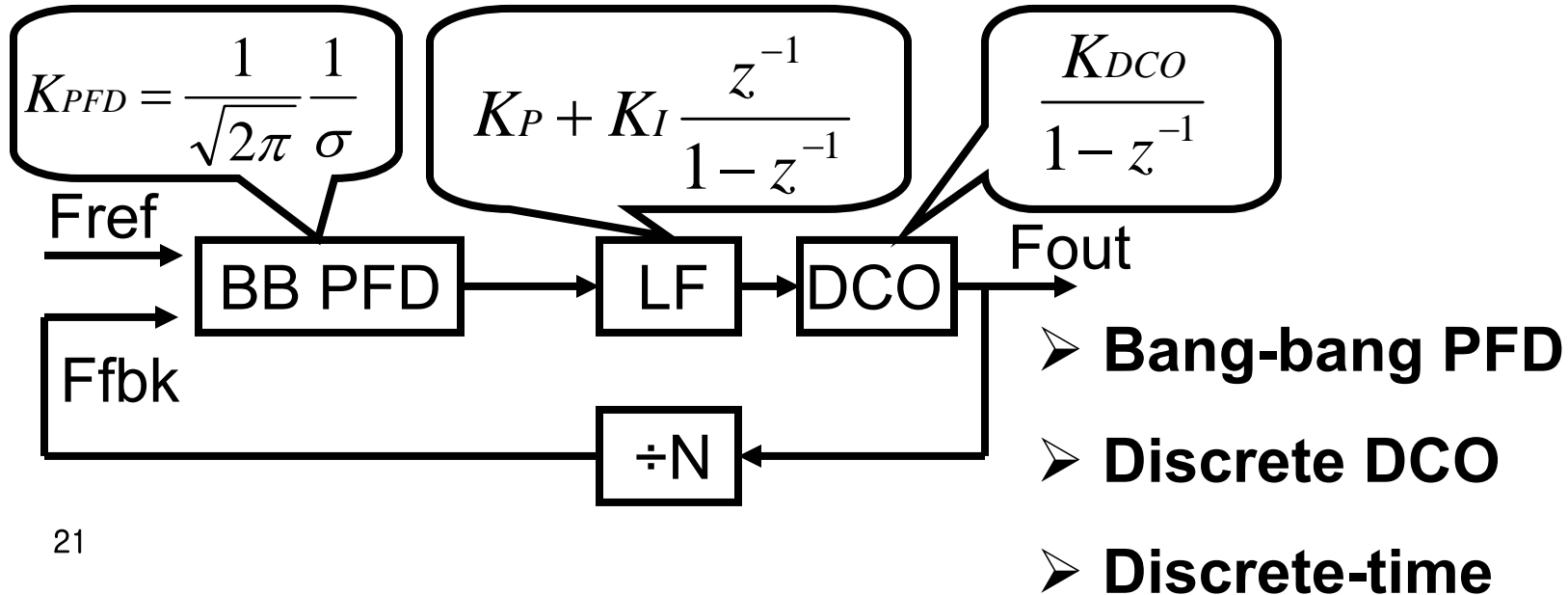
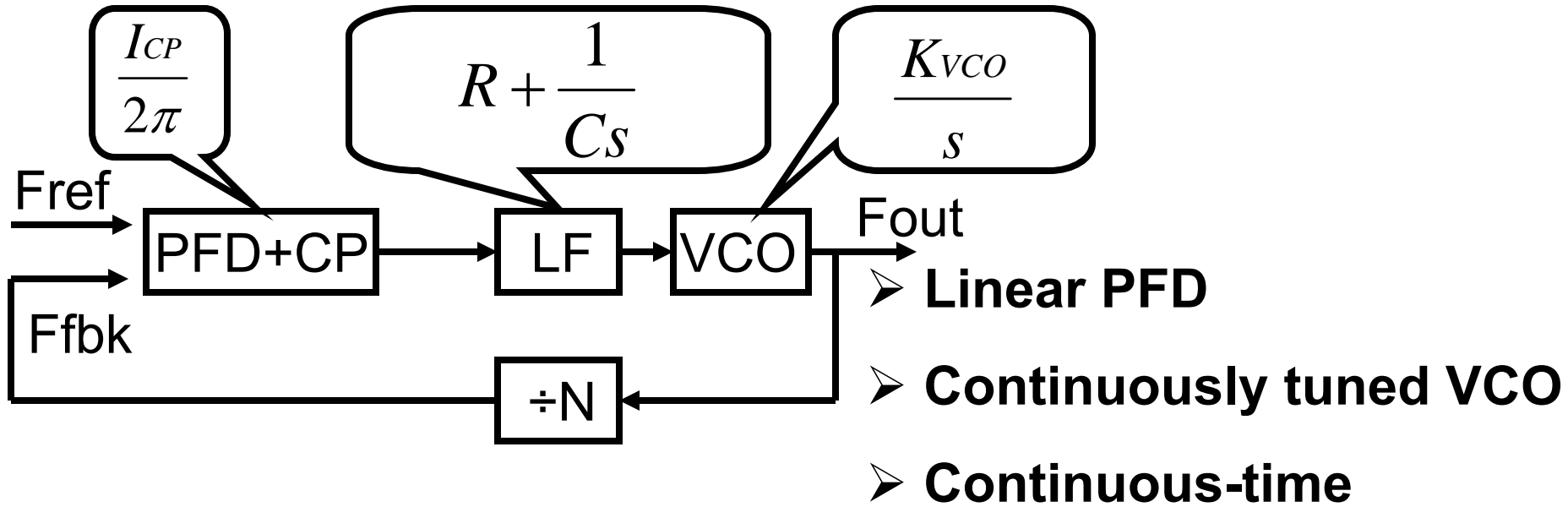
$$G(s) = K_d \cdot F(s) \cdot \frac{K_v}{s}$$

$$H(s) = \frac{\theta_o}{\theta_i} = \frac{G(s)}{1 + G(s)} = \frac{K_d K_v F(s)}{s + K_d K_v F(s)}$$

$$E(s) = \frac{\theta_e}{\theta_i} = \frac{1}{1 + G(s)} = \frac{s}{s + K_d K_v F(s)}$$

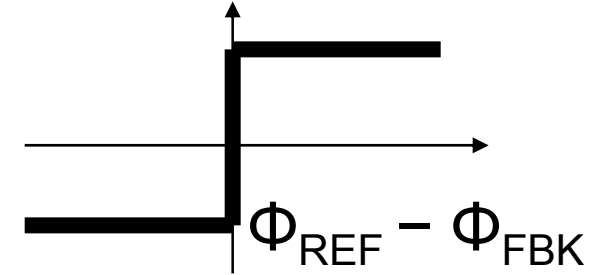
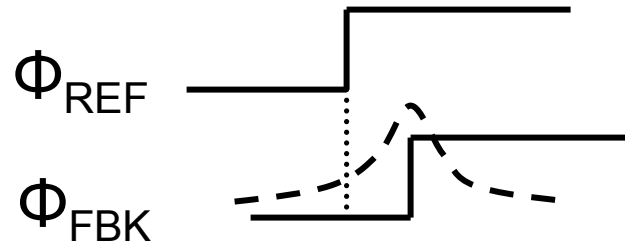
- Order - Number of poles of $H(s)$
- Type - Number of integrators within loop

Charge-Pump APLL vs BB-DPLL



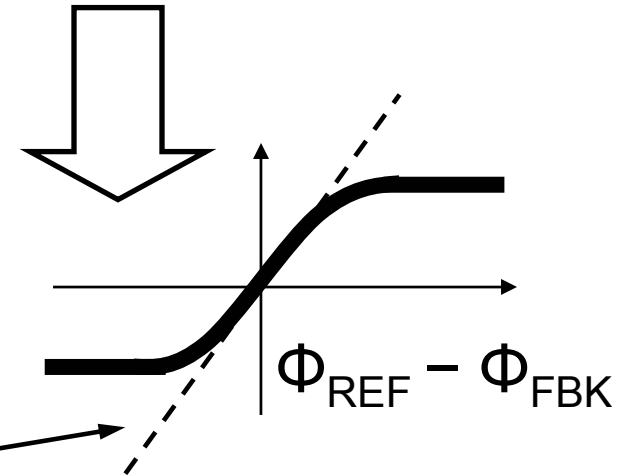
BB-PFD Linearization and Gain

Original non-linear transfer function:



Linearized transfer function:

$$K_{PFD} = \frac{1}{\sqrt{2\pi}} \frac{1}{\sigma_{IN}}$$



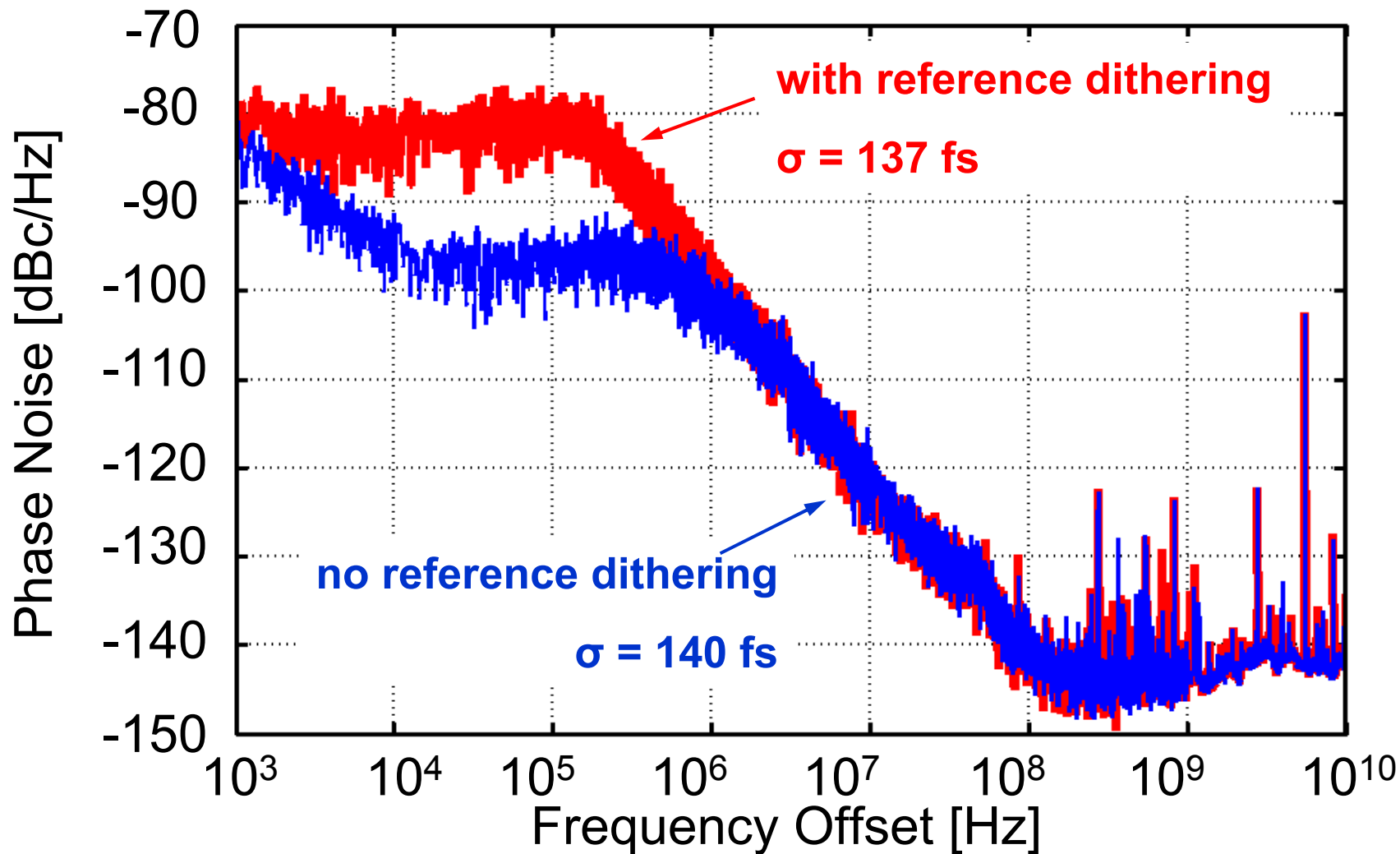
J. Lee 2004

N. Da Dalt 2008

- BB-PFD gain is inversely proportional to input jitter
- Low-noise BB-DPLL will have non-linear dynamics

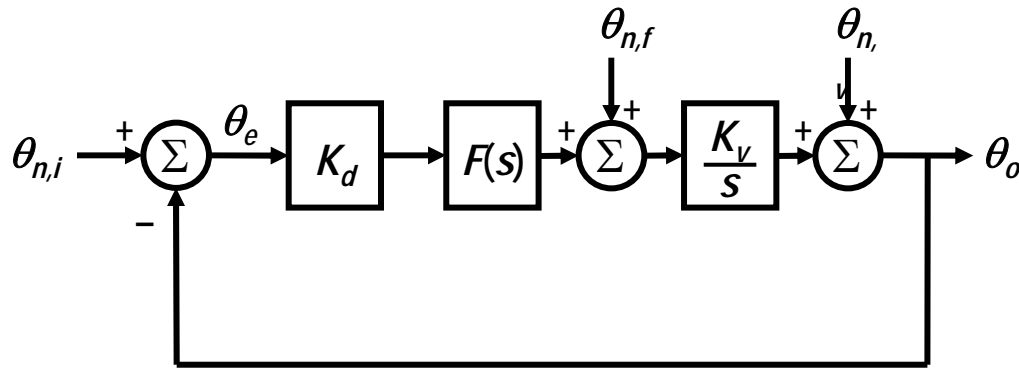
DPLL Bandwidth Control by Reference Dithering

A. Rylyakov et al, "Bang-Bang Digital PLLs at 11 GHz and 20 GHz with sub-200-fs Integrated Jitter for High-Speed Serial Communication Applications" ISSCC'09



- Measured phase noise plots shown for 11-GHz DPLL with LC-DCO
- Reference dithering does not degrade the rms jitter σ (6.5 MHz to 5.5 GHz)

Noise Transfer Function

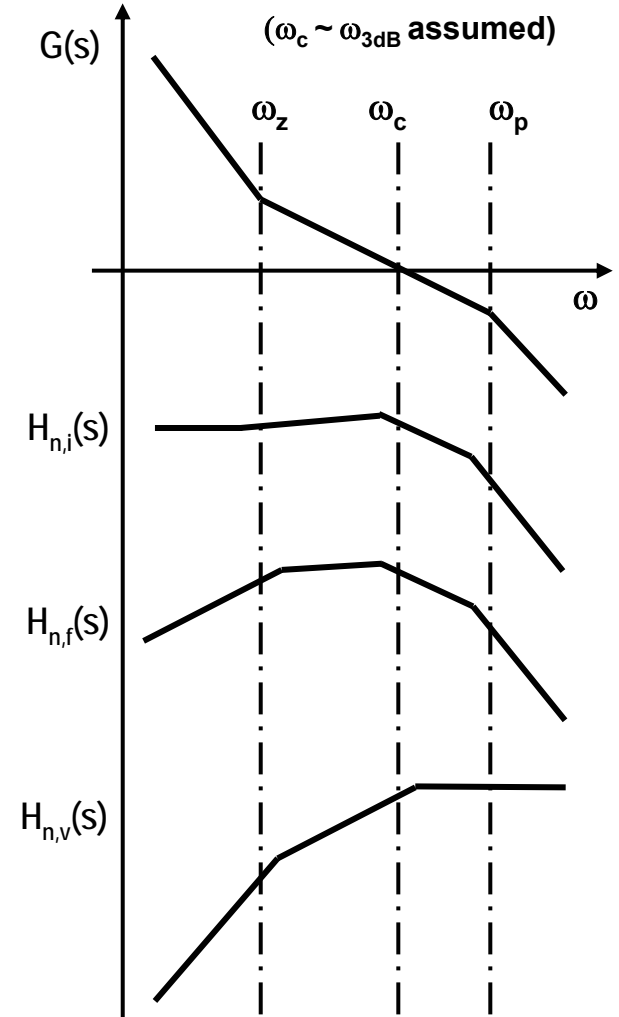


$$G(s) = K_d \cdot F(s) \cdot \frac{K_v}{s}$$

$$H_{n,i}(s) = \frac{\theta_o}{\theta_{n,i}} = \frac{G(s)}{1 + G(s)}$$

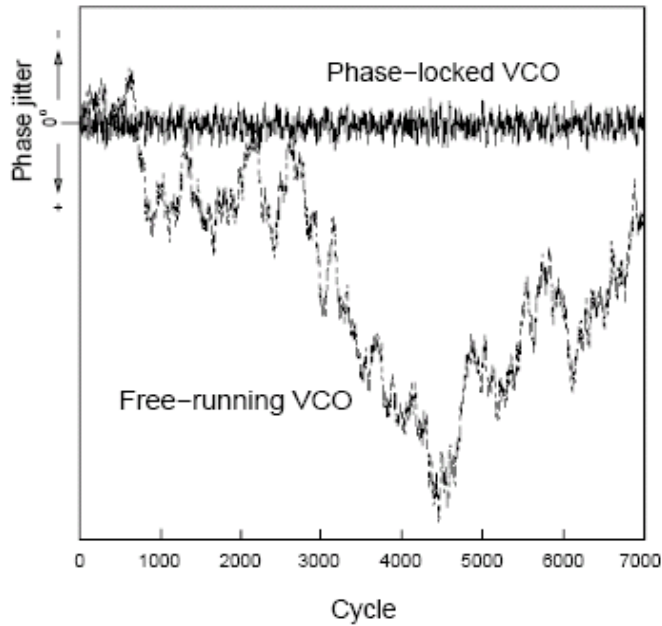
$$H_{n,f}(s) = \frac{\theta_o}{\theta_{n,f}} = \frac{K_v / s}{1 + G(s)}$$

$$H_{n,v}(s) = \frac{\theta_o}{\theta_{n,v}} = \frac{1}{1 + G(s)}$$

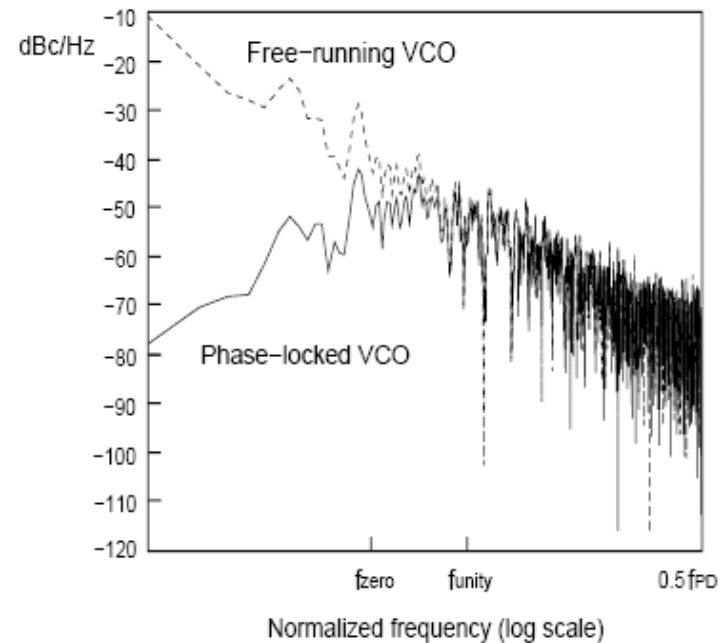


Simulation: VCO Noise Suppression

Time Domain



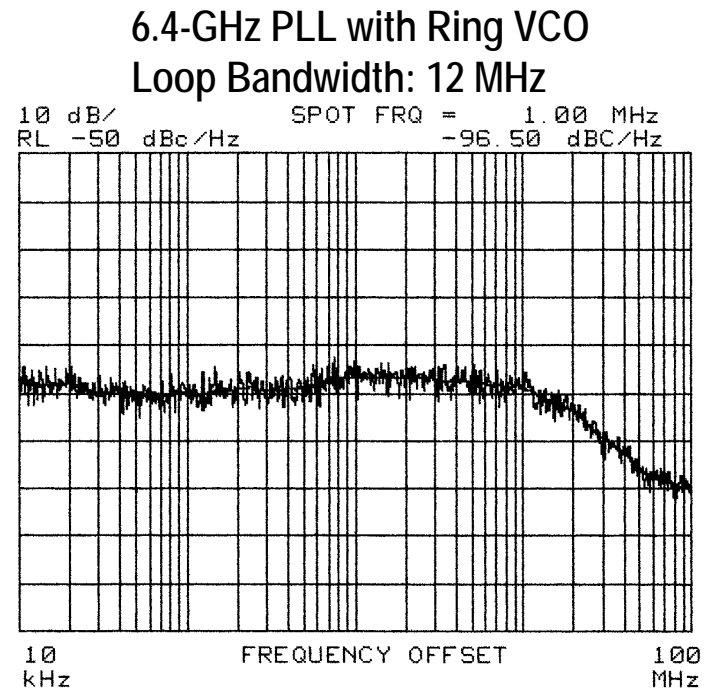
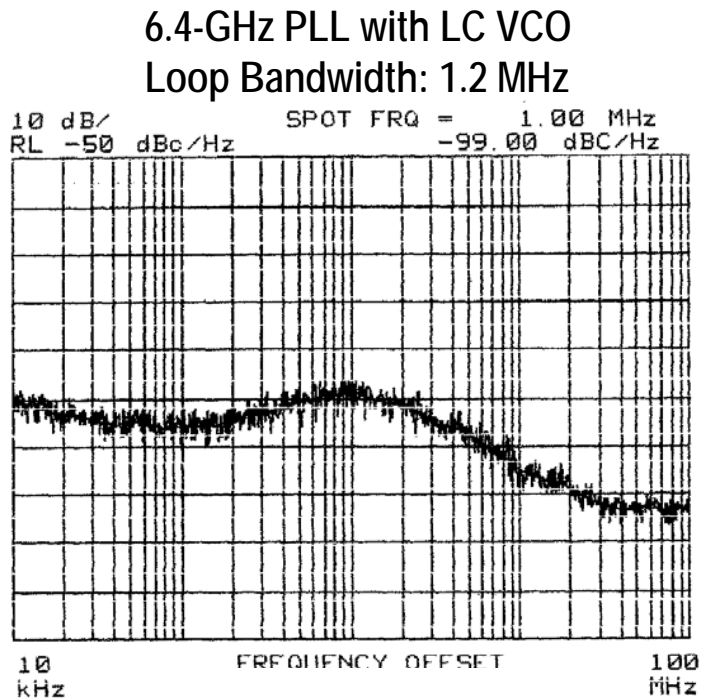
Frequency Domain



- **Low-frequency noise suppressed by open-loop gain**

After W. Rhee, ICSICT 2008 Short Course on Frequency Synthesizers and PLLs

Noise Performance: LC vs. Ring



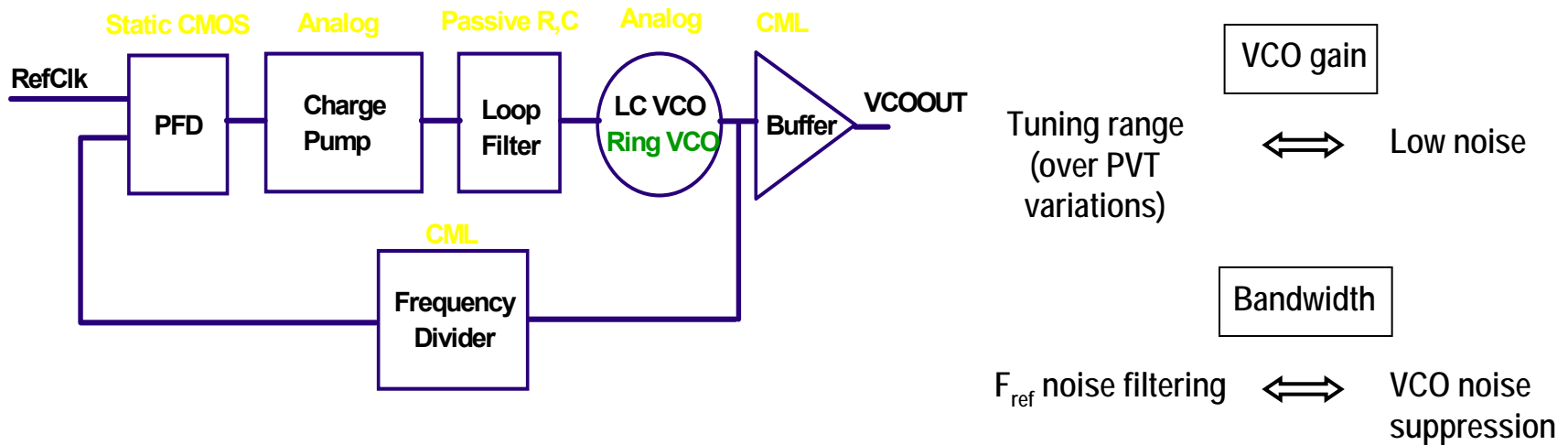
- Similar phase noise at 1MHz offset, but RJ is different
- Higher-gain ring VCO is more sensitive to substrate noise

After W. Rhee et al, "Experimental Analysis of Substrate Noise Effect on PLL Performance"
IEEE Tran. CAS-II, July 2008

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Clock Generation: Analog CP-PLL



Challenges

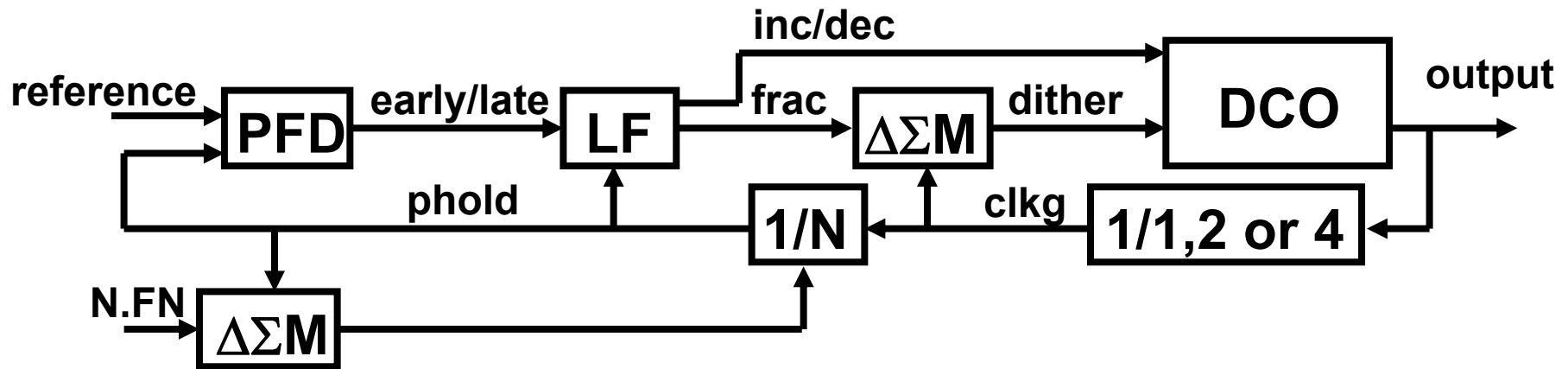
- Technology scaling
- Multiple data rates
- Large loop filter components
- Special analog devices
- Noise isolation, deterministic jitter

Can All-Digital PLL Help?

- **Scales with technology node**
 - Analog passive element is a bottleneck for area
 - Area/cost reduction with all-digital solution
- **Programmable**
 - Loop parameters can be accurately controlled
 - Advantageous when models are not mature
- **Immune to leakage current**
 - Large capacitor is not needed anymore
 - No need of thick-oxide transistor just for LPF

Digital PLL Example: Block Diagram

A. Rylyakov et al, "A Wide Tuning Range, 1 GHz – 15 GHz Fractional-N All Digital PLL in 45nm SOI" CICC08

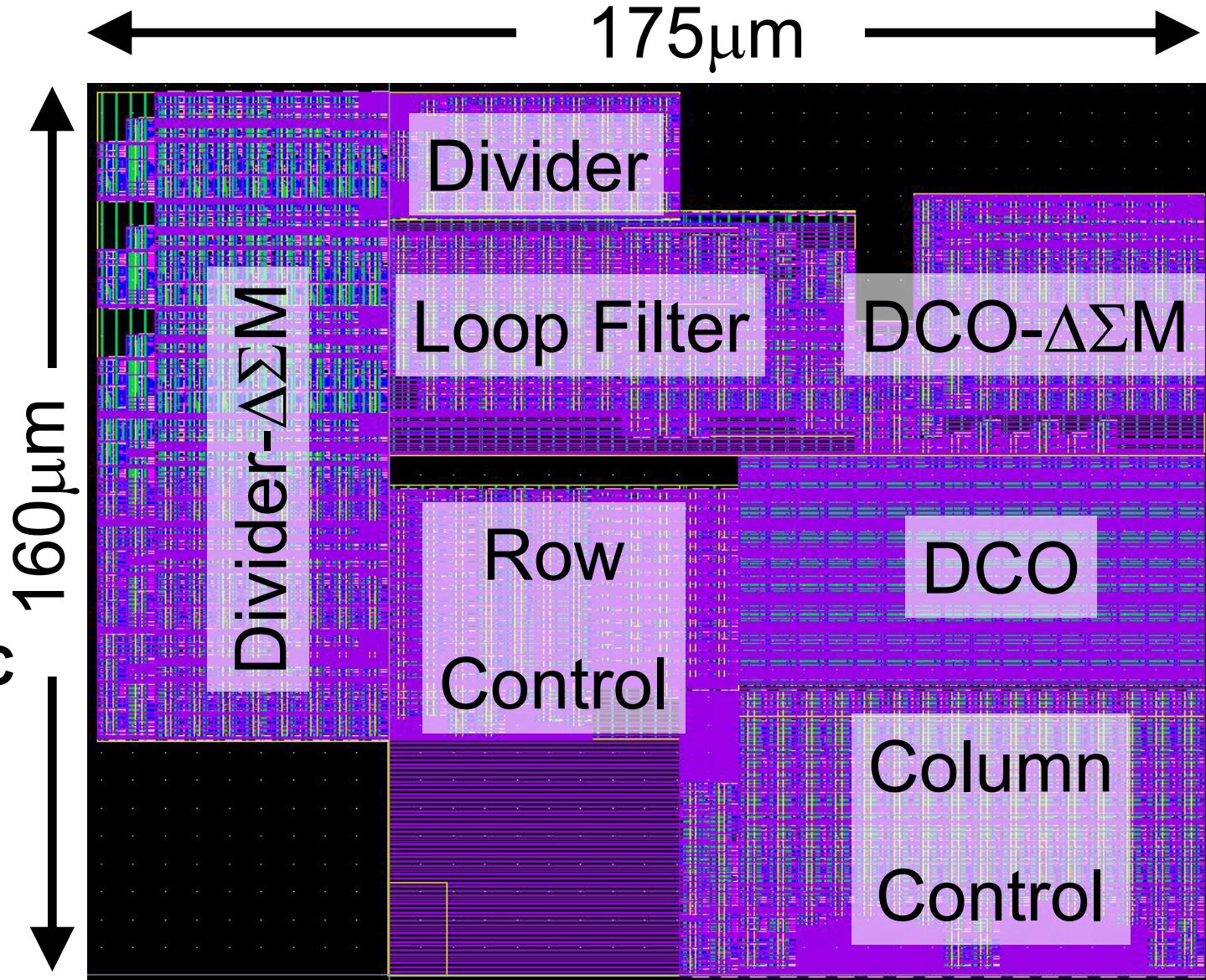


- All gates are static CMOS (no CML, etc)
- 3 custom cells: 1 in the PFD, 1 in the DCO, plus voltage level shifter between the DCO and the logic power supplies
- Highly modular design: loop filter (LF), multimodulus feedback divider (1/N) and both $\Delta\Sigma$ modulators use same adder

DPLL Example: Physical Design

A. Rylyakov et al, "A Wide Tuning Range, 1 GHz – 15 GHz Fractional-N All Digital PLL in 45nm SOI" CICC 08

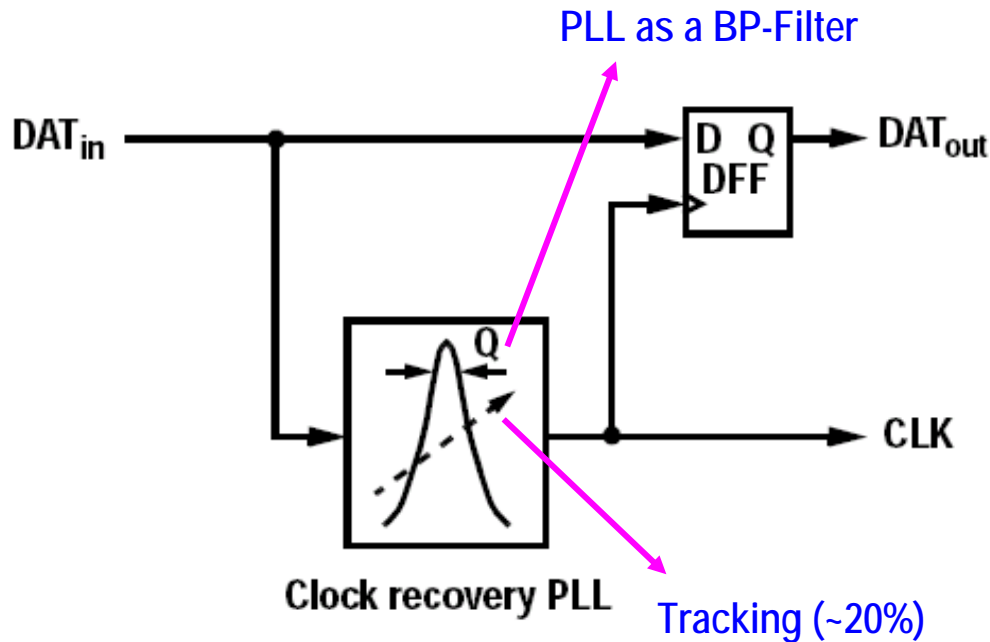
- Technology:
IBM 45nm
SOI CMOS
- Transistor
Count: ~25k
- Pd: 19mW,
Jpp: 13ps @
4GHz, 1V, 65°C



Outline

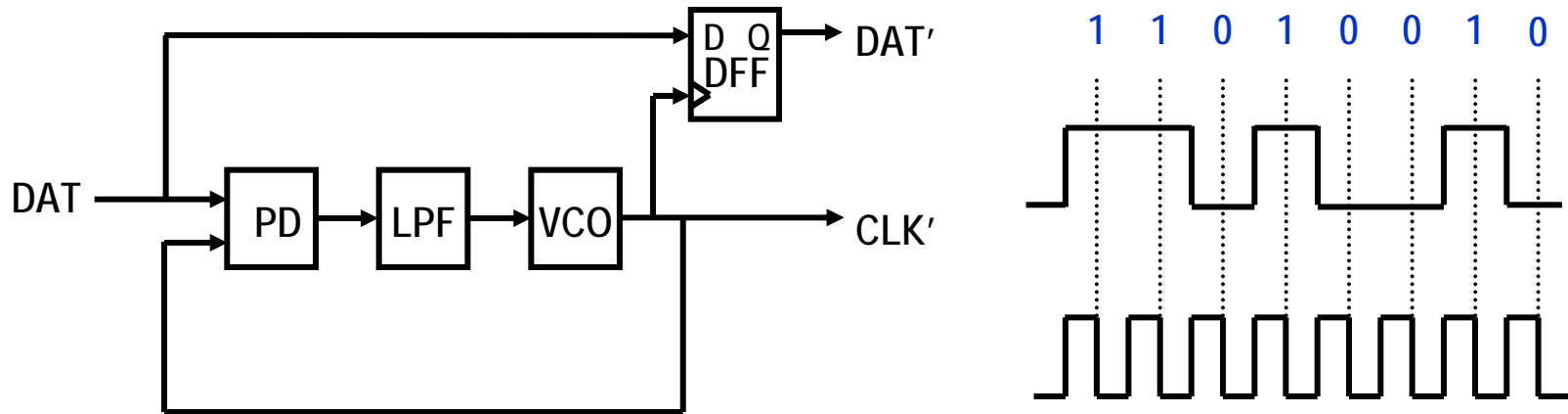
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PLL-Based Clock Recovery



- Requires frequency acquisition (e.g. quadri-correlator)
- Bang-bang loops preferred over traditional approaches
 - Narrow-band filtering approach requires non-linear processing of NRZ data spectrum
 - ✓ Binary quantized phase detectors maintain optimum sampling point over PVT => good for integration

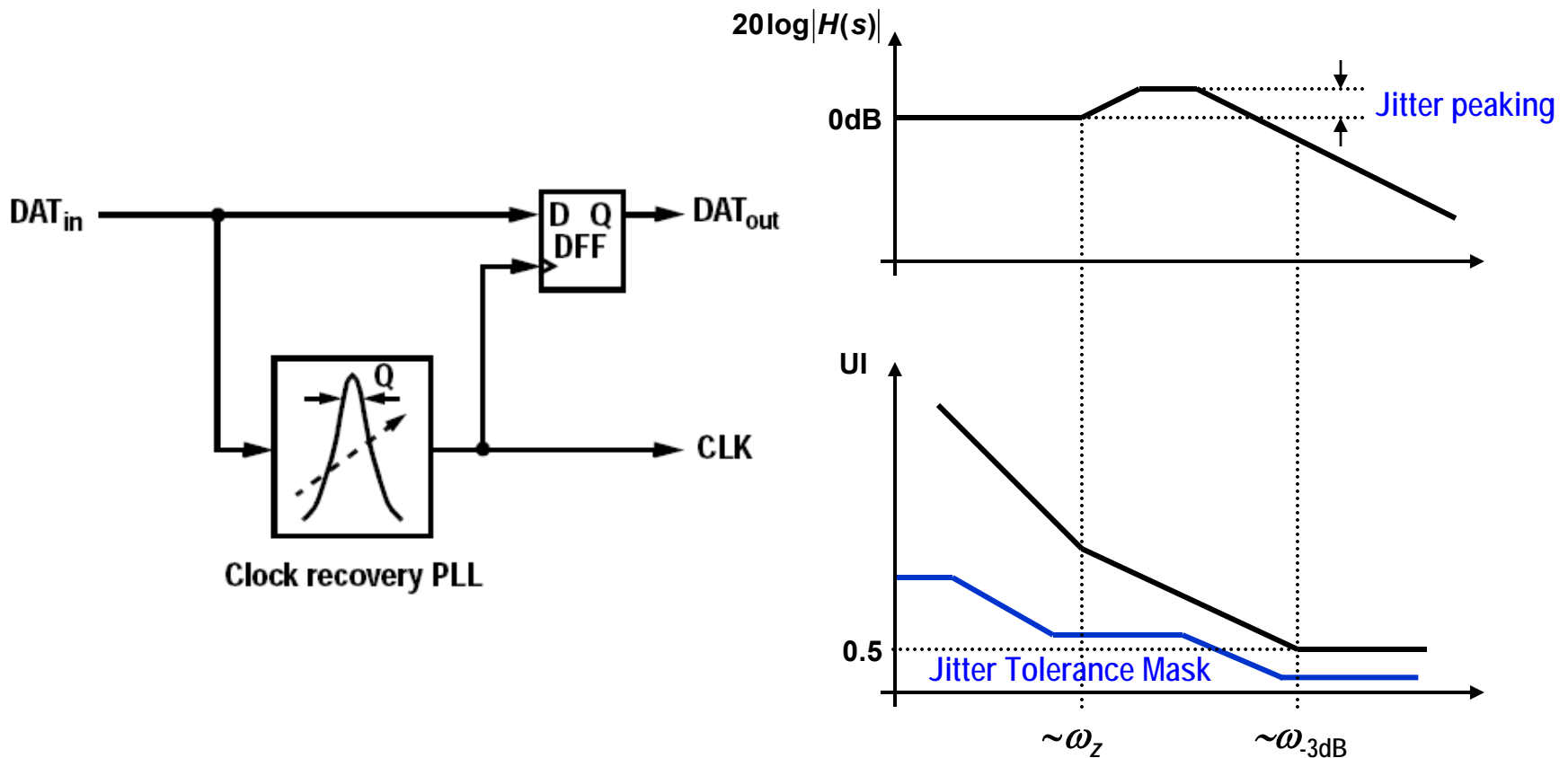
Data Retiming with Recovered Clock



- **Optimum sample time is at middle of bit window**
e.g. Synchronizing at CLK rising edge & data slicing at falling edge
- **Bit error when clock jitter $> 0.5UI$**
- **Data-retiming latch can be part of PD (e.g. Hogge and Early/Late PDs)**

For more on bang-bang loop CDR design methodology: R. Walker, "Clock and Data Recovery for Serial Digital Communication", ISSSCC Short Course, February 2002

Jitter Transfer and Jitter Tolerance



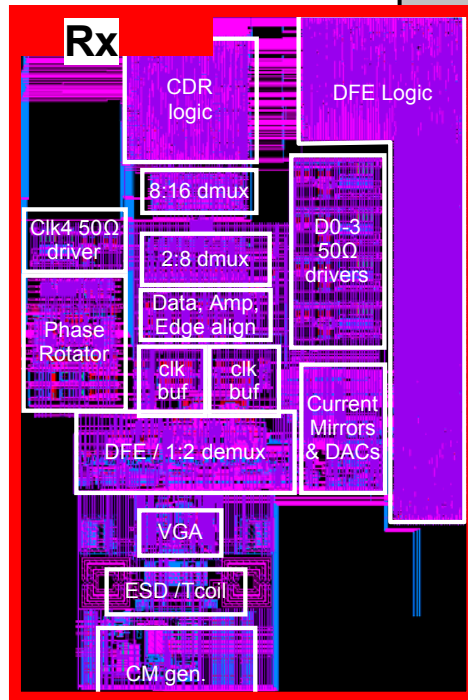
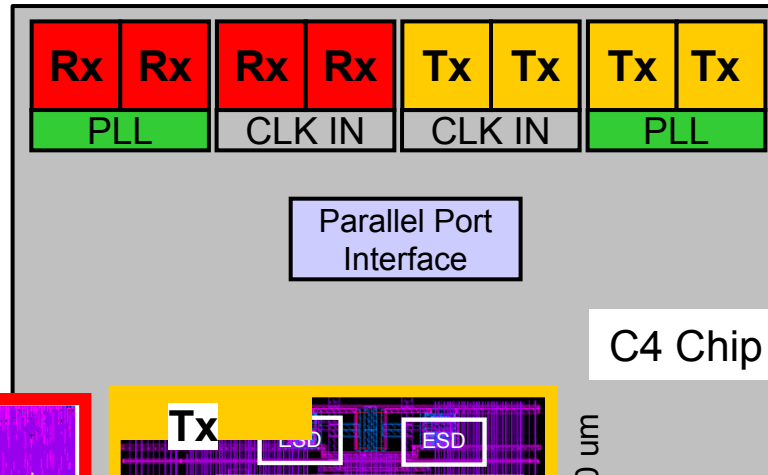
- **Extract clock information from noisy data and do retiming**
 - Jitter transfer – Noise filtering performance of PLL
 - Jitter tolerance – Data tracking performance of PLL

Dual-Loop CDR: A 10-Gb/s Demonstrator

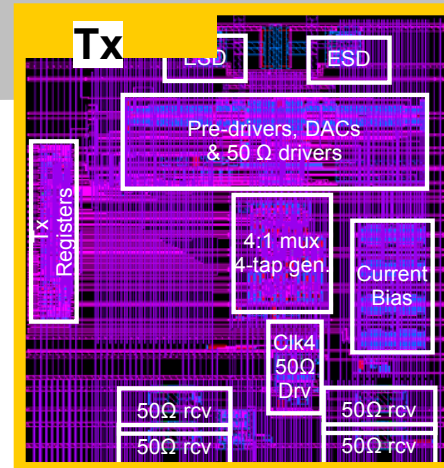
M. Meghelli et al, "A 10Gb/s 5-tap DFE / 4-Tap FFE Transceiver in 90nm CMOS Technology", ISSCC'06

Goal:

- Minimize PLL/pin ratio in complex SoC ICs
- Reduce power and area

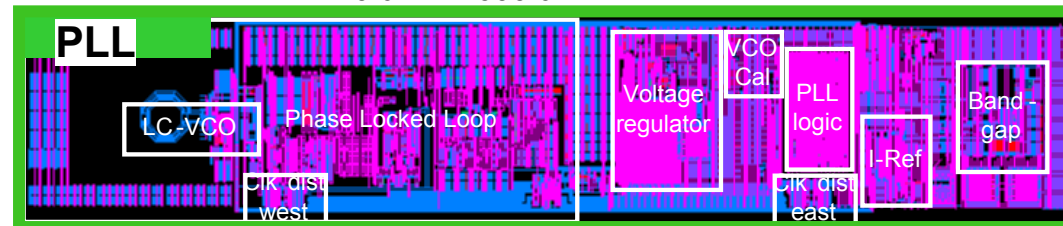


800 um x 540 um

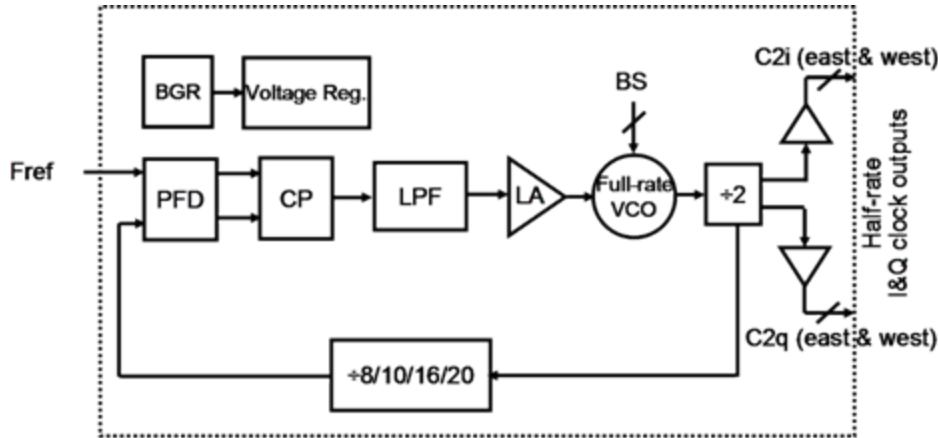


400 um x 400 um

270 um x 1600 um



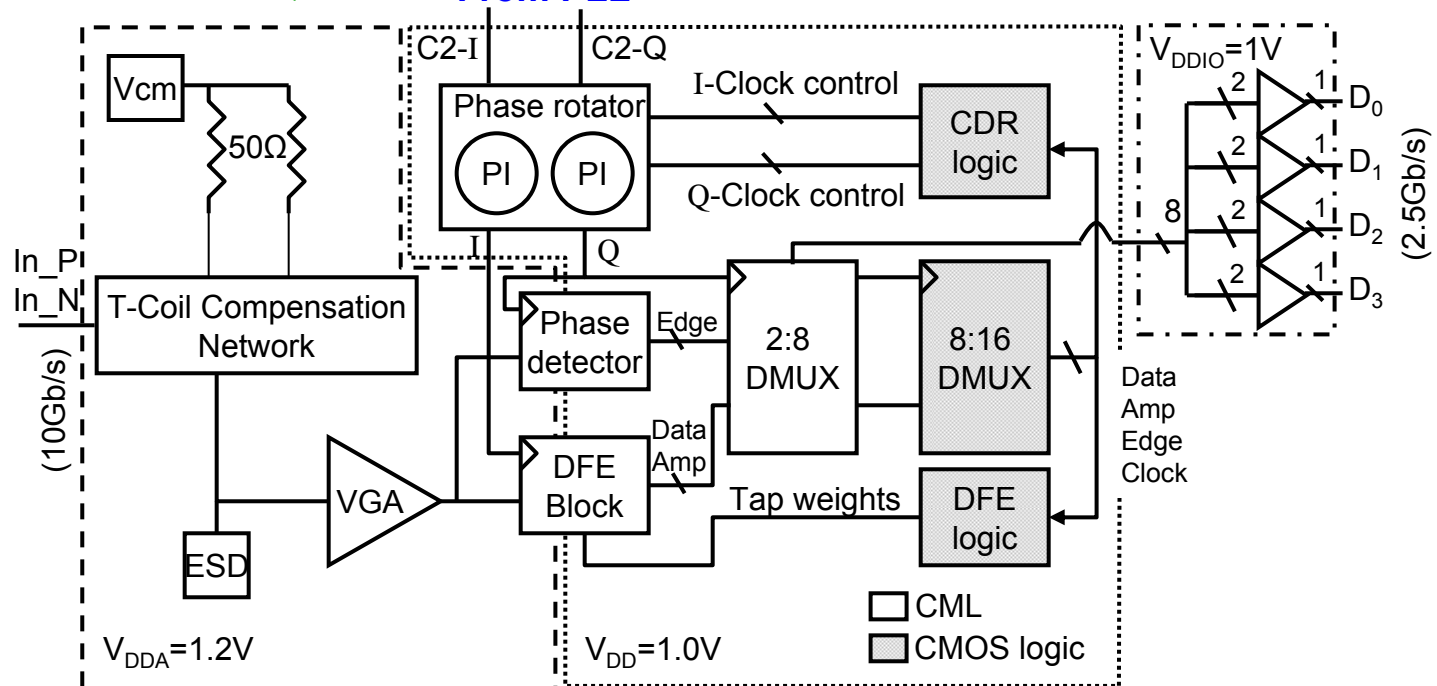
10-GHz PLL and 10Gb/s Receiver



Design Features:

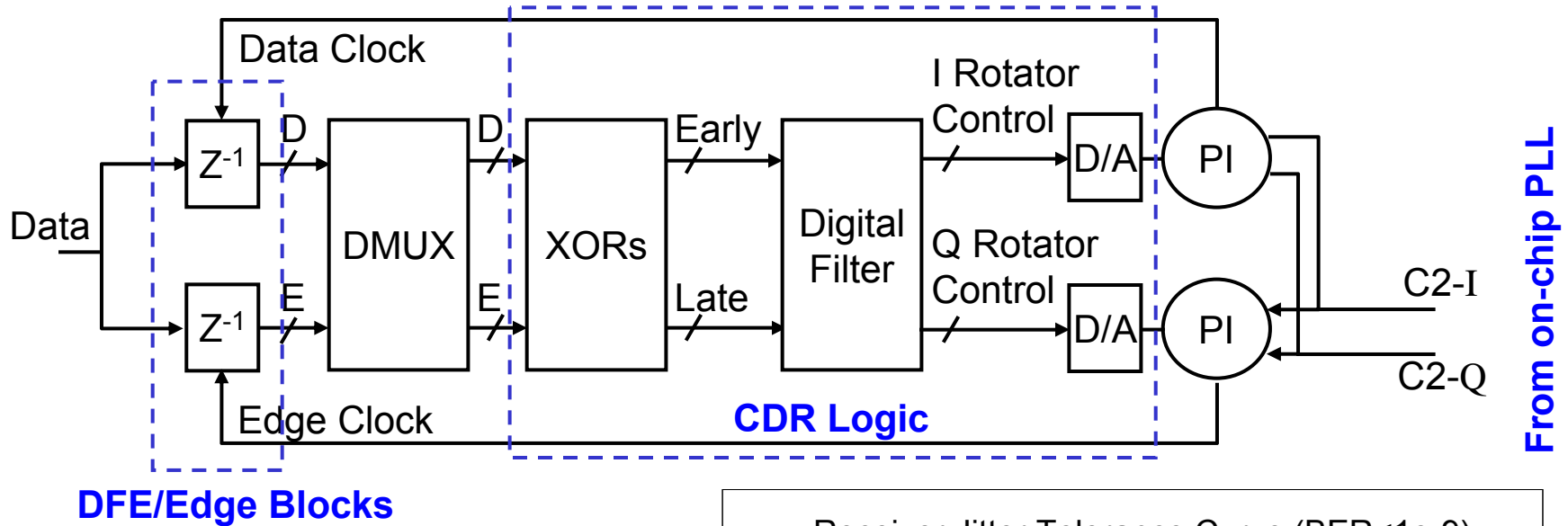
- Digital CDR using phase interpolation*
- Half-rate clocking with 5-GHz PLL
- 130mW (with DFE & CDR logic)

10-GHz PLL to generate 5-GHz I/Q clocks From PLL



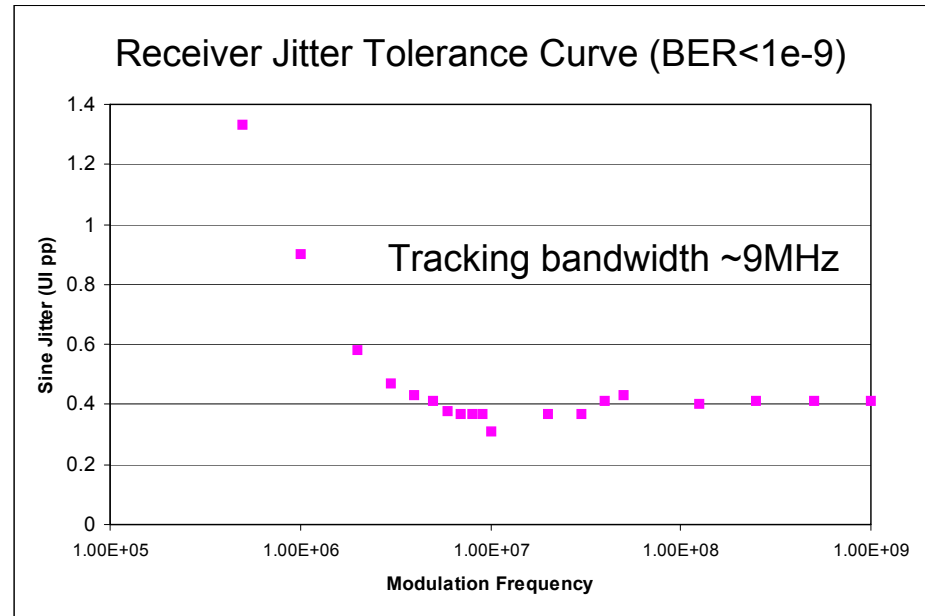
10-Gb/s Receiver with CDR and DFE Loops

CDR Loop



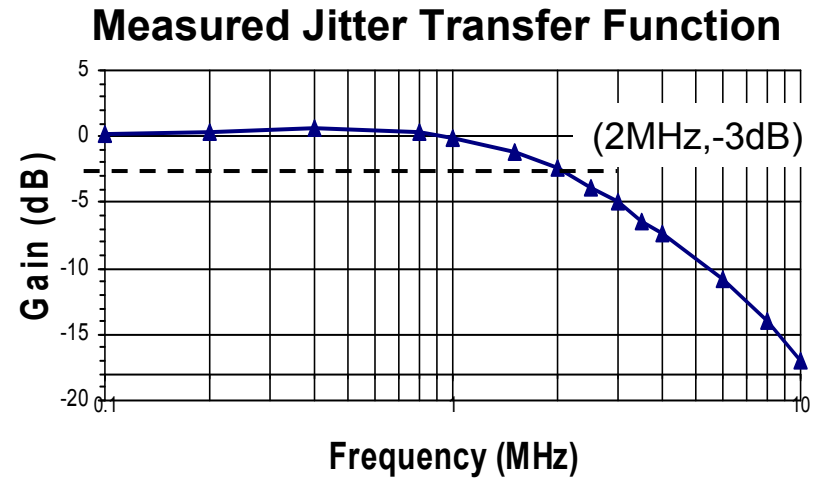
Key Features:

- Fully-digital “bang-bang” loop
- Can handle up to +/- 4000ppm frequency offset
- Independent I,Q control

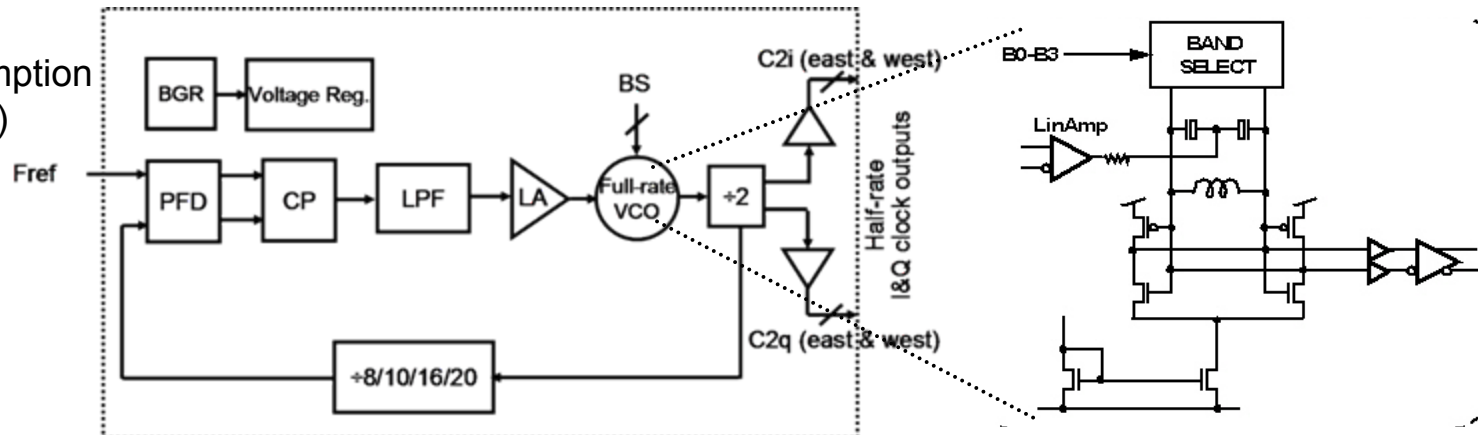


10-GHz PLL Characteristics

PLL Performance	TxPLL	RxPLL
Min freq (GHz)	8.98	8.96
Max freq (GHz)	13.54	13.47
Mean freq (GHz)	11.26	11.22
Lock range (GHz)	4.56	4.52
	+/-20.2%	+/-20.1%
Fine tune hold range	5.8%	5.8%
Phase noise @ 10MHz offset (dBc/Hz, quarter rate clock)	-117.8	-117.7
	1.5	1.4
	0.64	0.64



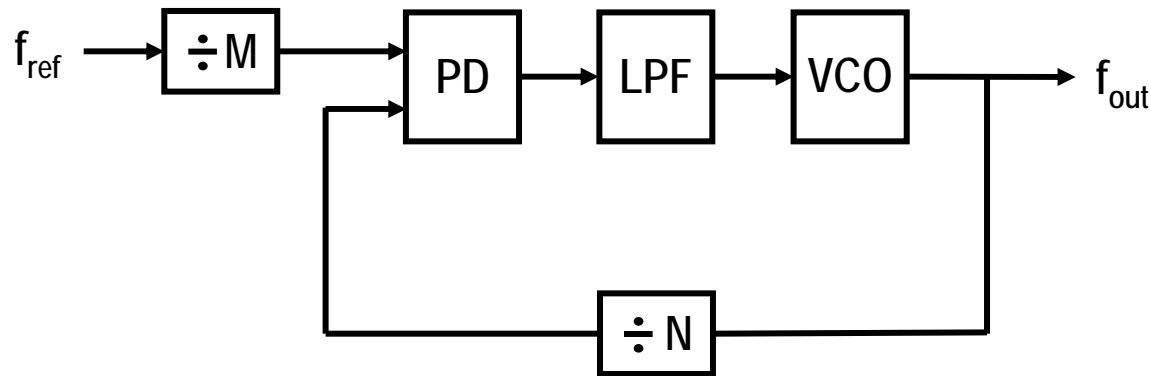
100mW power consumption
(with clock distribution)



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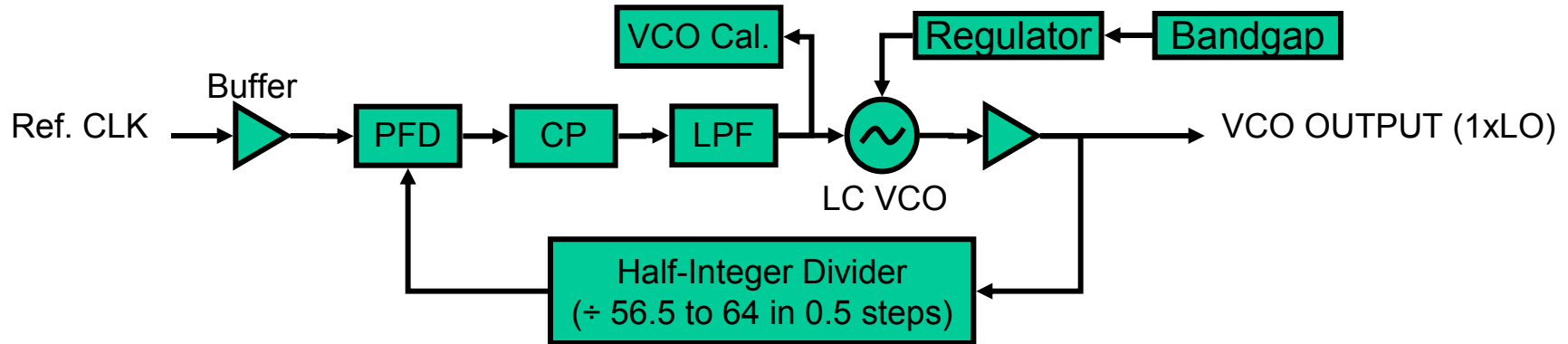
Frequency Synthesis by Phase Lock



$$f_{out} = \left(\frac{N}{M} \right) \cdot f_{ref}$$

- **Simple frequency synthesis by changing division ratio**
- **Frequency accuracy is as good as reference**
- **Longer settling time for larger N**

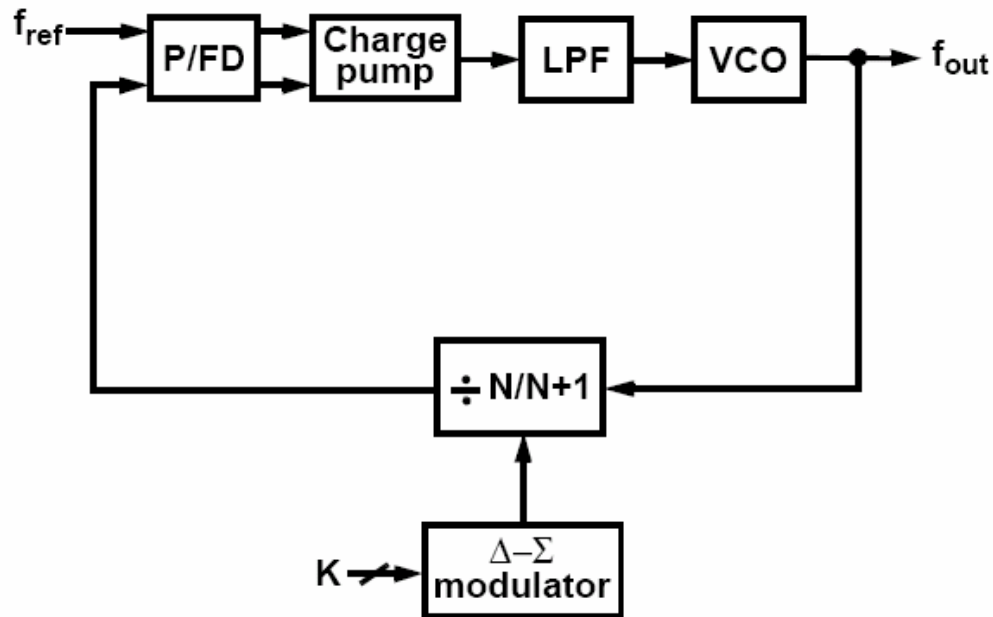
20-GHz Frequency Synthesizer for mmWave Wireless



Power Consumption	144 mW
Reference Clock/Resolution	285.71 MHz / 500 MHz 308.57 MHz / 540 MHz
VCO Frequency	15.95-18.81 GHz (16.5%)
In-band Phase Noise @100kHz	-90 dBc/Hz
Phase Noise @10MHz	-126 to 123 dBc/Hz
Fractional Spur	-55 to -78 dBc
Reference Spur	-60 to -77 dBc
RMS Noise/Jitter (1MHz-1GHz integration)	0.5° to 1° 0.08 to 0.16ps

- **Type-II, 4th order PLL**
- **Supports IEEE 802.15.3c 60-GHz frequency plan (with a tripler at the output)**
- **Half-integer divider allows finer resolution at higher ref-clock**
- **LC-VCO includes amplitude control loop**
- **Implemented in SiGe BiCMOS**

Fractional- N with $\Delta\Sigma$ Modulation



- Randomized modulus control with noise shaping
- Arbitrarily fine resolution with digital word
- Fractional- N PLL can also provide a solution for wireline by enabling multiple reference frequencies

Outline

- Introduction
- PLL Components
- PLL Modeling and Noise
- Design Examples
 - Clock Generation
 - Clock and Data Recovery
 - Frequency Synthesis
- **Summary**

Active Research Topics

- **Low-jitter dual-loop PLL/DLL CDRs for high-speed serial links**
- **All-digital PLLs**
- **Adaptive PLLs with self calibration**
- **On-chip testability and diagnosis (BIST)**
 - **Jitter monitor, supply voltage monitor**
- **Low-noise wide-range VCOs**
- **Clock generation with spread-spectrum for EMI reduction**
- **Wideband $\Delta\Sigma$ fractional-N PLLs for wireless/wireline links**
 - **Addressing nonlinear effects and quantization noise**

→ More innovation required!

Summary

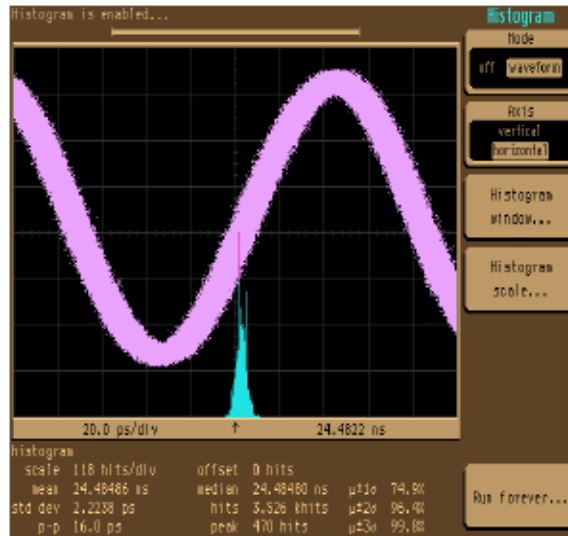
- **PLL is a “simple and elegant” control system with a lot of complexity**
- **Both time and frequency domain techniques are required for leading-edge PLL design and analysis**
- **There is still room for creativity and innovation in PLL-based sub-system design!**

Acknowledgements:

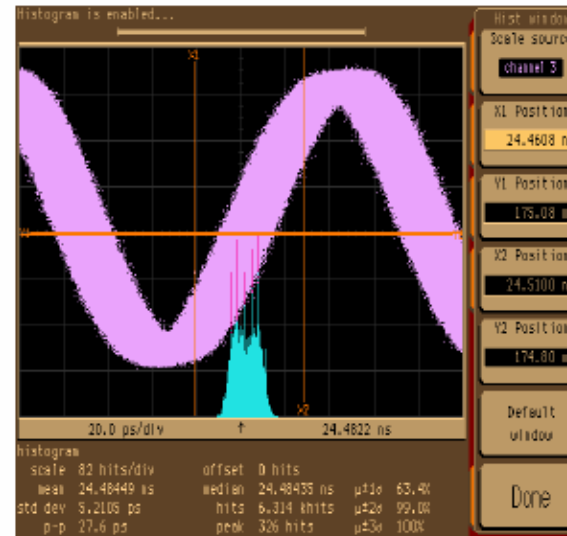
Many thanks to ex-IBM'er Prof. W. Rhee of Tsinghua University, for his 2008 ICSICT Short Course material on Frequency Synthesizers and PLLs. I am also grateful for the input from my colleagues, M. Meghelli, A. Rylyakov, D. Friedman and B. Floyd, at IBM.

More on Noise in Clock Subsystems

Quiet Environment



with Substrate Noise

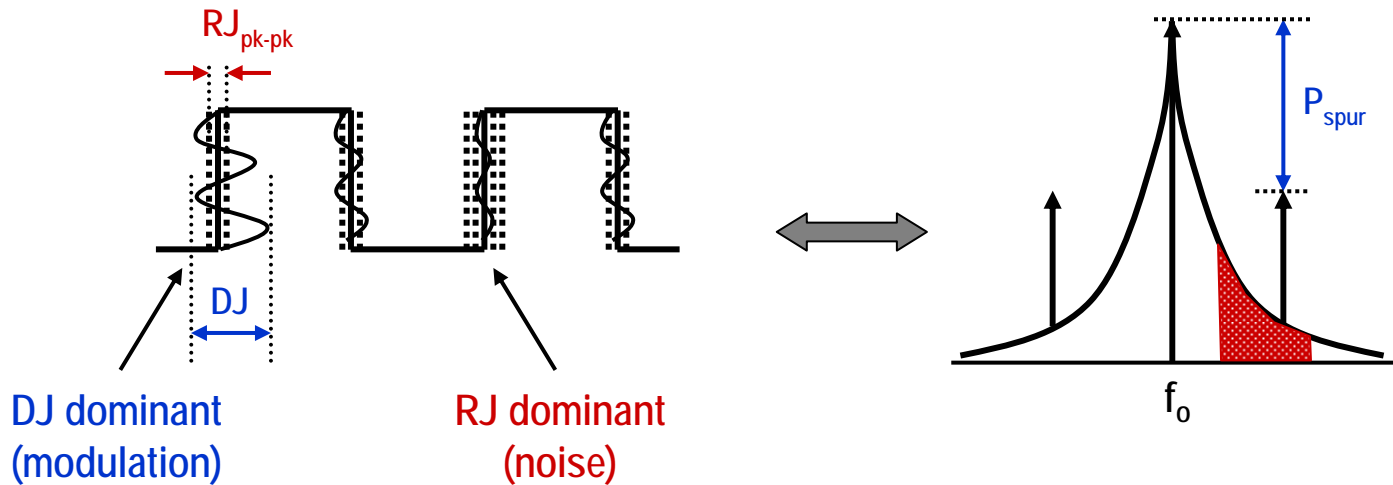


- **Difficult to identify noise contribution from each source in time domain**
- **Use frequency and time domain analysis**

Clock Noise

Time Domain

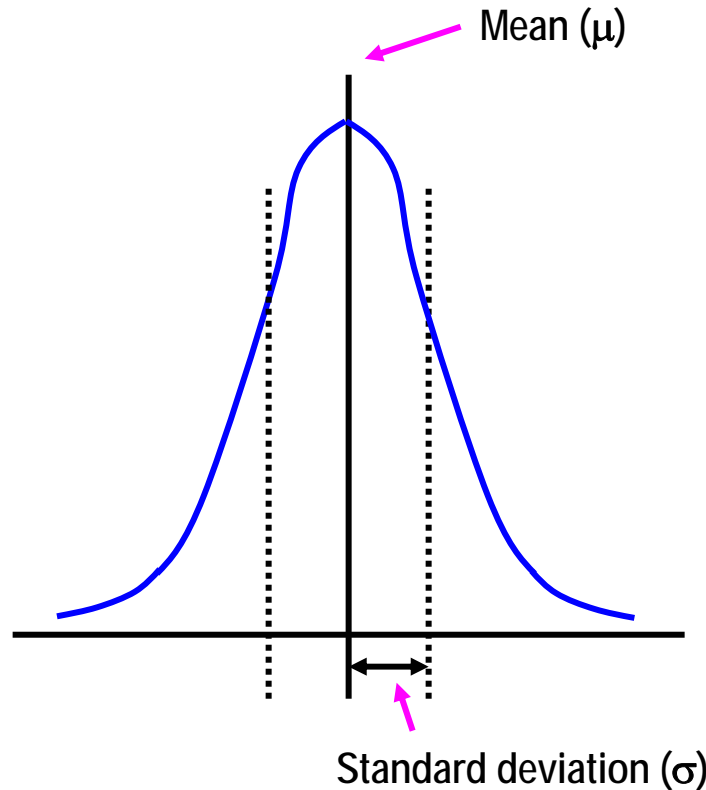
Frequency Domain



- **Total jitter (TJ)**
= **Random jitter (RJ) + Deterministic Jitter (DJ)**

Random Jitter (RJ)

Conversion Between RMS and Peak-to-Peak Jitter at a Specified BER

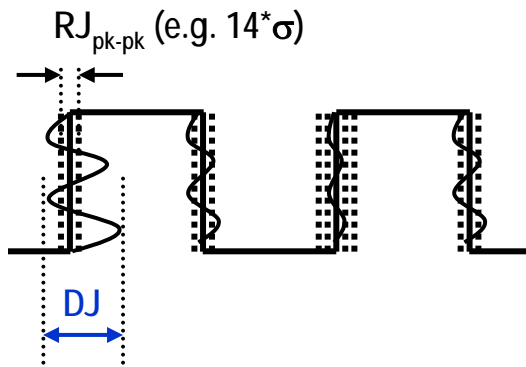


BER	RJ _{pp}
1.35×10^{-3}	6σ
3.17×10^{-5}	8σ
2.87×10^{-7}	10σ
9.87×10^{-10}	12σ
1.00×10^{-12}	14.069σ

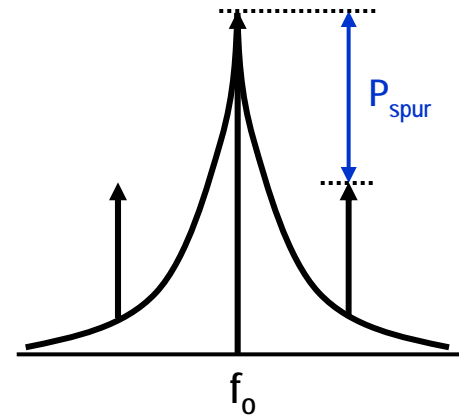
- **Gaussian distribution extends indefinitely beyond σ**
- **Need boundaries for communication link jitter budget**
- **Samples outside peak-to-peak range \Rightarrow BER as $\text{erfc}(x)$**

Deterministic Jitter (DJ)

Time Domain



Frequency Domain



$$DJ = 0.01 UI_{pk-pk} \longleftrightarrow P_{spur} = 10 \log \left(\frac{\Delta f_{pk}}{2f_m} \right)^2 \approx -36 \text{dBc}$$

$$DJ_{pp} = \frac{2}{\pi} \cdot 10^{\frac{\Delta P}{20}} UI_{pk-pk}$$