Designing Electronic Systems for Space

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Introduction

- **“Spacecraft” includes a wide variety of applications**
  - Communication satellites
  - Earth-observing satellites
  - Manned laboratories
  - Manned exploration vehicles
  - Robotic observatories
  - Planetary probes
  - Launch vehicles
- **Focus on communication satellites**
  - Electronic components & systems
- **Design requirements & constraints**
  - Individual issues are common to specific terrestrial design domains
  - Collectively, the set is unique

Outline

- **Space Design Requirements & Constraints**
  - Performance
  - Radiation
  - Reliability
  - Logistics
- **Communication Satellite Building Blocks**
  - Impact of issues above
- **Design for Radiation & Reliability**
  - Common mitigation design techniques
  - Emphasis on custom bipolar integrated circuits
- **Design for Qualification & Test**
  - Product characterization & qualification requirements

Space Design Issues
Performance

- **Function & Performance Metrics**
  - e.g. throughput, bandwidth, gain, accuracy, noise factor
  - Flow down from system requirements
- **Flexibility**
  - Flexibility or programmability in function or performance
  - Changing user requirements
  - Limited development schedule
- **“Size”, “Weight” and “Power” (“SWaP”)**
  - Dominant performance constraints
  - Size & weight usually limited by launch vehicle

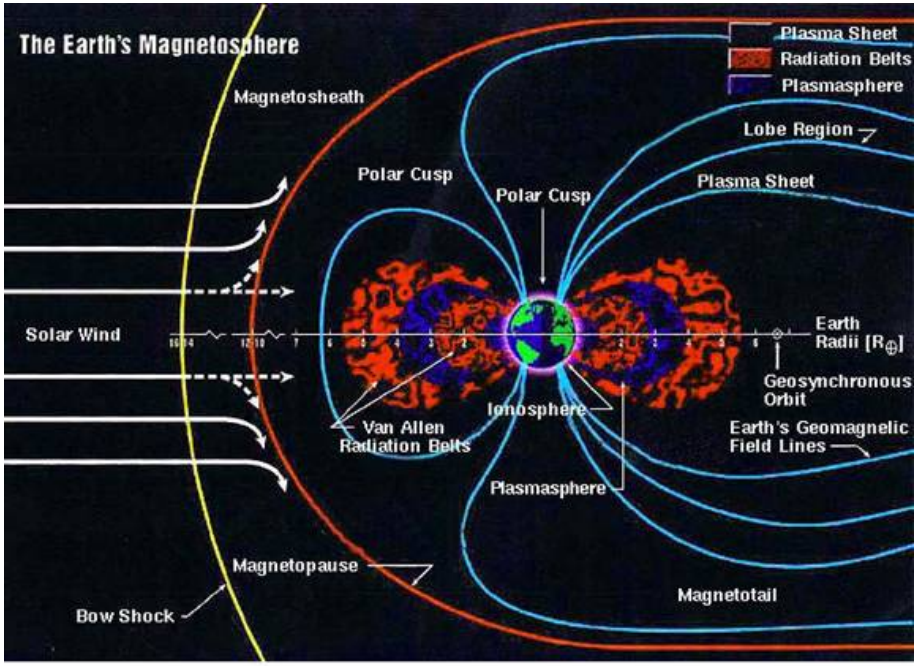
Space Design Issues
Performance (continued)

- **"Power" is influenced by three distinct constraints:**
  - Power generation
    - Typically from solar cells
  - Heat dissipation
    - Transfer within satellite by conduction, away by radiation
  - Reliability
    - Most failure mechanisms are thermally activated
- **Comparison to terrestrial applications**
  - SWaP constraints similar to portable consumer electronics
  - Level of performance required is far greater
    - e.g. throughput, bandwidth

Satellites can be thought of as delivering "mainframe performance on a laptop budget"

Space Design Issues
Radiation - Environment

- **Internally generated**
  - Electromagnetic Interference (EMI)
  - Crosstalk
- **“Man-made” sources**
  - Not discussed here
- **Natural sources**
  - Charged particles
  - Galactic or solar origin
  - Radiation belts around planets
- **Varies with location & time**
  - Orbital altitude & inclination
  - 11-year solar sunspot cycle
  - Solar flares



Source: NASA

Spacecraft must operate within a complex and variable radiation environment

Space Design Issues
Radiation – Cumulative Effects

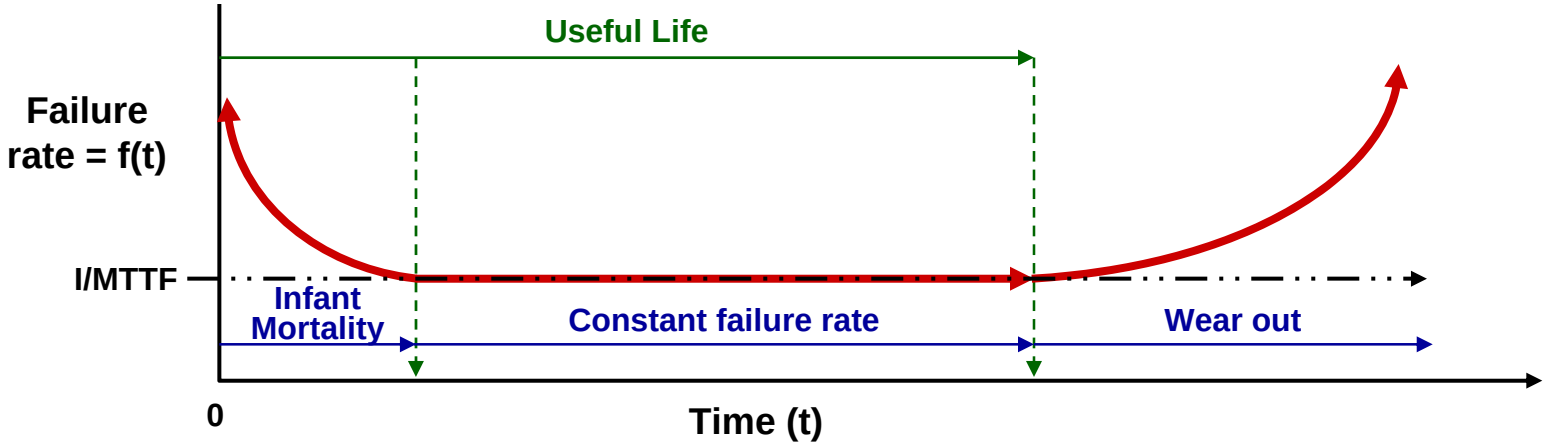
- **Measurements**
  - Integral fluence (particles/cm^2)
  - Total Ionizing Dose (TID, in “Rads”) for specific material
- **Gradual damage**
  - Charge buildup on surfaces & dielectrics
  - Disruption of lattice (“displacement”)
- **Device impact**
  - Threshold voltage shift
  - Leakage current
  - Degradation of mobility
  - Degradation of bipolar gain

Space Design Issues
Radiation – Single Event Effects (SEE)

- **Impact of specific particle causes ionization track within device**
- **Deposited charge or field disturbance changes circuit behavior**
- **Circuit change can be temporary**
  - "Single Event Transient", SET
- **Change in stored memory state**
  - "Single Event Upset", SEU
  - If changes function – "Single Event Functional Interrupt", SEFI
- **May be destructive**
  - "Single Event Latchup", SEL
  - "Single Event Burnout", SEB
  - "Single Event Gate Rupture", SEGR

Space Design Issues
Reliability

- **Mission success criteria**
  - Probability that function is maintained for expected life of spacecraft
  - Flows down from system requirements
- **Operational life**
  - Satellite “design life” can be very long (e.g. 15 years)
  - “Normal” devices must not “wear out” when exposed to operational stress
- **Fault tolerance**
  - Allows for early failure in non-normal elements (“random failures”)
  - Limits system impact of single event effects



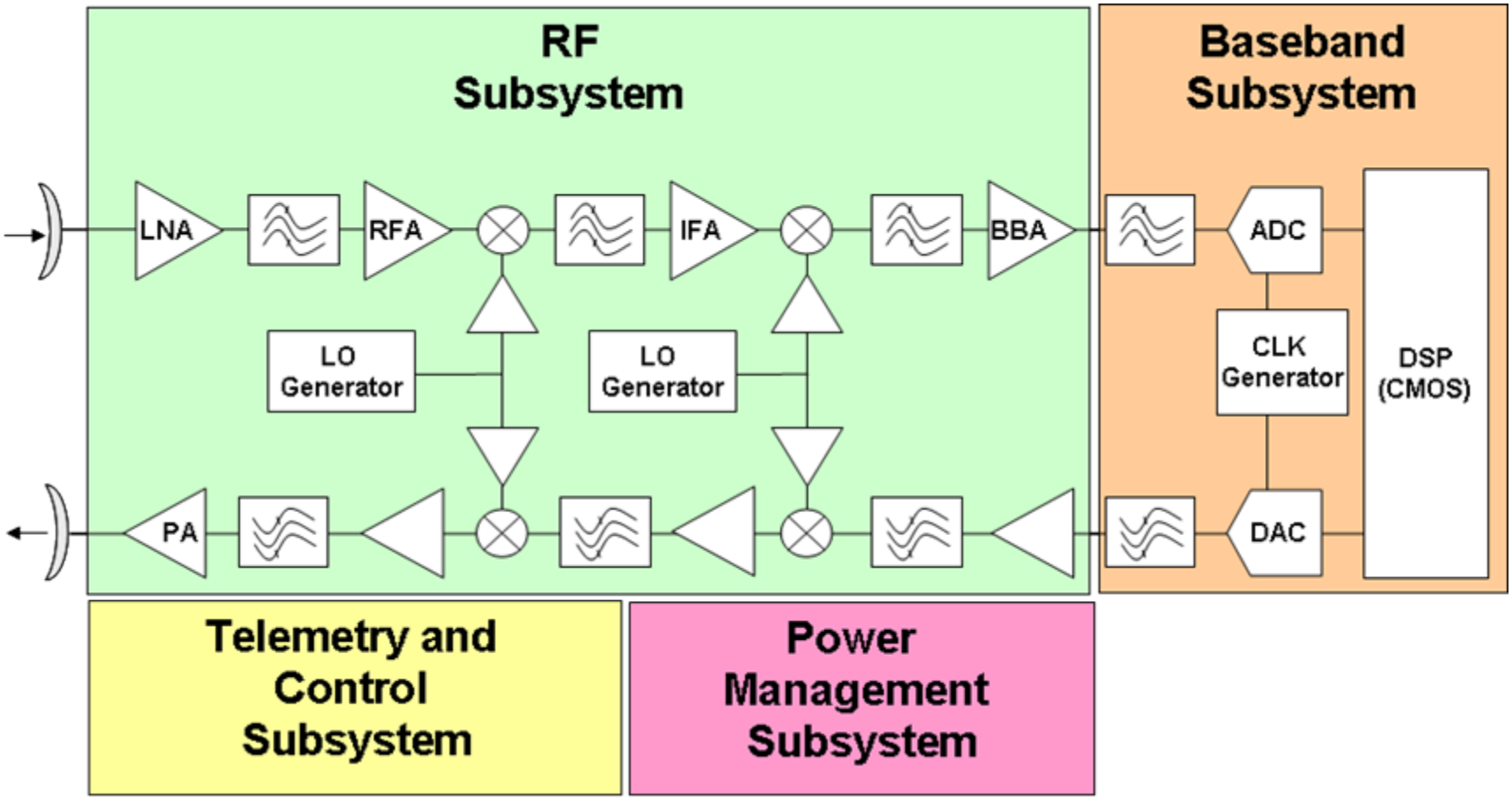
Space Design Issues
Reliability (continued)

- **Operating temperature**
  - High temperature accelerates most failure mechanisms
  - Wider range (esp. colder) than normally seen on ground
- **Temperature cycle**
  - Mechanical wearout is accelerated by differential thermal expansion
  - Frequency and depth of the thermal cycle typically depend on orbit
- **Vibration & Shock**
  - Launch & pyrotechnic deployments
- **Radiation & Vacuum**
  - Can cause some materials to decompose or degrade
- **Moisture/corrosion/contamination**
  - Moisture accumulated while on ground
  - Lingering effects once in space (e.g. corrosion & expansion)

Space Design Issues
Logistics

- **Cost, schedule & risk**
  - Satellites typically largely customized, built in very small quantities
  - Program cost & schedule dominated by non-recurring design phase
  - Minimizing cost, schedule & risk in this period is paramount
- **Test coverage**
  - Design/manufacturing errors & faulty components not repairable
  - High precision & robust verification at each step is critical
- **Supply life**
  - Components should be “mature” at program start to minimize risk
  - Schedule from concept to last launch may be very long
  - We must often consider component obsolescence

Communication Satellite Building Blocks
Payload Conceptual Block Diagram

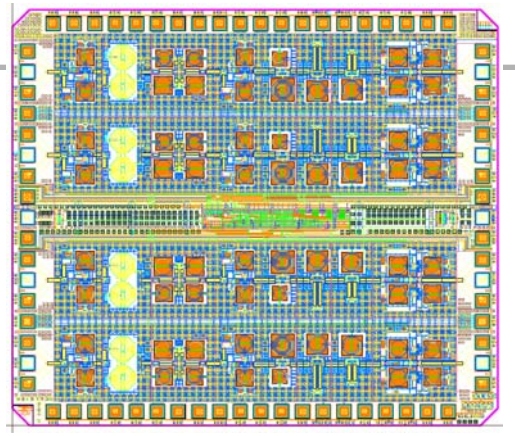


Communication Satellite Building Blocks
RF Subsystem

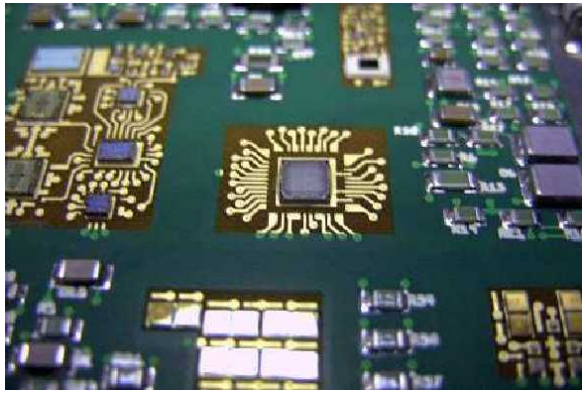
- **Components**
  - Antenna (incl. phased array)
  - Amplifier (LNA, PA, VGA, RF, IF, BB, Buffer)
  - Mixer
  - Filter
  - Switch
  - Attenuator, Isolator
  - Pad, Power Splitter
  - Phase Shifter
- **Dominant issues**
  - Performance
  - Long life
  - Reliability
  - Power/thermal
  - Volume/mass

Communication Satellite Building Blocks
RF Subsystem

- **Critical issues performance related**
  - Tie closely to system specifications
  - e.g. bandwidth, gain, output power, crosstalk isolation, stability
- **High bias voltage & current**
  - For high output power & bandwidth
  - Leads to wearout life, power dissipation & thermal load concerns
  - Multipaction (resonant breakdown in vacuum)
- **Small geometry**
  - Forced by volume/mass constraint & bandwidth requirement
  - Exacerbates crosstalk
- **Contamination**
  - III-V RF devices are sensitive to hydrogen poisoning



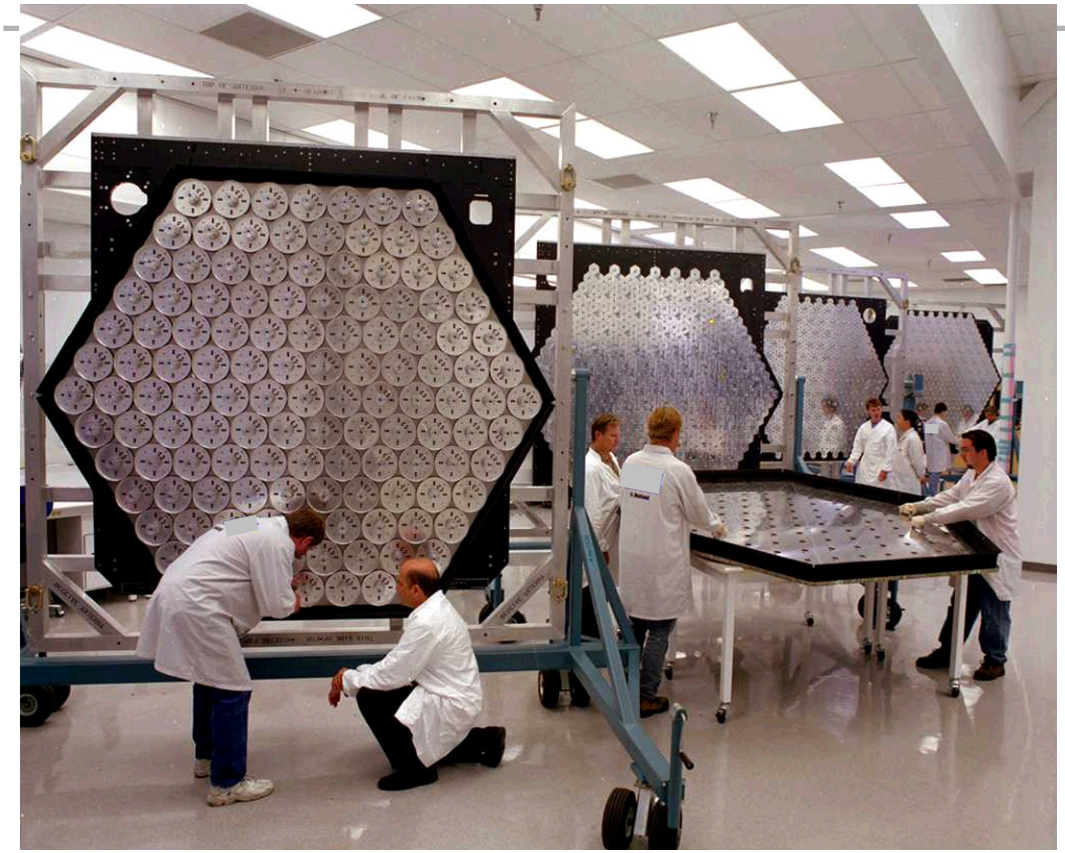
4-ch SiGe Ku band Beamformer

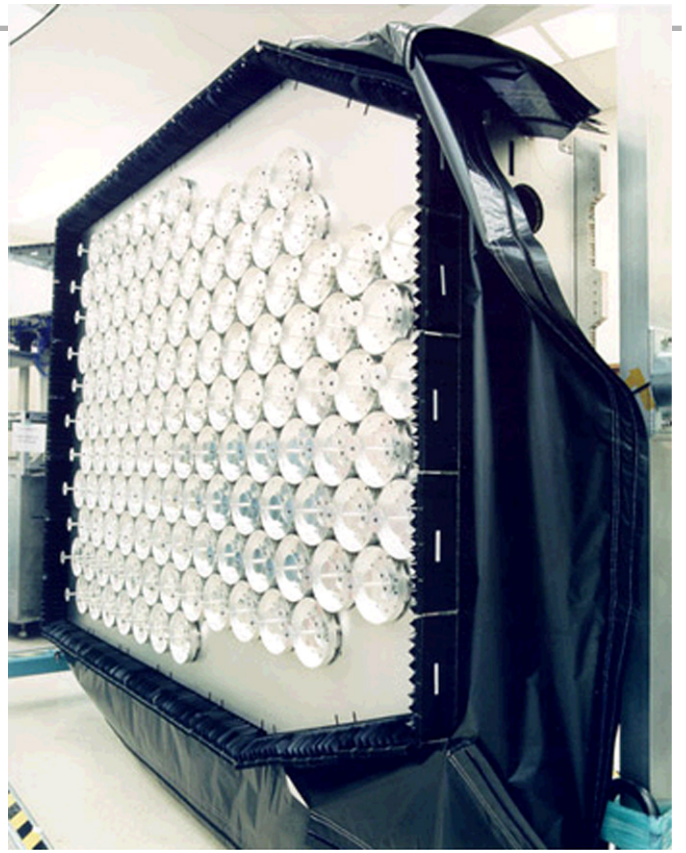


Chip-on-board Manufacturing

Single-chip and Chip-on-board integration improve performance and Size/Weight/Power

Communication Satellite Building Blocks
Phased Array Antennas





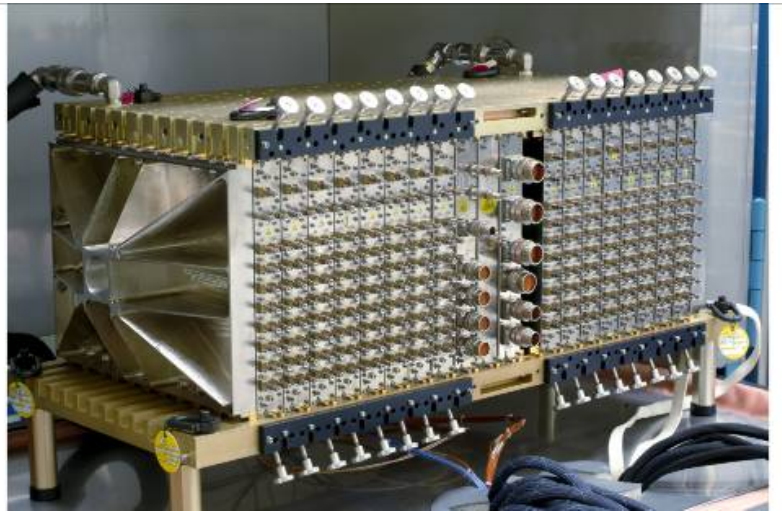
Distributed architecture drives voltage & temperature variation across array, making specifications more challenging to meet

Communication Satellite Building Blocks
Baseband Subsystem

- **Components**
  - Data converter (ADC, DAC)
  - Clock: PLL, DLL, Divider
  - Muliplexor, Demultiplexor
  - Memory
  - Serializer/Deserializer
  - Digital Signal Processor (DSP)
- **Dominant issues**
  - Performance
    - e.g. bandwidth, accuracy, throughput, clock skew
  - Power/thermal
  - Volume/mass
  - Radiation (particularly SEE)
  - Verification/test

Communication Satellite Building Blocks
Baseband Subsystem

- **High data conversion frequency**
  - Minimizes RF hardware
  - Adds system flexibility
- **Challenging ADC/DAC specs**
  - Cover TID/wearout parameter shift
- **Vast memories**
  - Must be protected against SEU, esp. configuration memory (SEFI)
- **Accurate high speed clocks**
  - Synchronize subsystem parts
  - Must be protected against SET
- **Complex system requires:**
  - Extensive design verification
  - High coverage manufacturing tests



Spaceway DSP Unit

- Performs equivalent of 62 TOPS
- Utilizes 0.13 m^3, 124 kg & 2100 W

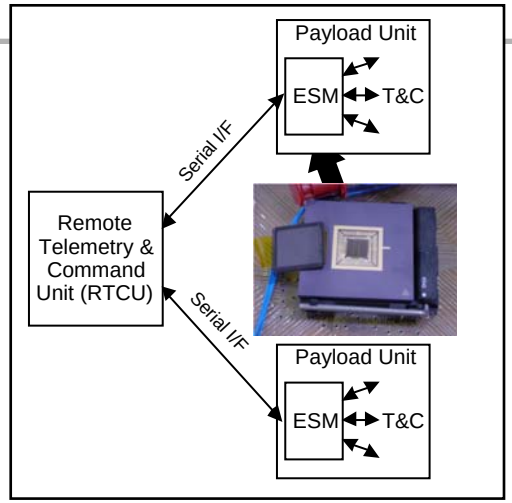
High conversion frequency & more processing in digital domain leads to very large & powerful DSP systems

Communication Satellite Building Blocks
Telemetry/Control Subsystem

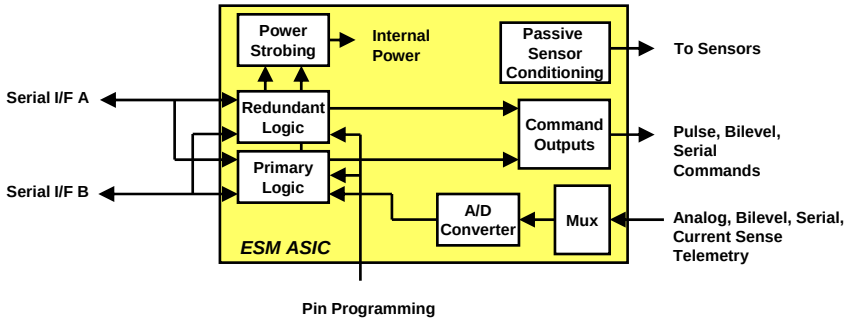
- **Components**
  - Sensor (e.g. high res. audio freq. ADC)
  - Mechanical Drive
  - RF Control
- **Dominant issues**
  - Performance
  - Fault tolerance
  - Thermal management
  - TID
  - SEE

Communication Satellite Building Blocks
Telemetry/Control Subsystem

- **Telemetric sensors**
  - High accuracy & low noise susceptibility; very low bandwidth
  - Strongly affected by TID-induced parameter drift & parasitic leakage
  - Worse environment (temp. & radiation)
- **RF array control analog electronics**
  - Maintain efficiency with changing environmental & load conditions
  - Minimize/compensate rad-induced leakage, offset & gain reduction
  - Protect control loops against SET
- **Critical for managing redundant assets**
  - Fault tolerance a special challenge
- **Increasingly distributed (embedded)**
  - Miniaturization is important



BiCMOS Embedded Services Module ASIC



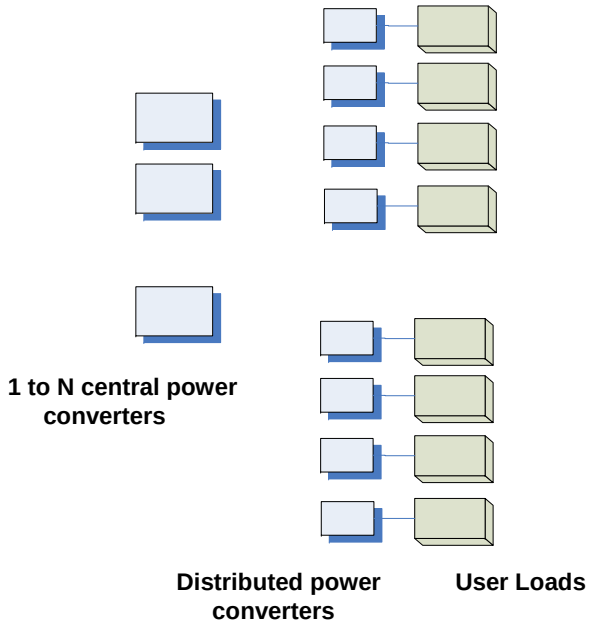
Single chip T&C services ASIC with serial interface & embedded redundancy management significantly reduces SWaP

Communication Satellite Building Blocks
Power Management Subsystem

- **Components**
  - Regulator
  - DC-DC Converter
  - Switch
  - Filter
  - Controller
  - Condition Sensor
- **Dominant issues**
  - Performance
  - Reliability
  - Thermal management
  - TID
  - SEE

Communication Satellite Building Blocks
Power Management Subsystem

- **High voltages required by primary PM & motor driver circuits**
  - Part selection for SEL/SEB/SEGR immunity is more difficult
- **Reduced IC operating voltage**
  - Need tight regulation
  - Extra sensitivity to TID headroom reduction in secondary regulators
- **Fast transient response under variable load**
  - Large energy storage
  - Robust Pulse Width Modulation
- **Critical for managing redundant assets**
  - Fault tolerance a special challenge
- **Increasingly distributed (embedded)**
  - Miniaturization is important, but more difficult with only "rad-hard" parts



Hybrid (central/distributed) power system for redundant units

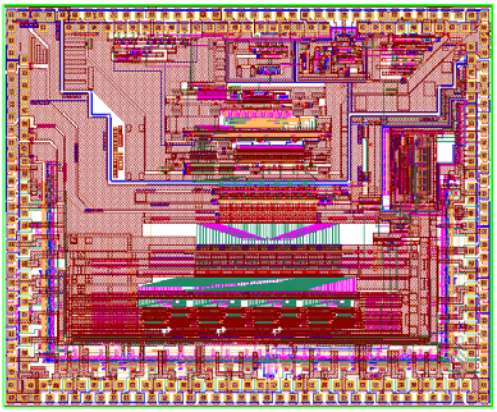
Combination of redundant centralized & distributed (Point Of Load) power converters improves reliability & efficiency

Communication Satellite Building Blocks
Bipolar/BiCMOS Usage

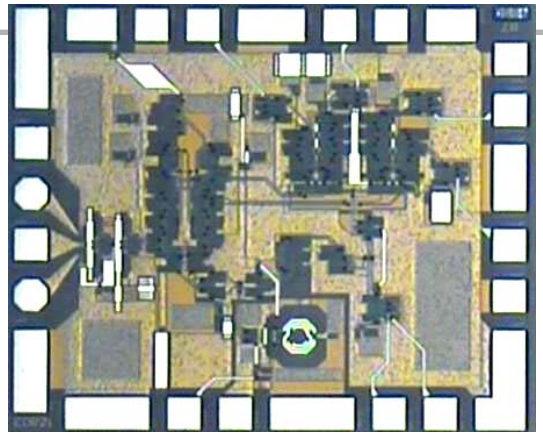
- **Advantages in bandwidth, output drive & precision**
- **Used in a wide variety of applications, e.g.:**
  - High speed clock generation
  - Analog to digital converters (ADCs)
  - Digital to analog converters (DACs)
  - RF/analog circuitry
  - Power supplies
- **GaAs, SiGe & InP HBT technologies offer highest performance**
- **SiGe HBTs**
  - Allow integration with silicon CMOS
  - Good for mixed signal SoC applications (e.g. data converters)
- **InP HBTs**
  - Direct bandgap good for optoelectronic integration
  - Best for ultra-high-speed PLL & SERDES devices

Bipolar technology plays a major role in space electronics

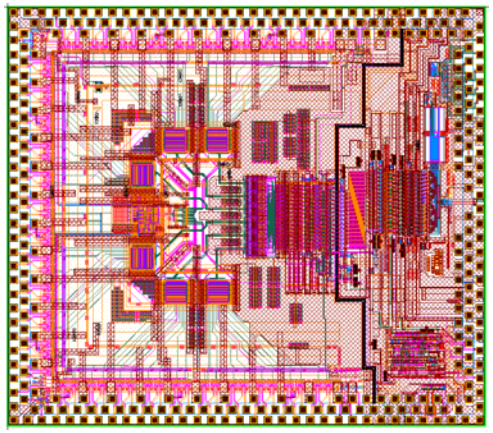
Communication Satellite Building Blocks
Bipolar/BiCMOS Usage – Examples



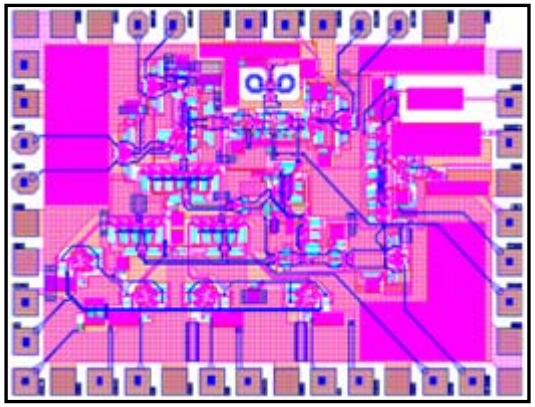
10b 1.5Gsps SiGe down-converting ADC / 1:4 DEMUX



40GHz InP 1:4 DEMUX / CDR



10b 3Gsps SiGe up-converting DAC / 6:1 MUX

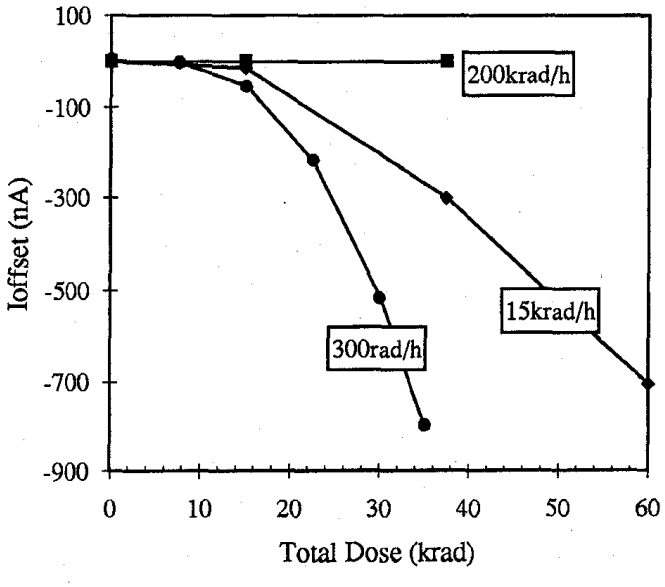


40GHz InP Clock Multiplier / 4:1 MUX

SiGe & InP HBT technologies utilized for highest performance

Design for Radiation
Part Selection

- **No way to shield against cosmic rays**
  - Need parts immune to SEL/SEB/SEGR
- **Reduce burden on designer**
  - Select for minimal parametric shifts due to TID, low SEU/SET rates
- **TID tolerance generally improves with reducing gate thickness**
  - Enables more use of commercial CMOS
- **Enhanced Low Dose Rate Sensitivity (ELDRS)**
  - Seen in some bipolar devices
  - Due to competition between trap creation & charge movement
  - Requires test at very low dose rate

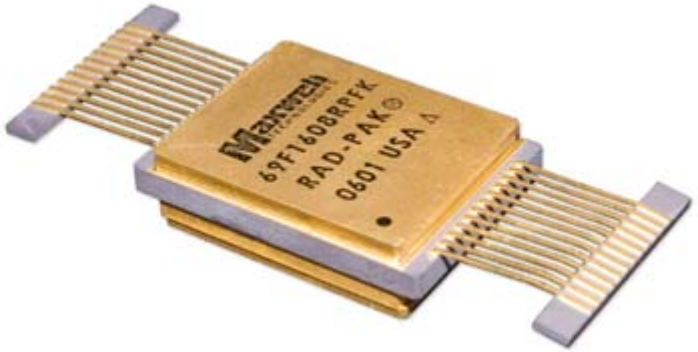


Dose rate dependence of TID degradation in Motorola LM139 (Carriere, IEEE TNS 42-6, 1995)

Part selection is "first line of defense" for most of circuits & radiation effects previously discussed

Design for Radiation
Shielding

- **Shielding generally effective for minimizing TID & surface charging**
  - Unlike case for cosmic rays
- **Natural shielding from spacecraft structures & unit enclosures**
  - Lessens design problem for deeply buried components
- **Added around "soft" components**
  - High-Z materials are most effective, but most costly in weight
- **Grounding of floating metals**
  - Prevents internal discharges from surface charging

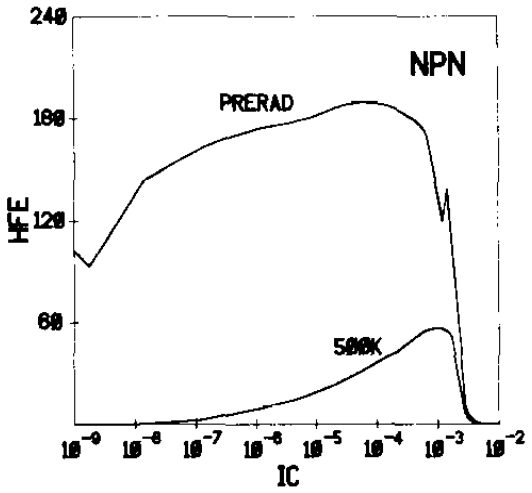


Shielded chip level packaging
(SOURCE: Maxwell Technologies)

Natural shielding helps a lot, but more can be added at unit or component level, trading hardness for weight

Design for Radiation
Worst-Case Circuit Analysis (WCCA)

- **Model TID effects & include in WCCA**
  - Where component selection & shielding do not eliminate problem
  - Requires local characterization & modeling
- **"Over design" circuits**
  - Extra components, higher bias compensate expected degradation
- **Increasing bias level of bipolar transistors**
  - Most sensitive to TID in low current regime
  - Improves radiation tolerance at expense of power dissipation
- **Renegotiation of system requirements**
  - e.g. increasing input signal swing, power budget or error allocation

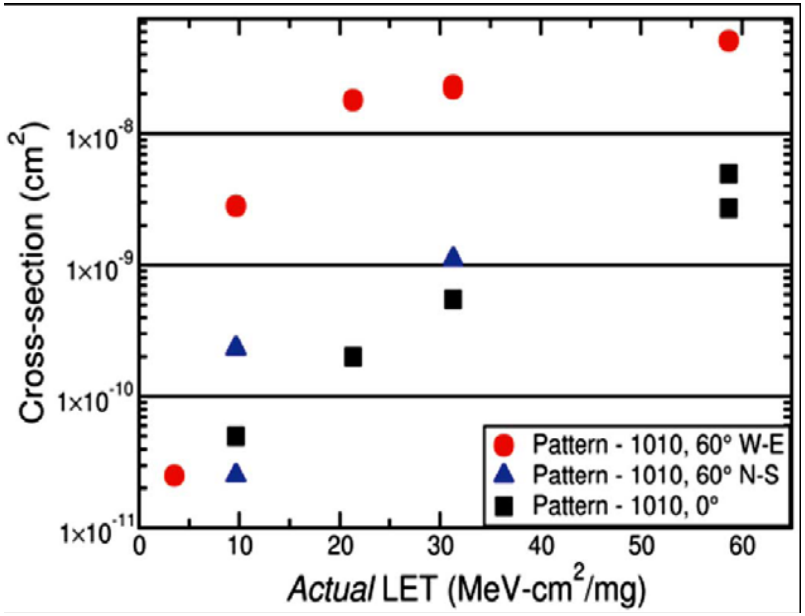


TID degradation in transistor gain vs. collector current (Kerns, Proc. IEEE 76-11, 1988)

If parametric degradation due to radiation is understood, it can be compensated for in circuit design

Design for Radiation
Single Event Upset / Transient

- **SEE has become increasingly important with:**
  - Device scaling
  - increasing complexity
  - Higher bandwidth
- **Must now consider issues which could previously be ignored**
  - SET in clock trees or logic paths
  - Multiple bit/node upsets from a single particle hit
  - Charge/well sharing
  - Nuclear reactions in overlayers

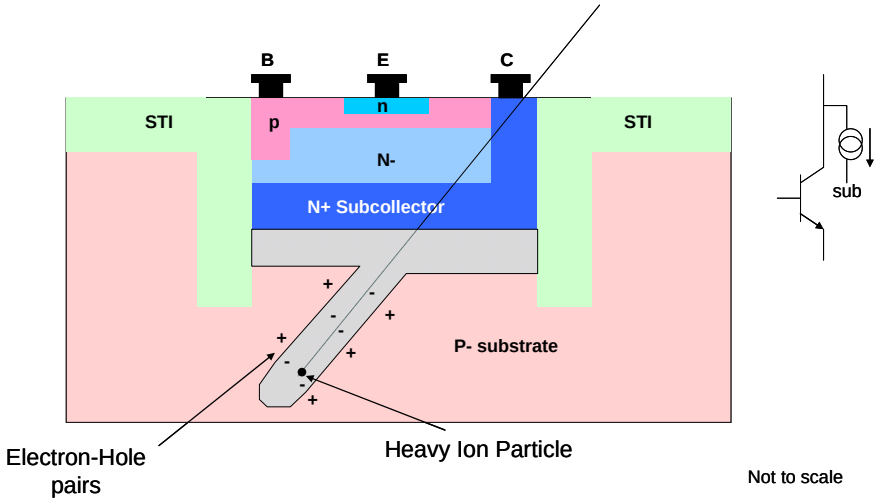


Strong directional dependence of upset rate in *hardened* 90nm CMOS flip-flop (Amusan, IEEE TNS 54-6, 2007)

More careful testing & device/circuit modeling is required to evaluate impact of complex Single Event interactions

Design for Radiation
Single Event Upset / Transient (cont)

- **Advanced bipolar devices are:**
  - Relatively tolerant to total dose & displacement damage
  - Particularly sensitive to SEU/SET
- **Relatively large collector-substrate junction area**
  - Represents significant target for charge collection
  - Far higher event rate than typically seen in modern CMOS
- **Process modifications**
  - Can improve SEE hardness to limited extent

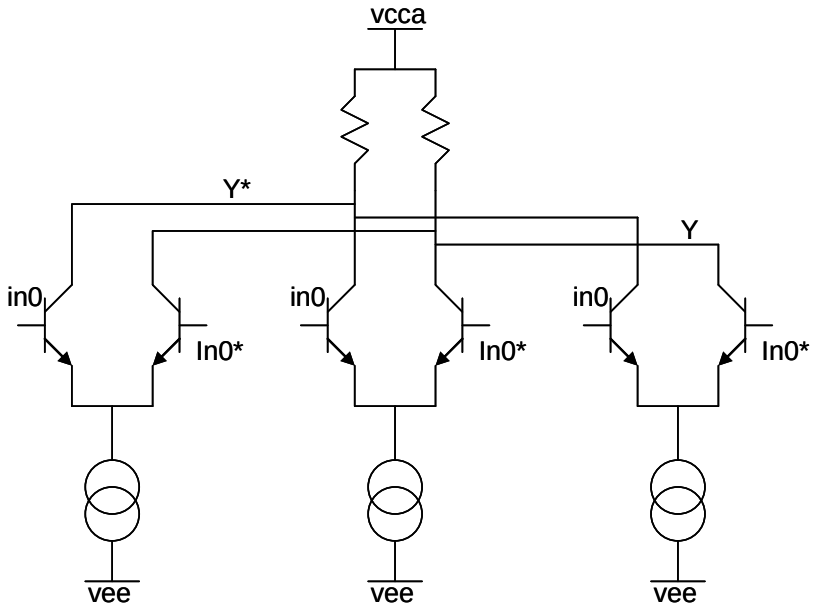


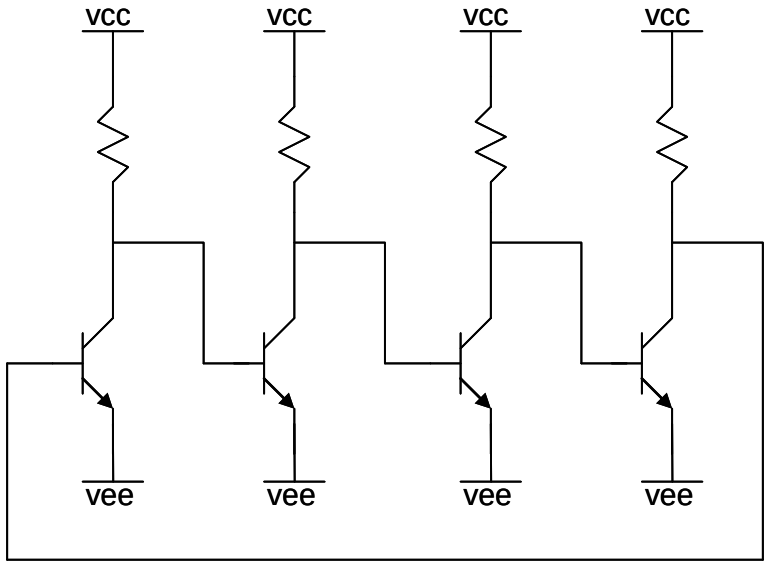
Circuit techniques & architectural design approaches are required to insure reliable operation in space

Design for Radiation
Memory SEU Hardening

- **Current sharing hardening**
  - Relies on several current paths to control circuit operation
  - Increase in current & redundancy improves SEU hardness

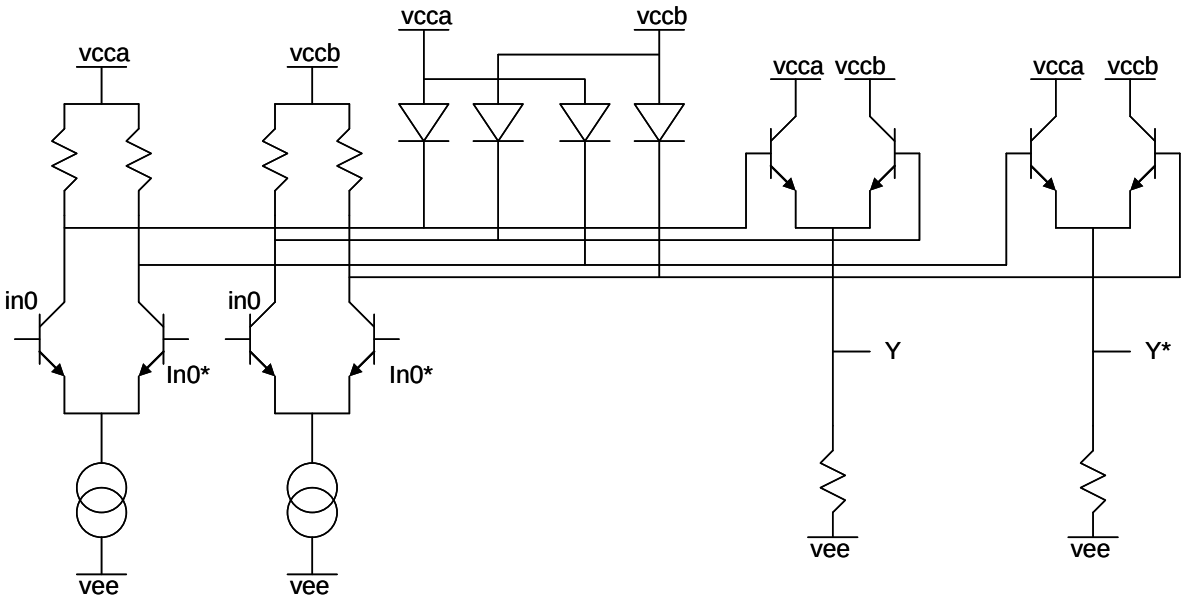
- **Dual interleaving**
  - Uses local redundant nodes to limit SEU impact





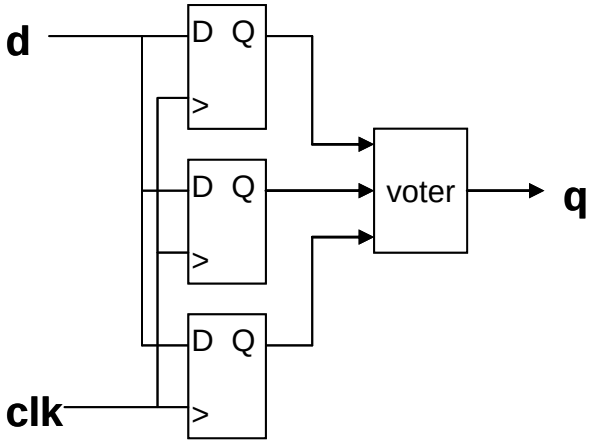
Design for Radiation
Memory SEU Hardening (continued)

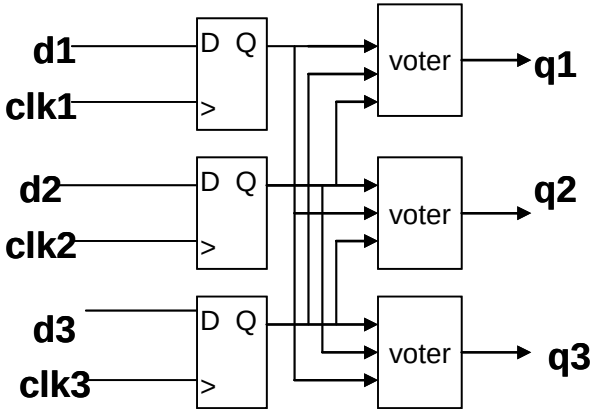
- **Gated feedback cell**
  - SEU hardness improved by redundancy of two sections
  - Separate power supplies allow testing of redundant circuits
  - Diodes limit current into substrate, allow faster recovery



Design for Radiation
SEU Architectural Hardening

- **Error detection and correction (EDAC) coding**
  - Used mainly for memory subsystems
- **Triple modular redundancy (TMR)**
  - Used for control & data paths where upsets cannot be tolerated
  - Voter compares outputs of three registers or delay flip flops
- **Simple TMR structure (left) subject to SET on clock & data lines or voter logic**
  - Not acceptable for command path or major clock tree affecting entire DSP or computer
  - Triplication of voters, inputs & outputs (right) increases SEU hardness
  - Large penalty in area, power & performance



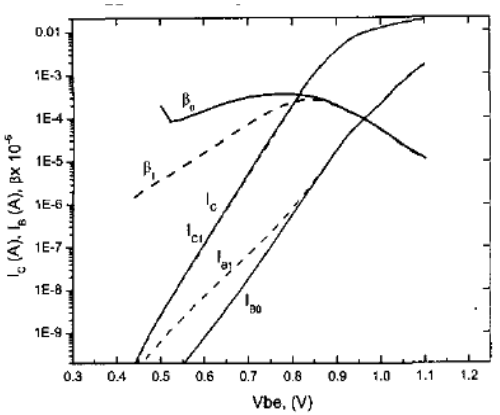


Design for Reliability
Wearout Life

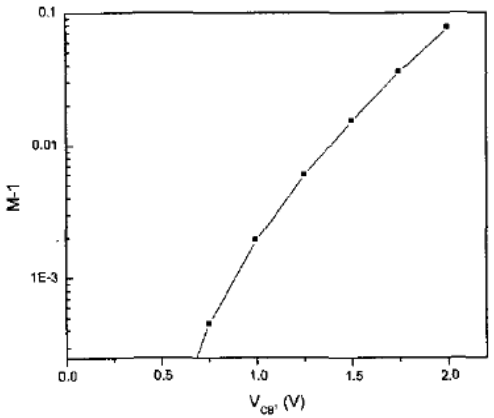
- **High reliability requires managing wearout life & random failure rate**
- **For wearout life, it is important to:**
  - Understand how devices wear out in response to stresses such as temperature, voltage, current & thermal cycling
  - Limit stresses seen by devices in product, consistent with this understanding & product life requirements
- **Characterization of wearout best done using special test structures**
  - Primitive device elements (e.g. transistors, passives, wires & vias)
  - Well controlled & highly accelerating stresses
- **Study & model distribution of failure time for each mechanism**
  - Predict median time to failure (MTTF) for given circuit conditions
  - Ensure sufficient margin beyond design life for statistical variation
- **Develop general stress guidelines**
- **Verify product stresses remain within guidelines**
  - Circuit simulation & electrical rules checker (ERC) programs

Design for Reliability
Parametric Drift

- **"End of life" models required for WCCA where wearout mechanism manifests as parameter drift**
  - e.g. bipolar gain reduction at low current due to hot carrier injection (HCI)
- **Compared to terrestrial circuits, long wearout life requirement of space applications often requires:**
  - "over-design" (increase in power level or complexity)
  - or "derating" (reduction in performance)
- **Examples**
  - Limit V_{CE} to reduce HCI, thereby degrading analog/RF signal-to-noise performance
  - Increase metal line width to improve electromigration life, introducing capacitance that limits circuit speed



Current gain degradation for 200GHz SiGe HBT with 1hr stress at V_{CB}=3.5V & V_{BE}=0.88V



Avalanche multiplication, which causes the degradation, is a strong function of V_{CB}

Source: Zhijan, IRPS'03

Design for Reliability
Random Failure Rate

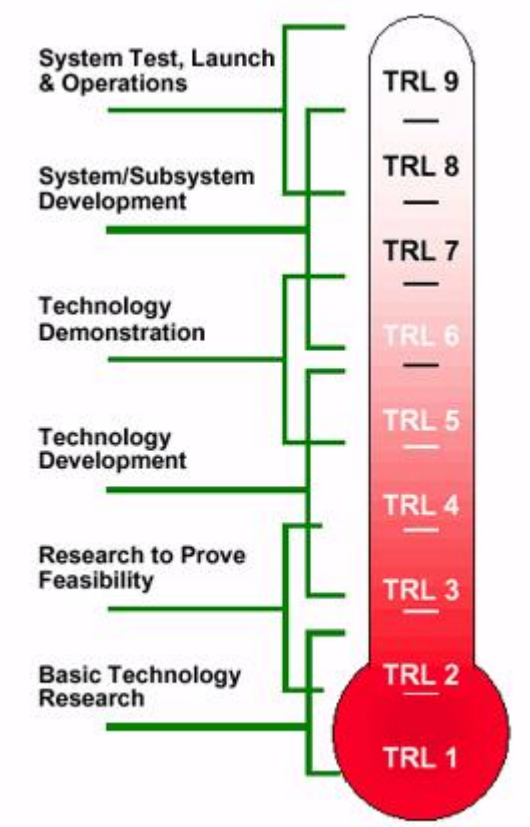
- **With intrinsic wearout minimized by limiting stresses, product failure rate is determined by "extrinsic" failures**
  - Early failure of abnormal elements present in any complex product
- **Estimate this failure rate**
  - Industry guidelines (e.g. MIL-HDBK-217)
    - Assumes constant failure rate vs. time, adjusted for use condition & part quality
  - Field failure data (from terrestrial applications)
  - Large population accelerated life tests
- **Add redundant elements to allow for some devices to fail**
  - At the unit level (e.g. duplicating entire functions)
  - Internal to a unit (e.g. "M-for-N" redundancy)
- **Compute overall system reliability considering redundancy**
  - Using custom statistical tools
- **Perform design trades to meet system reliability requirement**
  - Where best to add redundant elements
  - Where greatest effort should be expended in thermal management
  - Both influence weight and cost

Design for Reliability
Random Failure Rate (cont.)

- **Redundant elements can be:**
  - Continuously powered (“active sparing”)
  - Unpowered until needed (“cold sparing”)
  - Some mixture of the two approaches
- **Failure Modes and Effects Analysis (FMEA)**
  - Studies specific types of device failures that might occur, and their impact on system
  - Circuits that drive or are driven by redundant elements must operate in presence of failures (e.g. shorted inputs or outputs)
  - Space systems often have requirement that no “single point failure” in electronics can cause entire mission to fail

Design for Qualification

- **Space electronics is virtually never installed in a satellite and launched until it is "qualified"**
  - Confirmed high probability to meet operational requirements for period exceeding mission life
- **Can't put product in operational environment (in satellite, in space) for mission life, so:**
  - Develop data during design to gain confidence
  - Perform specific tests at selected conditions to verify expectations
- **Qualification should be hierarchical**
  - Verify underlying parts, materials, processes before moving to higher levels of assembly
  - Include design libraries, models and tools



Technology Readiness Level (TRL) scale (SOURCE: NASA)

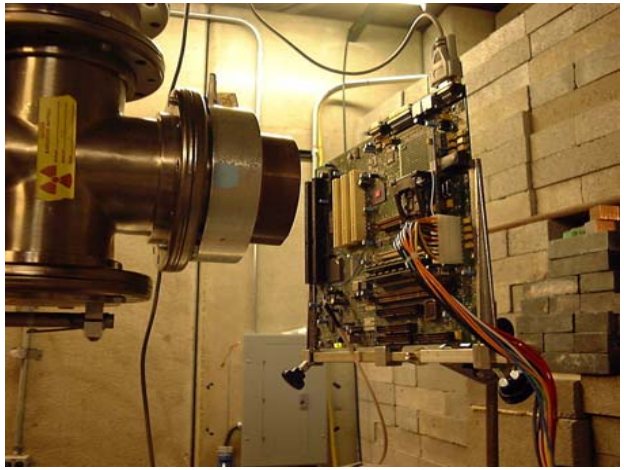
NASA TRL scale is one of many tools in maturity assessment

Design for Qualification (cont.)

- **Frequent design reviews ensure that:**
  - Requirements and interfaces are understood
  - Function and performance meet expectations in all operating modes (including failure conditions)
  - Size, weight and power are within budget
  - Wearout life of all components exceed design life
  - Variation due to process, voltage & temperature, as well as parametric drifts due to radiation & wearout, included in WCCA
  - Random failure rate will be acceptable
  - Disturbances from SEE occur no more frequently than allowed, with manageable system impact
  - Product can be readily manufactured
  - Manufacturing tests can detect faulty components

Design for Test

- **Functional & parametric qualification test**
  - On “proof of design” (POD) or “engineering model” (EM) prototypes
  - Wider than normal environmental exposure
- **Radiation testing**
  - γ-ray, X-ray, neutron, proton & heavy ion labs
  - Sophisticated modeling to calculate orbital rates
- **Complex fixtures, special test equipment (STE)**
- **“Flight” products put through battery of “acceptance” tests**
  - Similar to qualification tests (same STE?)
  - Emphasizes detecting faulty or out-of-spec components, not verifying design
- **Acceptance tests also done hierarchically**
  - Part replacement more costly late in assembly

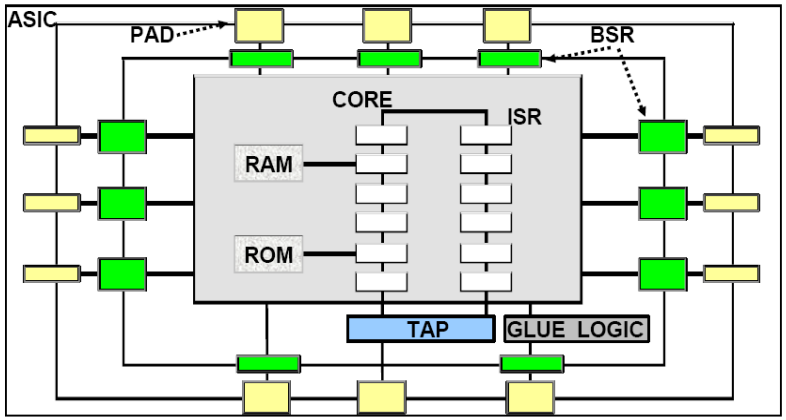


Heavy ion SEE test setup (SOURCE: JPL)

Qualification (including radiation) & Acceptance testing have similar requirements, but different goals

Design for Test (continued)

- **For both Qualification & Acceptance test, circuits should be designed with DFT concepts**
  - Examples: test points, scan register chains, boundary scan, self-test
  - Improve both “controllability” & “observability”
  - Low probability of missing faults in Acceptance tests
  - Simplifies design of STE
  - Simplifies debugging issues found in Qualification testing



ASIC test based on IEEE 1149.1 (Lee, AUTOTESTCON’99)

IEEE 1149.1 Boundary Scan enables hierarchical system test

Summary

- **In this tutorial, we have:**
  - Reviewed requirements & constraints facing designers of electronic components & systems intended for spacecraft
  - Discussed how design of key electronic building blocks in communication satellites is influenced by these issues
  - Reviewed design techniques typically used to deal with these issues, particularly for mitigating radiation effects
  - Illustrated some of these techniques with examples taken from custom bipolar integrated circuits
  - Discussed how compliance with these requirements & constraints is demonstrated in resulting products
  - Suggested how DFT methods can assist with this demonstration

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