3D Stacking of Silicon Chips

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Outline

- Introduction - trend in the semiconductor industry
- 3D Technologies
- The European e-CUBES project
- Application Scenarios
  - DRAM
  - Power
  - Integrated Camera
Increasing Cost Require Large Volumes or Entities to keep Development and Invest Affordable

Cost Trends in Million $US

Source: Credit Suisse CSFB, SCE Weekly, 10/27/04
Semiconductor Business News 01/07/03 IC Insights, McClean Report 2002
Log (Monthly semiconductor revenues in Billion US $)

Annual growth rate: +16%

Revenue in US$

Trend line in the 90's

Present trend line
A maturing Industry?

...... consolidation and concentration !!!?????
Decreasing Capacities with Latest Technologies

% capacities from top 2 leading edge nodes*

Source: SIA, SICAS

*in Wafer starts per month
Scalability Limits for Several Technologies – Only Memory and High-performance Logic Strictly follow ITRS Roadmap

Minimum Feature Size [µm] (half pitch dimensions)

- Bipolar-Analog
- IGBT
- DMOS Analog BiCMOS
- 5V CMOS
- RF BIPOLAR RF BiCMOS
- CMOS logic DRAM

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Observations

- Increasing cost for development of newest technology generations and products
- reduced growth rates
- Reduced fraction of products in newest technology generations
- Reduced miniaturization speed in special technologies such as Analog, Sensors, Power, High-voltage, Bipolar, Embedded NVM (e.g. Shrink of Embedded Flash from 130 to 90 nm may provide only few percent cost reduction)
- Due to reduced speed of productivity improvement: reduced importance of shrink scenarios that follow Moore's Law
- However: An increasing number of niches provide sweet spots (foundry, equipment, fabless etc.)
Trend

- Moore’s Law is no longer the only industry driver due to architectural and physical constraints
- More-than-Moore is a new hype

... but what means More-Than-Moore?
Eniac Initiative in More than Moore

- Beyond Silicon
- Design Platform
- **Heterogeneous Integration**
- Infrastructure, Access and Education
- Materials and Equipment
Heterogeneous Integration:  
The Integration of Si-Chips into Smart Modules

Yesterday
- Mostly PCB
- Some MCM

Tomorrow
- Lots of smart solutions depending on application requirements
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Examples for **Heterogeneous Integration**

- Finepitch interchip vias
- Coarsepitch interchip vias
- Capacitive /inductive interchip communication
- Traditional bond wires on chipstacks
- μ-Flip Chip
- MID
- Stack of small PCBs
- Bare die on PCB

... all of these are 3D integration
Three-Layer Stack of Chips

Vertical System Integration by Using Inter-Chip Vias and Solid-Liquid Interdiffusion Bonding
P. Ramm, A. Klumpp, R. Merkel, J. Weber, R. Wieland
Invited Paper
ASET’s Coarse-pitch Process

Backside etch diameter 40 µm
Inductive Communication

N. Miura (ISSCC’05 #14.5) 195Gb/s Inductive-Coupling Transceiver 2.5/mm²/Tb/s, 6mW/Gb/s, Wired Clock

Transceiver Channel Array

50 µm Inductor

Tx
Rx

Upper Chip
Bottom Chip

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Baw Filter Package – *Enabler for Stacking Technology*
Stacking of Memory Chips using wire bonds
MID-Version (Molded Interconnect Device)

- 3D substrate / flexible geometry
- Limits in pad/conductor layout
- Designrules ?
Package on Package
OPC – One Package Computer

Assembly Controller TC1796A
LP 27x27mm² , bottom

Flash

Microcontroller

SRAM
OPC – One Package Computer / Details

Packaging of the Controller
PCB embedded Chips

Target:

- Simplification of packaging process by combination of logic and power interconnects in one process
- Development of an integration technology for increased number of pins
- Simplification of value chain and reduction of cost
- Cooperation with AT&S (PCB manufacturer)
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e-CUBES
3-D-Integrated Micro/Nano Modules for Easily Adapted Applications

- 21 partners from 11 European countries
- total budget is € 20.8 Mio, requested grant € 12 Mio
- Project kicked off Feb 1st, 2006, ran for three years until July 31st
- this project dealt with wireless sensor networks…
- … and 3D integration technologies
- It implemented 3 different demonstrators (aeronautic, health and fitness, automotive)
3D Integration Technologies

- IZM-M: Through Silicon Via
- IMEC/IZM-B: Thin Chip Integration
- 3D-PLUS: Stacking of Packages
Source: SINTEF
D3 Progressive System Demonstrator with Energy Harvesting Power Supply

3D Integration on Sensor level

3D Integration on ASIC level

3D Double Stack Integration

3D Integration on System level

Energy Harvesting MEMS (WP 3.2)

Cap./thin film bat.

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..finished stacks
e-BRAINS is the successor to e-CUBES

Best-Reliable Ambient Intelligent Nanosensor Systems by Heterogeneous Integration

- again 21 partners
- total budget is € approx. 15 Mio, requested grant € 10 Mio
- Project will kicked off June 1st, 2010, will run for three years
- this project deals with small geometry applications …
- … using heterogeneous integration
- It implemented 5 different demonstrators
e-BRAINS benefits from e-CUBES:

novel 3D-enabled nano sensing applications

- Nano Sensors
- Smart communication
- Energy Management
- Low-T TSV technology (TSV-SWACF)
- Low-Cost 3D-WLP (TCI/UCTS)
- Chip Stacking 3D-SIP (WDoD)
- Layer Transfer Bonding (LTfB)
- High-Performance Interposer (PAECE)
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Why 3D stacking of DRAMs?
### Example for Termination Scheme in Application:

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Slot 1</th>
<th>Slot 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write to Slot 1</td>
<td>RTT_WR=120 Ω</td>
<td>RTT_Nom=20 Ω</td>
</tr>
<tr>
<td>Write to Slot 2</td>
<td>RTT_Nom=20 Ω</td>
<td>RTT_WR=120 Ω</td>
</tr>
</tbody>
</table>

#### Write to Slot 1:

Controller → DIMM (TL) → Receiving DRAM → TL → Terminating DRAM
Example Memory

- Support functions run permanently on all memory devices today (about 1W/device)
  - Command decoders
  - Synchronization circuits
  - On-die termination

- Increased power consumption with increased clock speed

- By increased integration level support functions need to run only on ‘master’ chip

- → major power saving

- Recent result from 3D conferences and studies of marketing institutes → some more delay for introduction of TSV in DRAMs (Elpida/Samsung)
recent announcements

- Elpida and Samsung are doing 3D today (Stacked Chips, Wirebonding, PoP); to enter markets with TSV solution in 2011
Activities at NXP … just an example

Conventional Complex Discrete

Package concept Embedded Discrete

Qual tests ongoing:
- PC acc. To MSL1 level
- TMCL: -65/+150 °C, 1000 cycles.
- PPOT: 96 hrs, Rh = 100%, 1atm, 121 °C.
- HTS: 1000 hrs, 175 °C

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5 March 2010
page 39
Trend (exploitation strategy)

- Do Coarse-pitch Via first and get immediate benefit from chip area saving
- … continue on with small-size vias and get benefit from redesigned large logic chips (should be started only when decent manufacturing experience on coarse-pitch via is available)
Existing Product: Toshiba Camera Module
3D stacked image sensors for size reduction

Toshiba’s small size camera system with Through Si-Vias for mobile phones
Final Conclusions

- The world is getting more complicated
  - In the chip industry
  - and in the sub-trend of system integration

- New system integration solutions provide solutions for specific application – no standardization seen
  - More special solutions?
  - How about platforms?

- Changes in the value chain
  - PCB can lose due to alternative solutions such as MID or chip stacks?
  - PCB can gain by migrating into the chip packaging area such as mounting bare dies?
Never stop thinking.