Constant-Current Threshold Voltage Extraction in HSPICE for Nanoscale CMOS Analog Design

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Motivation

- MOSFET threshold voltage – V_T
  - Strong surface inversion for channel conduction
- Simulated V_T does not match well to silicon
  - Short-channel effects → complex structure, non-idealities
  - Discrepancy critical with lower V_{DD} & (V_{GS} – V_T)
  - Measurement cannot determine V_T condition
- Design concurrent with technology development
  - Extrapolative (predictive) models → periodic updates
  - Faster time to market for complex ICs
- Need simulated V_T to match silicon for faster design of robust nanoscale analog circuits

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Outline

- Motivation
- MOSFET – Then and Now
- Existing HSPICE V_T Extraction
- V_T Measurement Methods
- New HSPICE V_T Extraction
- Evaluation of New Feature
- Conclusion

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Flatband Condition ($V_{GS}=V_{FB}$)

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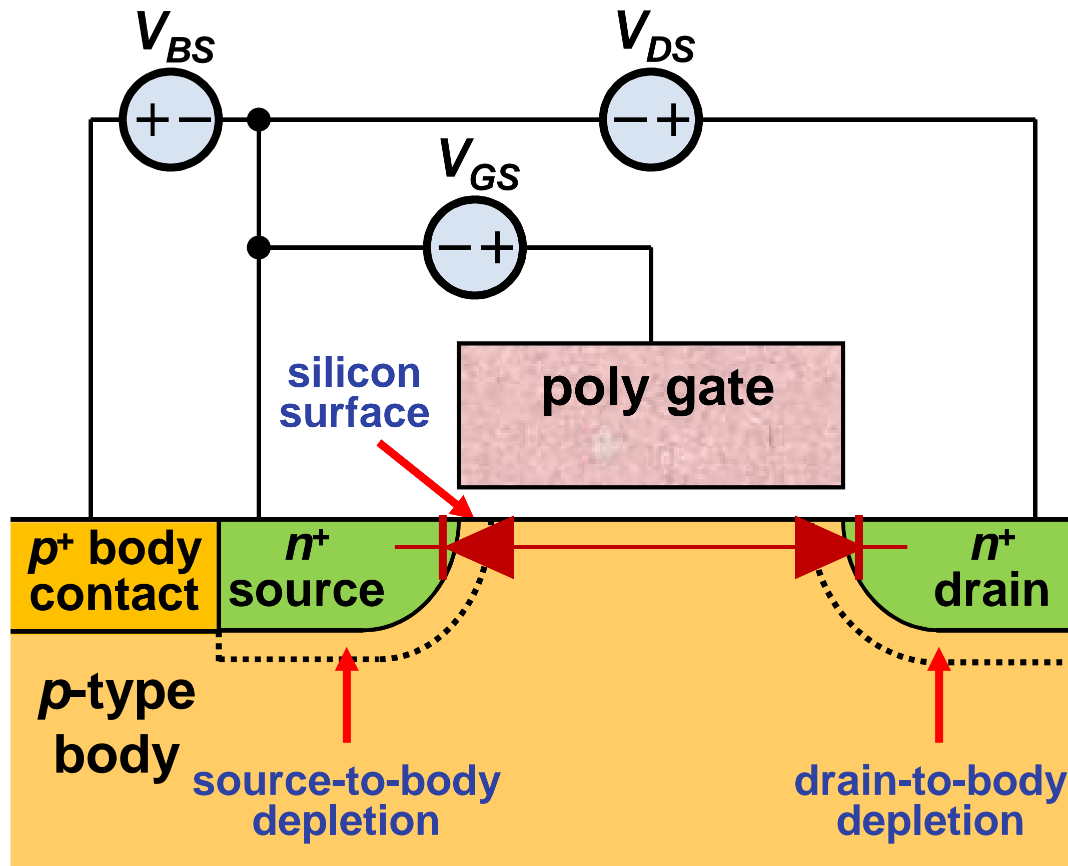

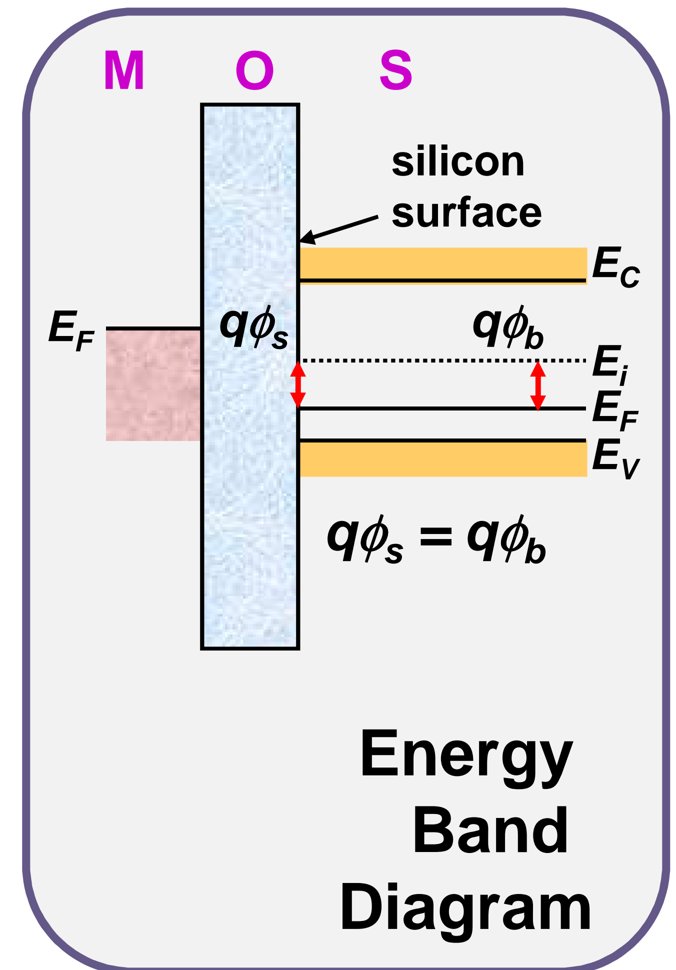

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Onset of Surface Inversion

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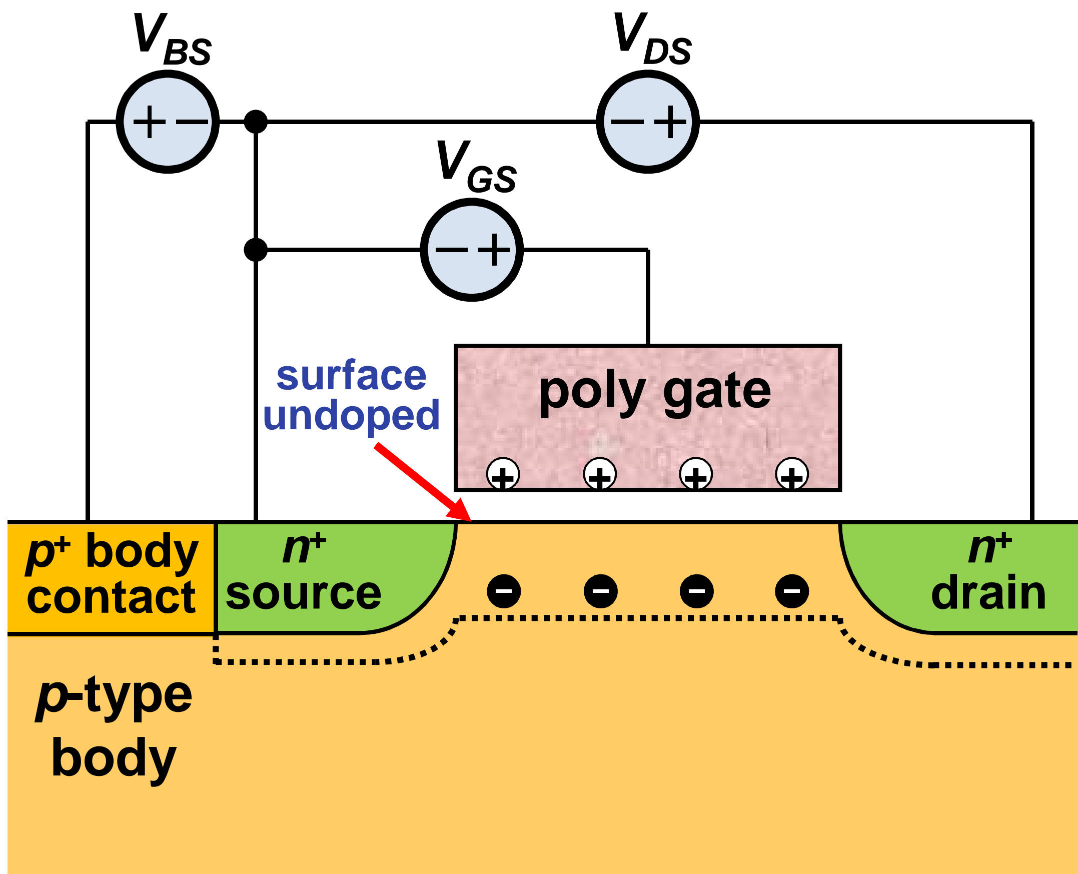

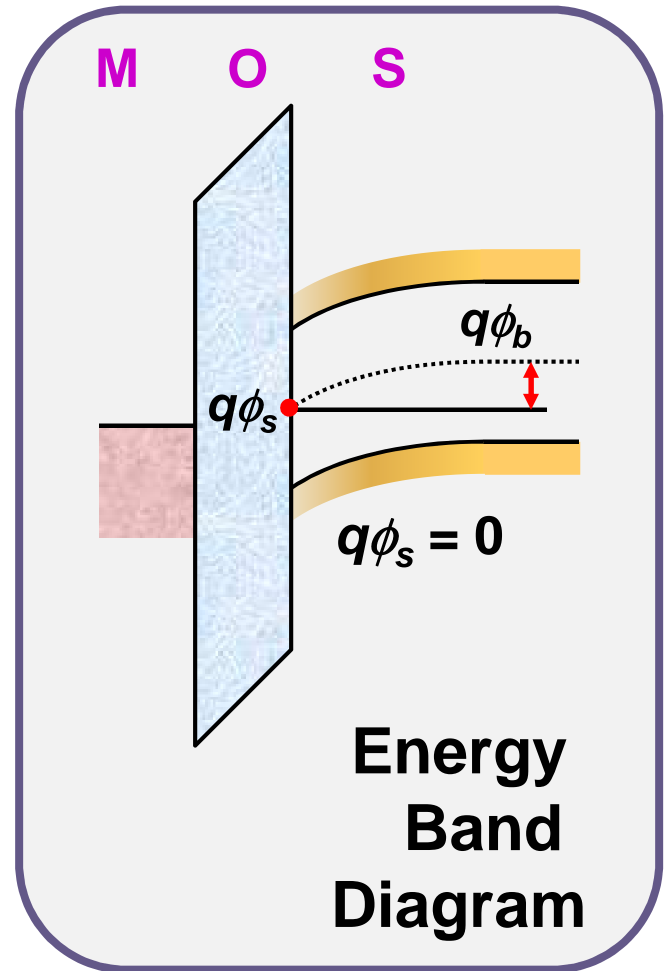

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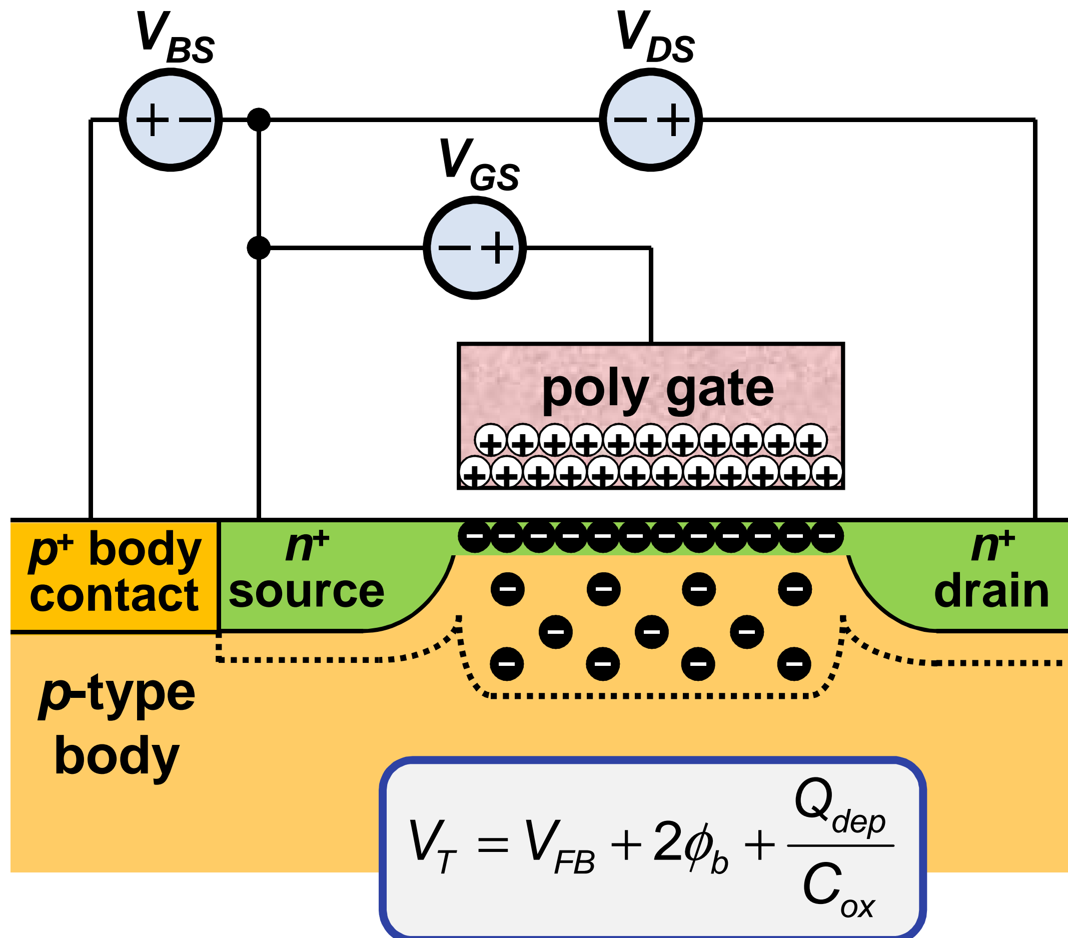
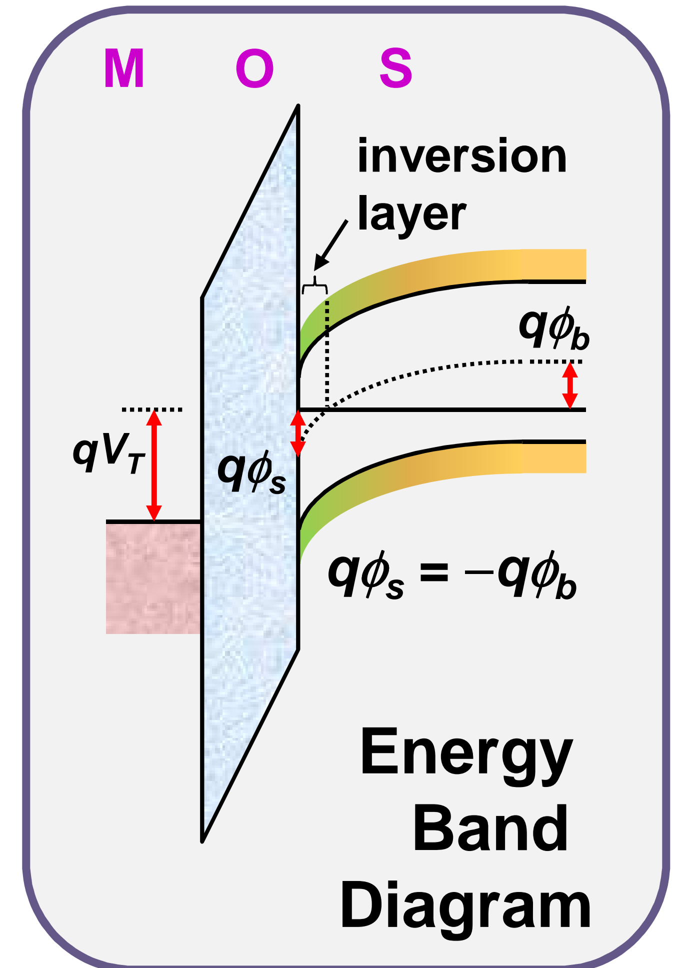
Onset of Strong Inversion ($V_{GS}=V_T$)



$$V_T = V_{FB} + 2\phi_b + \frac{Q_{dep}}{C_{ox}}$$



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Ideal Square Law Behavior

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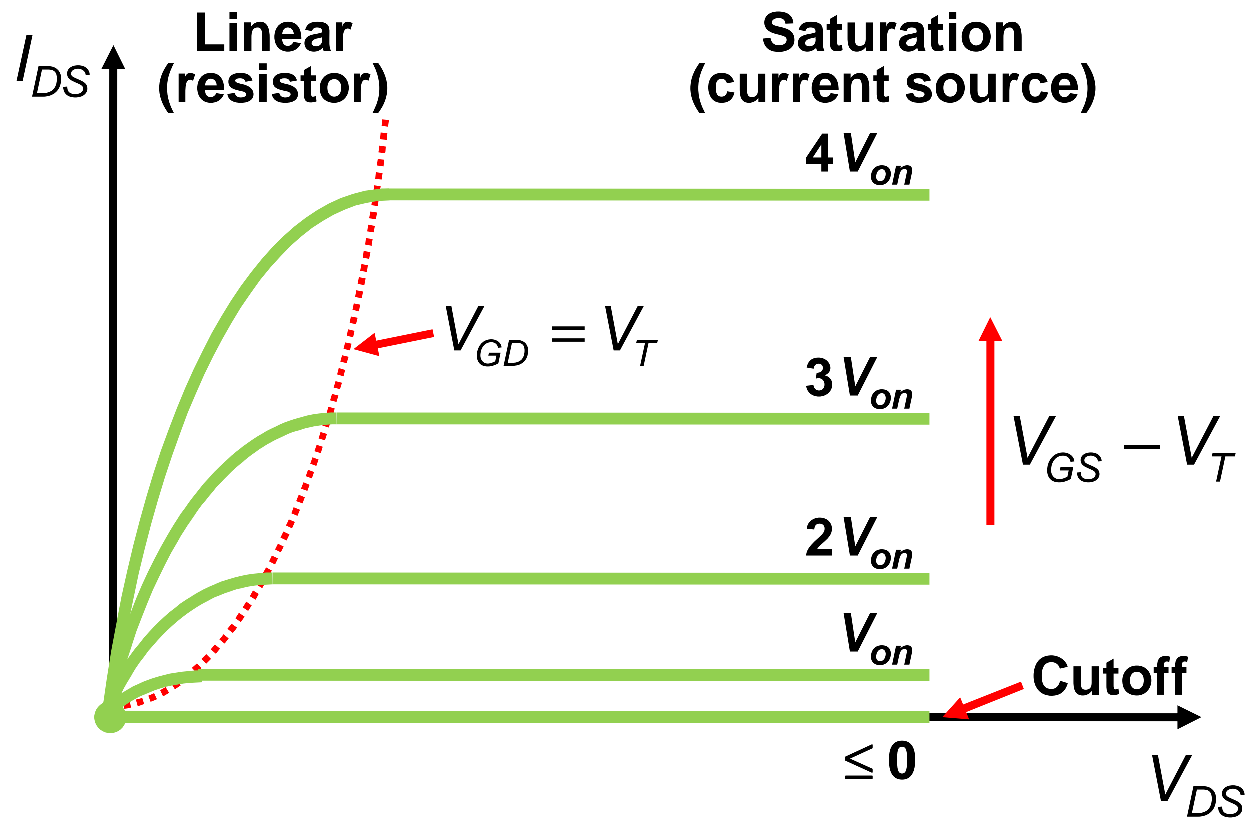
$$I_{DS} = \mu_N C_{OX} \frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS}$$

$$I_{DS} = \frac{1}{2}\mu_N C_{OX} \frac{W}{L}\left(V_{GS} - V_T\right)^2$$



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Short-Channel Effects

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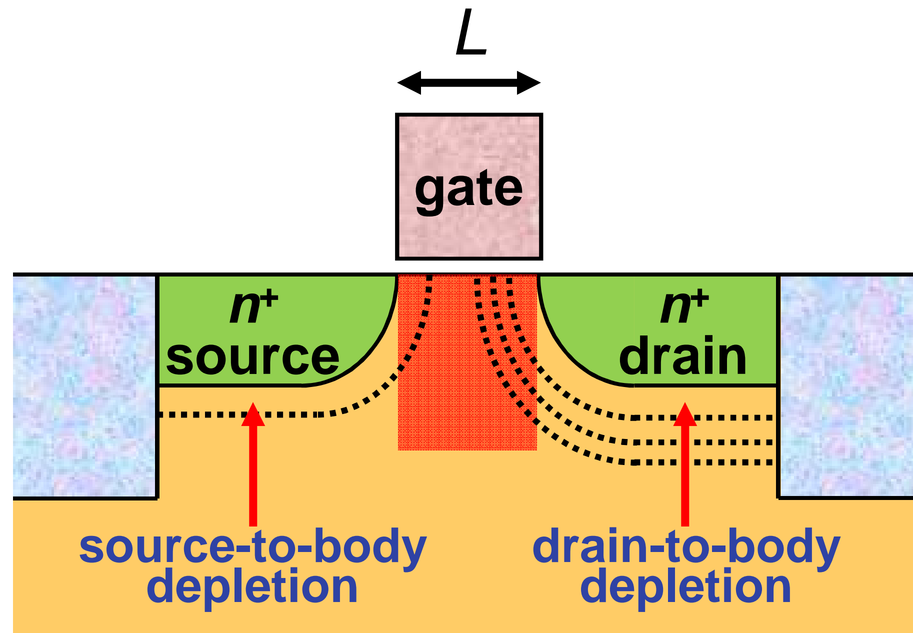

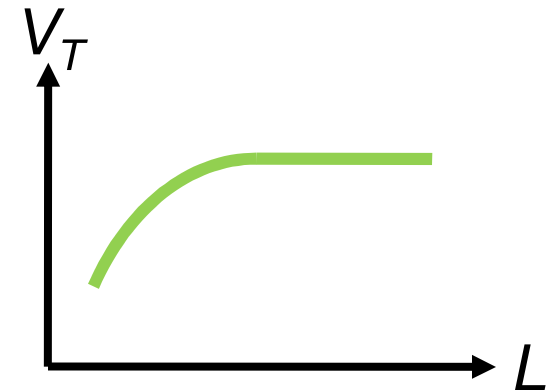

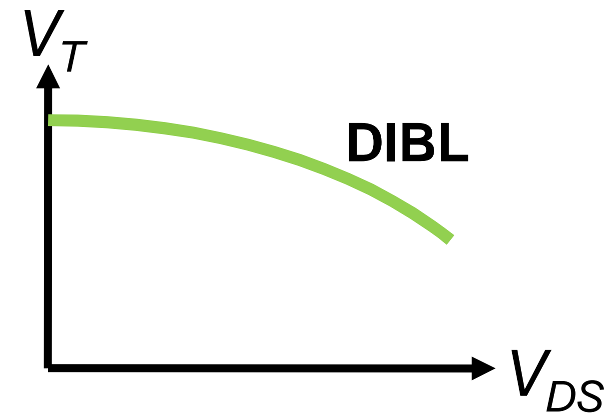

V_{DD} not scaling as aggressively as L

→ Higher channel electric fields

– Velocity saturation

– Mobility degradation

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Overcoming Short-Channel Effects

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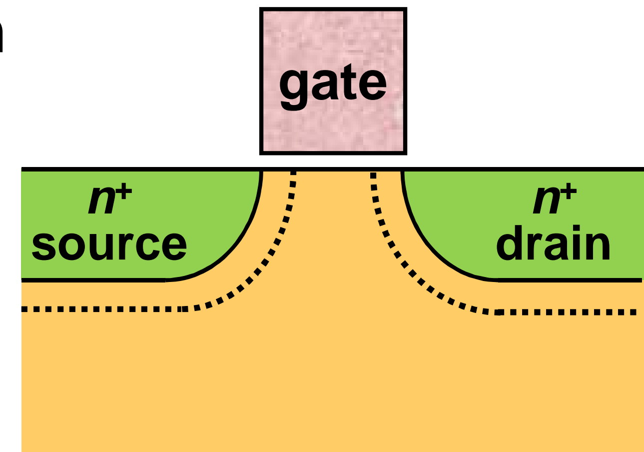
Improve gate control of channel charge

- Higher body doping but higher V_T
- Shallower source/drain but higher R_s
- Thinner T_{ox} but higher gate leakage
- High-K dielectric to reduce tunneling
- Metal gate to overcome poly depletion

$$x_j \propto \frac{1}{\sqrt{doping}}$$

Stressors for mobility enhancement

- Stress over-liners
- Embedded-SiGe source/drain
- Stress memorization



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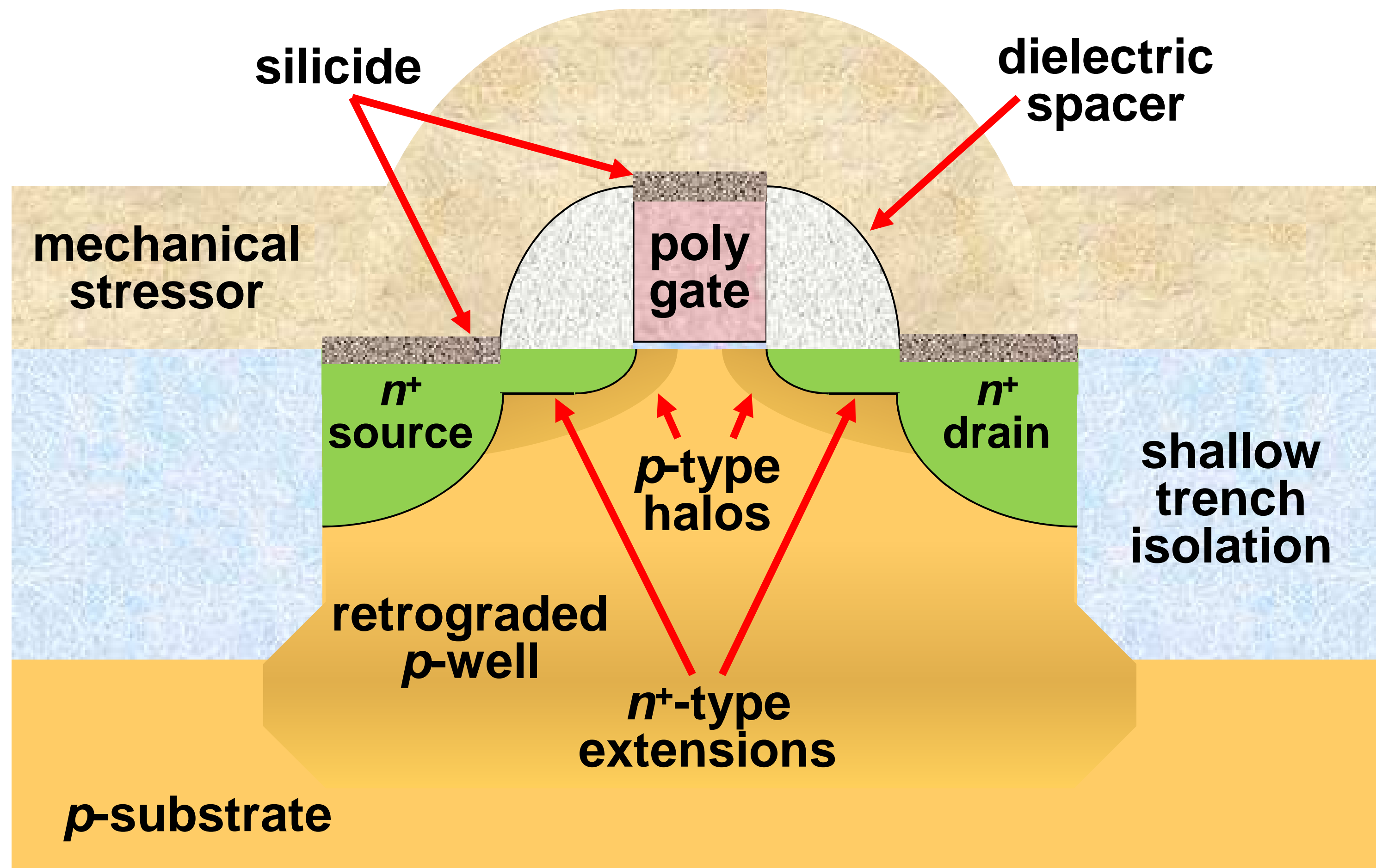
Modern-Day MOSFET



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BSIM V_T Equation

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- Calculated V_T reported in **LV9** output template

$$V_T = VTH0 + \left(K_{1ox} \cdot \sqrt{\Phi_s - V_{BSeff}} - K1 \cdot \sqrt{\Phi_s}\right)\sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox}V_{BSeff}$$

$$+ K_{1ox}\left(\sqrt{1 + \frac{LPEB}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + \left(K3 + K3B \cdot V_{BSeff}\right)\frac{TOXE}{W'_{eff} + W0}\Phi_s$$

$$- \left[\frac{DVT0W}{\cosh\left(DVT1W\frac{L_{eff}W'_{eff}}{l_{tw}}\right) - 1} + \frac{DVT0W}{\cosh\left(DVT1\frac{L_{eff}W'_{eff}}{l_t}\right) - 1}\right]\frac{V_{bi} - \Phi_s}{2}$$

$$- \frac{ETA0 + ETAB \cdot V_{BSeff}}{\cosh\left(DSUB\frac{L_{eff}}{l_{t0}}\right) - 1}\frac{V_{DS}}{2} - n\frac{k_B T}{q}\ln\left\{\frac{L_{eff}}{L_{eff} + DVTP0\left[1 + \exp\left(-DVTP1 \cdot V_{DS}\right)\right]}\right\}$$

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Please… Physics *not* Math

- Based on fundamental strong inversion criterion
- Extended to behaviorally model
  - Body effect ($V_{BS} < 0$ in NMOS, $V_{BS} > 0$ in PMOS)
  - Short-channel effect including DIBL
  - Narrow-width effect
  - Non-uniform lateral doping – halo implants
  - Non-uniform vertical doping – retrograded well
  - LOD effect from STI compressive stress
  - Well proximity effect from implant mask scattering
- Late to model new silicon V_T dependencies

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Linear Extrapolation Method

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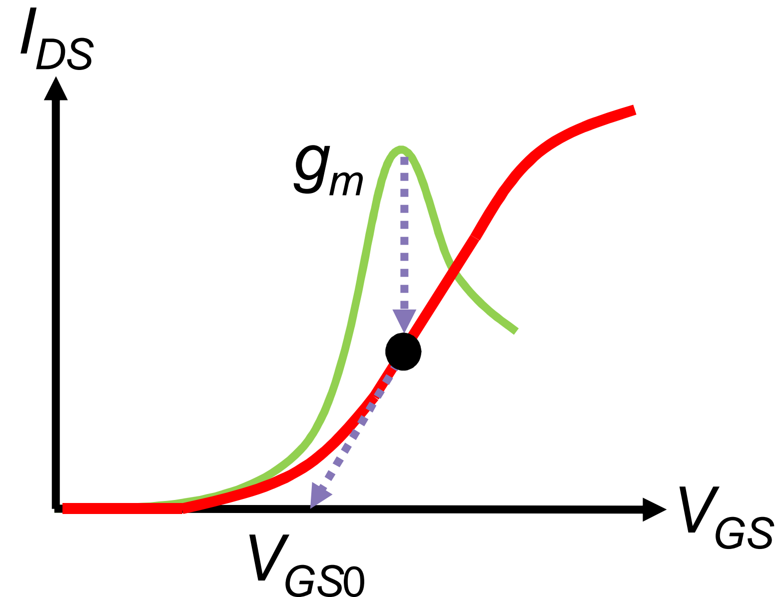
- Measure linear V_T

$$I_{DS} \propto \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

- Sweep I_{DS} vs. V_{GS} at low V_{DS} (e.g., 50 mV) & fixed V_{BS}

- Draw tangent line at peak $g_m = \dfrac{\partial I_{DS}}{\partial V_{GS}}$



$$V_{Tlin} = V_{GS0} - \frac{V_{DS}}{2}$$

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Quadratic Extrapolation Method

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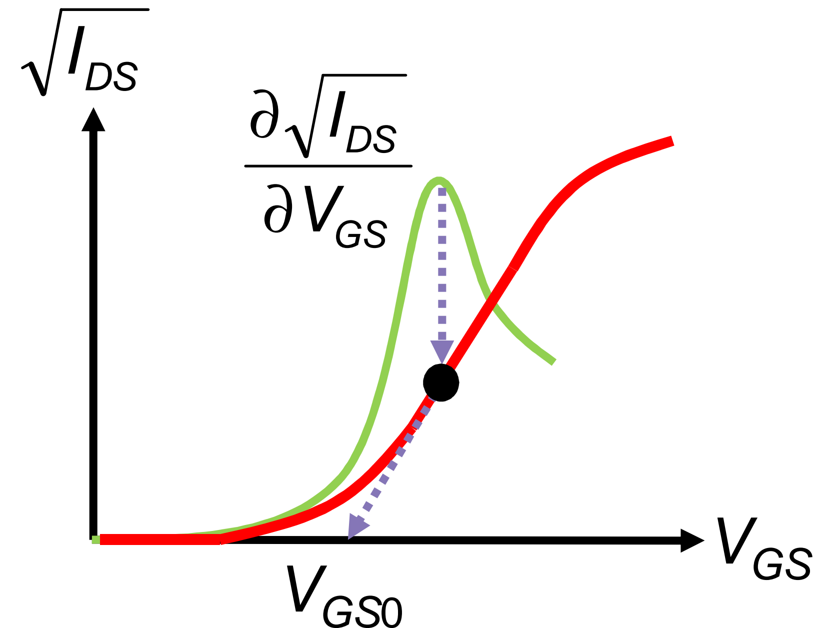
- Measure saturation V_T

$$I_{DS} \propto (V_{GS} - V_T)^2$$

- Sweep I_{DS} vs. V_{GS} at high V_{DS} (e.g., V_{DD}) & fixed V_{BS}
- Draw tangent line at peak $\dfrac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}$



$$V_{Tsat} = V_{GS0}$$

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Constant-Current Method

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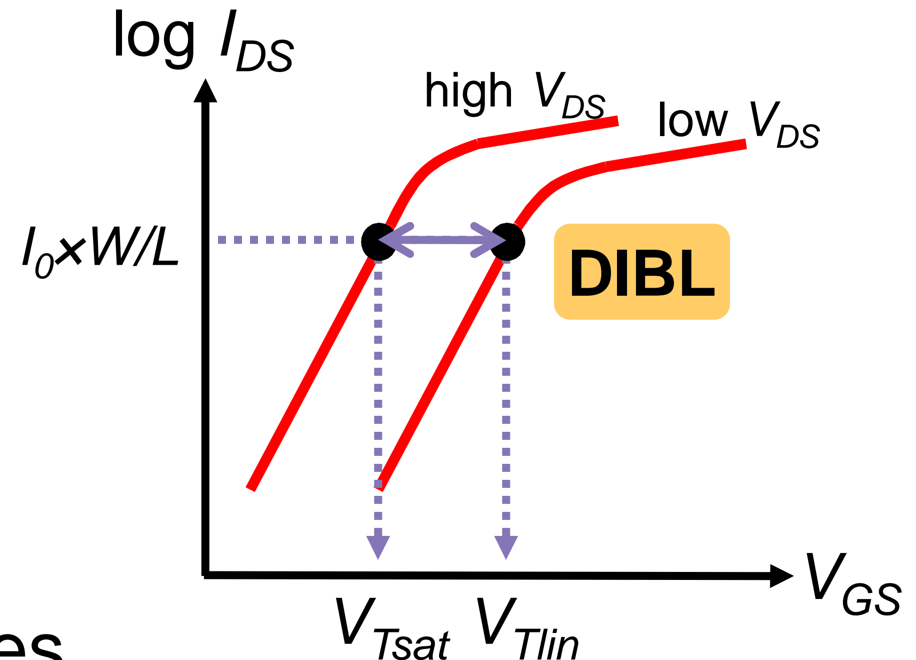
- Sweep log I_{DS} vs. V_{GS} at fixed V_{BS}
- Choose V_{DS} depending on region of operation
  - $V_{Tlin} \rightarrow$ low V_{DS}
  - $V_{Tsat} \rightarrow$ high V_{DS}
- Find V_{GS} when I_{DS} crosses user-specified threshold I_0 normalized to W / L
- Typical I_0 ~ 50 to 500 nA



$$V_T = V_{GS}\Big|_{I_{DS}=I_0 \times \frac{W_{drawn}}{L_{drawn}}}$$

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How The Fab Measures V_T

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- Linear / quadratic extrapolation
  - Popular decades ago
  - Short-channel effects → velocity saturation
  - Square law relations no longer valid
- Constant-current method
  - Most popular today to measure, specify & monitor V_T
  - Does not assume square law or other I_{DS} relationships
  - I_0 is user-/process-specific, can evolve with technology
  - No physical connection to onset of strong inversion, but threshold condition cannot be measured anyways

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.OPTION IVTH

Syntax

- `.OPTION IVTH=val | IVTHN=val1 | IVTHP=val2`

Description

- Extracts V_T using constant-current method

Supported MOSFET Models

- BSIM4 (level 54), BSIMSOI4 (level 70), PSP (level 69)

Supported Analyses

- .OP, .DC, .AC, .TRAN

Result

- `LX142` output template

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Example

- I_0 = 100 nA for both NMOS & PMOS

```
...
.OPTION IVTH=100n
.OPTION BYPASS=0
.PROBE TRAN LX142(m*)
...
```

- For different NMOS & PMOS thresholds

```
...
.OPTION IVTHN=300n IVTHP=70n
.OPTION BYPASS=0
.PROBE TRAN LX142(m*)
...
```

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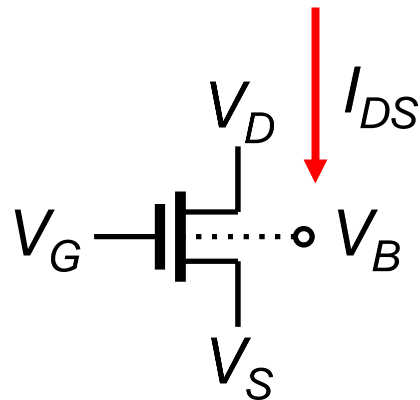
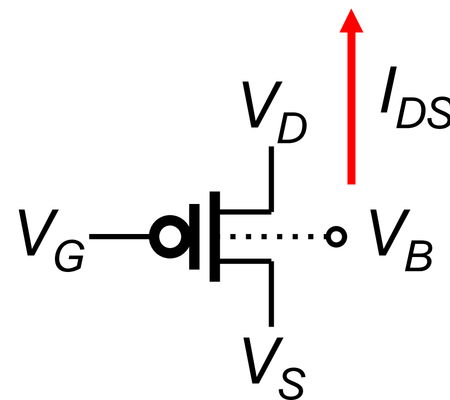
What HSPICE Will Do

- Determine FET node voltages at given instant
- Determine V_{GS} for $I_{DS} = I_0 \times W_{drawn} / L_{drawn}$
- Report extracted V_T in **`LX142`** output template

V_{GS} = ? for
I_{DS} = **`IVTHN`** $\times W / L$



V_{GS} = ? for
I_{DS} = **`IVTHP`** $\times W / L$



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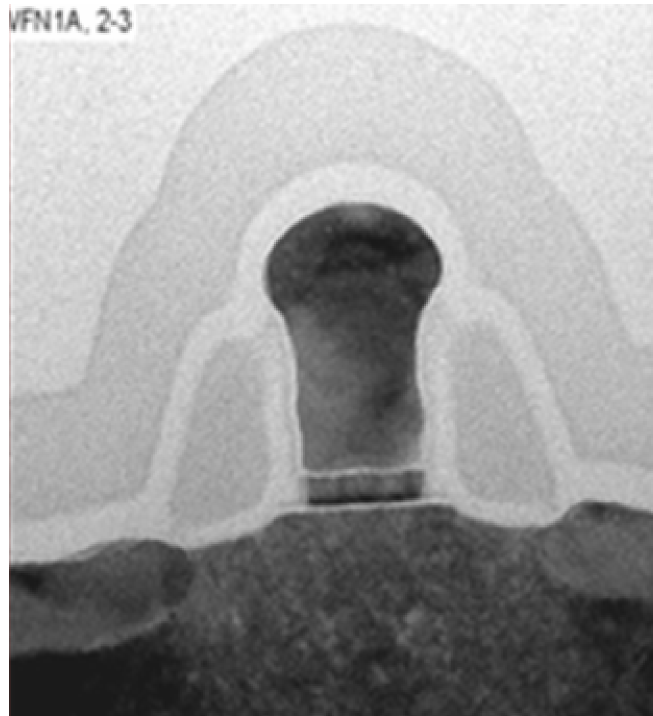
Evaluation Technology

- Predictive 32-nm SOI-CMOS models for high-performance logic technology



- Fab I_{DS} thresholds
  - NMOS → 300 nA × W/L
  - PMOS → 70 nA × W/L
- $W / L = 2 \times 1$ µm / 40 nm floating-body devices

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DC Test : V_{GS} Ramp

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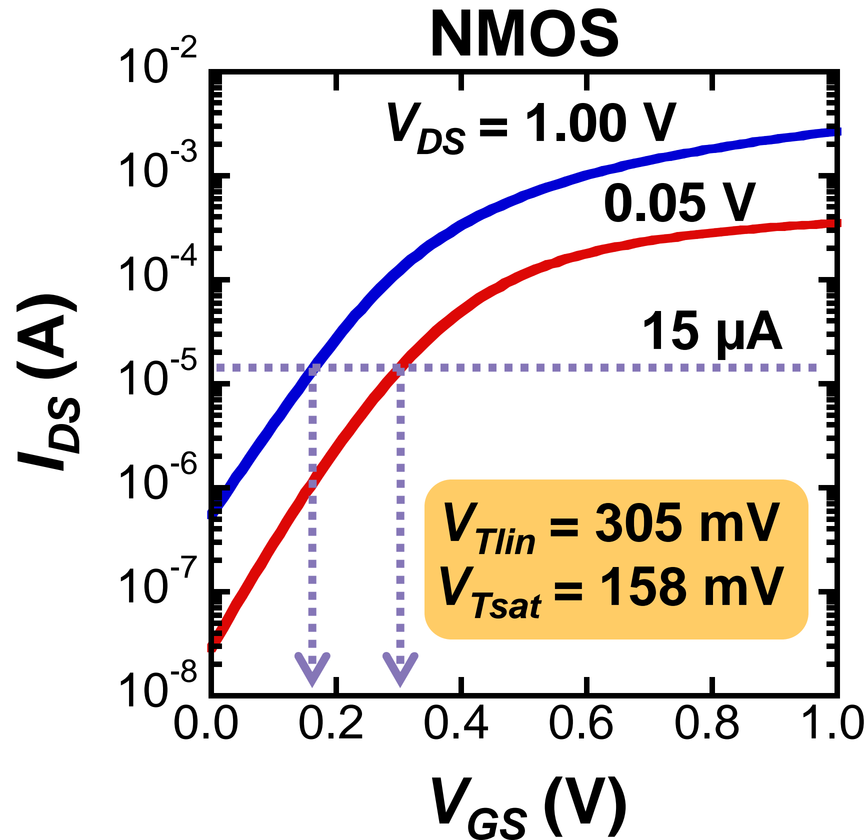

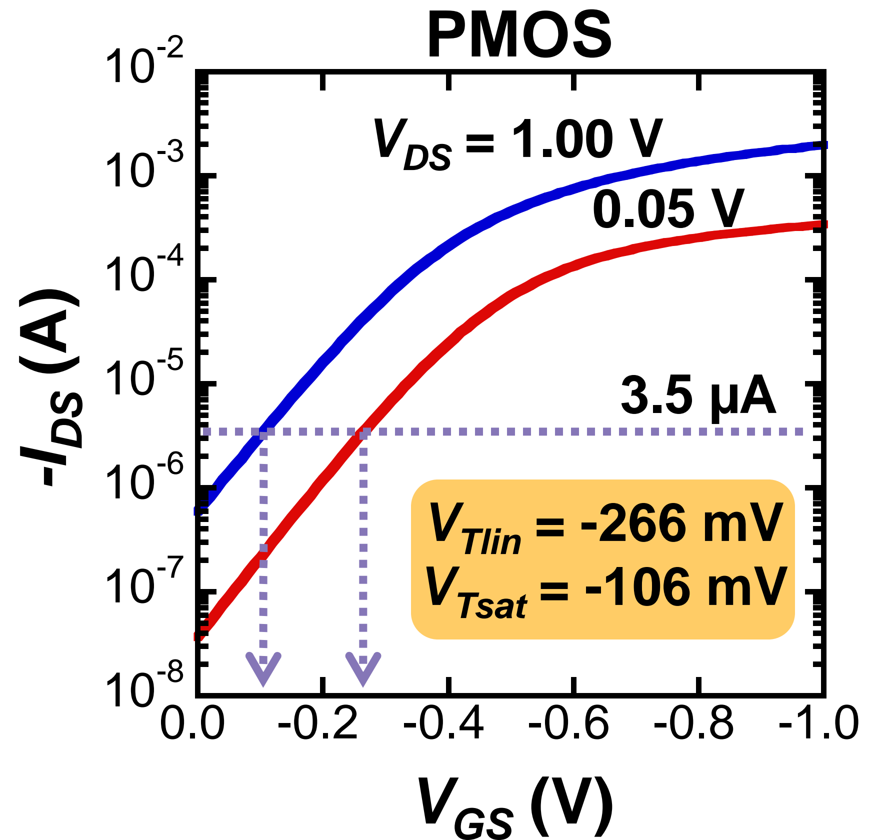

V_{Tlin} & V_{Tsat} results match `LX142`

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Transient Test 1: V_{DS} Ramp

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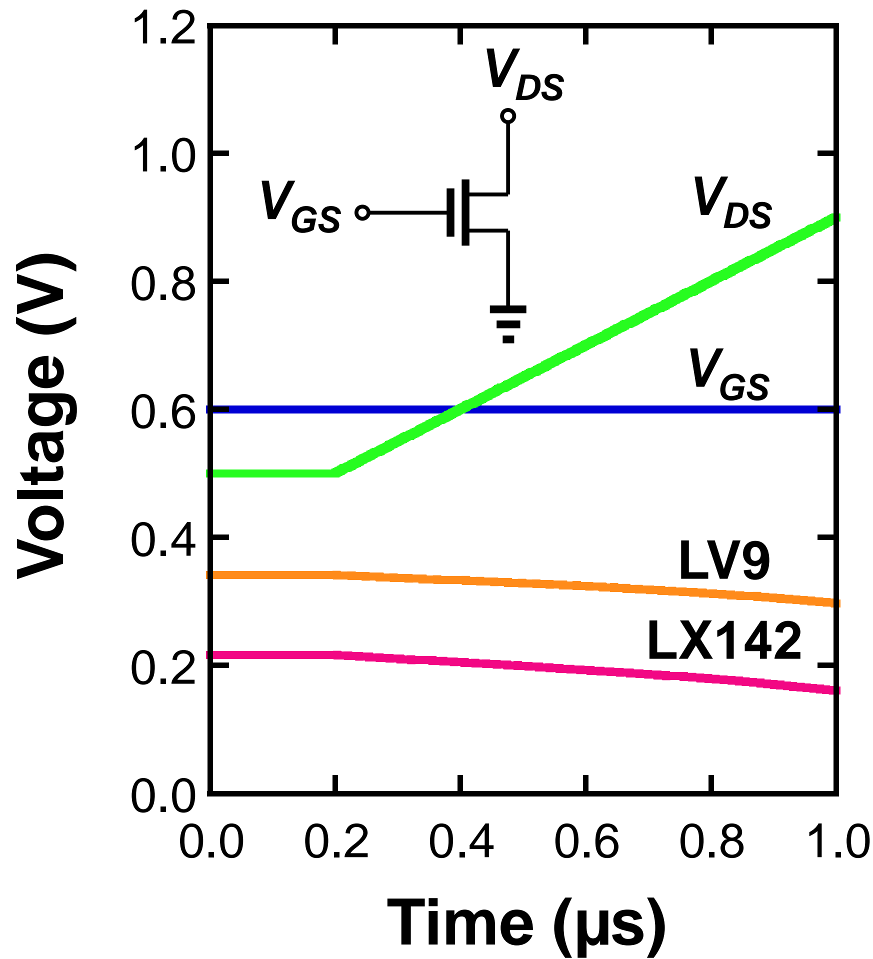

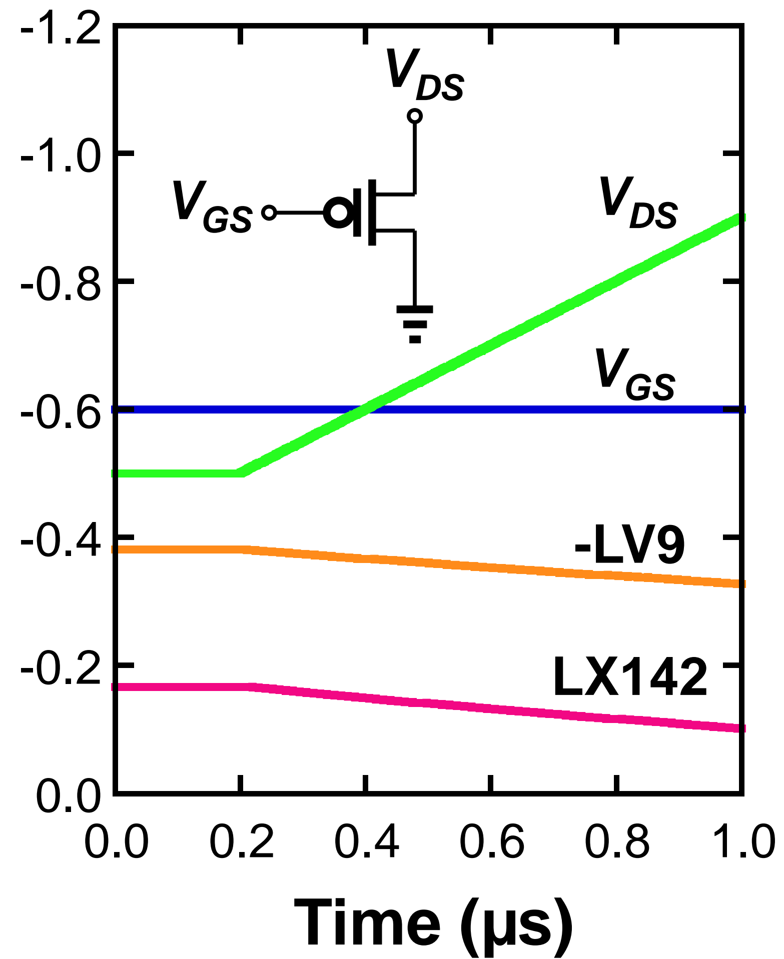

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Transient Test 2: V_{GS} Ramp

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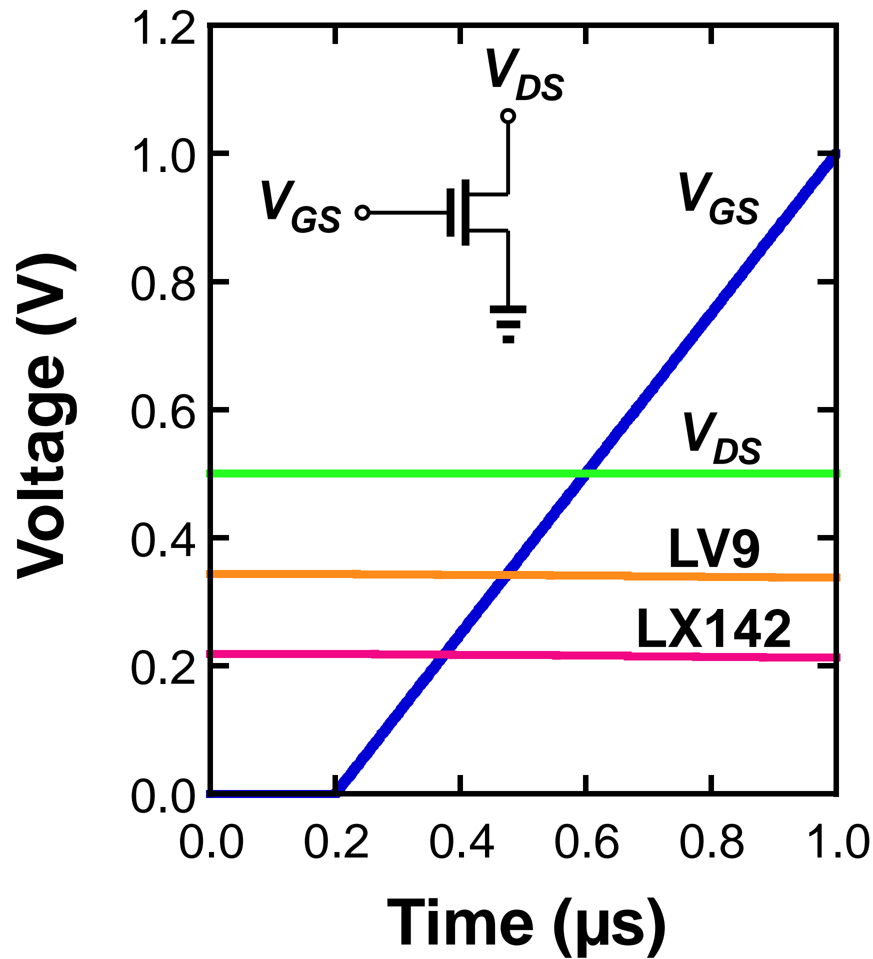

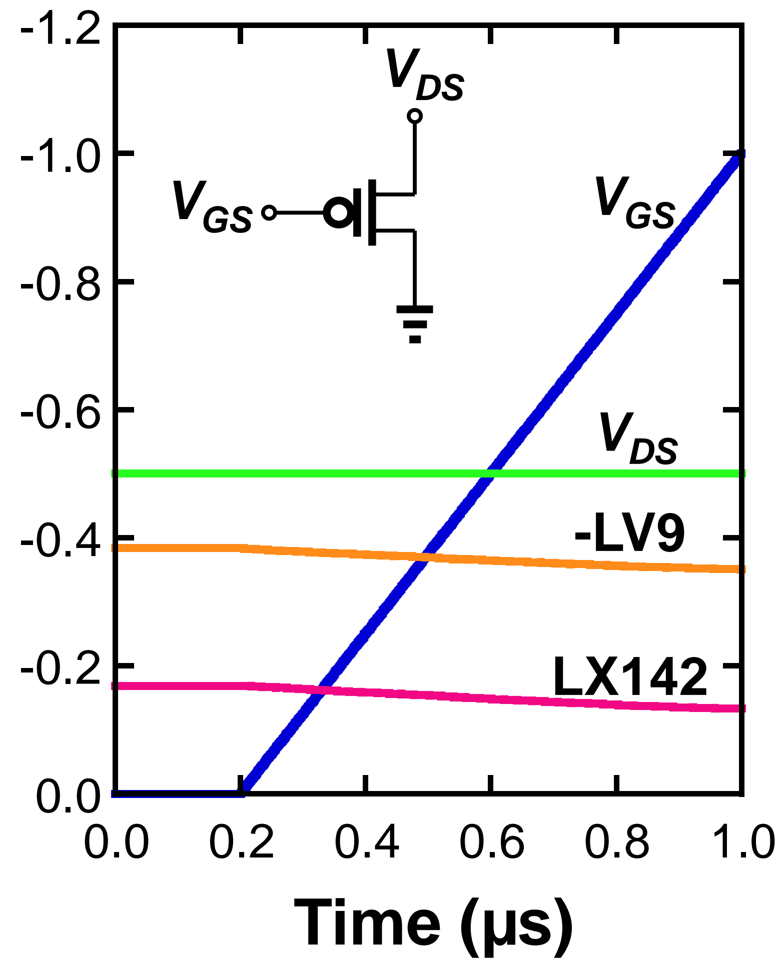

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Impact on `.TRAN` Runtime

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- **`.TRAN`** simulations most relevant & time-consuming
- Low-voltage bandgap reference (analog content)
- Need HSPICE optimization to remove **`BYPASS=0`**

`.OPTION IVTH`	`.OPTION BYPASS`	Normalized Runtime
Disabled	Default	1.0
Enabled	Default	1.2
Enabled	0	2.3

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Conclusion

- HSPICE can now conveniently extract V_T that matches exactly how V_T is measured in the fab using constant-current method
- Feature supports **`.OP`**, **`.DC`**, **`.AC`** & **`.TRAN`** analyses for industry-standard BSIM4, BSIMSOI4 & PSP models
- Usage
  - **`.OPTION IVTHN=`*`val1`*` IVTHP=`*`val2`*` BYPASS=0`**
  - V_T result in **`LX142`** MOSFET output template

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Acknowledgments

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