Multi-Gbps Optical Receivers with CMOS Integrated Photodetectors

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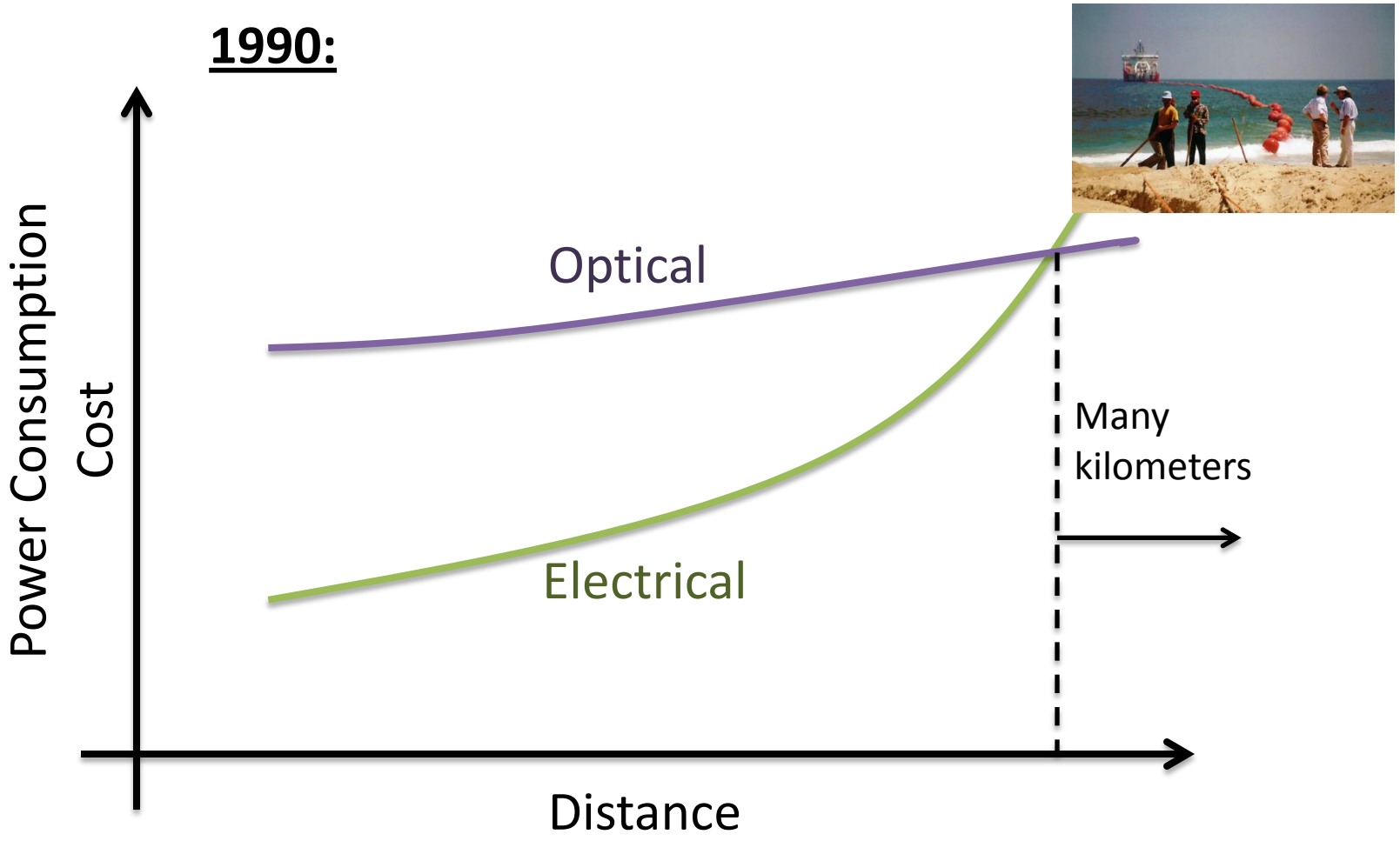
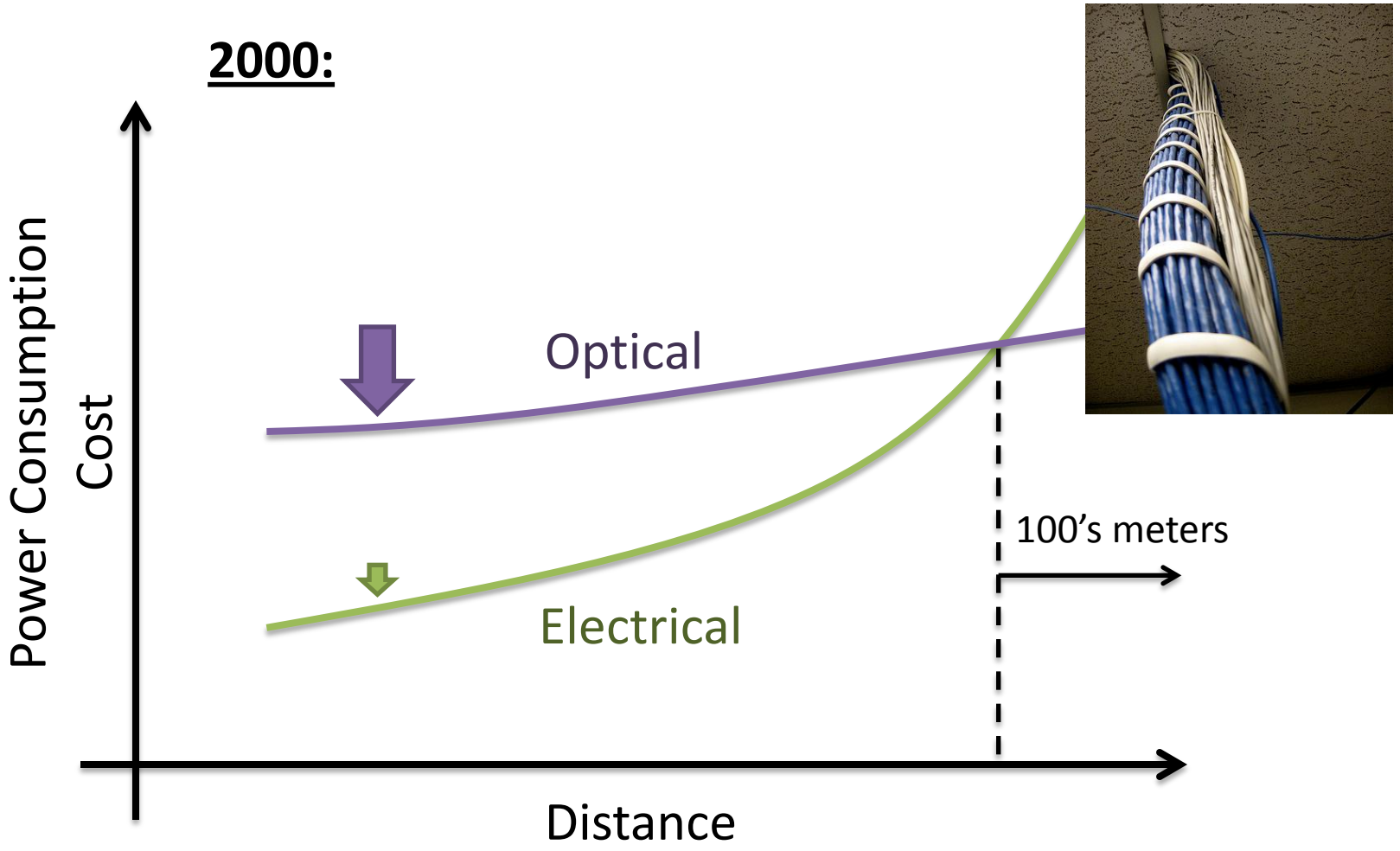
Outline

- **Introduction**
  - **Trend towards short-reach optical**
  - **Trend towards highly integrated transceivers**
- Tutorial on High-speed CMOS photodetection
  - Optical properties of silicon
  - Standard CMOS photodetectors
  - Diffusion-shielded photodetectors
  - Spatially modulated light detectors
- Equalization to improve CMOS photodetectors
  - Analog equalization
  - Decision-Feedback Equalization
- Case study: 0.18 μm CMOS integrated optical receiver
  - SML detector
  - Analog equalizer
- Photodetectors in nanoscale CMOS technologies
  - Experimental results from a 65 nm process

Optical Communication Evolution



Optical Communication Evolution



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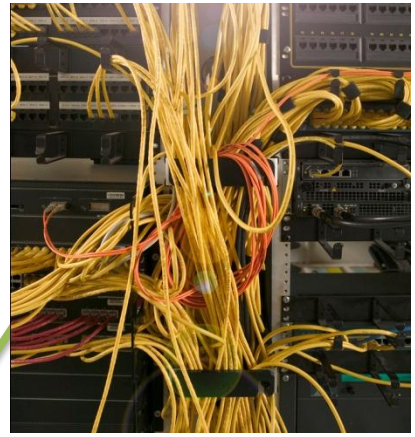

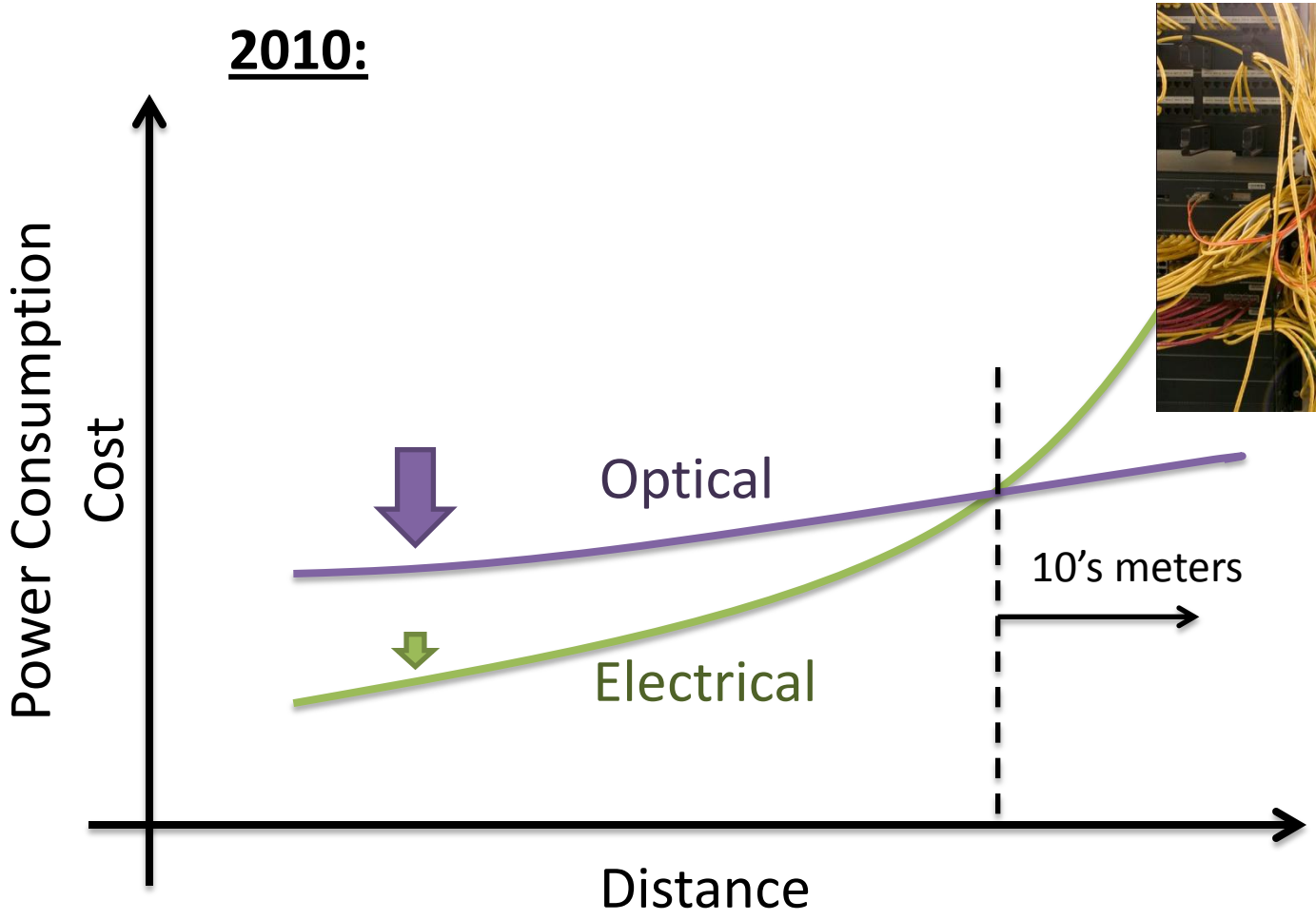

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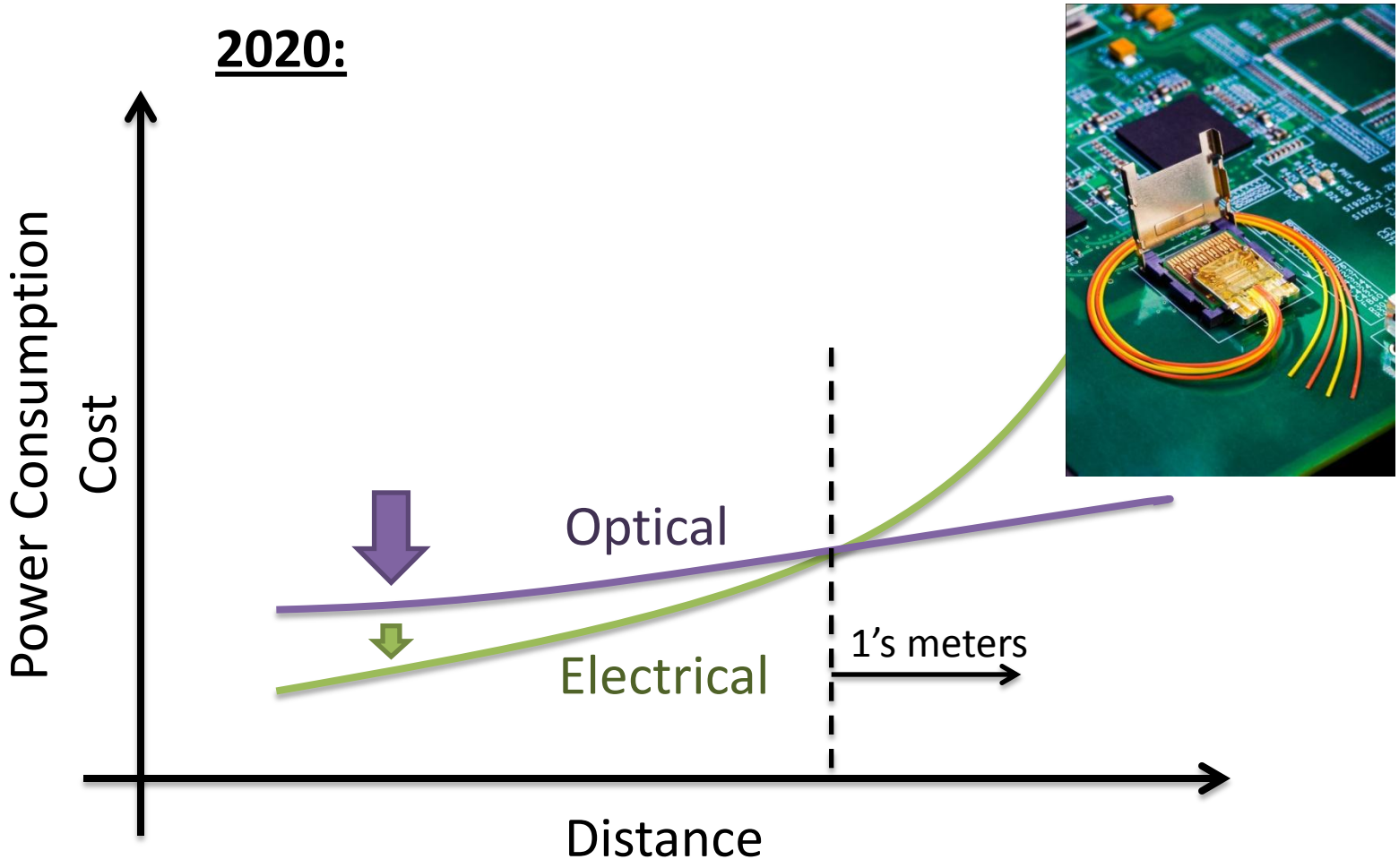

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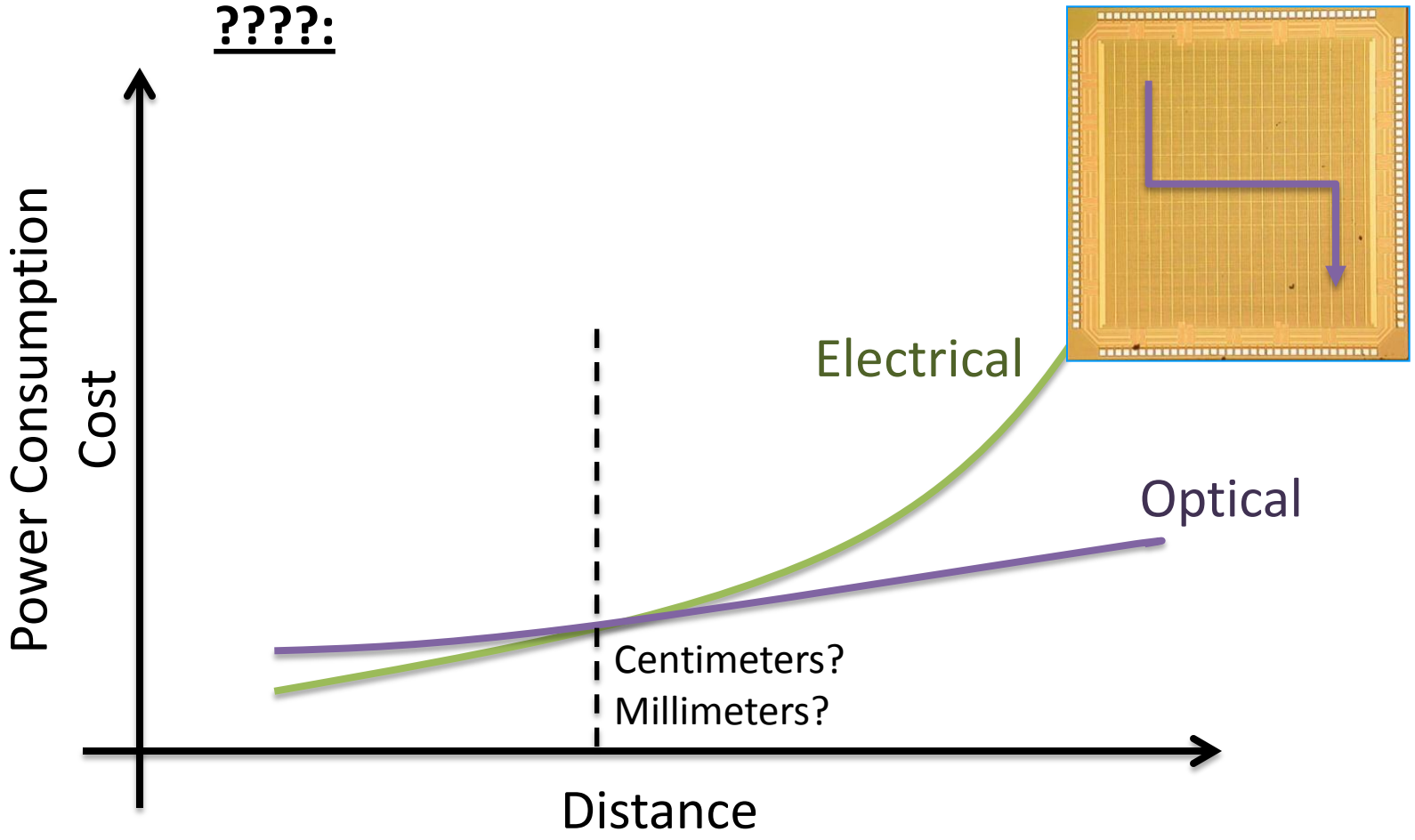


Short-Reach Optical Communication

Characteristics

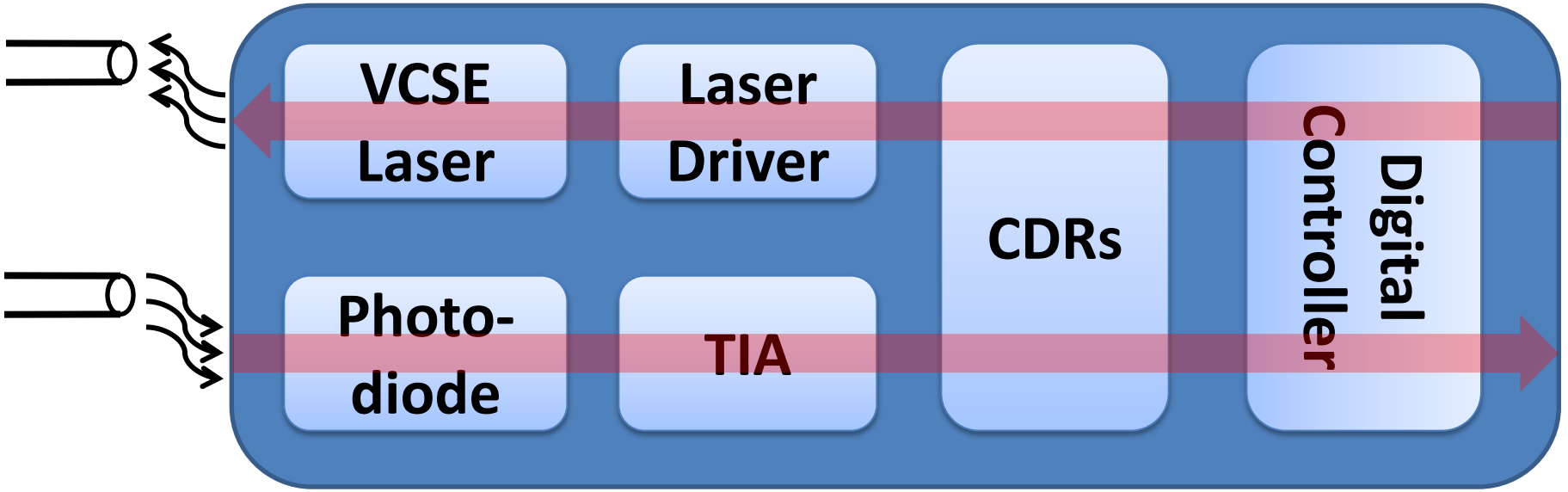
- High volume
- High port density

Requirements

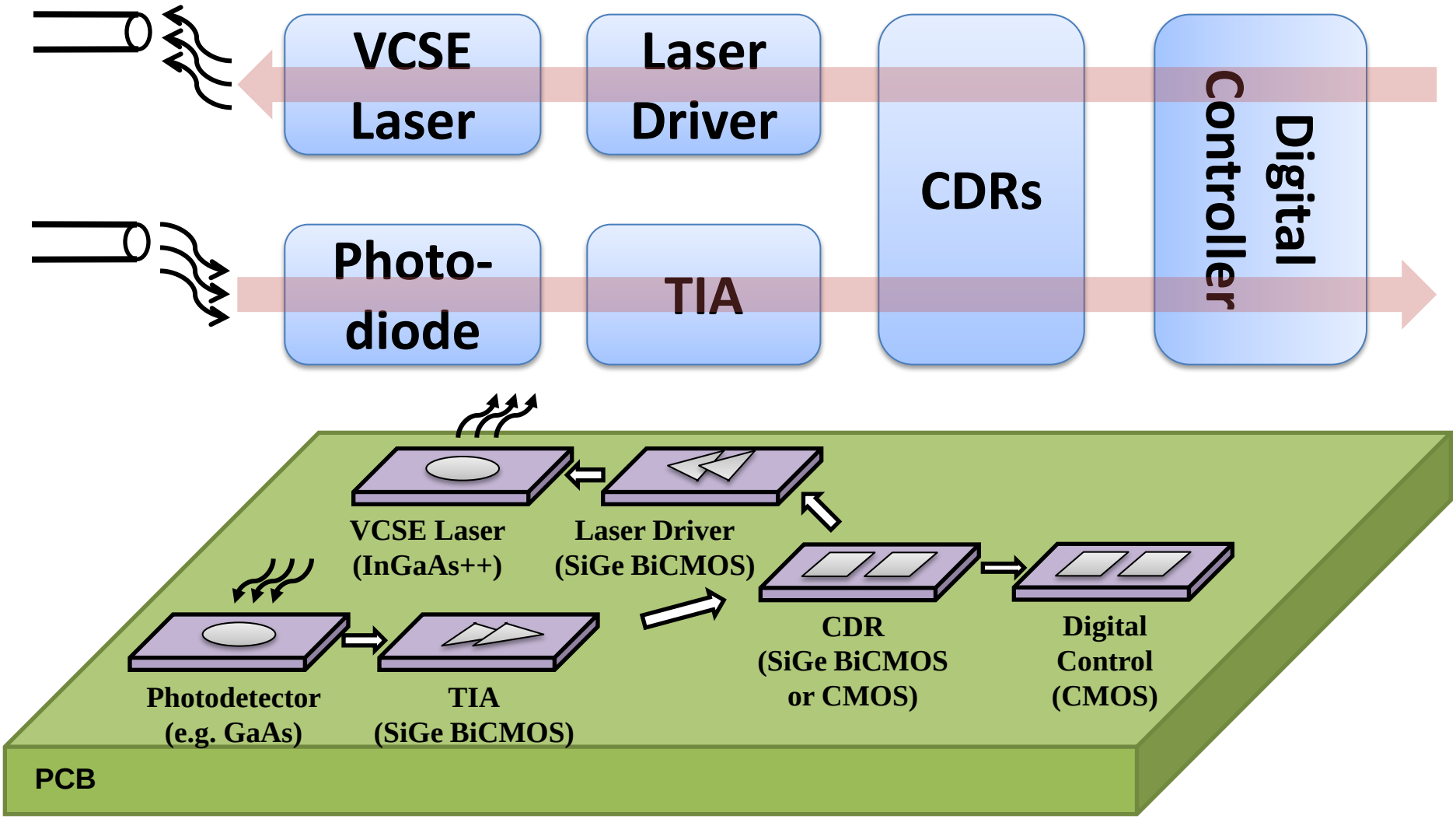
- CHEAP!
  - VCSEL lasers at λ = 850nm
  - Multimode fiber
- Integration
- Low-power

Good recipe for CMOS!

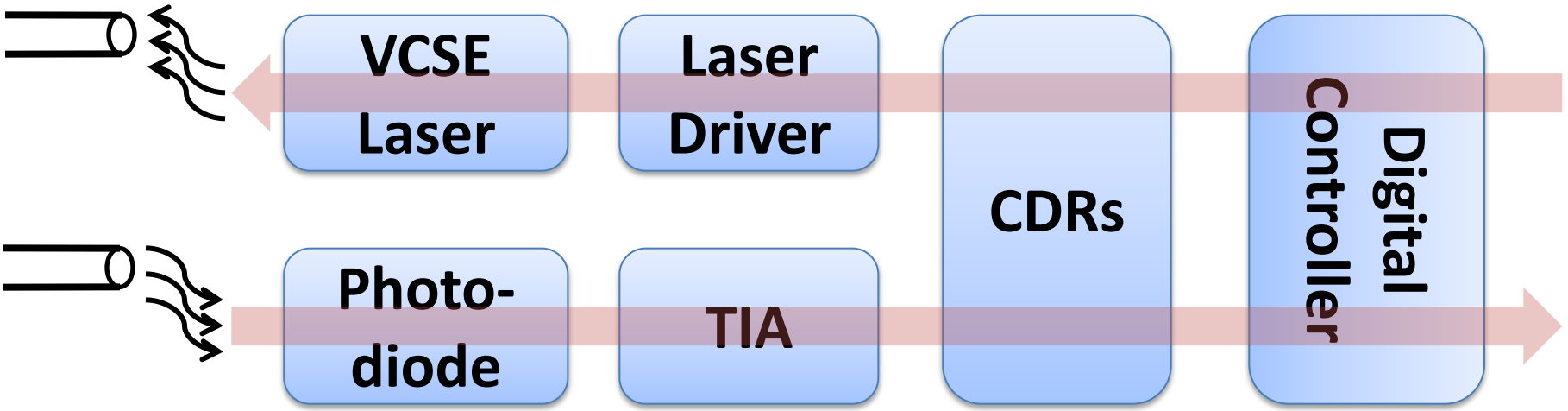
Optical Transceiver

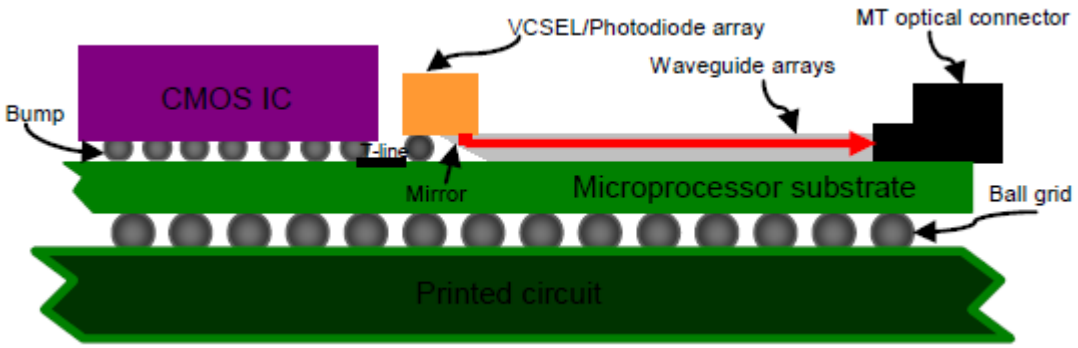


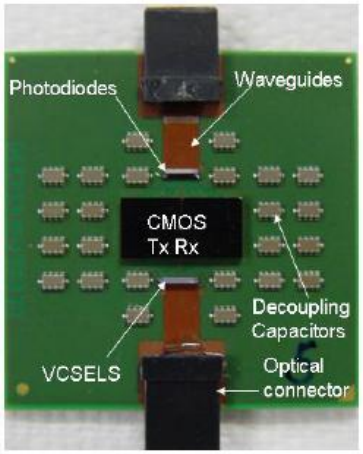
Optical Transceiver



Optical Transceiver – SiP

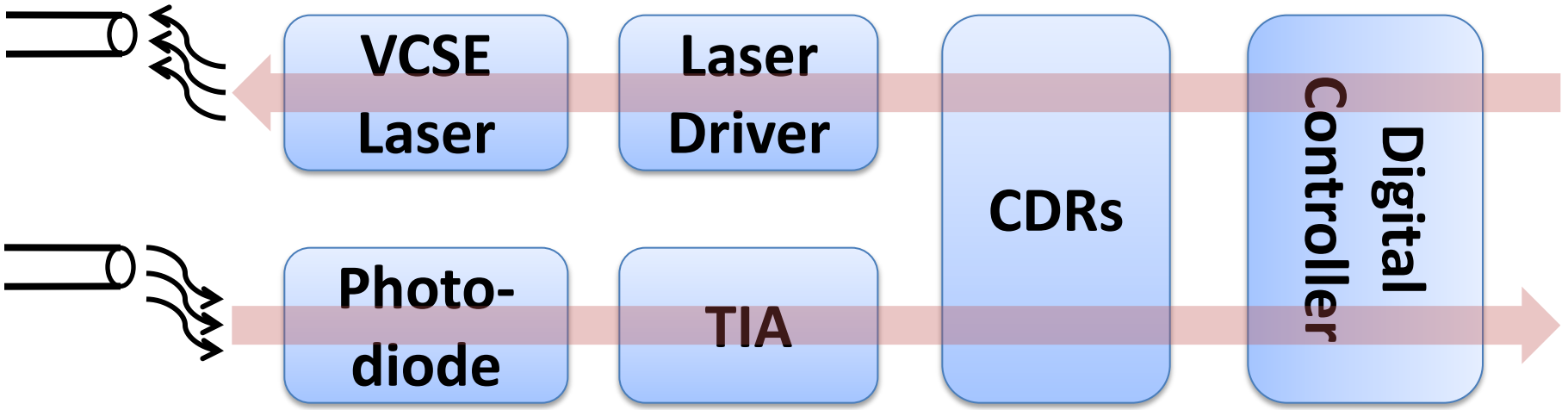


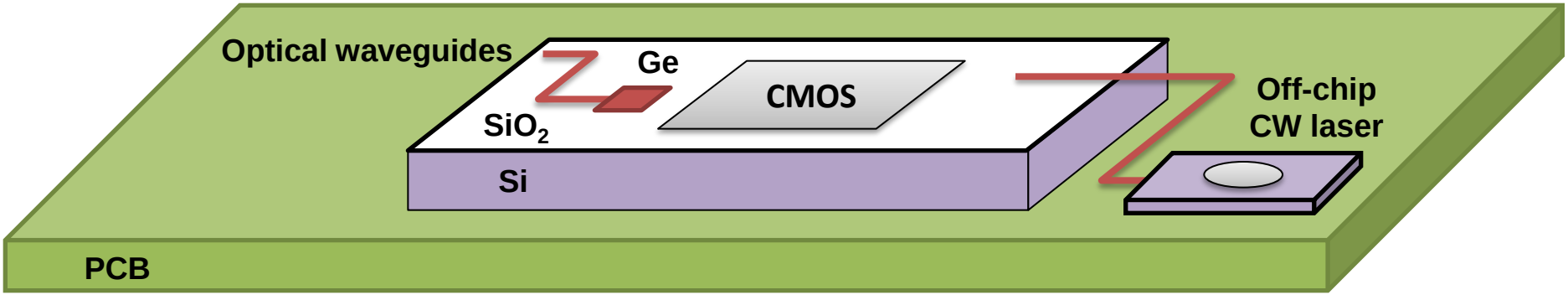




I. Young et al, "Optical I/O technology for tera-scale computing," *JSSC*, Jan. 2010.

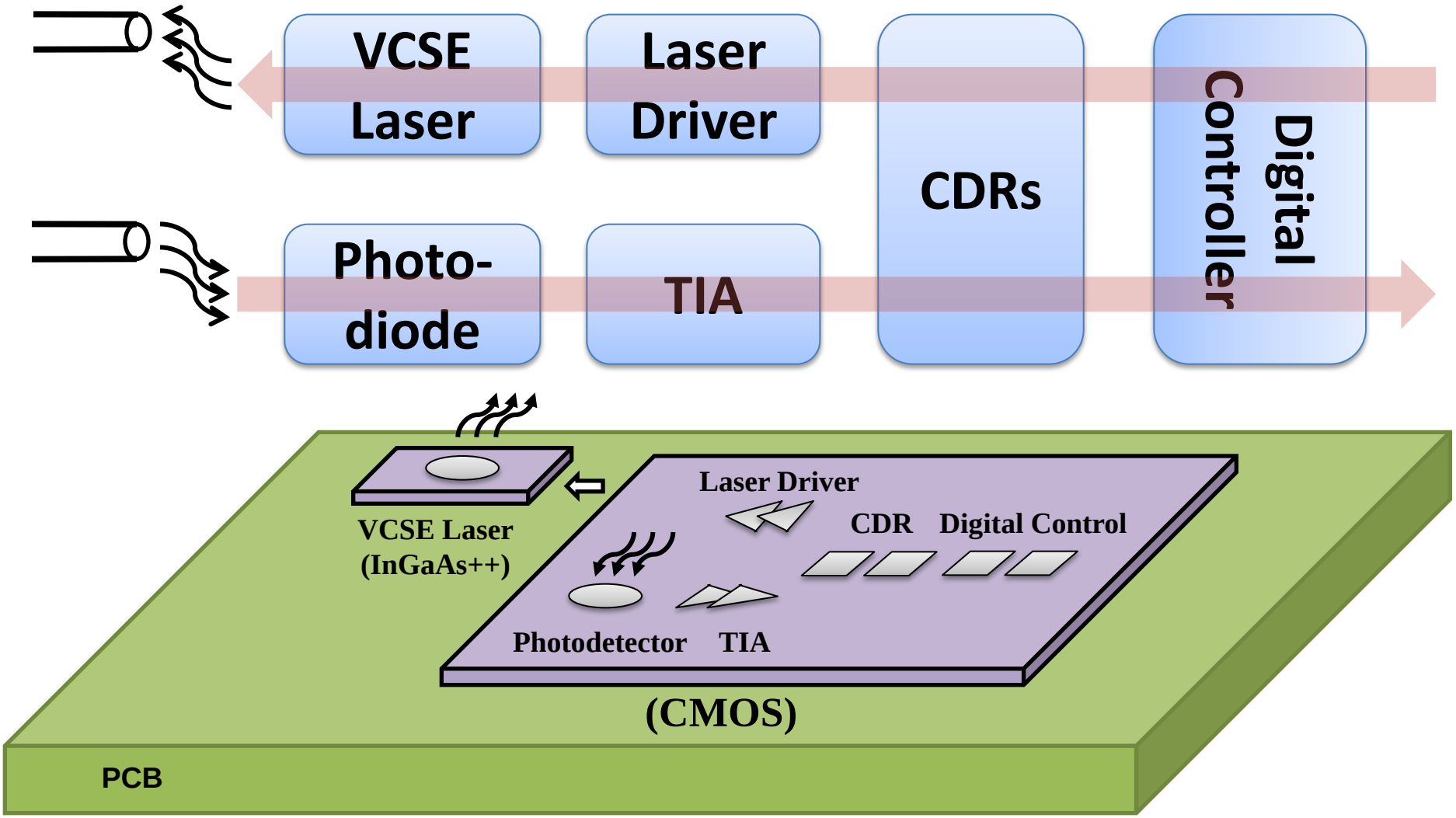
Optical Transceiver – Silicon Photonics





e.g. I. Young et al, "Optical I/O technology for tera-scale computing," *JSSC*, Jan. 2010.
Analui et al, "A Fully Integrated 20-Gb/s Optoelectronic Transceiver Implemented in a Standard 0.13-µm CMOS SOI Technology," *JSSC*, Dec. 2006.

Optical Transceiver



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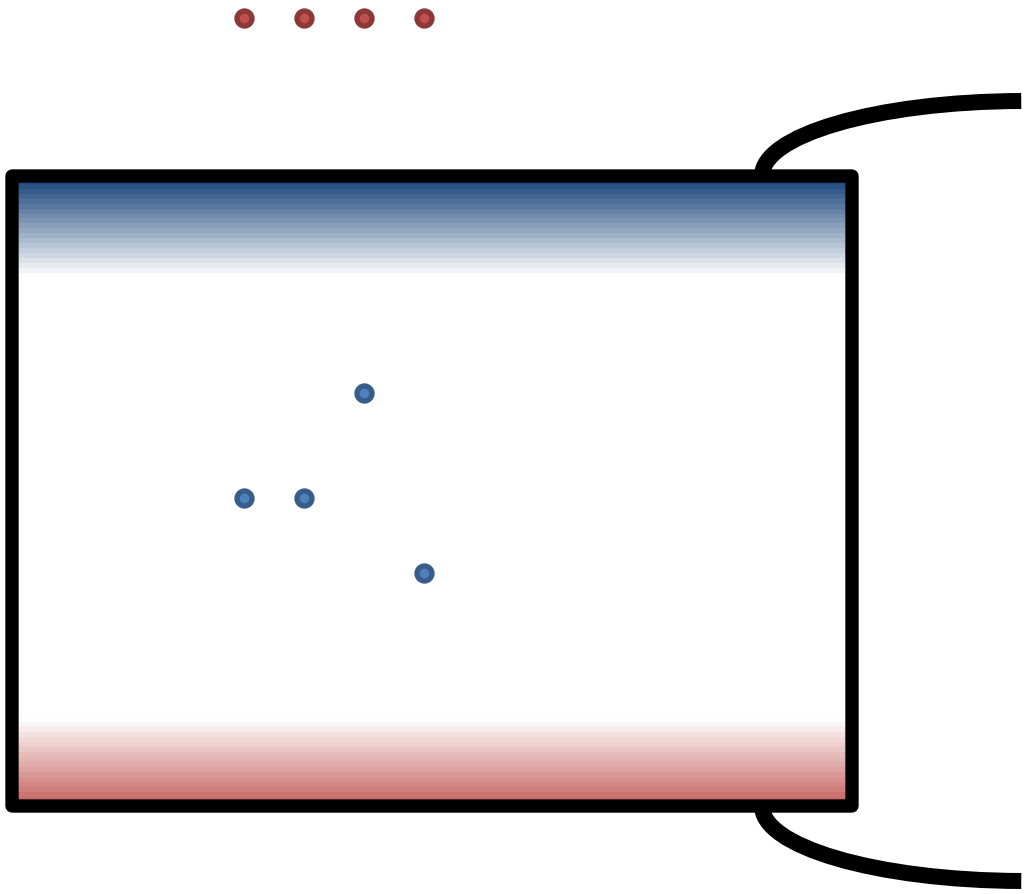
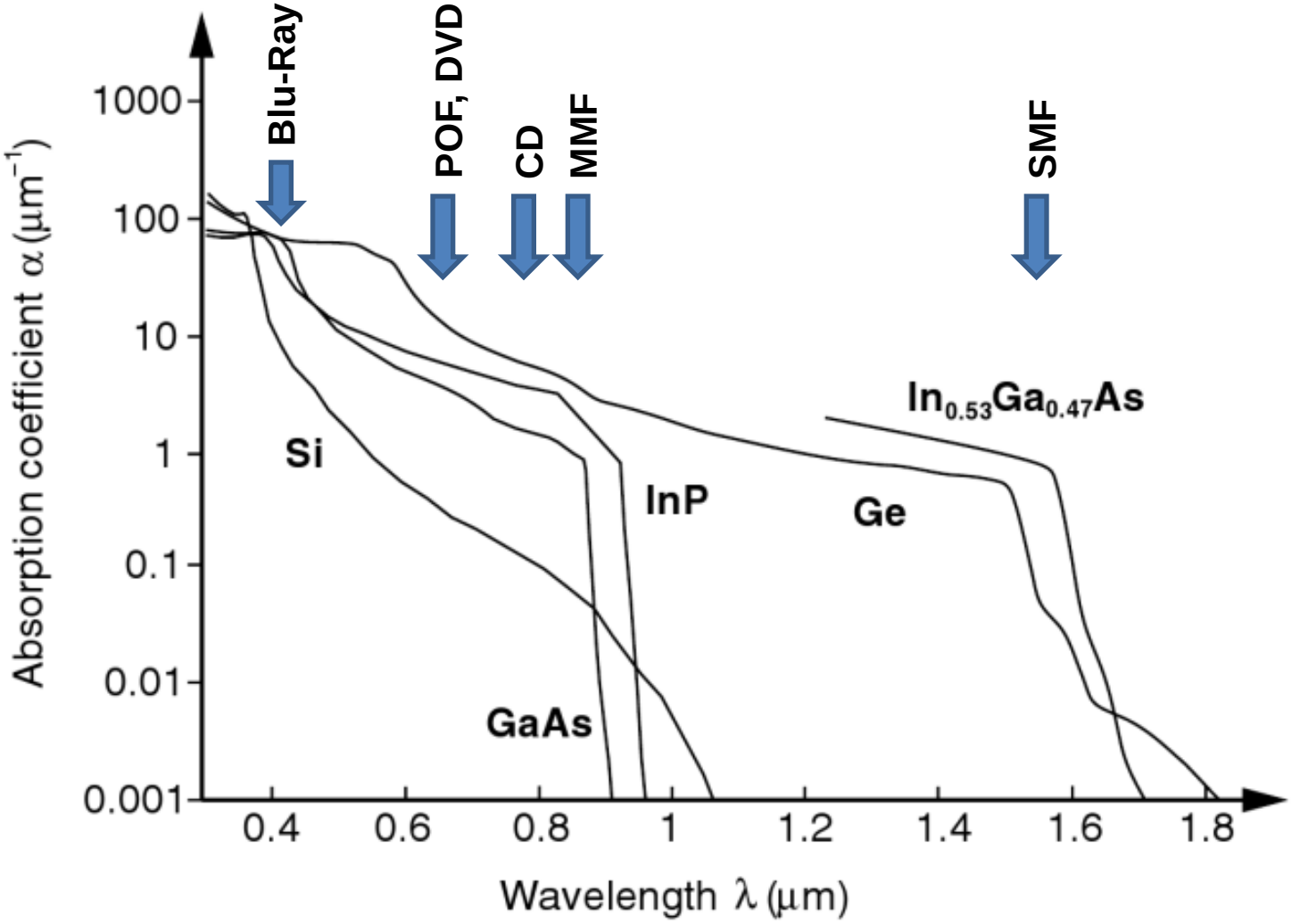
High-Speed Photodetectors

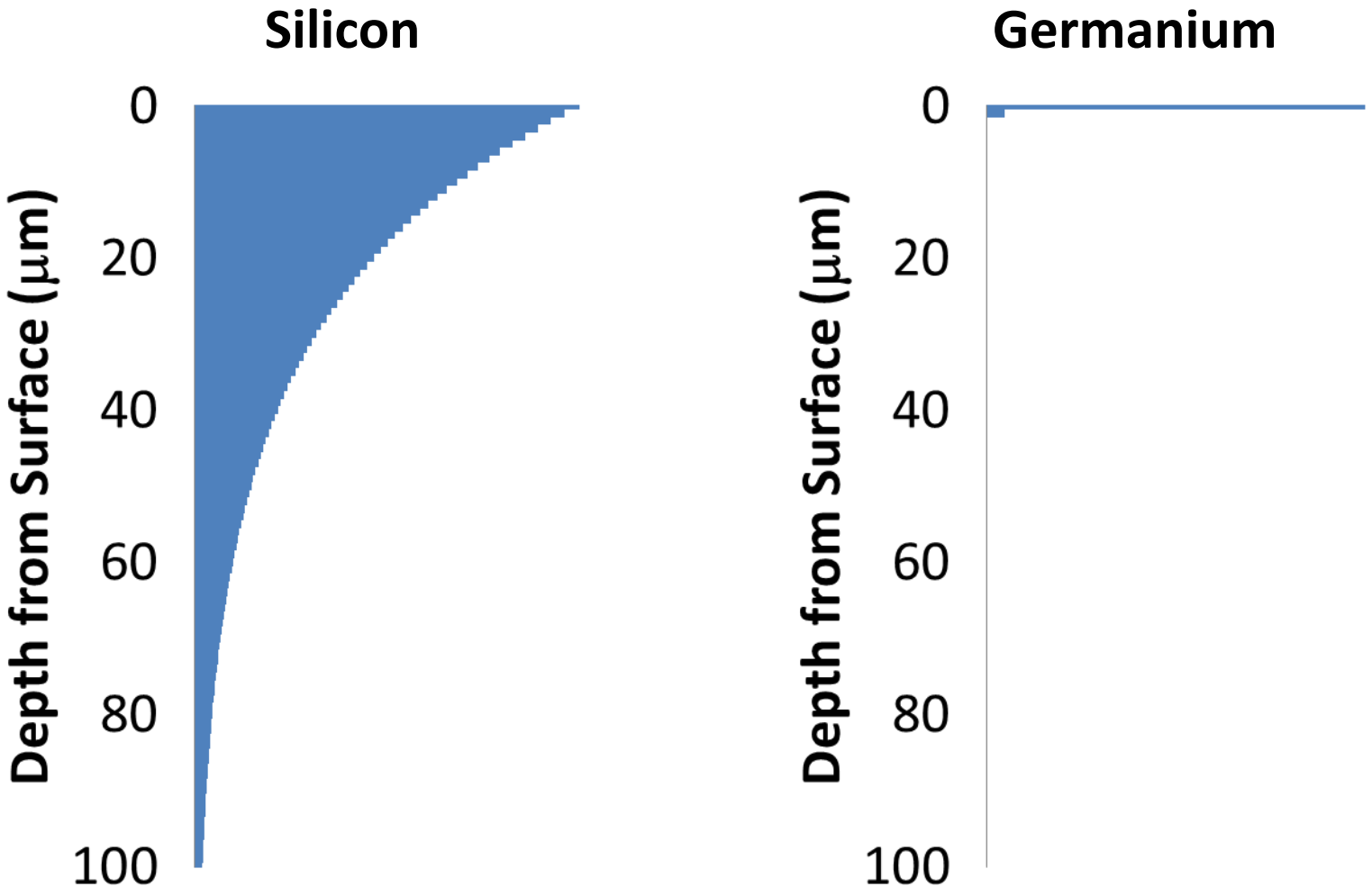


Optical Absorption of Semiconductors

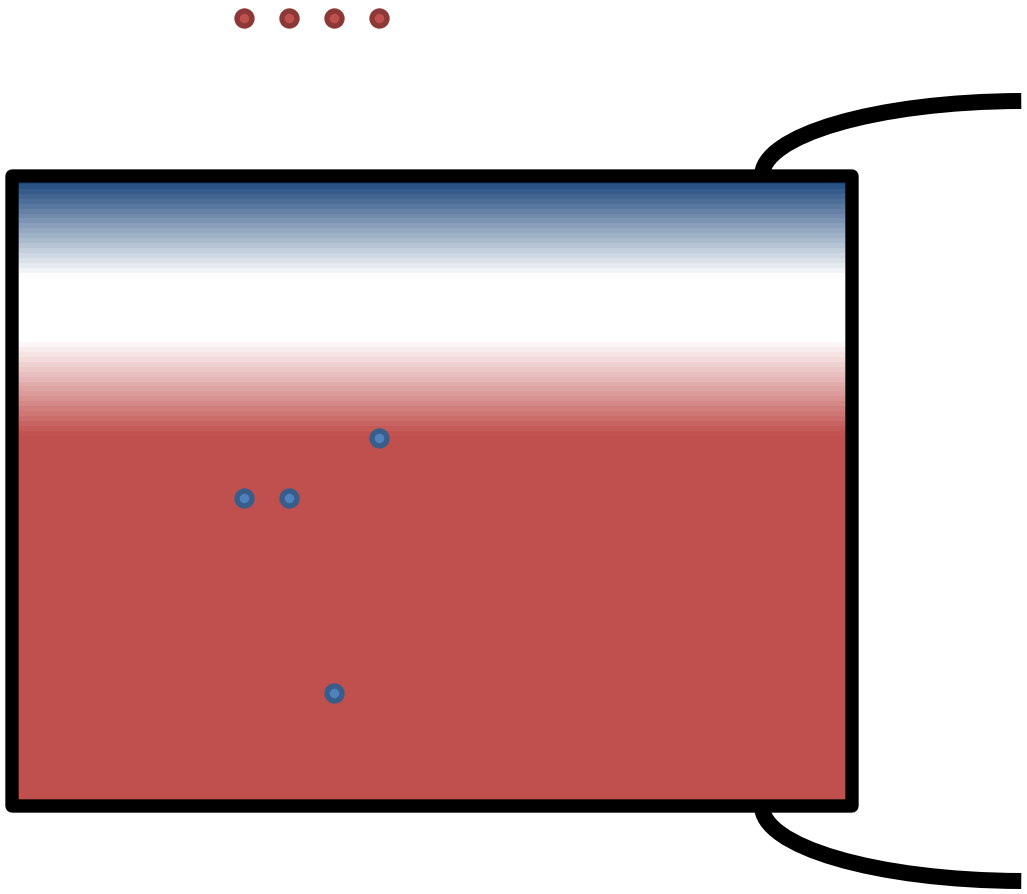


From: H. Zimmermann, *Silicon Optoelectronic Integrated Circuits*, Springer, 2004.

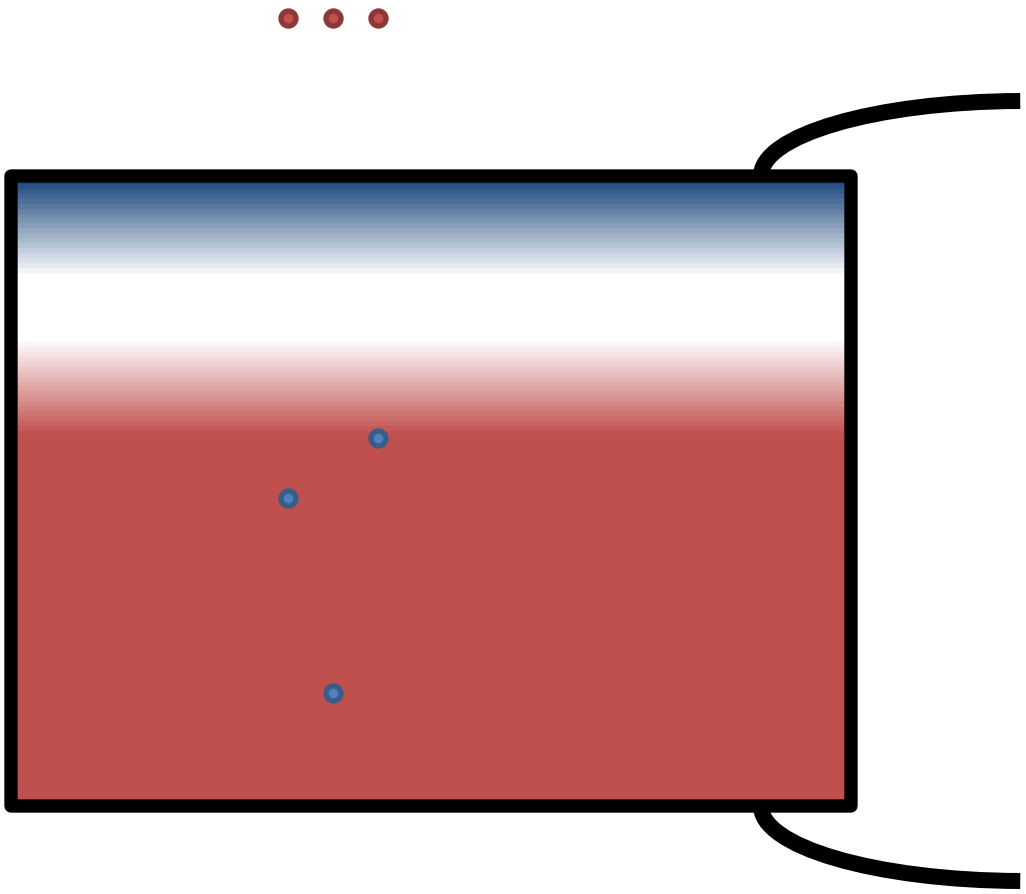
Absorption PDF of light at λ = 850 nm



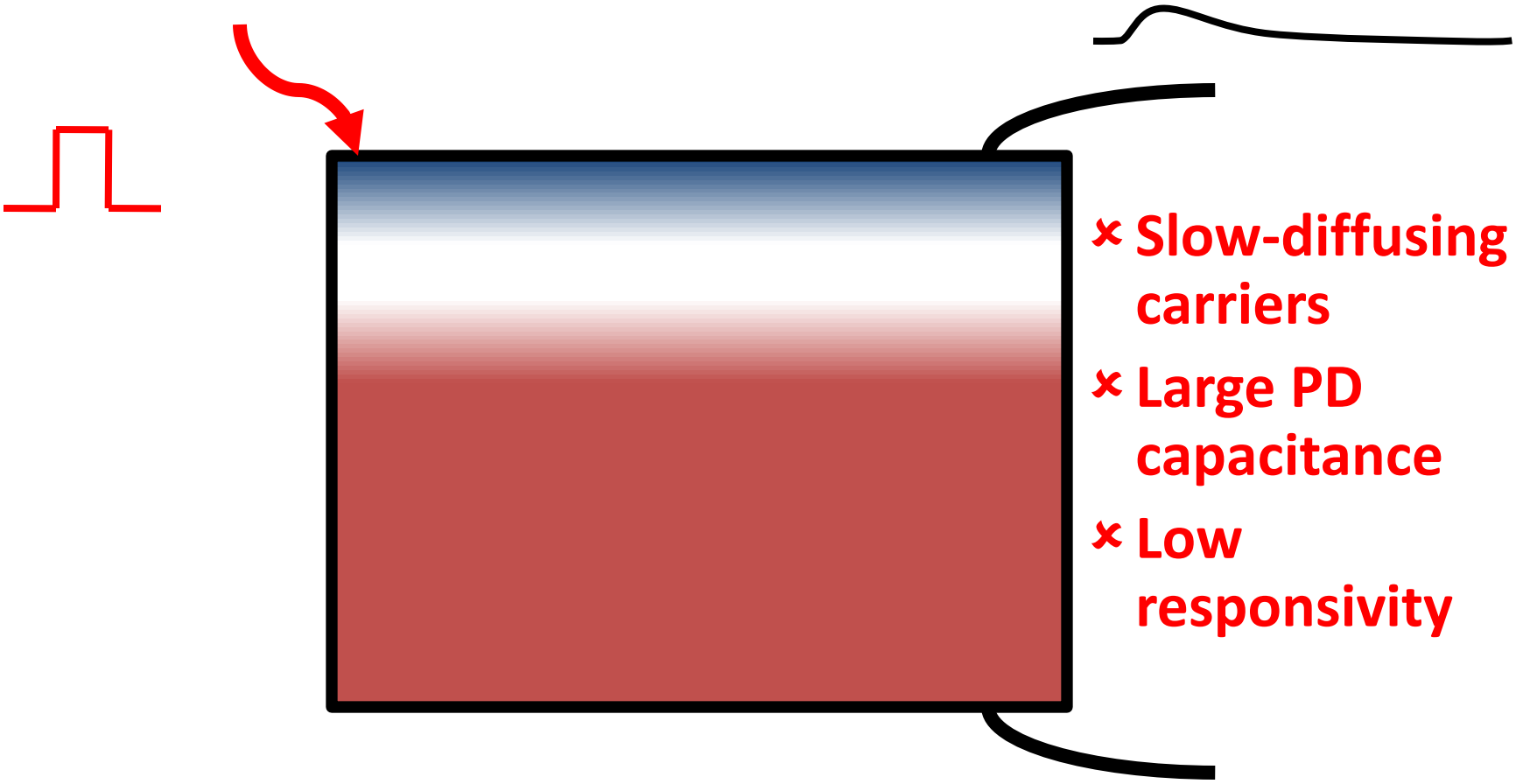
CMOS Photodetectors



Recombination



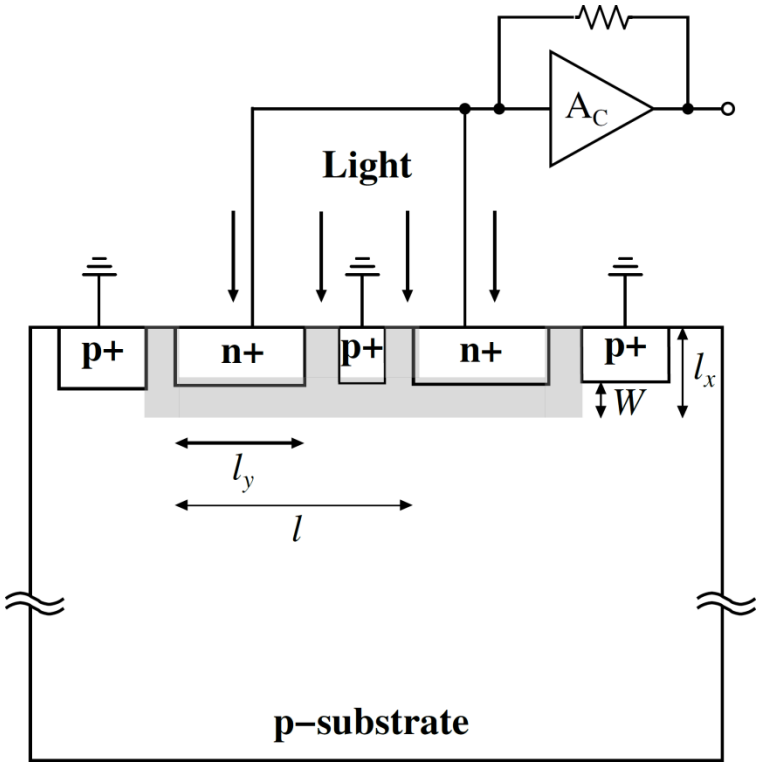
CMOS Photodetectors



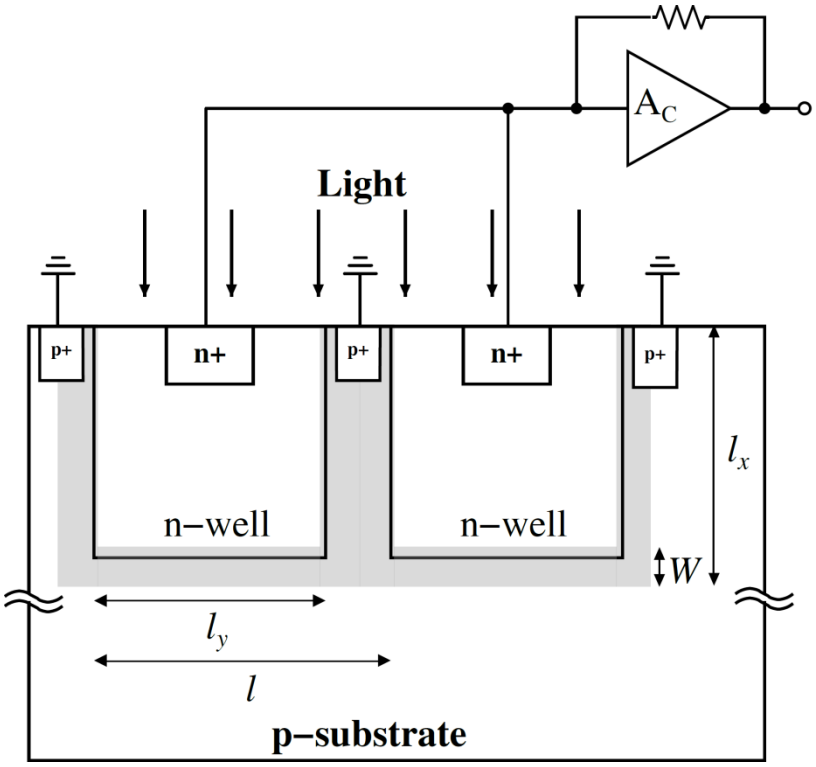
- Slow-diffusing carriers
- Large PD capacitance
- Low responsivity

CMOS Photodetector Examples

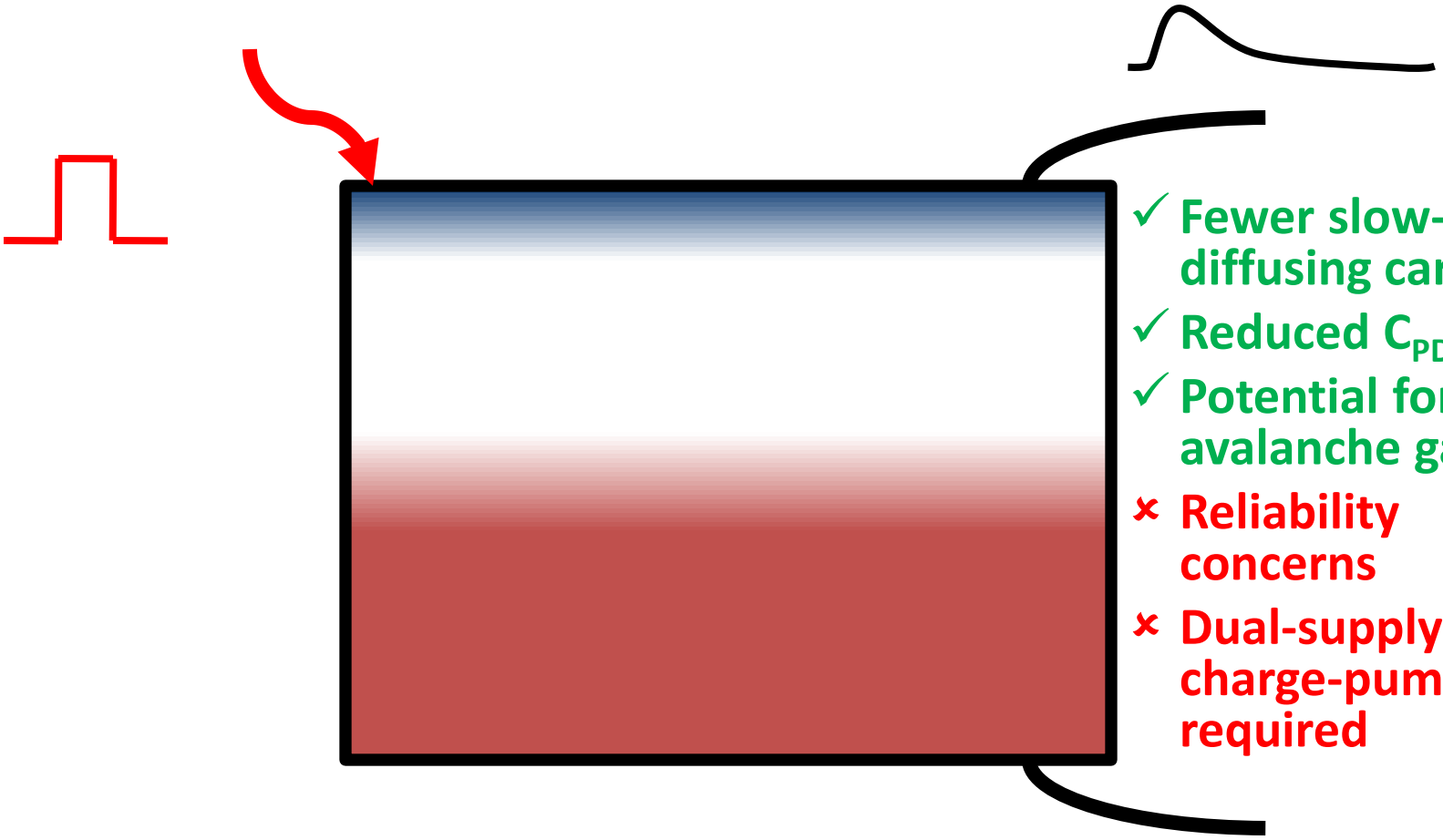
n+/p



n-well/p



High Reverse Bias

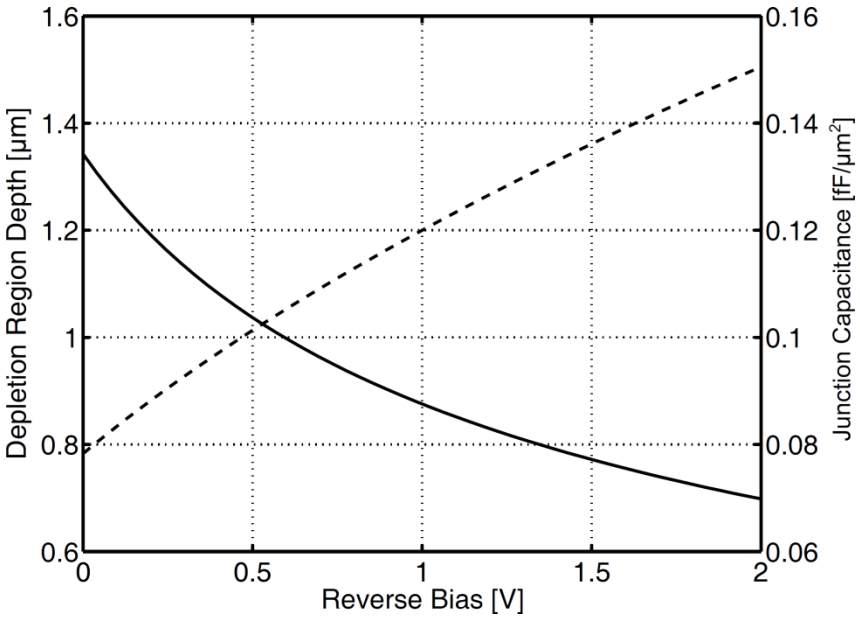


- ✓ Fewer slow-diffusing carriers
- ✓ Reduced C_{PD}
- ✓ Potential for avalanche gain
- × Reliability concerns
- × Dual-supply or charge-pump required

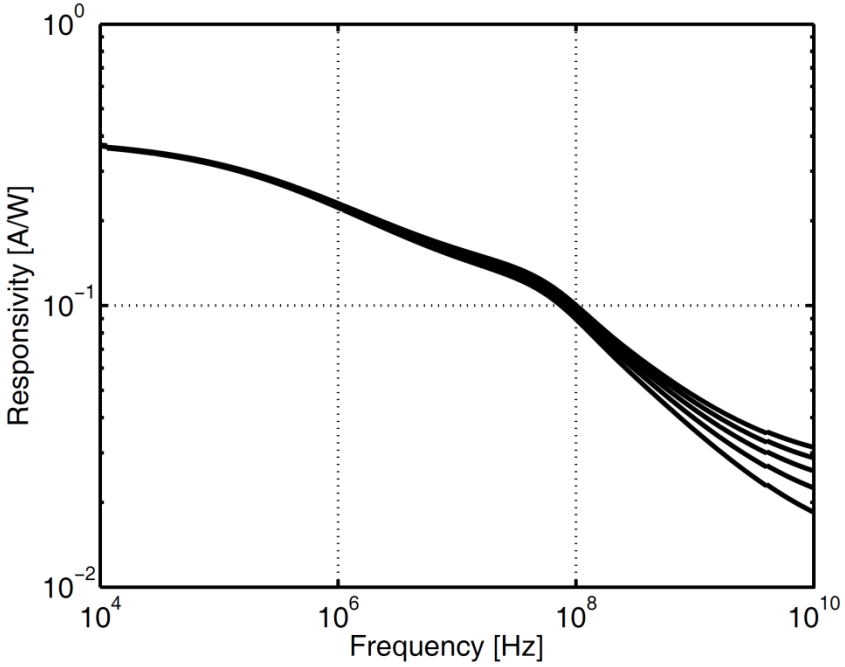
e.g. 14.2-V reverse bias in S.-H. Huang & W.-Z. Chen, "A 10-Gbps CMOS single chip optical receiver with 2-D meshed spatially-modulated light detector," *CICC*, Sept. 2009

Impact of Reverse Bias Voltage

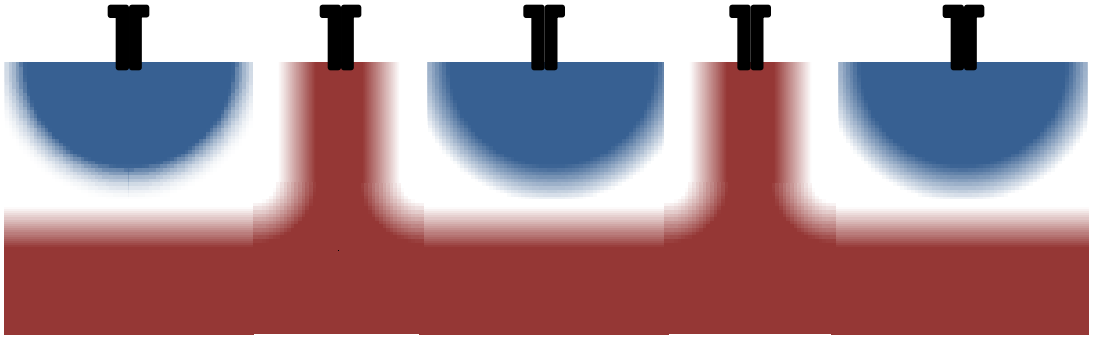
Junction capacitance



Intrinsic frequency response



Layout Considerations



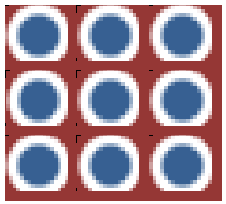
Few/Wider strips:

- ✓ Less contact metal blocking light
- ✓ Smaller C_{PD}

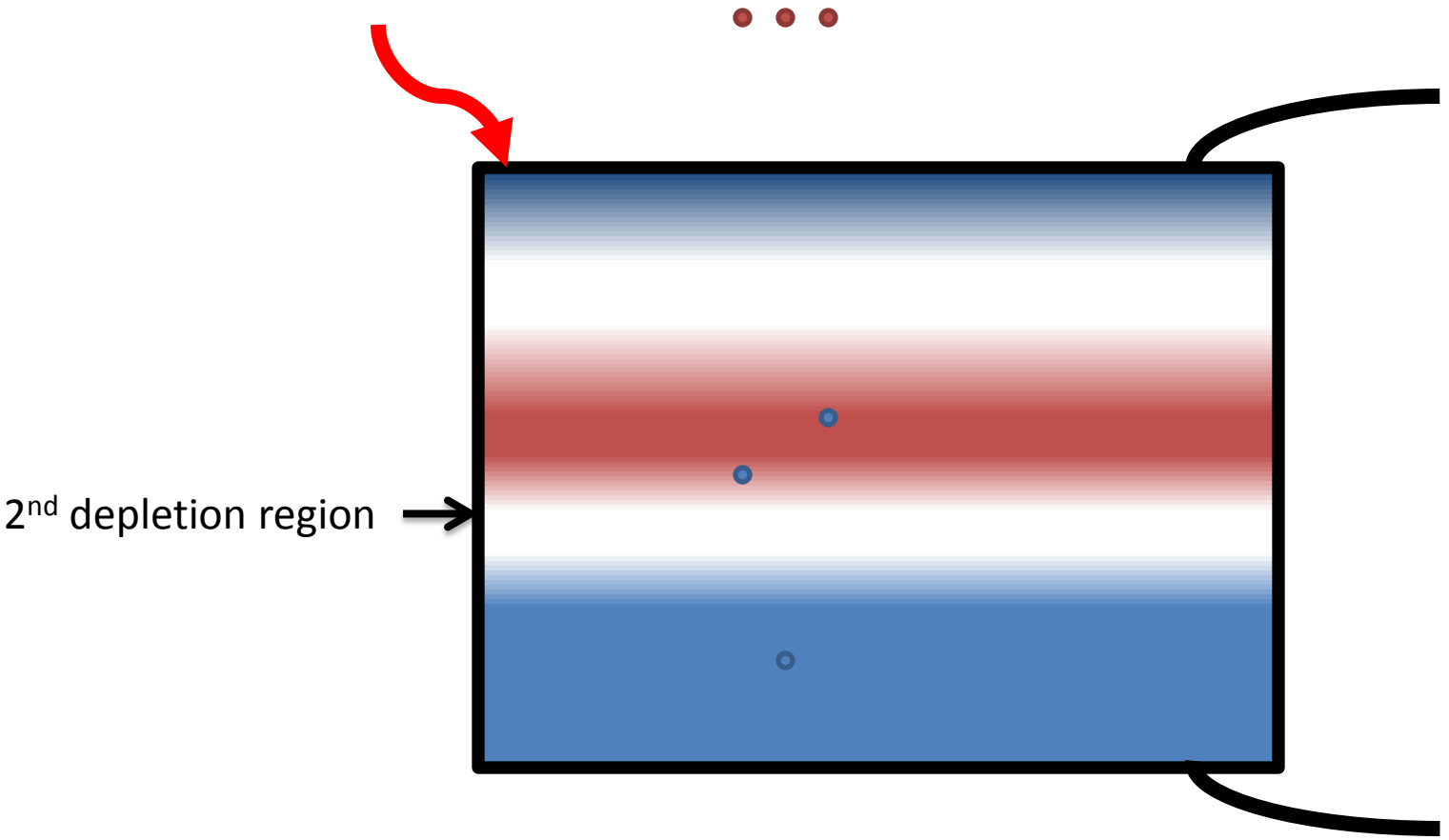
More/Smaller strips:

- ✓ Short diffusion times for the carriers to get to the contacts
- ✓ Additional sidewall depletion regions for light absorption

Similar tradeoffs arise between 1-D and 2-D contact arrays

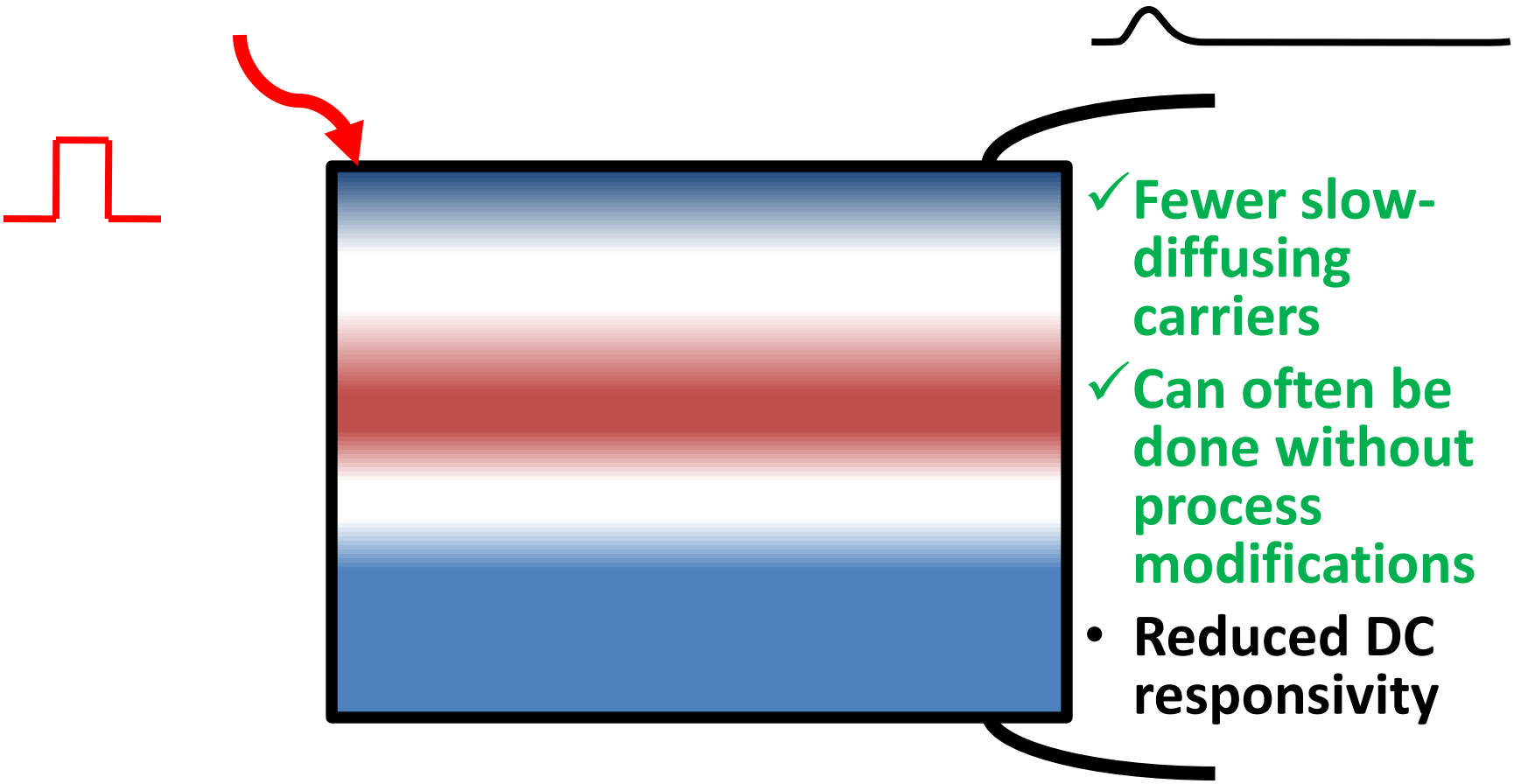


Diffusion-Shielded Photodetectors



Similar effect provided by SOI

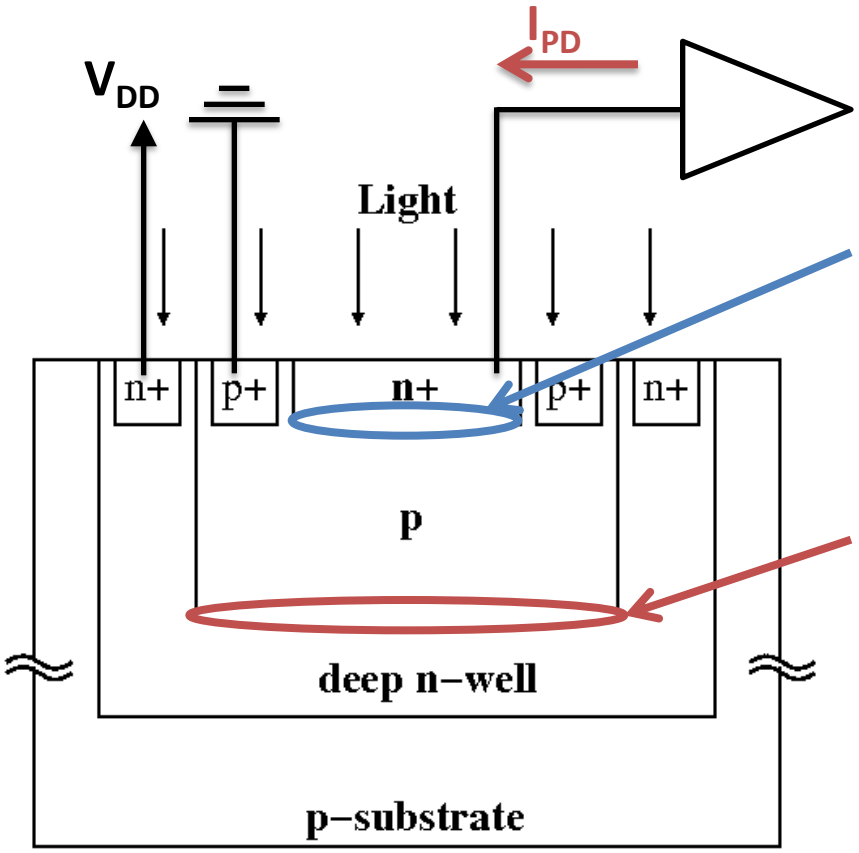
Diffusion-Shielded Photodetectors



- ✓ Fewer slow-diffusing carriers
- ✓ Can often be done without process modifications
- Reduced DC responsivity

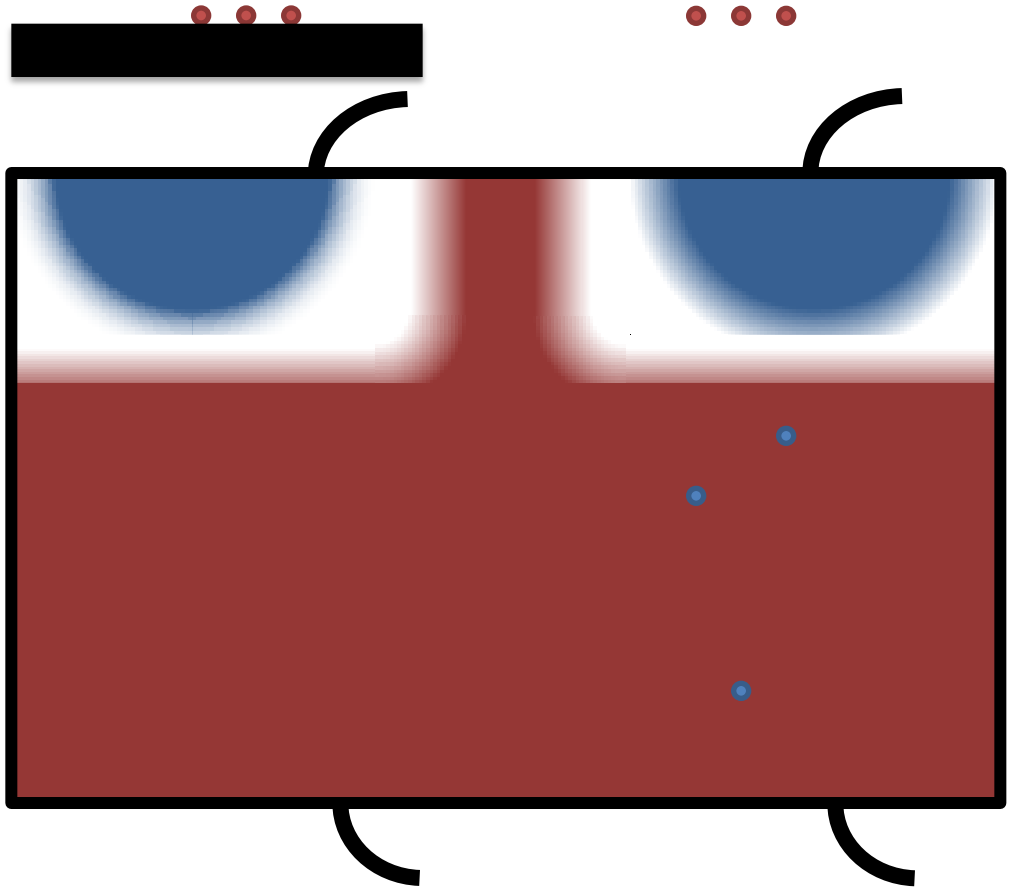
P. J. Lim et al, “A 3.3-V monolithic photodetector/CMOS preamplifier for 531 Mb/s optical data link applications,” *ISSCC* 1993
T.K. Woodward & A.V. Krishnamoorthy, "1 Gbit/s CMOS photoreceiver with integrated detector operating at 850 nm," *Electronics Letters*, Jun 1998.

Diffusion-Shielded Photodetector Example

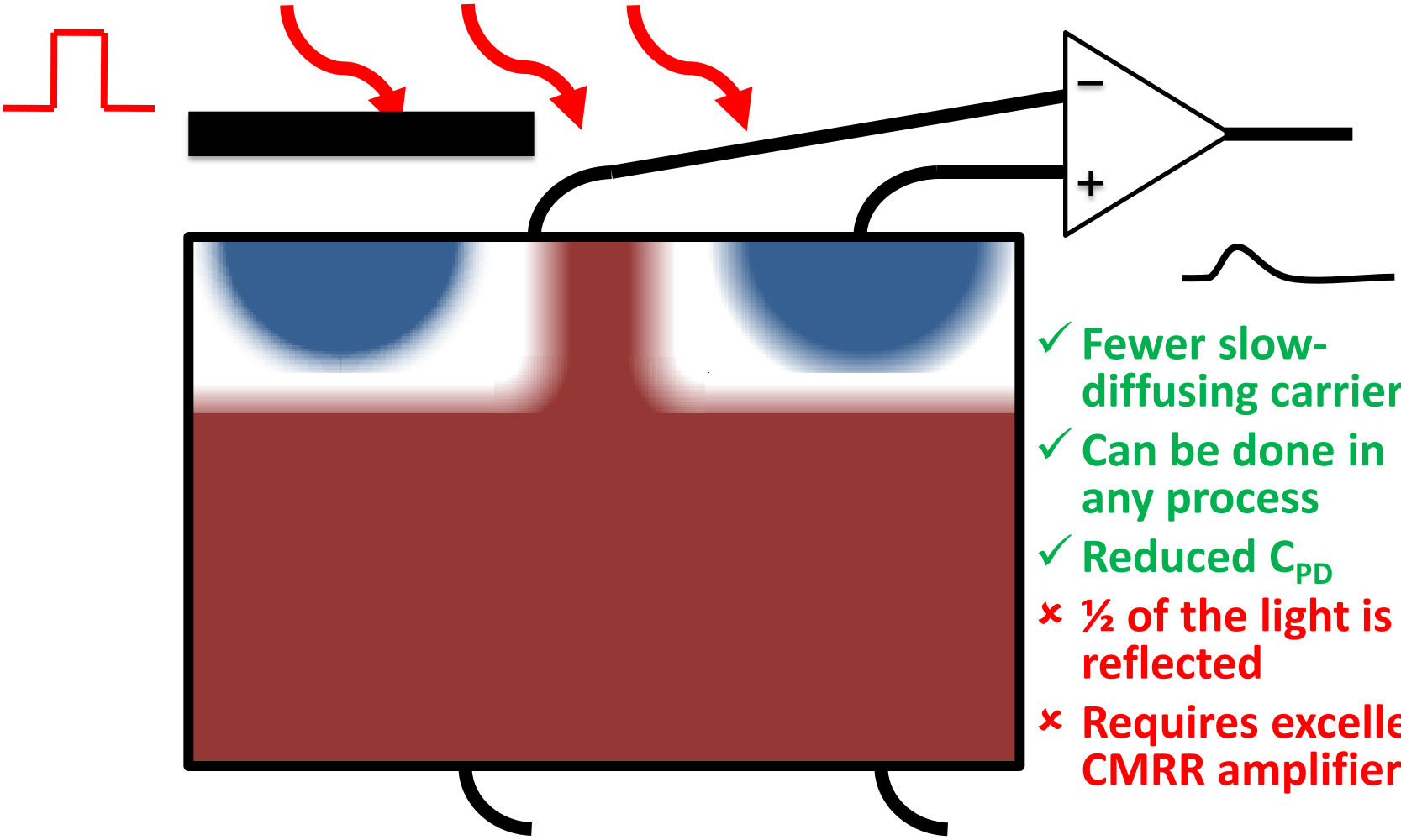


- n+/p junction is reverse-biased and used as the active photodetector
- p/n-well junction is reverse biased to collect and discard photocarriers generated far below the n+/p junction

Spatially Modulated Photodetectors



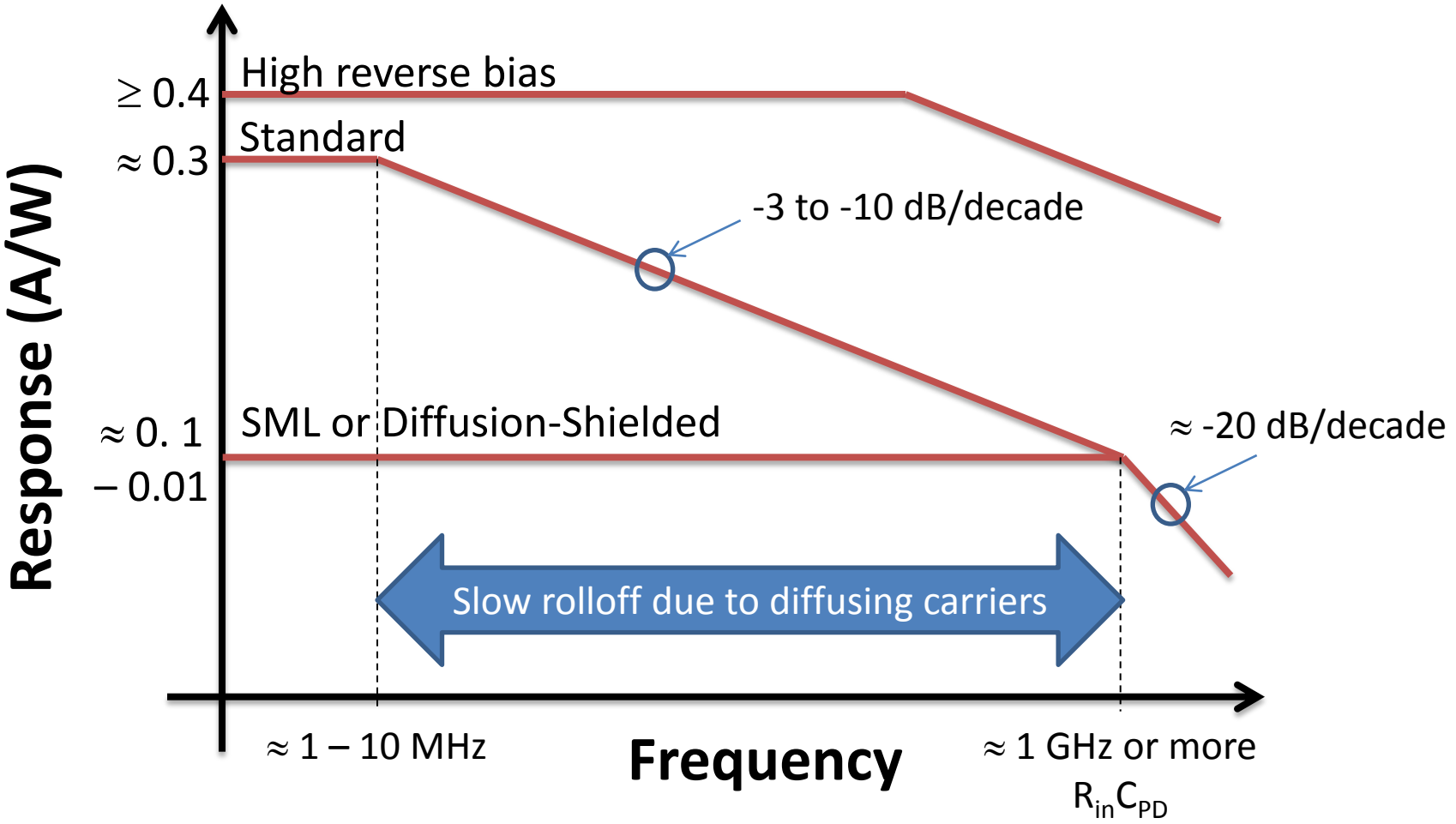
Spatially Modulated Photodetectors



- ✓ Fewer slow-diffusing carriers
- ✓ Can be done in any process
- ✓ Reduced C_{PD}
- × ½ of the light is reflected
- × Requires excellent CMRR amplifiers

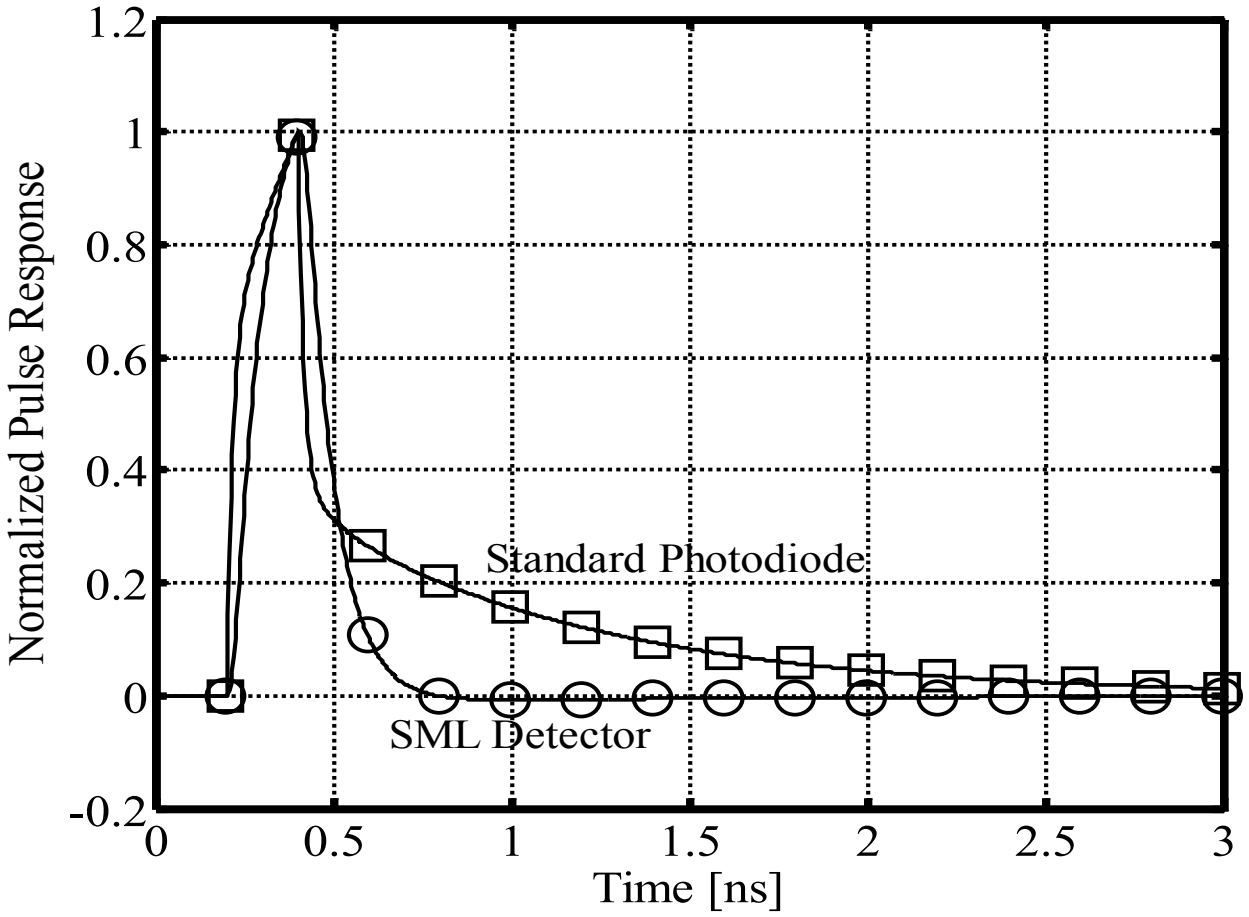
Kuijk et al, "Spatially modulated light detector in CMOS with sense-amplifier receiver operating at 180 Mb/s for optical data link applications and parallel optical interconnects between chips," *IEEE J. Sel. Top. Quant. Elec.*, Nov/Dec 1998.

Typical CMOS PD Frequency Responses



Representative of photodiodes in 0.18 μm CMOS process with light at λ = 850 nm

Typical CMOS PD Pulse Responses



Representative of photodiodes in 0.18 μm CMOS process with light at λ = 850 nm at 5 Gbps

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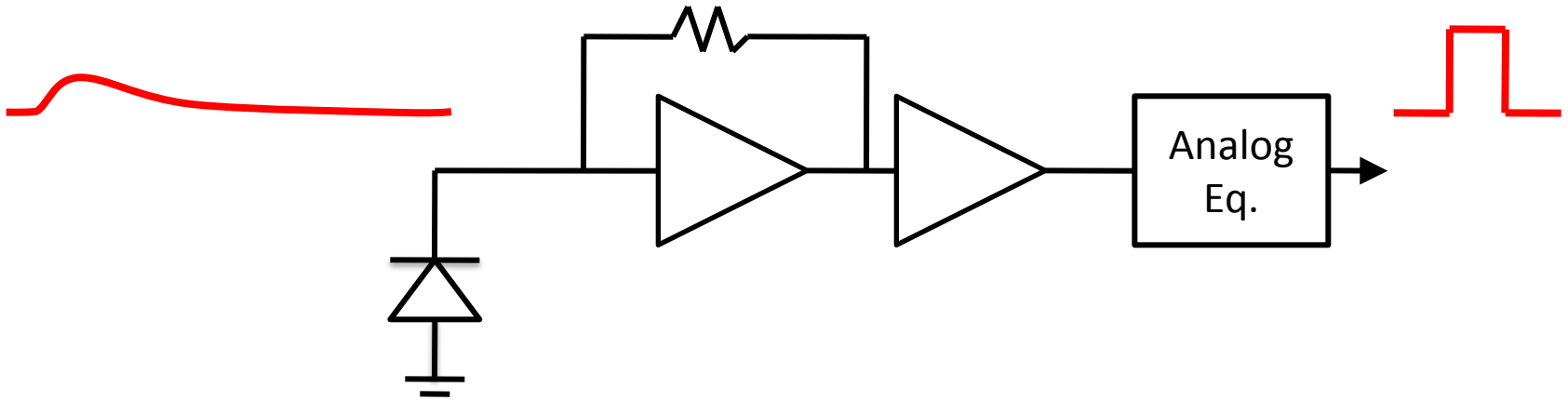
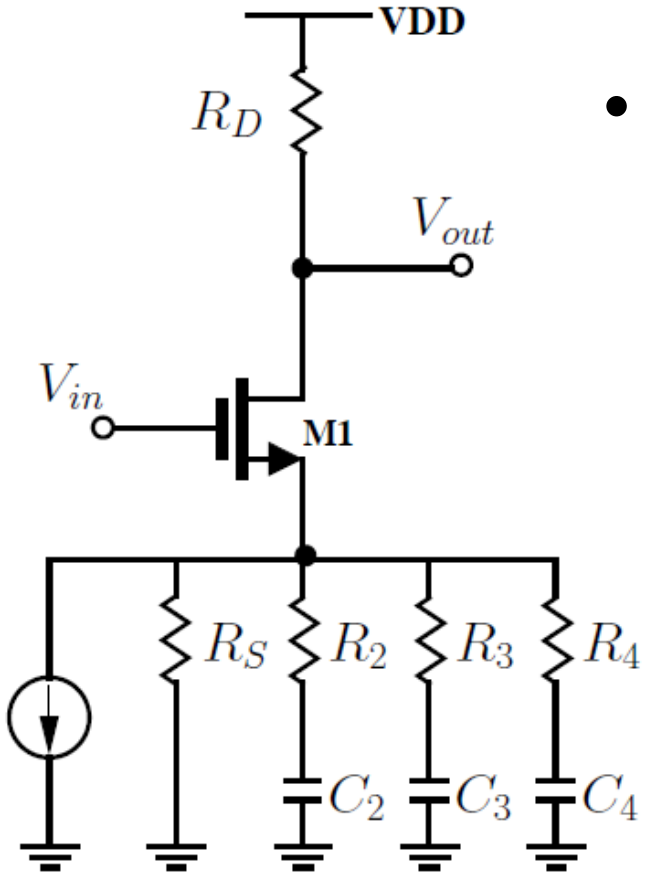
Equalization of the Pulse Response



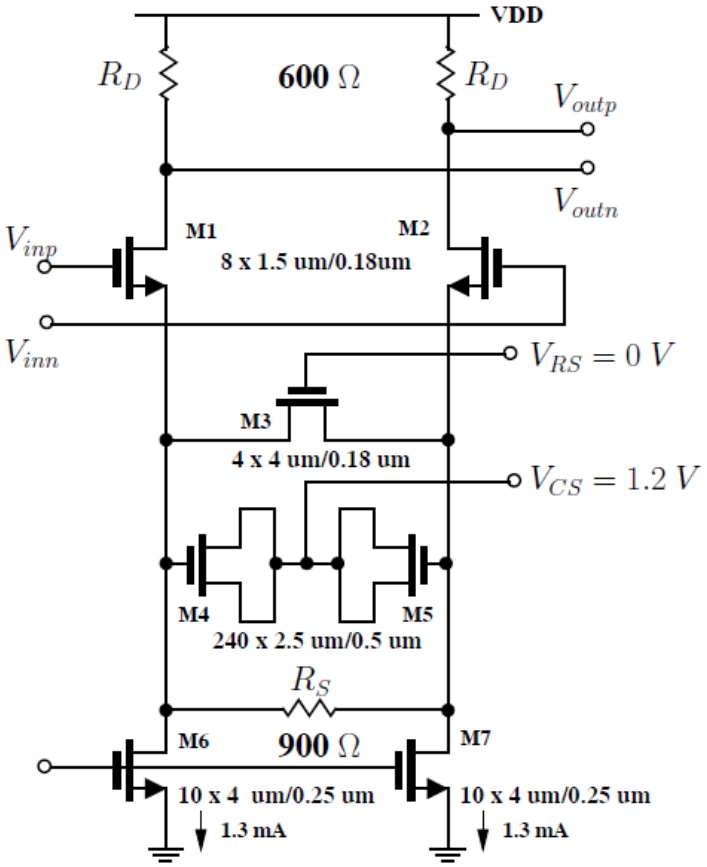
Analog Equalization



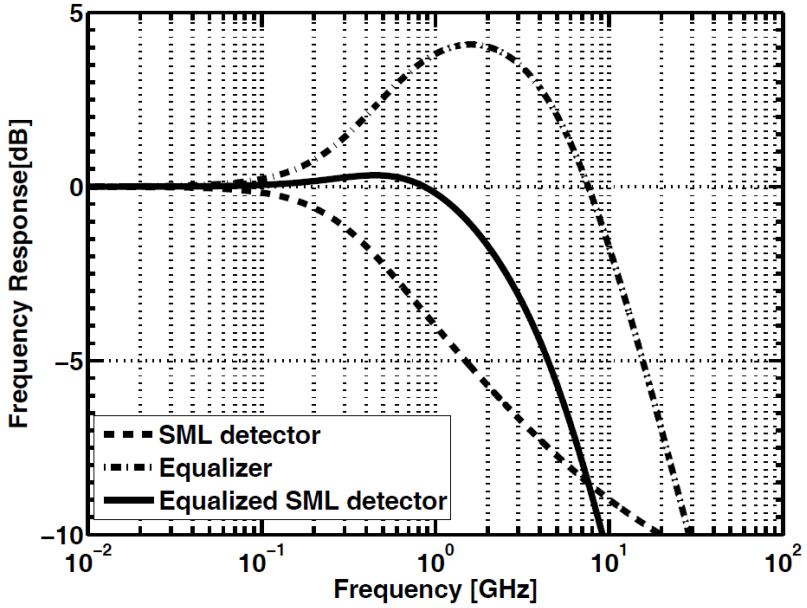
- High-order transfer function is required to equalize the ≈ 5 dB/decade slope

Radovanovic, Annema, Nauta, "A 3-Gb/s optical detector in standard CMOS for 850-nm optical communication," *JSSC*, Aug. 2005.

SML + Analog Equalization

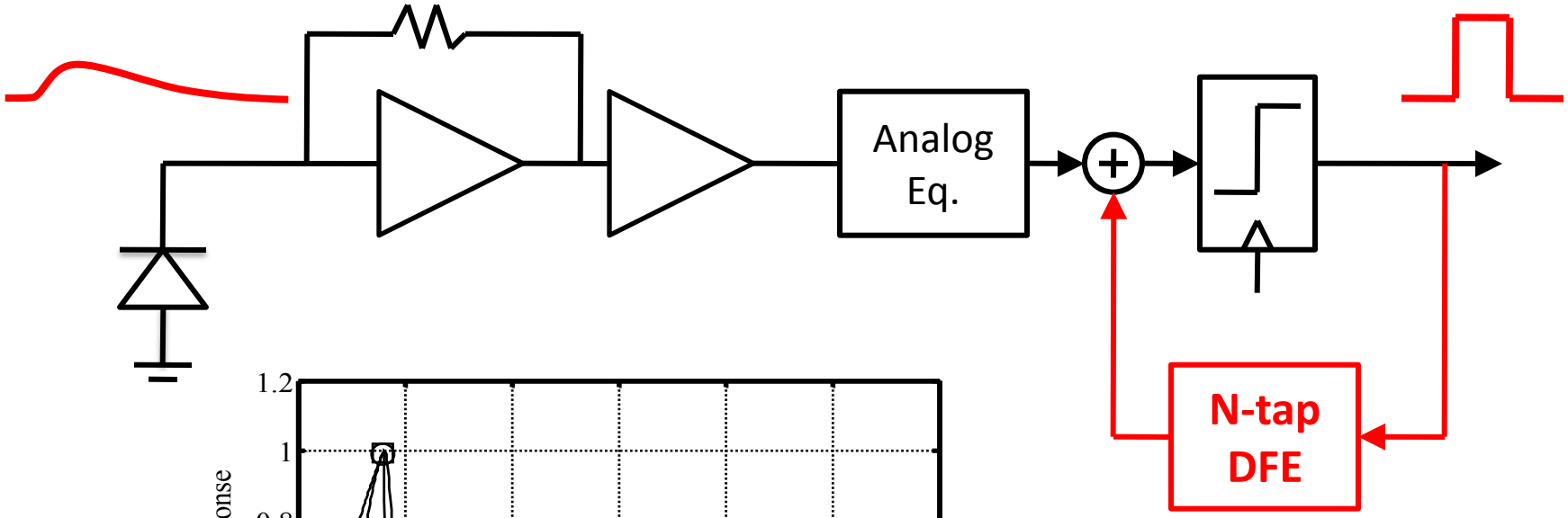


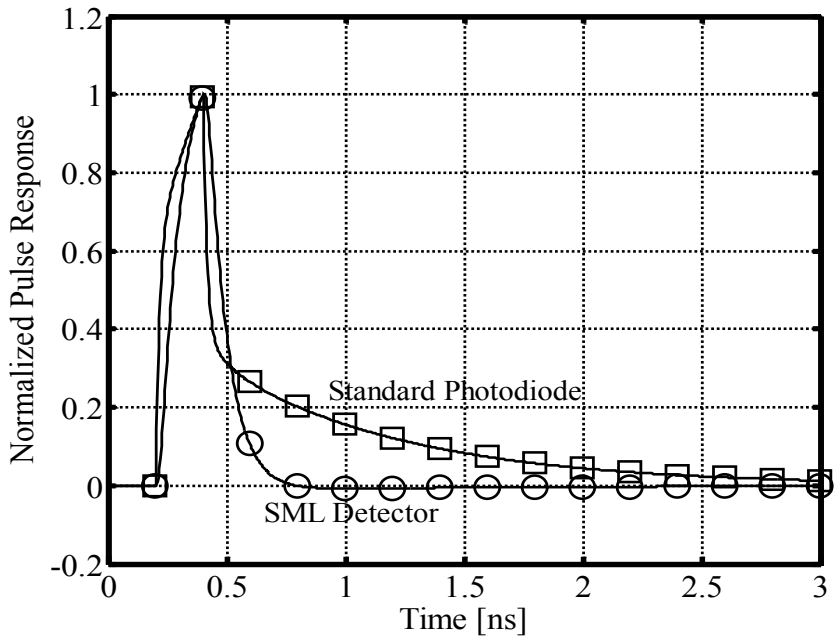
When combined with a SML detector, a first-order equalizer may suffice [Hermans, ESSCirc 2006]



Kao and Chan Carusone, "A 5-Gbps Optical Receiver with Monolithically Integrated Photodetector in 0.18-um CMOS," *RFIC Symposium*, June 2009.

Equalization of the Pulse Response

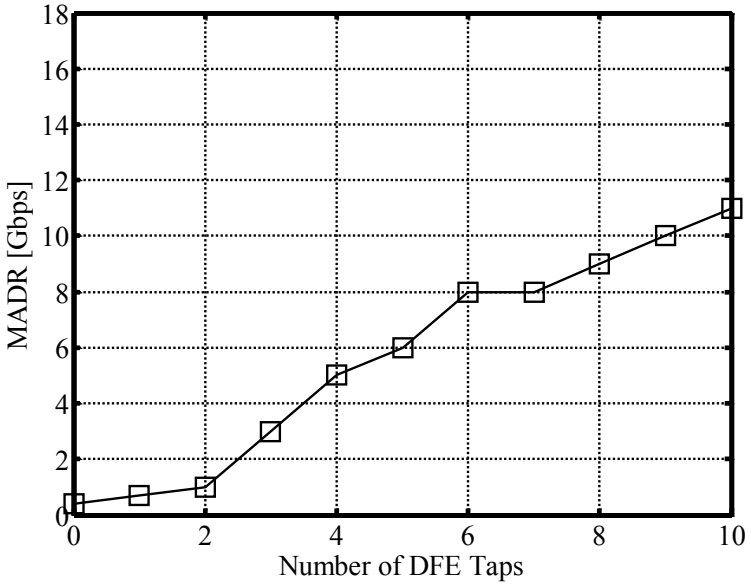




Mostly post-cursor pulse responses suggest that a DFE may be effective

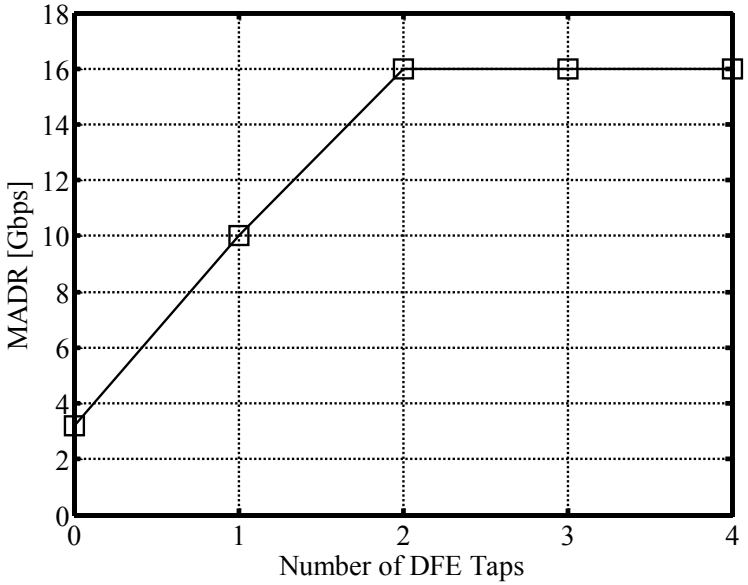
Maximum Data Rates: Analog Eq. + DFE

Standard Photodetector



- Many DFE taps are required to accurately cancel the distant post-cursor ISI

SML Photodetector



- High-gain low-noise TIA is required due to the reduced responsivity of an SML detector

High-Speed CMOS Photodetector Summary

- Slowly-diffusing carriers
  - Maximize depletion regions via layout
    $\Rightarrow$ increases capacitance
  - Maximize depletion regions via large reverse bias
    $\Rightarrow$ need for dual-supplies or charge pump, reliability concerns
  - Shield diffusing carriers
  - Signal processing techniques:
    - SML $\Rightarrow$ decreases responsivity
    - equalization
- Low responsivity
  - Low-noise/high-sensitivity TIA
- High capacitance
  - Low input-resistance TIA

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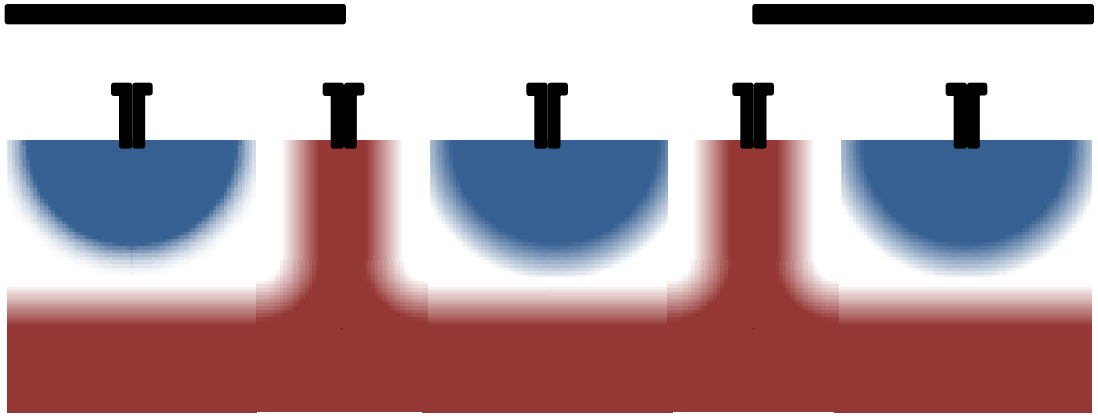
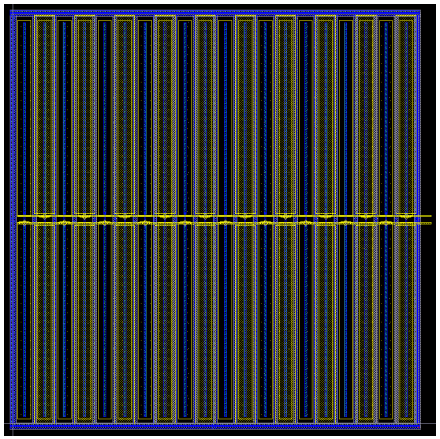
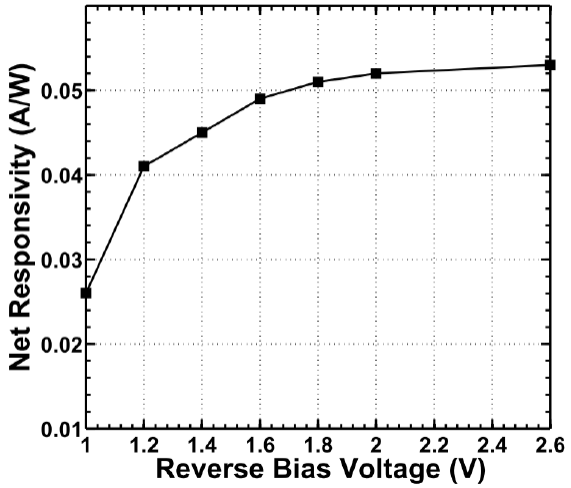
SML Photodetector Example

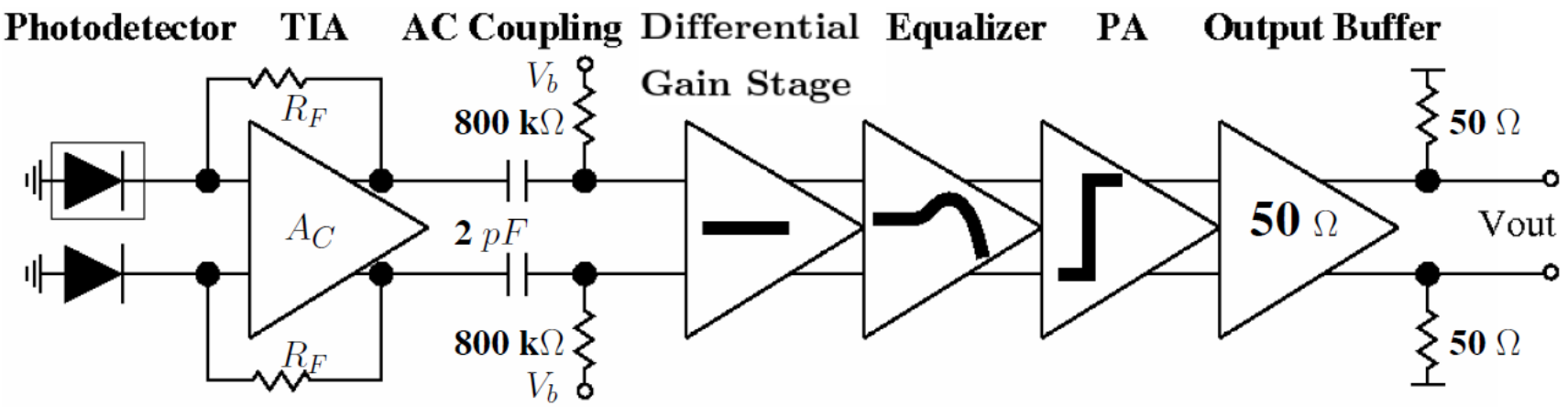






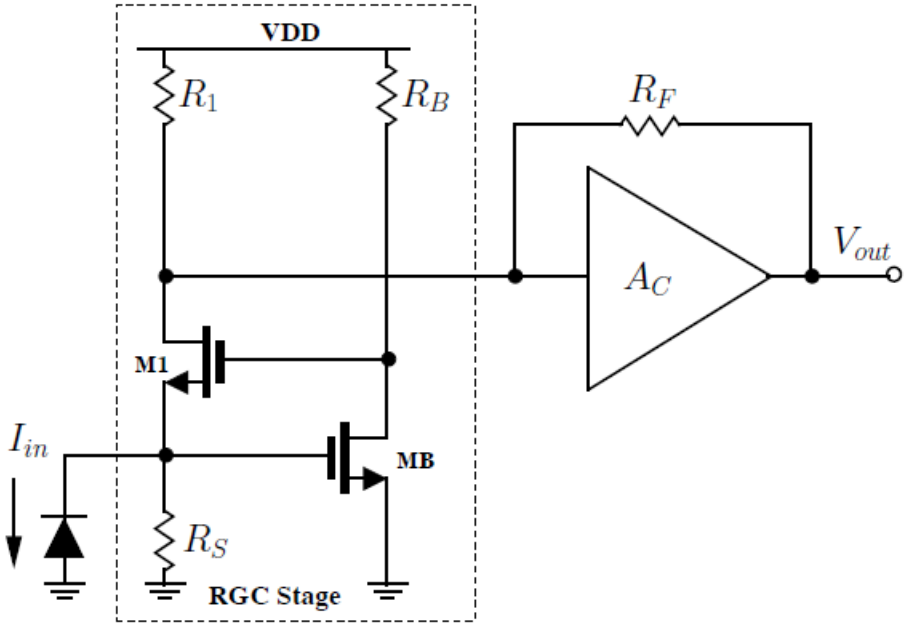
- 0.18 μm bulk CMOS process
- M1 is used for contacts, M2 is used to block light
- Junction side-walls also collect photons
- 20 strips (10 light + 10 dark) across a 75um x 75um area

System Design



- Responsivity, R = 0.03 A/W & Input optical power of -5 dBm ⇒ **Photodiode current, I_{PD} = 9 μA**
- BER = 10^{-12} ⇒ **TIA input-referred noise of 0.65 μA_{rms}**
- TIA output of 50 mV makes noise performance of subsequent stages non-critical ⇒ **R_F = 5.6 kΩ**
- Similar architecture reported in:
  - C. Hermans et al, "A Gigabit optical receiver with monolithically integrated photodiode in 0.18-μm CMOS," *ESSCIRC*, Sept. 2006.
  - Chen et al, "A 3.125 Gbps CMOS Fully Integrated Optical Receiver with Adaptive Analog Equalizer," *ASSCC*, Nov. 2007.
  - Tavernier & Steyaert, "High-Speed Optical Receivers With Integrated Photodiode in 130 nm CMOS," *JSSC*, Oct. 2009.
  - Lee et al, "An 8.5Gb/s CMOS OEIC with on-chip photodiode for short-distance optical communications," *ISSCC*, Feb. 2010.

Regulated Cascode Input?

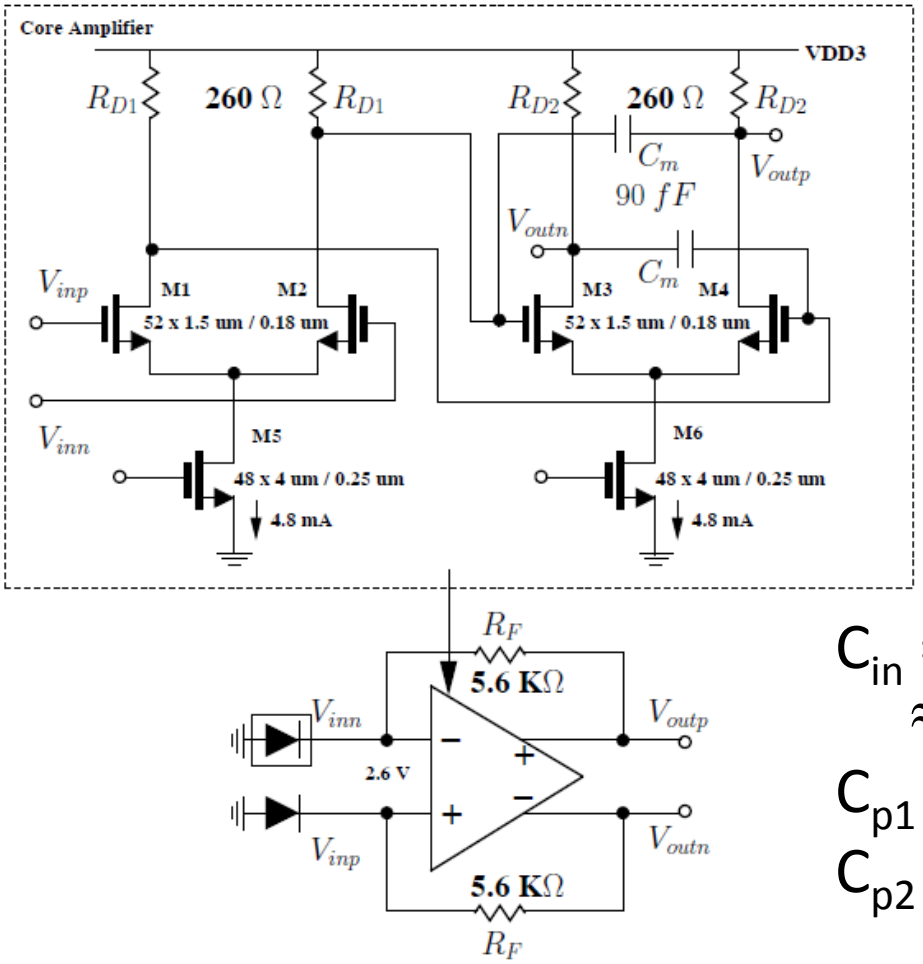


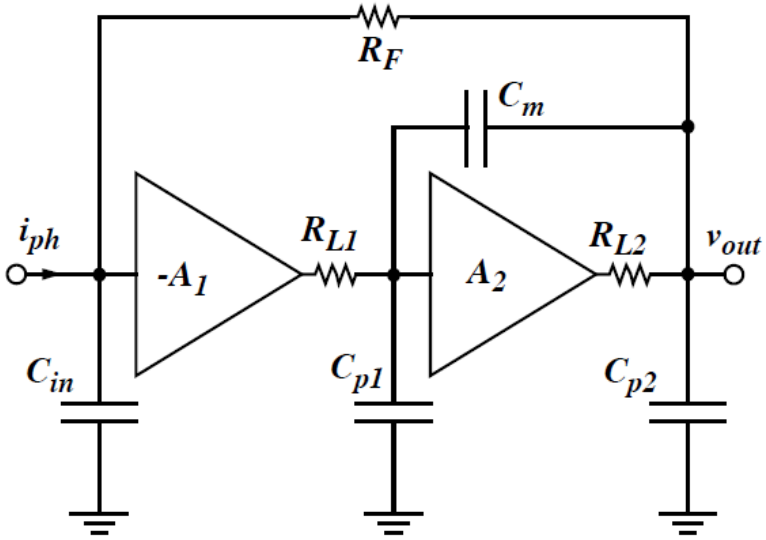
- Low responsivity SML detector
- High system bandwidth (5-Gbps)

➢ Very low input-referred noise required

➢ **No regulated cascode at the input**

Transimpedance Amplifier





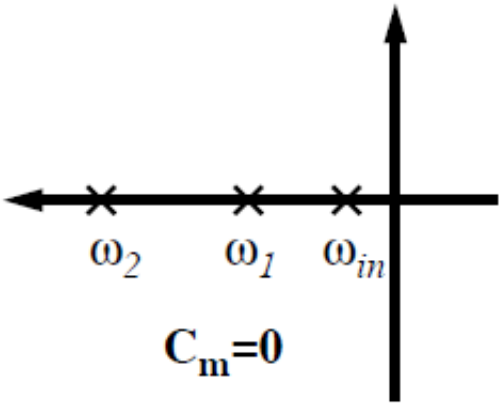
$C_{in} = C_{PD} + C_{A1}$
≈ 500 fF + 500 fF = 1 pF

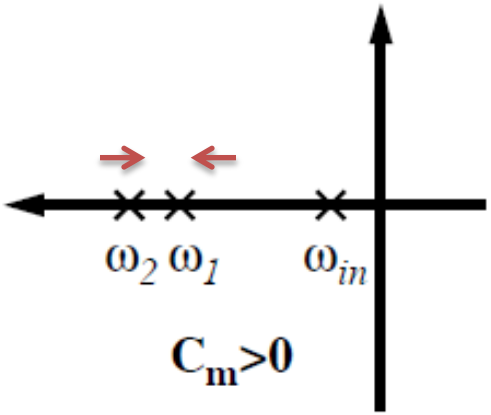
$C_{p1} \approx 680$ fF

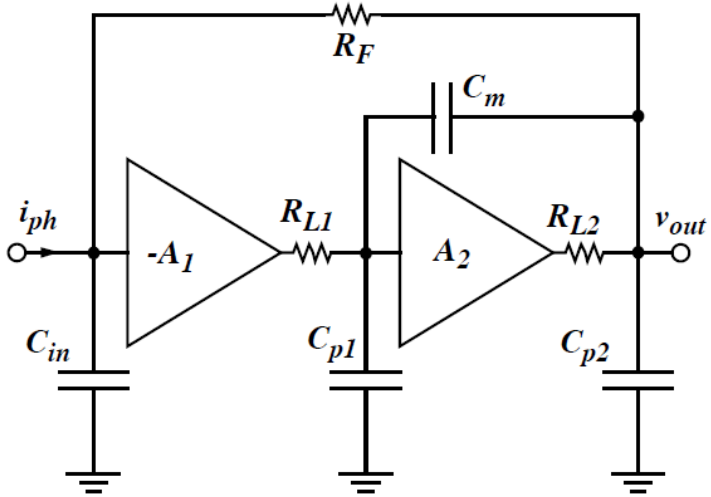
$C_{p2} \approx 100$ fF

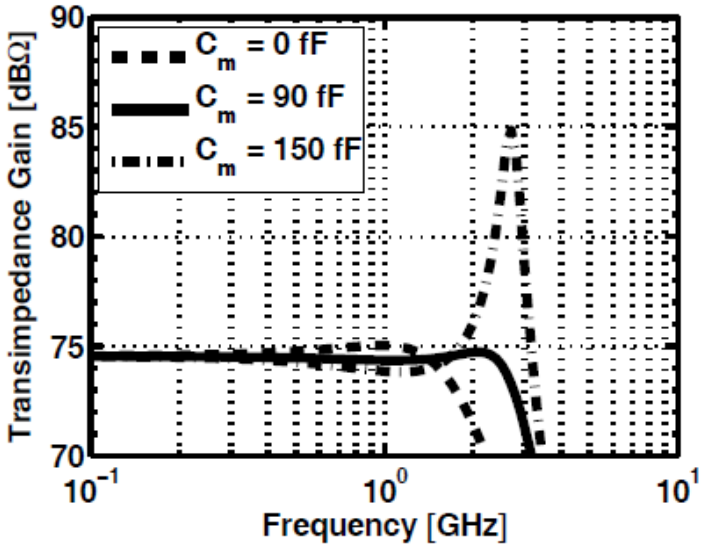
Notice $V_{PD,dc} \approx V_{DD} - 625$ mV

Transimpedance Amplifier

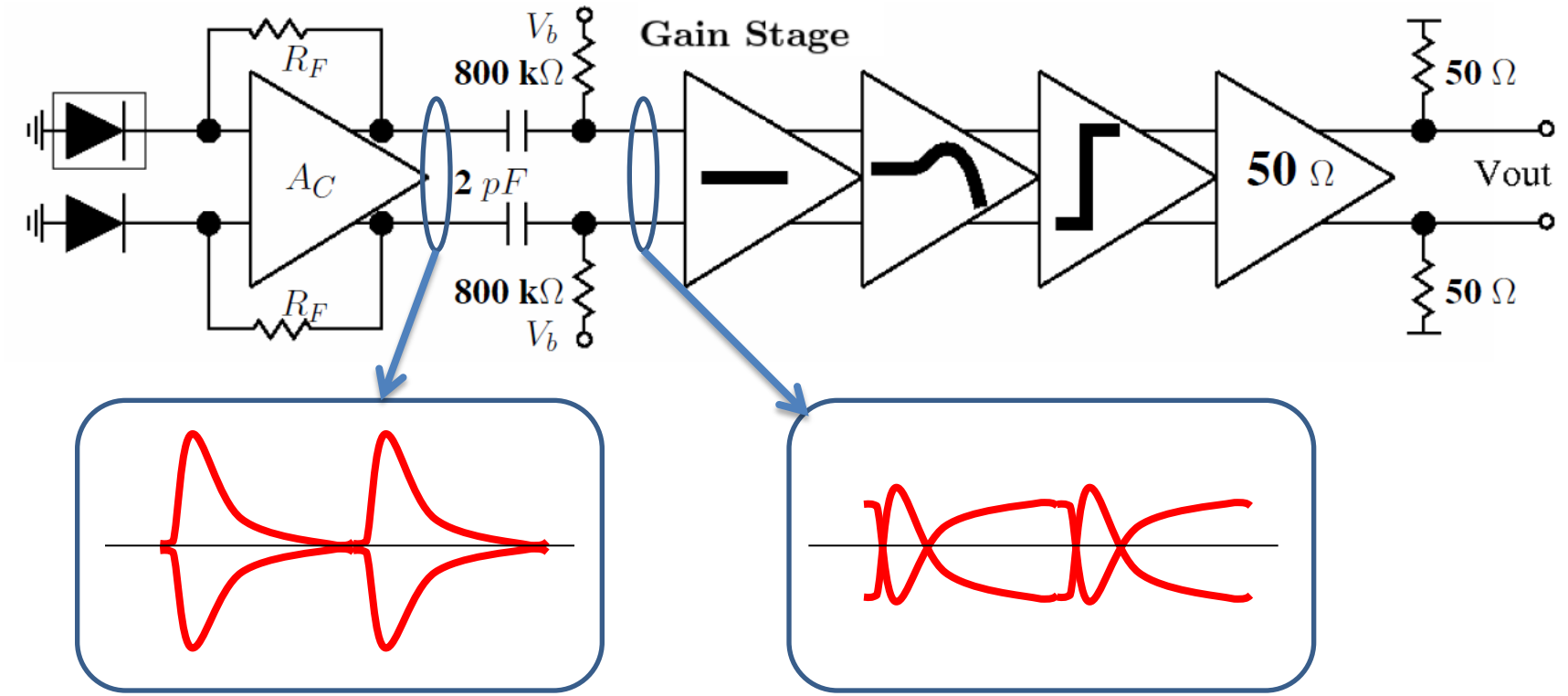








AC Coupling

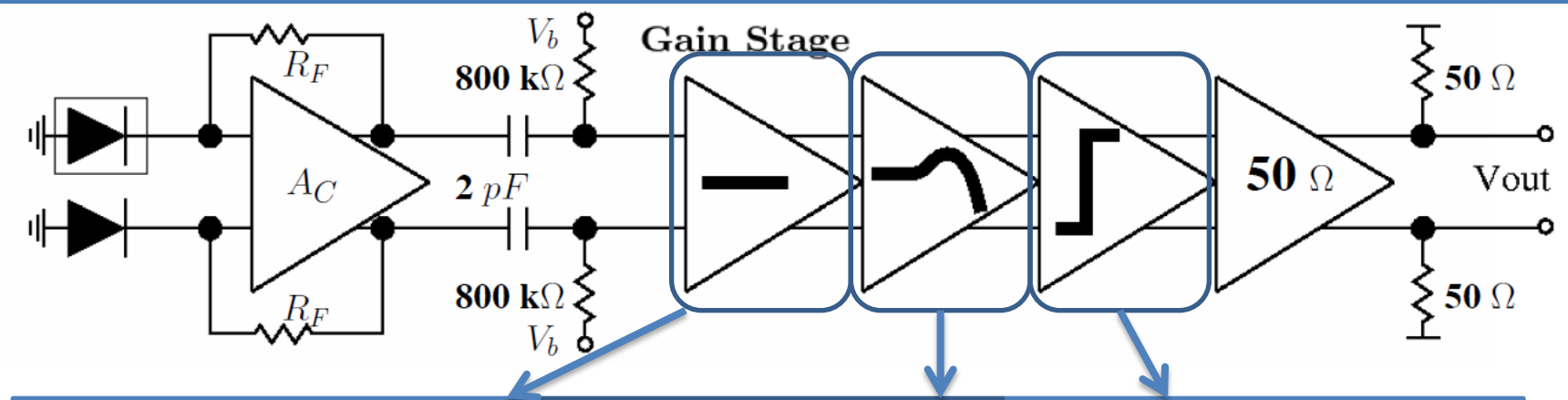


- Converts single-ended signal to fully-differential
- Facilitates the operation of the TIA from a higher supply voltage

$\Rightarrow$ Higher reverse bias applied across the photodetector

$\Rightarrow$ Increased responsivity approximately 60%

Equalization + Limiting Amplifier

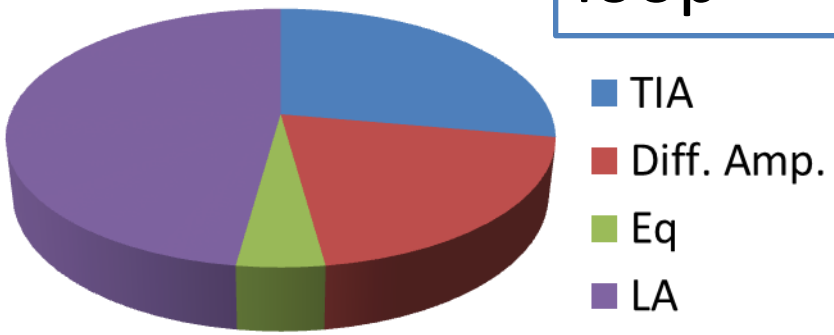


Additional differential gain required to improve CMRR

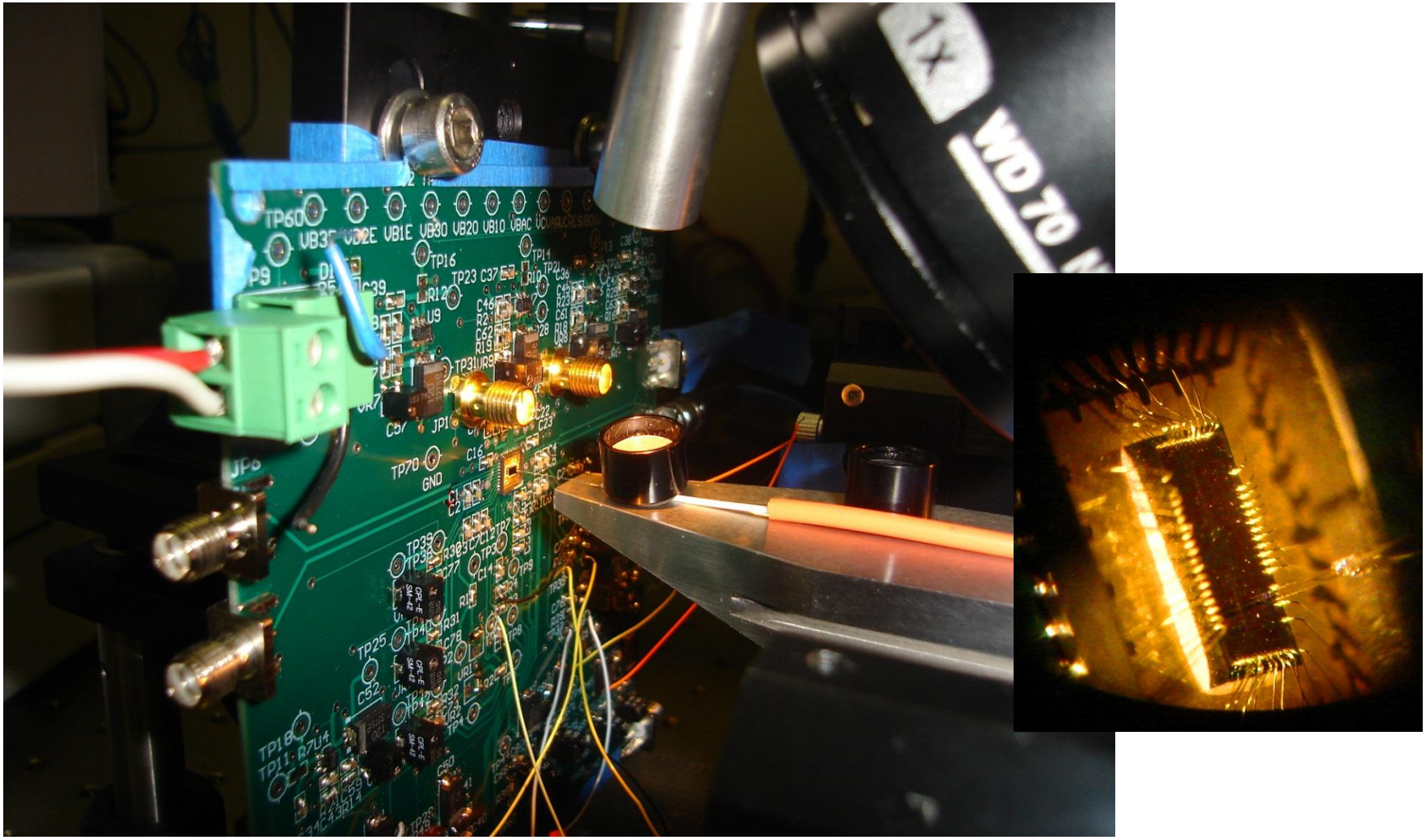
Analog Eq.

Limiting amplifier with DC offset compensation loop

Power Breakdown
(Total 115mW)



Optical Alignment in Measurements

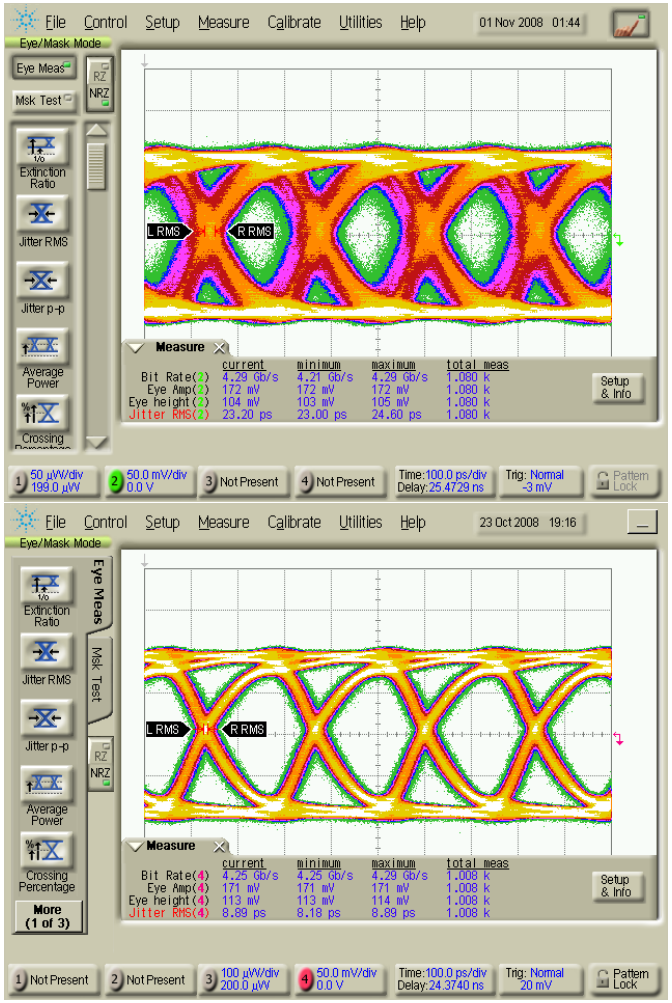


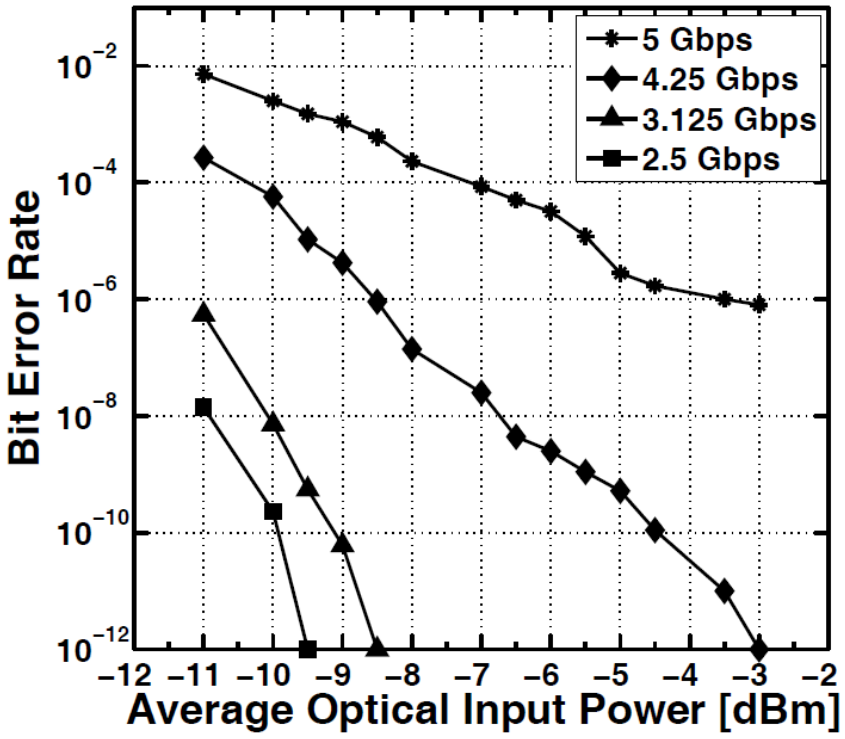
Measurement Results

At 4.25 Gbps

Without equalization

With equalization





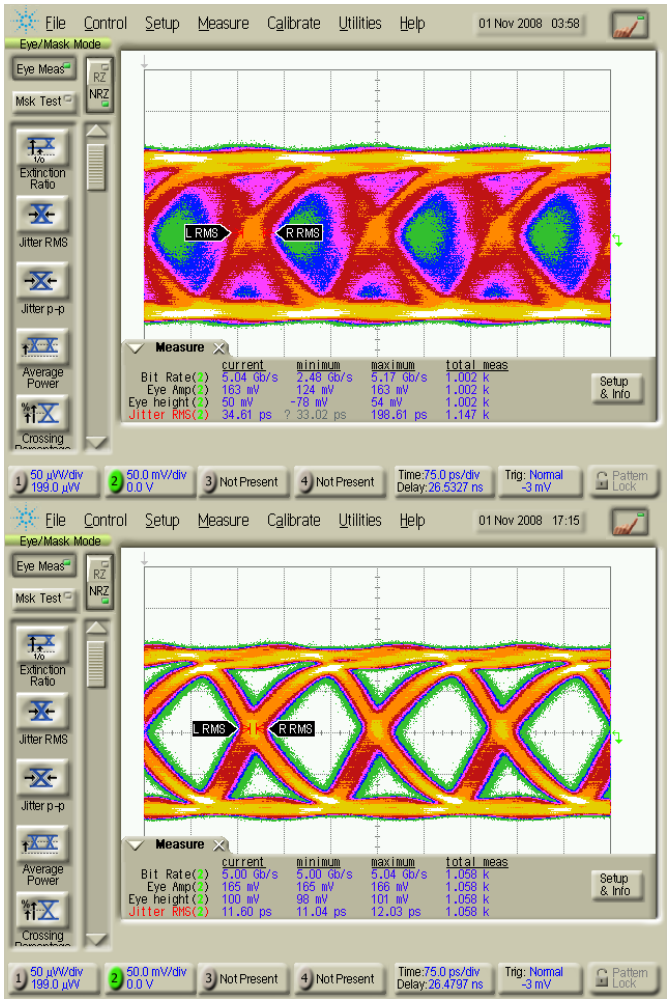
BW-limited at 5 Gbps

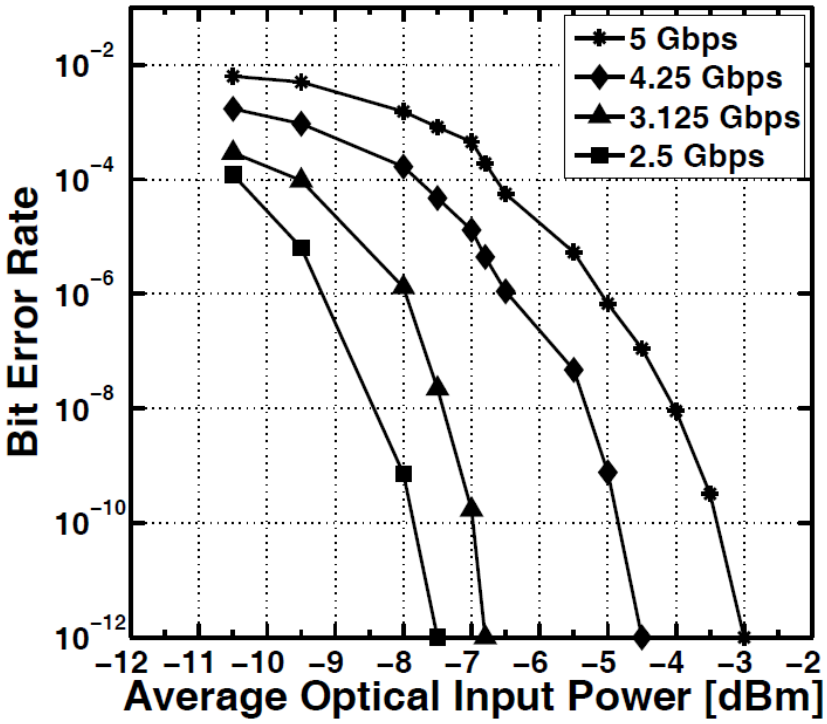
Measurement Results

At 5 Gbps

Without equalization

With equalization

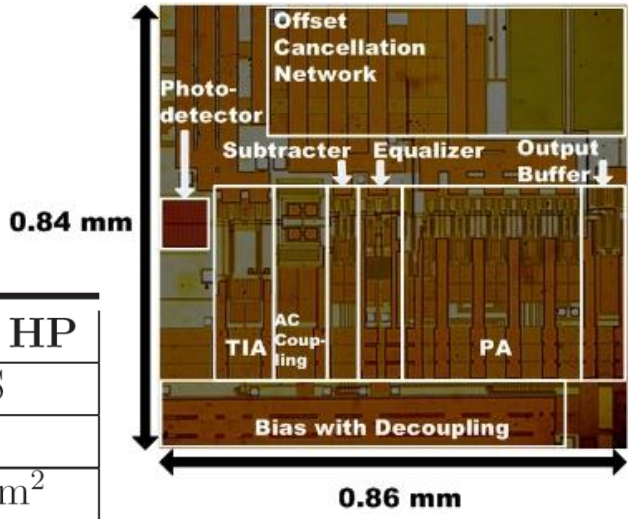




Increased current consumption in the TIA

$\Rightarrow$ **Noise limited at 5 Gbps**

Measurement Summary

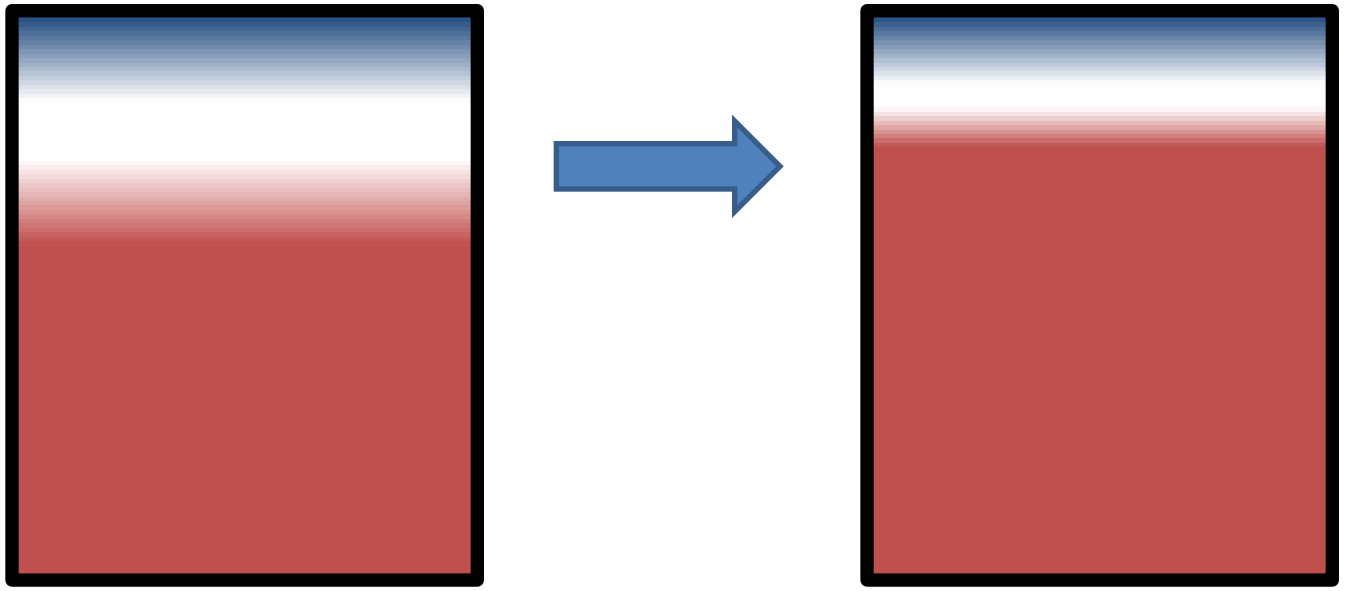


	LP	HP
Technology	0.18-μm CMOS	
Supply voltages	3.3 V, 1.8 V	
Total chip area	1.5 x 2.8 = 4.2 mm^2	
Core area of optical receiver front-end	0.86 x 0.84 = 0.72 mm^2	
Optical wavelength	850 nm	
Average input power	-3 dBm	
Highest data rate with BER less than 10^{-12}	4.25 Gbps	5 Gbps
RMS jitter	8.89 ps	11.6 ps
Total power consumption with output buffer	144 mW	183 mW
Power consumption without output buffer	129 mW	168 mW

Outline

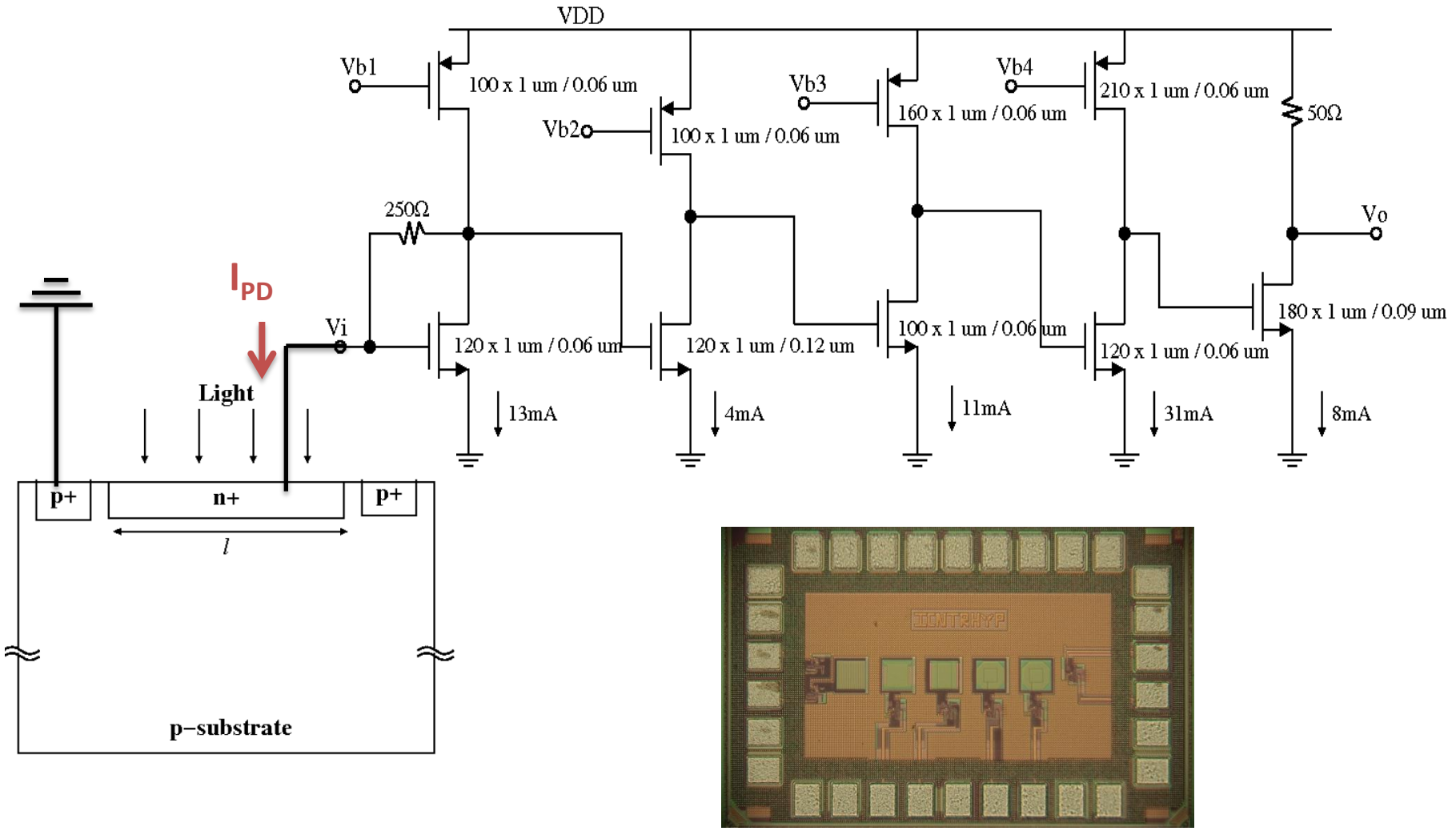
- Introduction
  - Trend towards short-reach optical
  - Trend towards highly integrated transceivers
- Tutorial on High-speed CMOS photodetection
  - Optical properties of silicon
  - Standard CMOS photodetectors
  - Diffusion-shielded photodetectors
  - Spatially modulated light detectors
- Equalization to improve CMOS photodetectors
  - Analog equalization
  - Decision-Feedback Equalization
- Case study: 0.18 μm CMOS integrated optical receiver
  - SML detector
  - Analog equalizer
- **Photodetectors in nanoscale CMOS technologies**
  - **Experimental results from a 65 nm process**

Impact of Technology Scaling

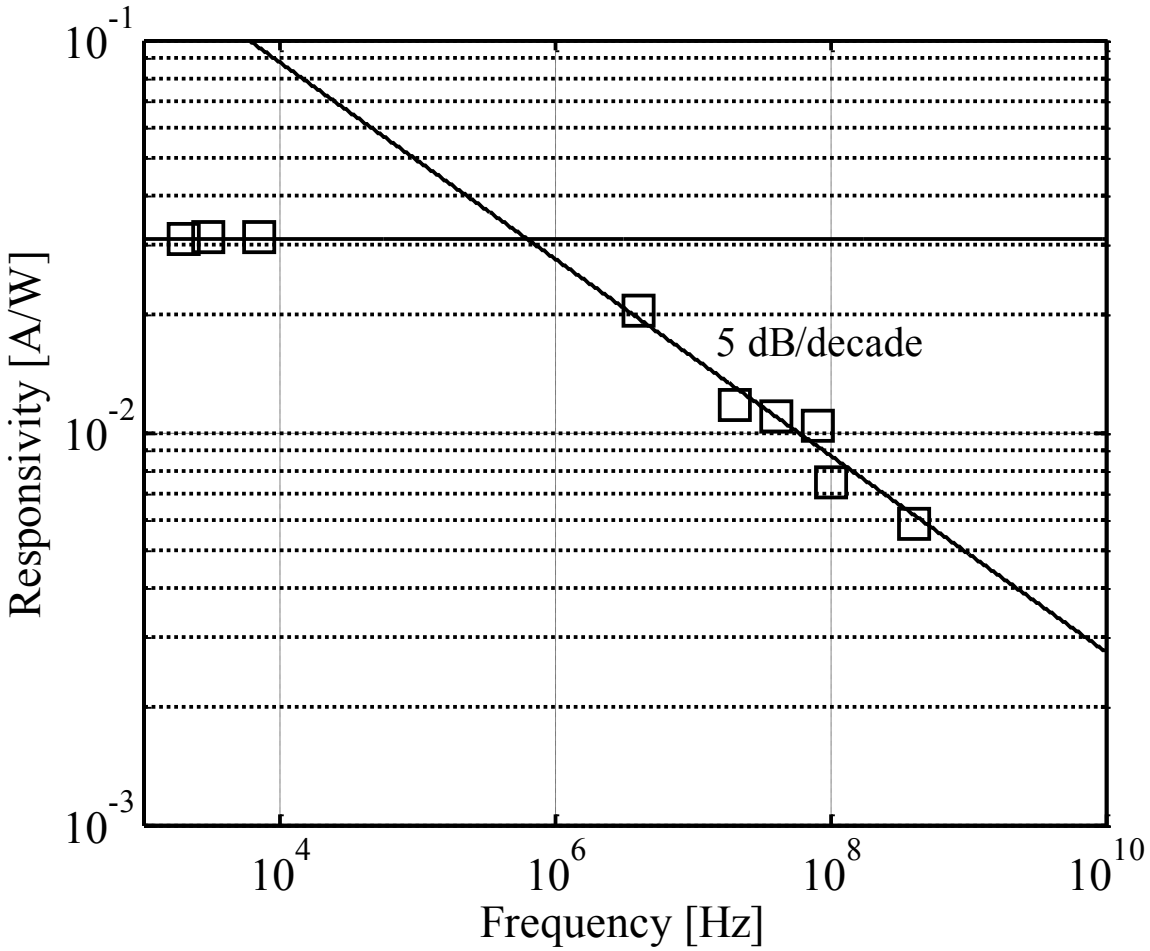


- ✗ Lower supply voltages ⇒ lower reverse bias voltages available ?
- ✗ Thinner depletion regions ⇒ less drift, more diffusion current, increased C_{PD} ?
- ✗ More complex dielectric stack ⇒ reduced light transmission
- ✓ Smaller metallization and contacts admits more light into the silicon
- ✓ "Standard" nanoscale processes provide many different materials, junctions
- ✓ Higher TIA bandwidth
- ✓ Lower power limiting amp, CDR, etc.
- ✓ More advanced signal processing solutions

Example: 65nm CMOS Photodetector



Example: 65nm CMOS Photodetector



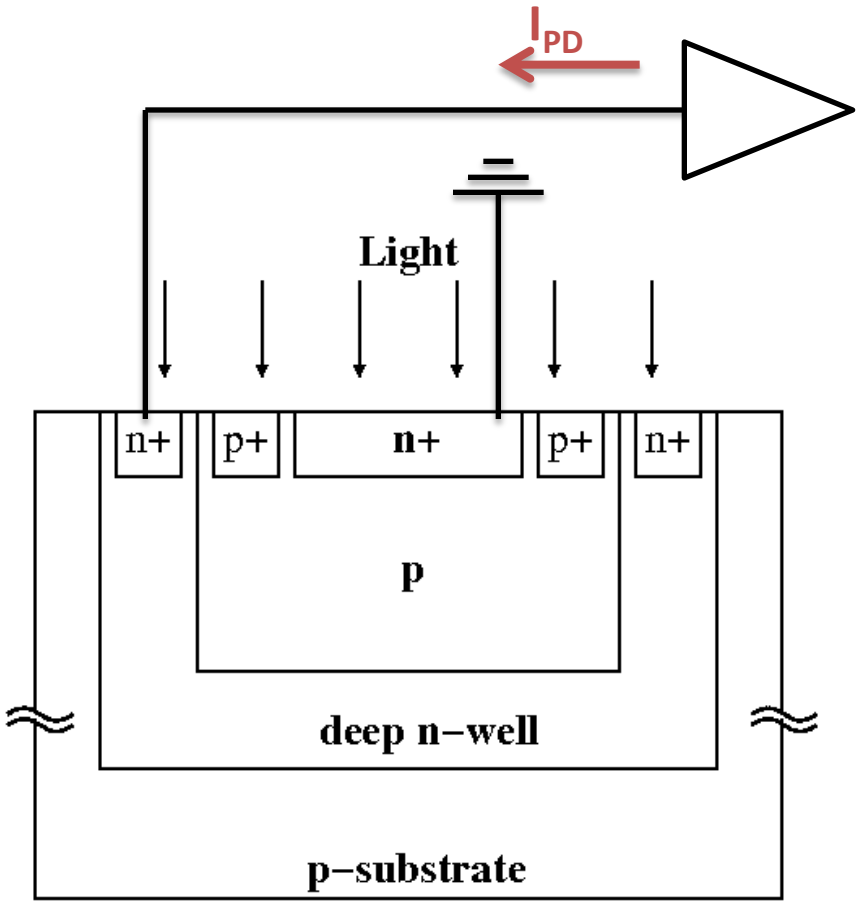
<u>n+/p-epi photodetector</u>
<u>670 mV reverse bias</u>

3-dB bandwidth of 2.5 MHz
20-dB bandwidth ≈ 6.3 GHz

DC responsivity = 0.03 A/W
c.f. ≈ 0.3 A/W typical
in 0.18 μm CMOS

- Shorter carrier lifetime?
- Reflection in dielectric stack?

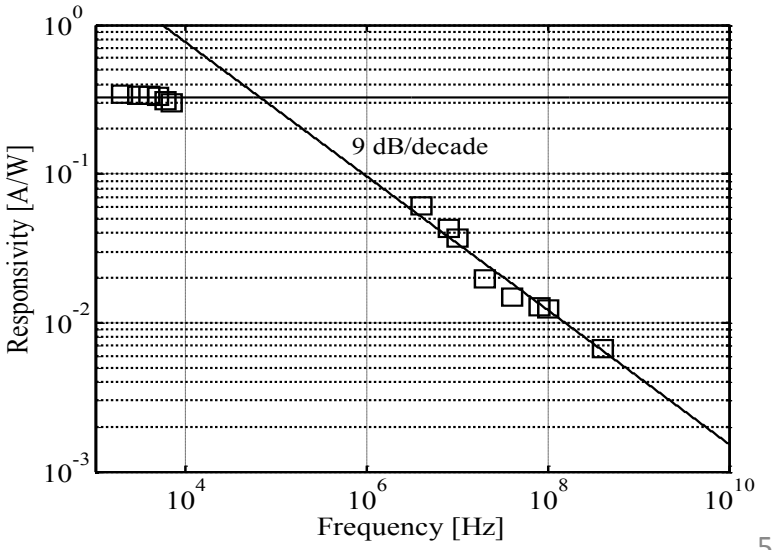
Phototransistor Experiment



- "Base" is left floating; base current is provided by photo-generated carriers
- The photocurrent observed at the "collector" is amplified by transistor action

<u>65-nm CMOS measurements:</u>

- > 0.3 A/W observed at low frequencies
- BUT 3-dB bandwidth of only 0.15 MHz



Conclusions

- There are applications at 850nm or shorter wavelengths where a high level of integration is more important than very high sensitivity
- A combination of
  - Clever use of existing CMOS process features
  - Signal processing circuitry

  have so far permitted performance in the range of 5 – 8.5 Gb/s @ -5 – 0 dBm input and 50 – 150 mW (better if very high supply voltages are permitted)
- Future progress:
  - Integration in nanoscale CMOS
  - Power reductions, speed improvements, sensitivity improvements
  - Demonstrable robustness in manufacture and test