Multi-Gbps Optical Receivers with CMOS Integrated Photodetectors

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February 2, 2011
Outline

• Introduction
  – Trend towards short-reach optical
  – Trend towards highly integrated transceivers

• Tutorial on High-speed CMOS photodetection
  – Optical properties of silicon
  – Standard CMOS photodetectors
  – Diffusion-shielded photodetectors
  – Spatially modulated light detectors

• Equalization to improve CMOS photodetectors
  – Analog equalization
  – Decision-Feedback Equalization

• Case study: 0.18 μm CMOS integrated optical receiver
  – SML detector
  – Analog equalizer

• Photodetectors in nanoscale CMOS technologies
  – Experimental results from a 65 nm process
Optical Communication Evolution

1990:

- **Power Consumption**
  - Optical: Increasing
  - Electrical: Increasing

- **Cost**
  - Optical: Increasing
  - Electrical: Increasing

- **Distance**
  - Many kilometers
Optical Communication Evolution

- **Distance**
  - 2000: 100's meters

- **Power Consumption**
  - Electrical
  - Optical

- **Cost**
  - Electrical
  - Optical

100’s meters
Optical Communication Evolution

2010:

Distance

Power Consumption

Cost

Optical

Electrical

10’s meters
Optical Communication Evolution

2020:

- **Power Consumption**
- **Cost**

*Electrical vs. Optical*

Distance

1’s meters
Optical Communication Evolution

Distance

Power Consumption

Cost

Centimeters?

Millimeters?

Electrical

Optical

?????:

Centimeters?

Millimeters?
Short-Reach Optical Communication

Characteristics
• High volume
• High port density

Requirements
➢ CHEAP!
   – VCSEL lasers at $\lambda = 850\text{nm}$
   – Multimode fiber
➢ Integration
➢ Low-power

Good recipe for CMOS!
Optical Transceiver

- VCSE Laser
- Laser Driver
- CDRs
- Digital Controller
- Photo-diode
- TIA
Optical Transceiver

- VCSE Laser
- Laser Driver
- CDRs
- Digital Controller

- Photodiode
- TIA

- Photodetector (e.g. GaAs)
- TIA (SiGe BiCMOS)
- VCSE Laser (InGaAs++)
- Laser Driver (SiGe BiCMOS)
- CDR (SiGe BiCMOS or CMOS)
- Digital Control (CMOS)

PCB
Optical Transceiver – SiP

Optical Transceiver – Silicon Photonics

VCSE Laser
Laser Driver
CDRs
Digital Controller

Photo-diode
TIA

Optical waveguides
Ge
CMOS
SiO₂
Si
Off-chip CW laser

PCB

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Optical Absorption of Semiconductors

Absorption PDF of light at $\lambda = 850$ nm

Silicon

Germanium
CMOS Photodetectors
Recombination
CMOS Photodetectors

- Slow-diffusing carriers
- Large PD capacitance
- Low responsivity
CMOS Photodetector Examples

n+/p

n-well/p
High Reverse Bias

- Fewer slow-diffusing carriers
- Reduced $C_{PD}$
- Potential for avalanche gain
- Reliability concerns
- Dual-supply or charge-pump required

Impact of Reverse Bias Voltage

Junction capacitance

Intrinsic frequency response
Layout Considerations

Few/Wider strips:
- Less contact metal blocking light
- Smaller $C_{PD}$

More/Smaller strips:
- Short diffusion times for the carriers to get to the contacts
- Additional sidewall depletion regions for light absorption

Similar tradeoffs arise between 1-D and 2-D contact arrays
Diffusion-Shielded Photodetectors

Similar effect provided by SOI
Diffusion-Shielded Photodetectors

- Fewer slow-diffusing carriers
- Can often be done without process modifications
  - Reduced DC responsivity

P. J. Lim et al, “A 3.3-V monolithic photodetector/CMOS preamplifier for 531 Mb/s optical data link applications,” ISSCC 1993
Diffusion-Shielded Photodetector Example

- The n+/p junction is reverse-biased and used as the active photodetector.
- The p/n-well junction is reverse biased to collect and discard photocarriers generated far below the n+/p junction.
Spatially Modulated Photodetectors
Spatially Modulated Photodetectors


- Fewer slow-diffusing carriers
- Can be done in any process
- Reduced $C_{PD}$
- $\frac{1}{2}$ of the light is reflected
- Requires excellent CMRR amplifiers
Typical CMOS PD Frequency Responses

![Graph showing typical CMOS PD frequency responses]

- **High reverse bias**: \( \geq 0.4 \) at \( \leq 0.3 \)
- **Standard**: \( \approx 0.3 \)
- **SML or Diffusion-Shielded**: \( \approx 0.1 \) – \( -0.01 \)
  - Slow rolloff due to diffusing carriers

- **-3 to -10 dB/decade**
- **\( \approx -20 \text{ dB/decade} \)**

- **Frequency**
  - \( \approx 1 \text{ - } 10 \text{ MHz} \)
  - \( \approx 1 \text{ GHz or more} \)

- **Response (A/W)**

---

Representative of photodiodes in 0.18 \( \mu \text{m} \) CMOS process with light at \( \lambda = 850 \text{ nm} \)
Typical CMOS PD Pulse Responses

Representative of photodiodes in 0.18 μm CMOS process with light at $\lambda = 850$ nm at 5 Gbps
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Equalization of the Pulse Response
Analog Equalization

- High-order transfer function is required to equalize the $\approx 5$ dB/decade slope
When combined with a SML detector, a first-order equalizer may suffice [Hermans, ESSCirc 2006]
Equalization of the Pulse Response

Mostly post-cursor pulse responses suggest that a DFE may be effective
Maximum Data Rates: Analog Eq. + DFE

- Many DFE taps are required to accurately cancel the distant post-cursor ISI
- High-gain low-noise TIA is required due to the reduced responsivity of an SML detector
• Slowly-diffusing carriers
  – Maximize depletion regions via layout
    ⇒ increases capacitance
  – Maximize depletion regions via large reverse bias
    ⇒ need for dual-supplies or charge pump, reliability concerns
  – Shield diffusing carriers
  – Signal processing techniques:
    • SML ⇒ decreases responsivity
    • equalization
• Low responsivity
  – Low-noise/high-sensitivity TIA
• High capacitance
  – Low input-resistance TIA
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SML Photodetector Example

- 0.18 µm bulk CMOS process
- M1 is used for contacts, M2 is used to block light
- Junction side-walls also collect photons
- 20 strips (10 light + 10 dark) across a 75um x 75um area
• Responsivity, $R = 0.03 \text{ A/W}$ & Input optical power of $-5 \text{ dBm}$ ⇒ **Photodiode current, $I_{PD} = 9 \mu\text{A}$**

• BER = $10^{-12}$ ⇒ **TIA input-referred noise of $0.65 \mu\text{A}_{\text{rms}}$**

• TIA output of $50 \text{ mV}$ makes noise performance of subsequent stages non-critical ⇒ $R_F = 5.6 \text{ k}\Omega$

• Similar architecture reported in:
Regulated Cascode Input?

- Low responsivity SML detector
- High system bandwidth (5-Gbps)
  - Very low input-referred noise required
  - No regulated cascode at the input
Transimpedance Amplifier

\[ C_{\text{in}} = C_{\text{PD}} + C_{A1} \approx 500 \text{ fF} + 500 \text{ fF} = 1 \text{ pF} \]

\[ C_{p1} \approx 680 \text{ fF} \]

\[ C_{p2} \approx 100 \text{ fF} \]

Notice \( V_{\text{PD,dc}} \approx V_{\text{DD}} - 625 \text{ mV} \)
Transimpedance Amplifier

$C_m = 0$

$C_m > 0$

Transimpedance Gain [dBΩ]

Frequency [GHz]
AC Coupling

- Converts single-ended signal to fully-differential
- Facilitates the operation of the TIA from a higher supply voltage
  ⇒ Higher reverse bias applied across the photodetector
  ⇒ Increased responsivity approximately 60%
Equalization + Limiting Amplifier

Additional differential gain required to improve CMRR

Analog Eq.

Limiting amplifier with DC offset compensation loop

Power Breakdown (Total 115mW)

- TIA
- Diff. Amp.
- Eq
- LA
Optical Alignment in Measurements
Measurement Results

At 4.25 Gbps

- Without equalization
- With equalization

BW-limited at 5 Gbps
Measurement Results

At 5 Gbps

- Increased current consumption in the TIA

⇒ Noise limited at 5 Gbps
## Measurement Summary

<table>
<thead>
<tr>
<th></th>
<th>LP</th>
<th>HP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18-μm CMOS</td>
<td></td>
</tr>
<tr>
<td>Supply voltages</td>
<td>3.3 V, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>Total chip area</td>
<td>1.5 x 2.8 = 4.2 mm²</td>
<td></td>
</tr>
<tr>
<td>Core area of optical receiver front-end</td>
<td>0.86 x 0.84 = 0.72 mm²</td>
<td></td>
</tr>
<tr>
<td>Optical wavelength</td>
<td>850 nm</td>
<td></td>
</tr>
<tr>
<td>Average input power</td>
<td>-3 dBm</td>
<td></td>
</tr>
<tr>
<td>Highest data rate with BER less than $10^{-12}$</td>
<td>4.25 Gbps</td>
<td>5 Gbps</td>
</tr>
<tr>
<td>RMS jitter</td>
<td>8.89 ps</td>
<td>11.6 ps</td>
</tr>
<tr>
<td>Total power consumption with output buffer</td>
<td>144 mW</td>
<td>183 mW</td>
</tr>
<tr>
<td>Power consumption without output buffer</td>
<td>129 mW</td>
<td>168 mW</td>
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</tbody>
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Impact of Technology Scaling

- Lower supply voltages ⇒ lower reverse bias voltages available?
- Thinner depletion regions ⇒ less drift, more diffusion current, increased $C_{PD}$?
- More complex dielectric stack ⇒ reduced light transmission

- Smaller metallization and contacts admits more light into the silicon
- “Standard” nanoscale processes provide many different materials, junctions
- Higher TIA bandwidth
- Lower power limiting amp, CDR, etc.
- More advanced signal processing solutions
Example: 65nm CMOS Photodetector
Example: 65nm CMOS Photodetector

n+/p-epi photodetector
670 mV reverse bias

3-dB bandwidth of 2.5 MHz
20-dB bandwidth ≈ 6.3 GHz

DC responsivity = 0.03 A/W
c.f. ≈ 0.3 A/W typical
in 0.18 μm CMOS

- Shorter carrier lifetime?
- Reflection in dielectric stack?
Phototransistor Experiment

- “Base” is left floating; base current is provided by photo-generated carriers
- The photocurrent observed at the “collector” is amplified by transistor action

65-nm CMOS measurements:
- > 0.3 A/W observed at low frequencies
- BUT 3-dB bandwidth of only 0.15 MHz

![Graph showingResponsivity vs Frequency](image)
Conclusions

- There are applications at 850nm or shorter wavelengths where a high level of integration is more important than very high sensitivity

- A combination of
  - Clever use of existing CMOS process features
  - Signal processing circuitry

have so far permitted performance in the range of 5 – 8.5 Gb/s @ -5 – 0 dBm input and 50 – 150 mW (better if very high supply voltages are permitted)

- Future progress:
  - Integration in nanoscale CMOS
  - Power reductions, speed improvements, sensitivity improvements
  - Demonstrable robustness in manufacture and test