A 45-nm SOI-CMOS Dual-PLL Processor Clock System for Multi-Protocol I/O

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Advanced Micro Devices, Inc., *GlobalFoundries
Outline

• Introduction

• Architecture and Circuits
  • Ring-based PLL
  • $LC$-based PLL

• Silicon Results

• Conclusion
The Vision

• I/O connectivity for integrated CPU + GPU
  • PCI Express® (PCIe) 1.1 & 2.0
  • DisplayPort™ (DP), DVI™, HDMI™
Multi-Protocol Requirements

- Wide range of operating modes
  - \( f_{\text{ref}} = 50 - 450 \, \text{MHz} \rightarrow f_{\text{out}} = 125 - 2500 \, \text{MHz} \)
  - 2 – 4 MHz BW @ < 2 dB Peaking
  - 5 – 8 MHz BW @ < 1 dB Peaking
  - 8 – 16 MHz BW @ < 3 dB Peaking

- Strict PLL phase jitter requirements < 1.0 – 1.5 ps rms

- Fast exit (< 5 µs) from power-down/sleep modes for low-power client applications
Design Challenges

• Partially-depleted (PD) SOI noise concerns
  • More FET noise than bulk from floating body and high-resistance body ties
  • More difficult to predict jitter since RF simulators cannot handle floating-body devices correctly

• PVT variation + mismatch → large $BW$ variation
  • e.g., 3x VCO gain variation

• Noisy operating environment
  • Multi-core CPU + graphics + memory controller
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Dual-PLL Architecture

- Low-jitter **LC-PLL** for PCIe 2.0 (narrow tuning range)
- Higher-jitter **Ring-PLL** for all other modes (wide tuning range)
- 10% area overhead for dual-PLLs (many shared circuits)
- Voltage regulators (from 2.5 V) to reduce power-supply noise
Ring-PLL – Dual-Path VCO Control

- **High-BW** / low-gain path ($V_{control}$)
  - Sets PLL bandwidth
  - Conventional 2-pole / 1-zero
  - Effective $K_{VCO} \downarrow \rightarrow$ jitter $\downarrow$
    (70% less jitter contribution from loop-filter resistor and charge-pump)

- **Low-BW** / high-gain path ($V_{slow}$)
  - Sets VCO “center” frequency
  - $BW (V_{slow}) < 0.2\% \times BW (V_{control})$
  - Contributes negligible jitter
  - Bypass $R_{slow}$ during fastlock mode (pay attention to stability)
  - $IR$ drop across $R_{slow}$ due to leakage $< 15$ mV $\rightarrow$ limits $BW (V_{slow})$
Ring-PLL – Slow-Path Jitter Analysis

• Low-pass filter shapes noise to control jitter
  - $V_n \propto \frac{1}{C_{slow} \sqrt{R_{slow}}}$
  - For constant $RC$, get lower jitter with larger $C_{slow}$ but area penalty
  - $R_{slow} = 600$ k$\Omega$ and $C_{slow} = 20$ pF
• Negligible slow-path jitter
  - Slow-path jitter < 75 fs
  - Fast-path jitter < 400 fs
  - VCO jitter < 1000 fs

$R_{slow} \cdot C_{slow} = \text{constant}$
Ring-PLL – VCO Design

• Dual-control path for lower effective gain
• Body-tied MOSFETs for jitter reduction and ability to simulate \(\rightarrow 2x\) speed penalty
• 5-stage Ring-oscillator VCO
  • 5 stages for easier oscillation
  • Cross-coupled inverters for fast slew rates and level shifting
• Source degeneration in current bias for noise reduction
• Amplifier in bias circuits to improve supply noise rejection
• Divide-by-2 \(\rightarrow 50\%\) duty-cycle
Body-Tied PD-SOI MOSFET (T-Gate)

• Enables body connection to undepleted FET well
• High $R_{\text{body}}$ and extra $C_{\text{gate}}$ limits $BW$ of body connection
• NMOS example

![Diagram of body-tied PD-SOI MOSFET (T-Gate)]
Ring-PLL – VCO Gain Calibration

- PLL in closed-loop operation with *fastlock* asserted
- Algorithm – reduce $K_v[3:0]$ until $V_{\text{control}} > V_{\text{ref}}$

- Result
  - $K_{vco}$ variation across PVT reduced by 43%
  - More constant $I_{bias}$ → 15% less jitter
  - → 9 dB lower ref spurs
Bandwidth and Peaking Measurements

- Algorithm based on Fischette et al., CICC 2009
  - Apply instantaneous half-period phase step by inverting RefClk
  - Measure $\tau_{crossover}$ ($\rightarrow BW$) and MaxOvershoot ($\rightarrow$ Peaking)

![Graph showing phase error and crossover time](image)
**LC-PLL – 10 GHz LC-VCO Design**

- Lower jitter than ring-VCO
- 29% tuning range
- Tune at 4x required frequency for smaller \( L \) and 50% duty cycle
- Low VCO gain → No slow path required
- Floorplan to avoid magnetic coupling from switching currents in surrounding circuits and supply bumps
LC-PLL – VCO Elements

- Body ties for gain and tail devices
  - Narrow widths for higher $BW$ connectivity
  - Lower channel and upconverted $1/f$ noise
  - Tuning range penalty from T-gate load
- Differential inductor
  - M11 turns with M10-M09-M08 underpass
  - Extensive dummy metal fill for CMP manufacturability
- Varactors
  - Accumulation mode n-well for good $Q$
  - Thick oxide for low $I_{gate}$
**LC-PLL – Coarse-Tuning Calibration**

- VCO coarse-tuned by 5-bit DAC, steps frequency by 0.5 – 0.8%
- Calibrate VCO using $RefClk$ and PLL feedback clock counters
- $RefClk$ has up to 0.5% spread spectrum frequency modulation
- Count over one 33 kHz spread spectrum period to desensitize calibration from modulation phase and preserve post-calibration tunability, otherwise risk non-monotonic calibration code
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Measured Phase Noise at 2.5 GHz
RMS Jitter Distributions at 2.5 GHz

- 1 MHz – 1.25 GHz integration window
- 27 parts (includes $V_T$ and resistor skew wafers)
Die Photograph

- Voltage Regulators
- ESD
- Ring VCO
- LC VCO
- Charge Pumps
- STATE Machines
- Loop Filters

Dimensions:
- Width: 388 µm
- Height: 715 µm
## Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ring-PLL</th>
<th>LC-PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>45 nm SOI-CMOS (36 nm (L_{\text{gate}}))</td>
<td></td>
</tr>
<tr>
<td>VCO Lock Range</td>
<td>1.0 – 8.5 GHz</td>
<td>8.3 – 11.1 GHz</td>
</tr>
<tr>
<td>RMS Jitter</td>
<td>Mean ± 3(\sigma)</td>
<td>975 ± 85 fs</td>
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<tr>
<td>Phase Noise</td>
<td>At 1 MHz Offset</td>
<td>–106.6 dBc/Hz</td>
</tr>
<tr>
<td></td>
<td>At 10 MHz Offset</td>
<td>–114.9 dBc/Hz</td>
</tr>
<tr>
<td>Reference Spur</td>
<td>At 100 MHz Offset</td>
<td>–58.4 dBc</td>
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<tr>
<td>Jitter Transfer</td>
<td>–3 dB Bandwidth</td>
<td>6.6 MHz</td>
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<tr>
<td></td>
<td>Peaking</td>
<td>0.41 dB</td>
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<tr>
<td>Supply Consumption</td>
<td>Current</td>
<td>28 mA</td>
</tr>
<tr>
<td></td>
<td>Voltage</td>
<td>1.8 – 2.7 V (2.5 V nom)</td>
</tr>
</tbody>
</table>
Conclusion

• Designed dual-PLL system for clocking multi-protocol wireline I/O in 45-nm SOI-CMOS processors

• Presented circuit and architectural techniques to minimize impact of PD-SOI floating-body and PVT variations

• Exceeded multi-protocol requirements
  • 1.0 – 11.1 GHz VCO lock range
  • 975±85 fs rms jitter for ring-based PLL
  • 535±76 fs rms jitter for LC-based PLL
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Thank you for your attention!