# Temperature Sensor Design for Power/Thermal Management in Emerging Semiconductor Processes

by
Randy Geiger

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**ABSTRACT**

Various methods of building on-chip temperature sensors will be reviewed. Performance requirements for on-chip temperature sensors needed for power/thermal management will be discussed. New approaches for building on-chip temperature sensors for multi-site temperature monitoring for power/thermal management in fine-feature processes will be presented. Techniques for designing temperature sensors which provide a Boolean representation of temperature without requiring either an ADC or a voltage reference will be introduced.

# Acknowledgements

Much of this work has been supported by the National Science Foundation and the Semiconductor Research Corporation

Results primarily due to the following students in the AMS program at Iowa State University

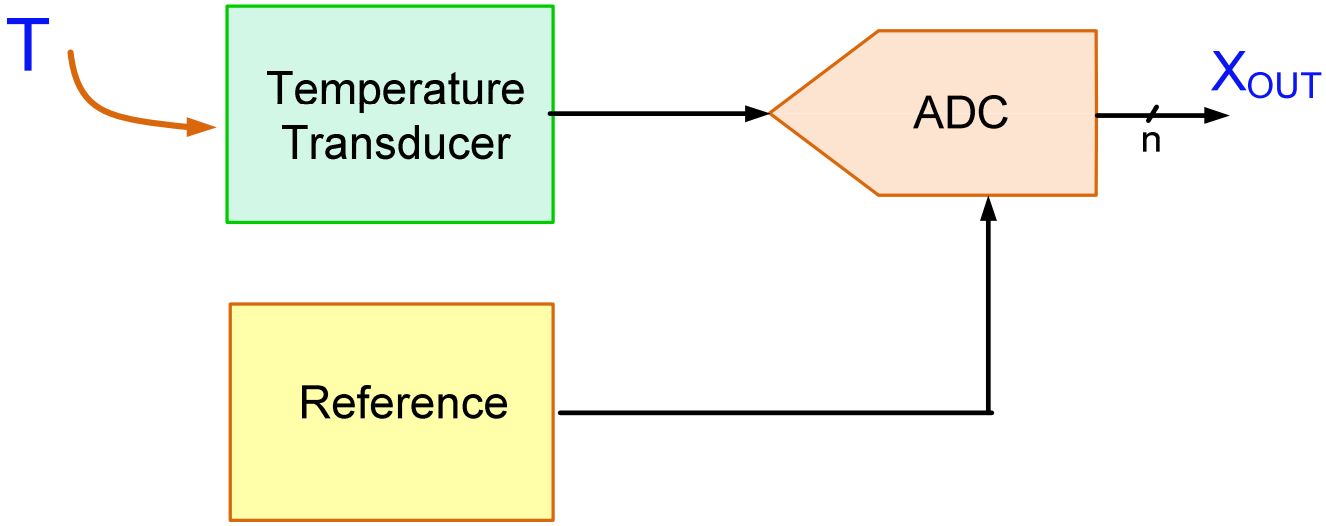
- Jun He
- Chen Zhao
- Alex Lee
- Tina Wang
- Karl Peterson

Project coordinated by faculty members Degang Chen and Randy Geiger

# Outline

- Review of Temperature Sensor Approaches
- Goal and Motivation
- Inverse Widlar Temperature Sensor
  - Description
  - Measured Results
- Second-Order Temperature Dependence to $V_T$
- Temperature Sensor with Improved Headroom
- Four-Transistor Dual-$V_T$ Temperature Sensor
- Temperature to Digital Converter
- Summary

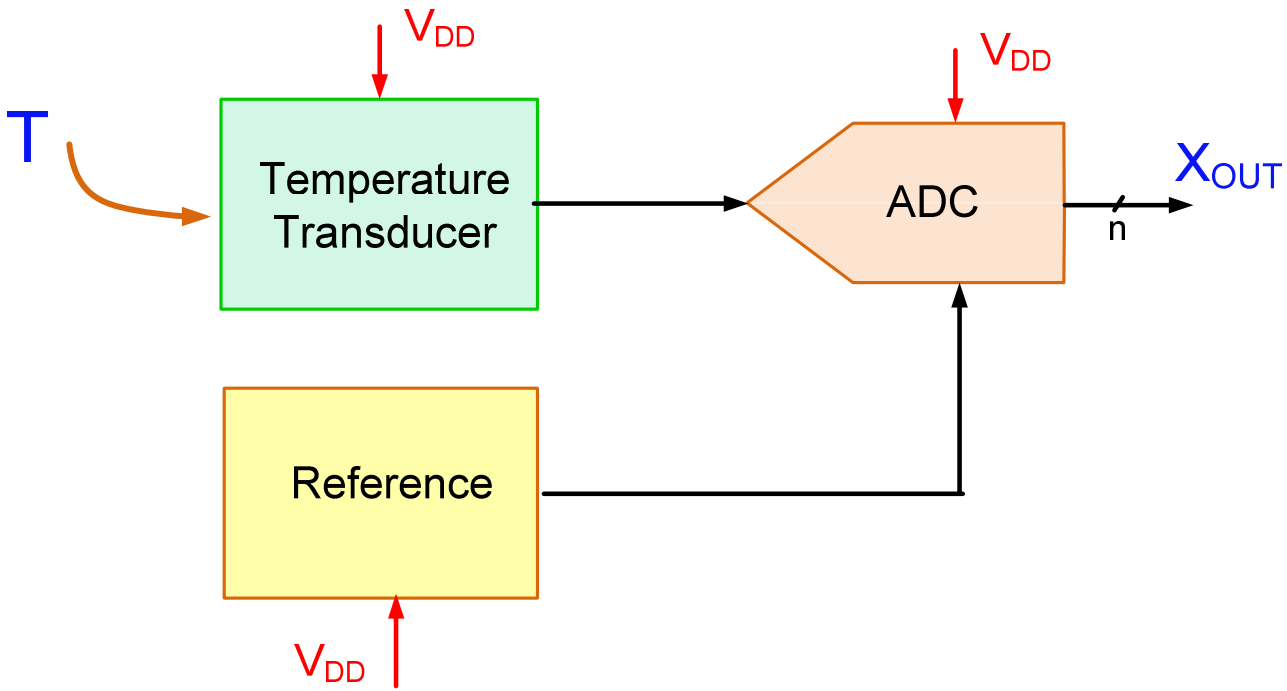
# Standard Approach to Temperature Sensor Design




- Temp transducer usually provides an output voltage
- Reference is usually a voltage reference
- Generally require calibration at one or more temperatures
- Viable solution for temperature sensor products but not attractive for multi-site on-chip temperature measurement for power/thermal management
    - Large area
    - Power dissipation
    - Accuracy

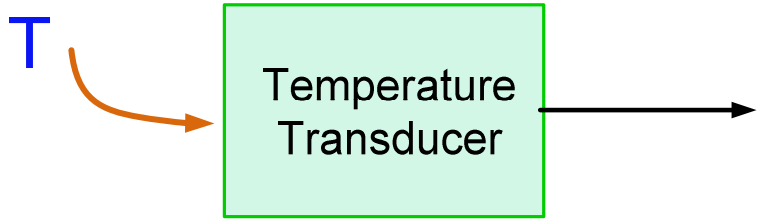
# Standard Approach to Temperature Sensor Design

And – all blocks require biasing



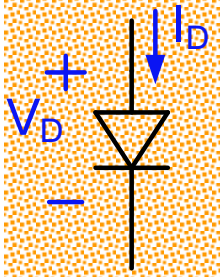

- Variations in supply voltage affect performance of Transducer, Reference, and ADC
- Introduce errors (often significant) in $X_{OUT}$ that can not be calibrated out

# Temperature Transducer Concepts

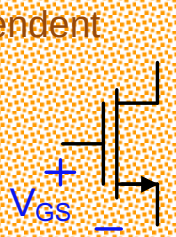



What is temperature dependent in MOS processes?

Noise is everywhere temperature dependent




$$I_D(T) = \left( J_{SX} A \left[ T^m e^{\frac{-qV_{G0}}{kT}} \right] \right) e^{\frac{qV_D}{kT}}$$




Strong inversion saturation

$$I_D(T) \simeq \mu C_{OX} \frac{W}{2L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

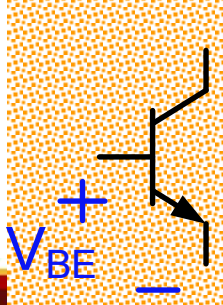
Weak inversion saturation

$$I_D(T) \simeq \mu C_{OX} \frac{W}{L} (V_T)^2 e^{\frac{q(V_{GS} - V_{TH})}{kT}} \left[ 1 - e^{\frac{-qV_{DS}}{kT}} \right]$$

$$\mu \simeq \mu_O T^m$$

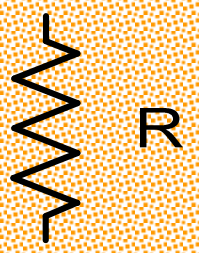
m around -1.5 but variable

$$V_{TH}(T) \simeq V_{TH0} + \gamma_{VT} T$$




$$I_C(T) = \left( \beta \hat{J}_{SX} A \left[ T^m e^{\frac{-qV_{G0}}{kT}} \right] \right) e^{\frac{qV_{BE}}{kT}}$$

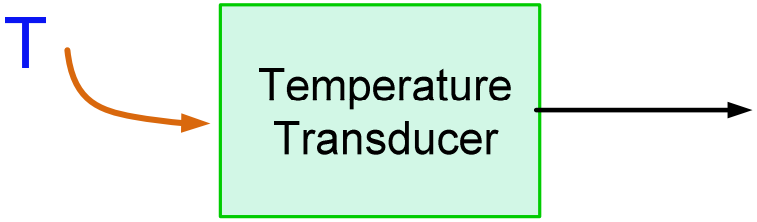
β and $R_B$ are nonlinearly dependent on T




$$R = R(T)$$

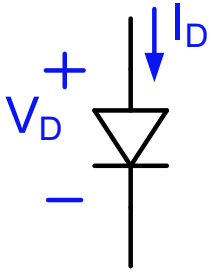
$$S_n(f) = 4kTR$$

# Temperature Transducer Concepts

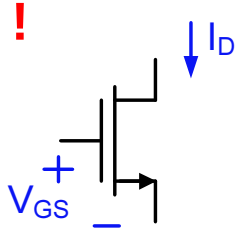



Which are used (proposed) as temperature sensors?

**All of them !**




$$I_D(T) = \left( \tilde{J}_{SX} A \left[ T^m e^{\frac{-qV_{G0}}{kT}} \right] \right) e^{\frac{qV_D}{kT}}$$




Strong inversion saturation

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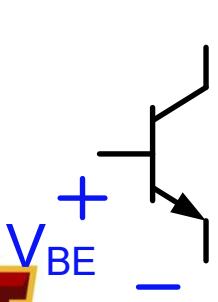
$$\mu \simeq \mu_O T^m$$ m around -1.5 but variable

$$V_{TH}(T) \simeq V_{TH0} + \gamma_{VT} T$$



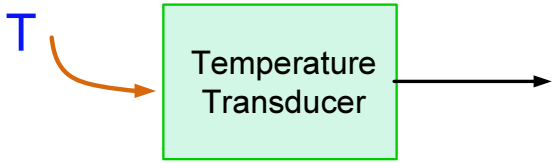

$$I_C(T) = \left( \beta \hat{J}_{SX} A \left[ T^m e^{\frac{-qV_{G0}}{kT}} \right] \right) e^{\frac{qV_{BE}}{kT}}$$

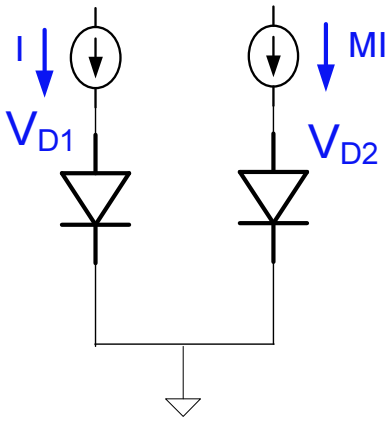
β and $R_B$ are nonlinearly dependent on T


$$R = R(T)$$

$$S_n(f) = 4kTR$$

# Temperature Transducer Circuits



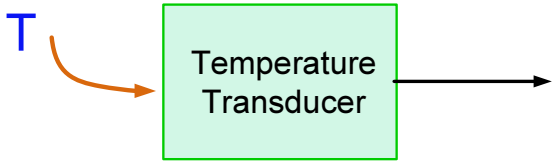

Assuming diodes matched

$$\left.\begin{aligned} I_{D1}(T) &= \left(\tilde{J}_{SX} A\left[T^m e^{\frac{-qV_{G0}}{kT}}\right]\right) e^{\frac{qV_{D1}}{kT}} \\ I_{D2}(T) &= \left(\tilde{J}_{SX} A\left[T^m e^{\frac{-qV_{G0}}{kT}}\right]\right) e^{\frac{qV_{D2}}{kT}} \\ I_{D2}(T) &= M I_{D1}(T) \end{aligned}\right\}$$

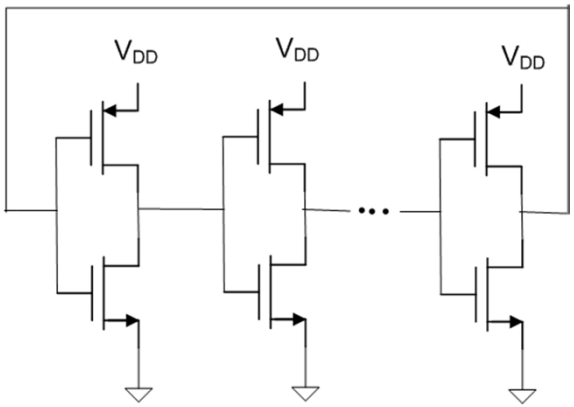
$$V_{D2} - V_{D1} = \frac{kT}{q}\ln(M)$$

- Most diode and BJT temp sensor circuits based upon this analysis
- Batch-level calibration often reported without details (compensates for $R_B$ and β)

# Temperature Transducer Circuits



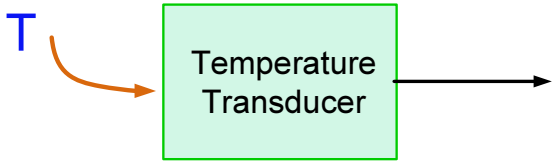

Ring oscillator based sensor



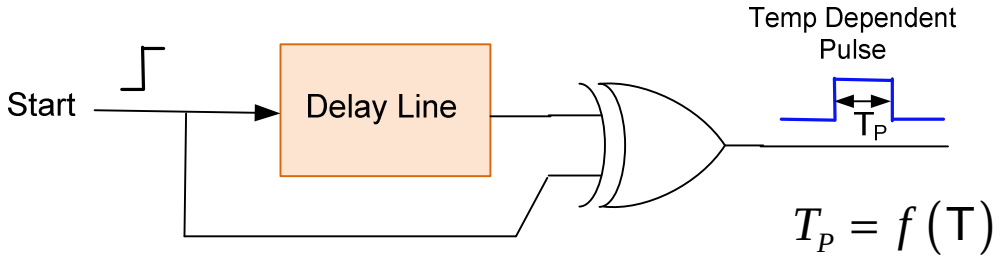

$$f_{OSC} = f(T)$$

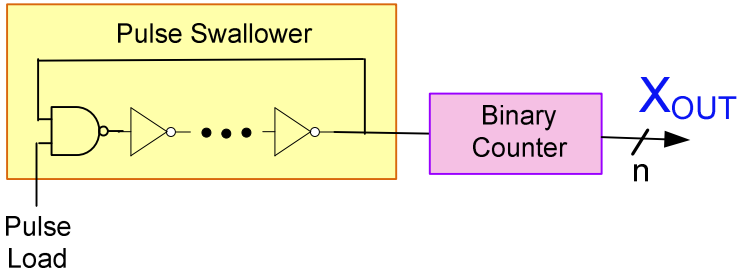
- Output signal is frequency
- ADC (not shown) is a frequency detector (counter)
- Depends nonlinearly on μ(T) and $V_T$(T)
- Depends upon $V_{DD}$

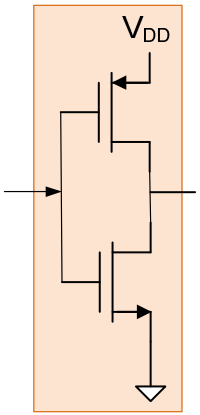
# Temperature Transducer Circuits




## Pulse-Swallowing Temperature Sensor



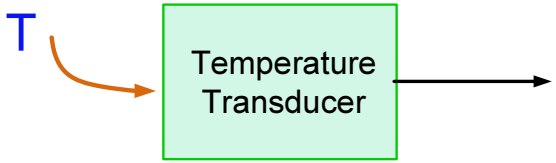




Delay Line

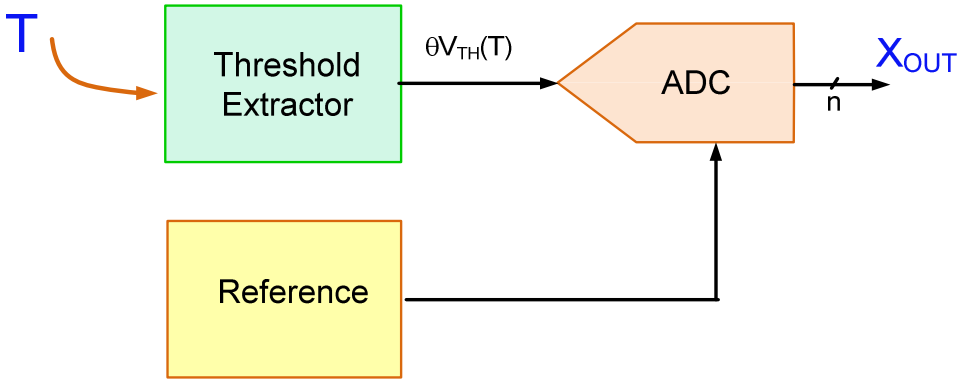
Pulse Swallower is an <u>even</u> number of inverters in a loop

- Output signal is pulse period
- ADC is Swallower/Counter
- Depends nonlinearly on μ(T) and $V_T$(T)
- Depends upon $V_{DD}$

# Temperature Transducer Circuits



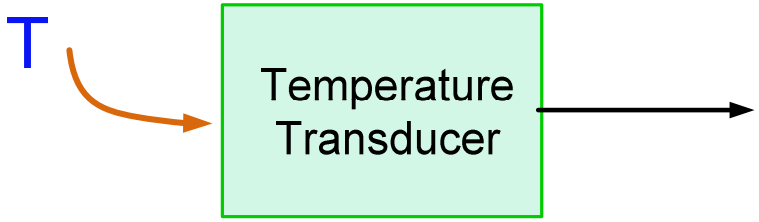

Threshold-Based Temperature Sensor



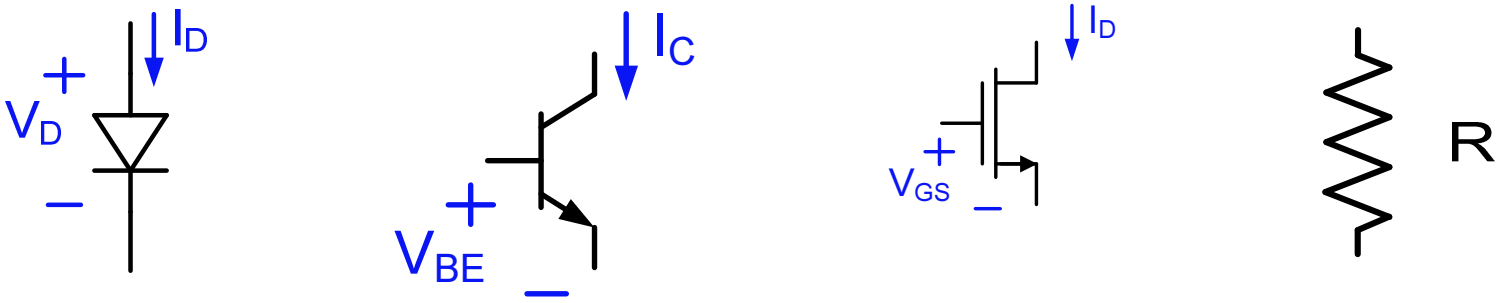

$$V_{TH}(T) \simeq V_{TH0} + \gamma_{VT} T$$

- Output "expresses" $V_{TH}$
- Output is highly linear in T
- Threshold Extractor can be small, low power

# Temperature Transducer Concepts




Which are used (proposed) as temperature sensors?




Little in literature suggests which type of temperature transducer is best

Little in literature suggests which circuit structure is best

- Experimental results based upon small samples
- Measurement procedures often questionable
- Models for temperature dependence of key parameters not well developed either functionally or statistically

Will focus here on threshold-based temperature sensors which show promise for multi-site applications needed for power/thermal management

- Small, low power, linear

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# Goal:

Develop $V_{DD}$-independent temperature sensor with Boolean output that is very small, very low power, that is useful for power/thermal management applications (1°C accuracy over 80°C to 110°C range)

Secondary Goal: Develop general-purpose temperature sensor with 0.5°C linearity over -20°C to 120°C range.

# Goal:

Develop $V_{DD}$-independent temperature sensor with Boolean output that is very small, very low power, for power/thermal management applications
(1°C accuracy over 80°C to 110°C range)

Premise:

1. Linearity of output with temperature is the major challenge
2. Single-temperature trim can compensate for most process variations
3. Batch calibration for slope adequate for modest temperature range
4. Second temperature trim for slope if needed

Standard Approach:

1. Develop sensor that provides linear temperature output
2. Develop ADC to convert this linear signal to Boolean form

# Rationale:

Rationale:

- Threshold voltage varies quite linearly with temperature
- Threshold extraction circuits should be small and low power
- Compatible with existing and emerging processes

Concerns:

- Precise temperature dependence of threshold voltage with temperature not well characterized
- In contrast to pn-junction PTAT voltage generators, threshold voltage does not project to 0V at T=0K

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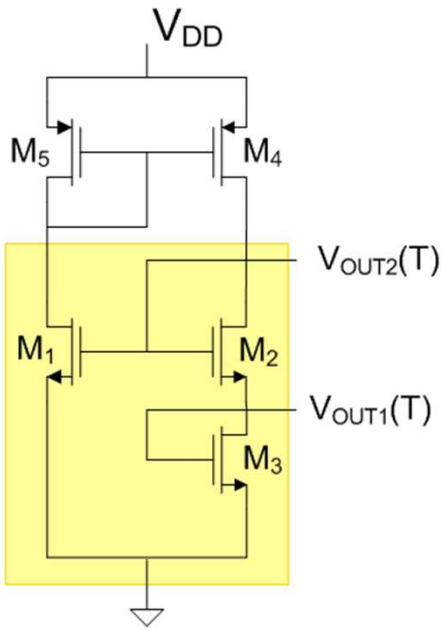
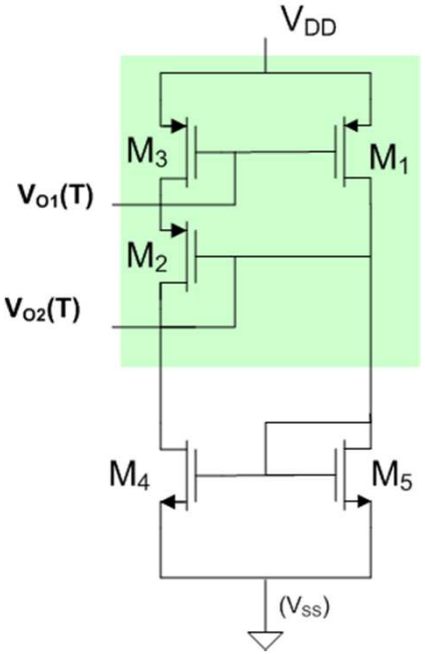
# Inverse-Widlar Temperature Sensor




n-type

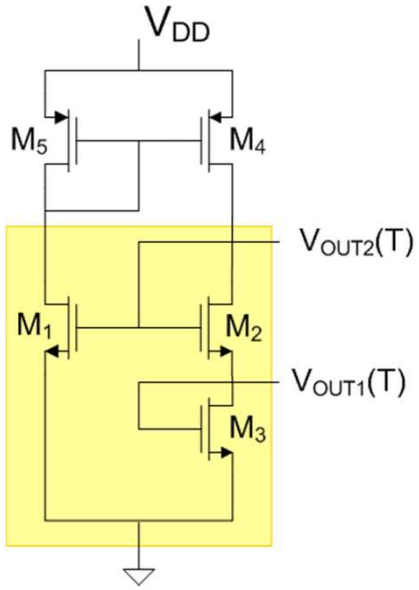



p-type

- Express threshold voltage at outputs
- Ideally supply independent
- Well-known as bias generators but not as temp sensors
- Seemingly simple structures but design space is large
- Start up circuits not shown

# Inverse-Widlar Temperature Sensors

Expression of threshold voltage




n-type

$$V_{01} = V_{Tn}\left(\frac{1-\sqrt{\frac{W_2L_1}{MW_1L_2}}}{1+\sqrt{\frac{W_2L_3}{W_3L_2}}-\sqrt{\frac{W_2L_1}{MW_1L_2}}}\right)$$

$$V_{02} = V_{Tn}\left(\frac{1+\sqrt{\frac{W_2L_3}{W_3L_2}}-2\sqrt{\frac{W_2L_1}{MW_1L_2}}}{1+\sqrt{\frac{W_2L_3}{W_3L_2}}-\sqrt{\frac{W_2L_1}{MW_1L_2}}}\right)$$

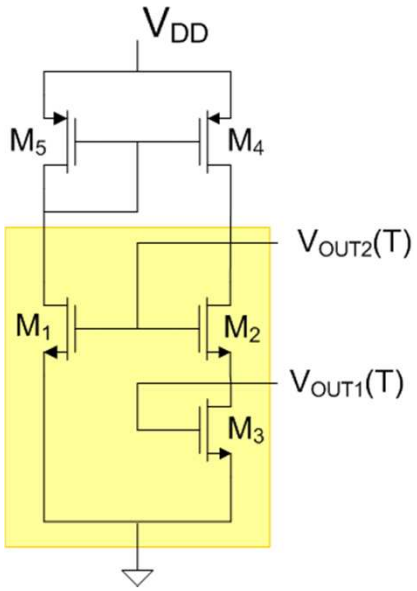
where M is the current mirror gain of $M_5$:$M_4$

$$V_{Tn} = V_{T0n} + \gamma_n T$$

- Used basic square-law model w/o γ or λ effects
- Outputs highly linear with T
- Outputs highly independent of $V_{DD}$
- Outputs of other structures similarly express $V_T$

# Inverse Widlar Temperature Sensors

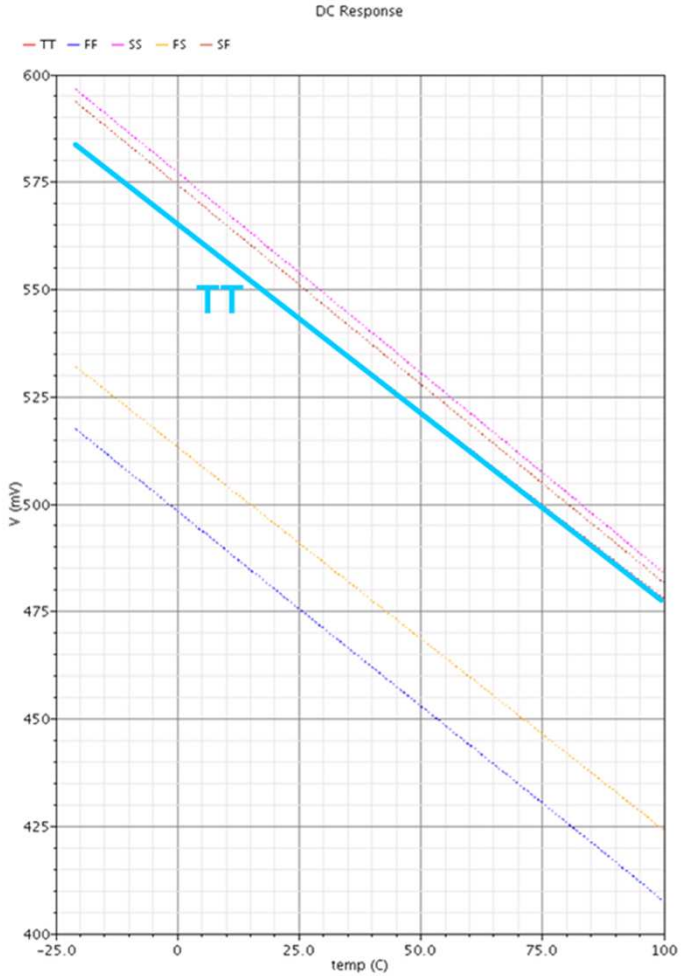
Simulation Results – TSMC 0.18u




n-type

$$\Delta V_{OUT1} \backsimeq 110mV$$

Over 120°C, output is quite linear at TT



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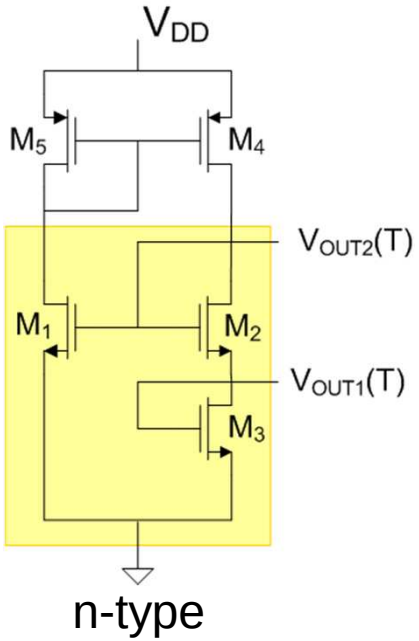


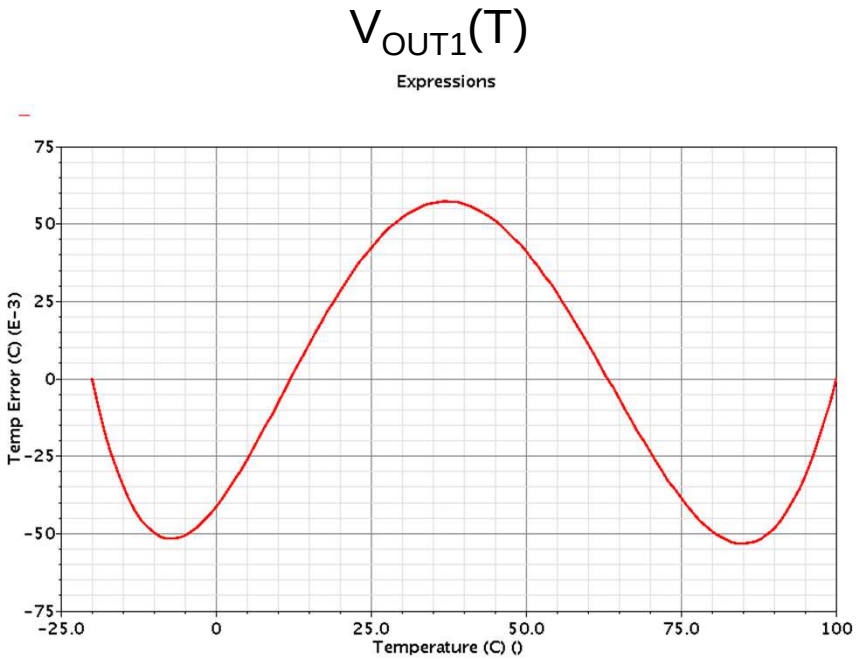


Over 120ºC, INL is about .055ºC at TT

# Inverse Widlar Temperature Sensors

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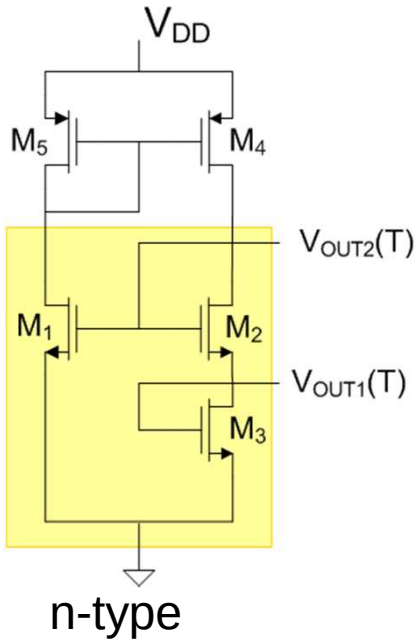
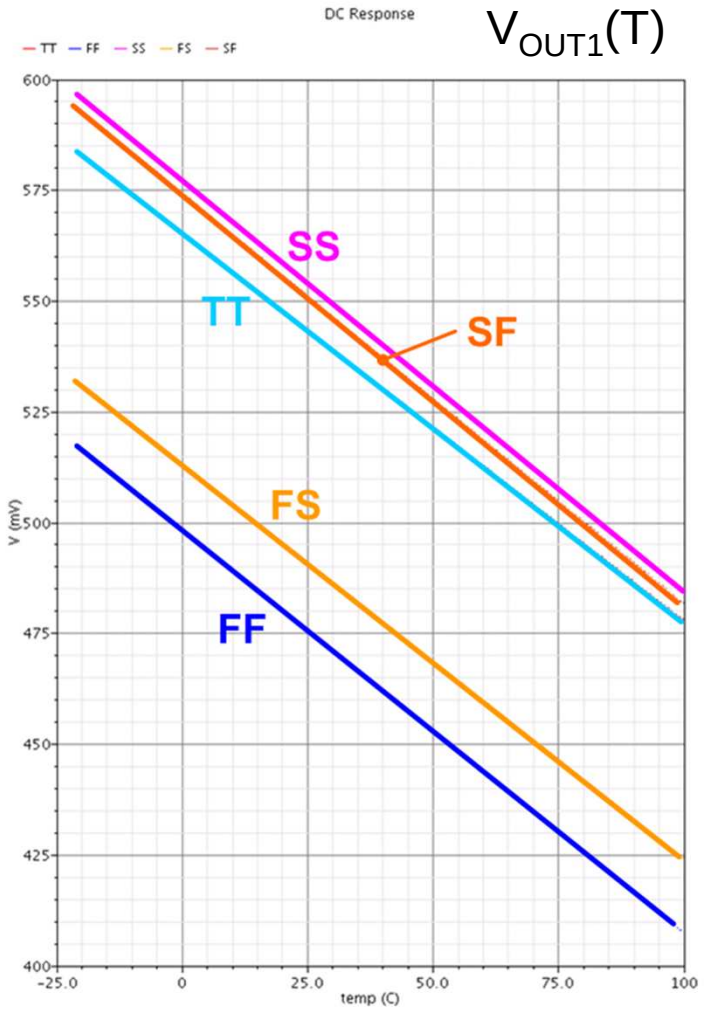



n-type

$V_{OUT1}(T)$




Linearity remains good over process corners

# Inverse Widlar Temperature Sensors

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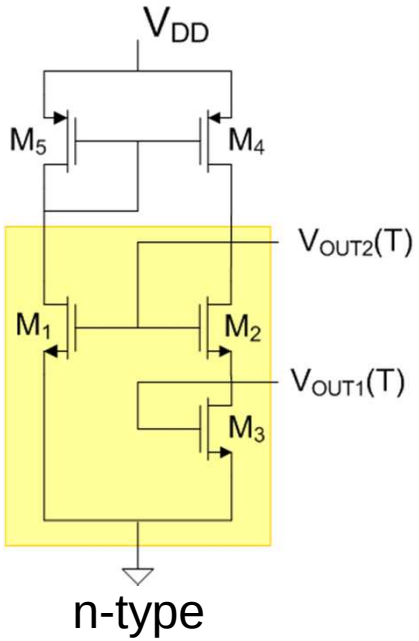


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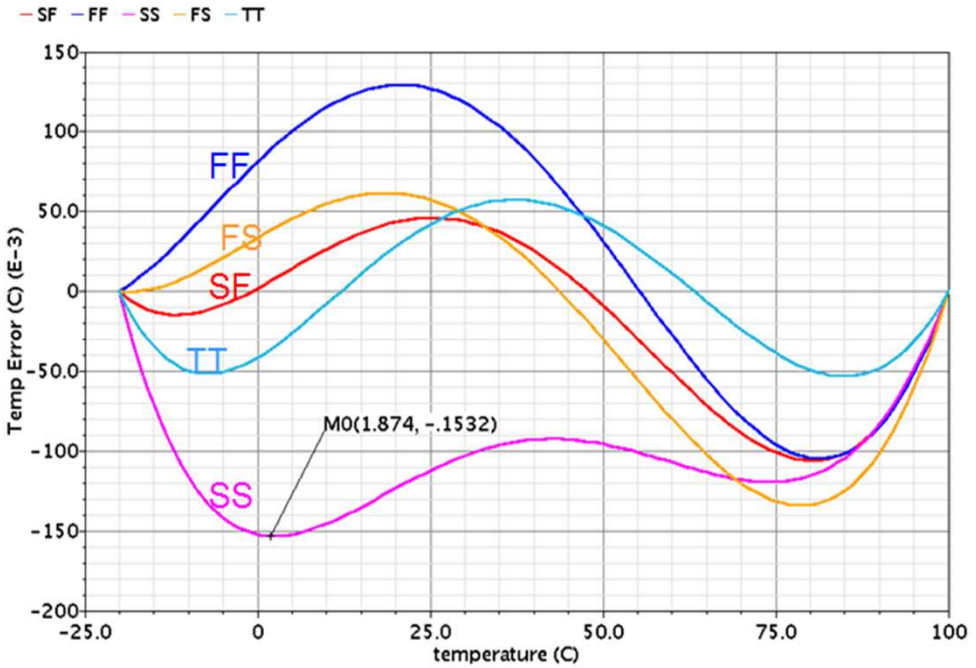
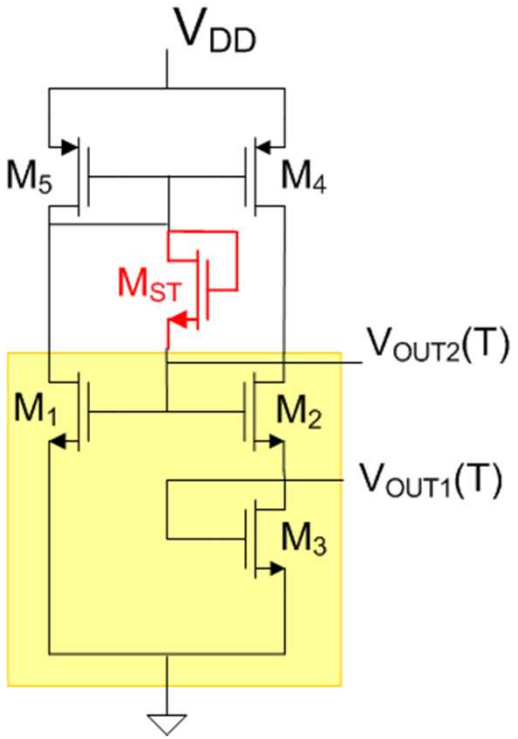



- Linearity error bounded by 0.16°C over process corners
- This suggests that linearity is robust to process variations
- Robustness is not discussed in any of the published results

# Inverse Widlar Temperature Sensors

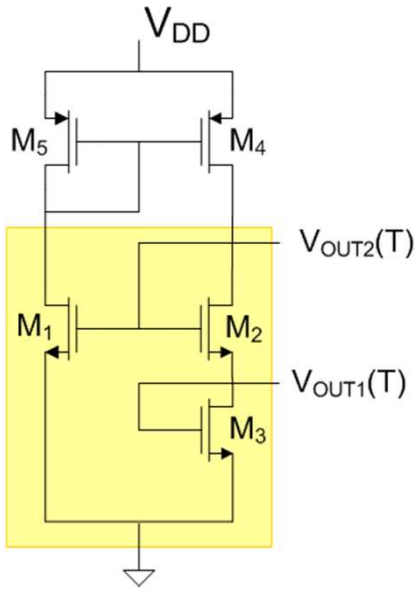
Start-up Circuit




- Some useful fundamental results for characterizing start-up circuits were developed
- These have not been reported in the literature
- Will not go into details in this review

# Inverse Widlar Temperature Sensors

Simulation results – TSMC 0.18u

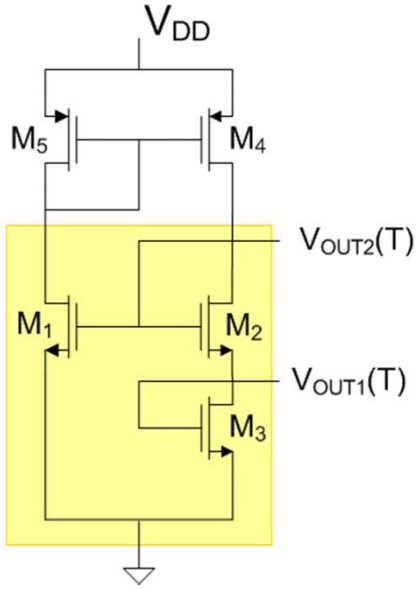



n-type

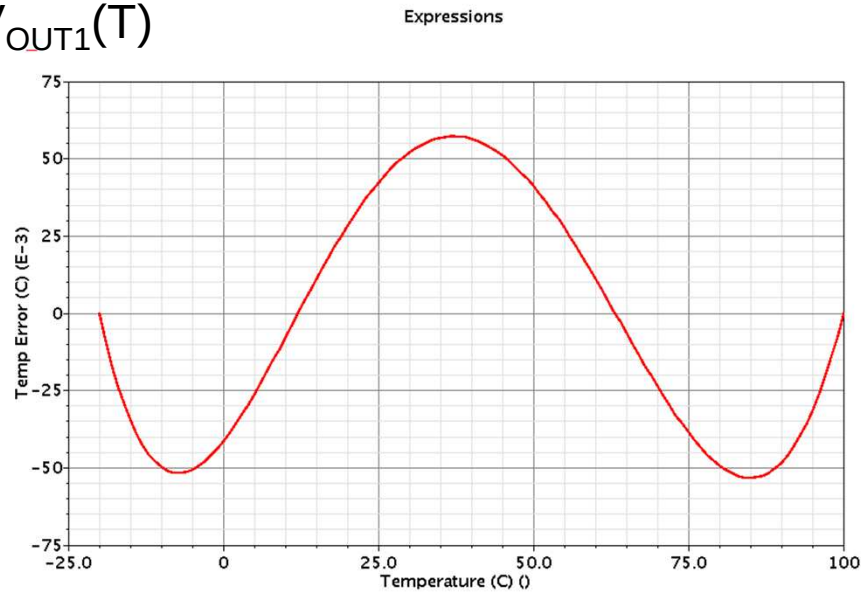
| *Parameters* | *Performances* |
|---|---|
| Maximum Temp Error (°C) at typical condition | 0.055 |
| Maximum Temp Error (°C) at worst corner | 0.16 |
| Maximum Temp Error (°C) at 500 # MC simulation | mu=0.11, std=0.04 |
| Current (μA) | 53.5 |
| Layout area estimated ($\mu m^2$) | 400 |
| Output Voltage Temp Coefficient (mV/°C) | -0.89 |

# Inverse Widlar Temperature Sensors

Expression of threshold voltage

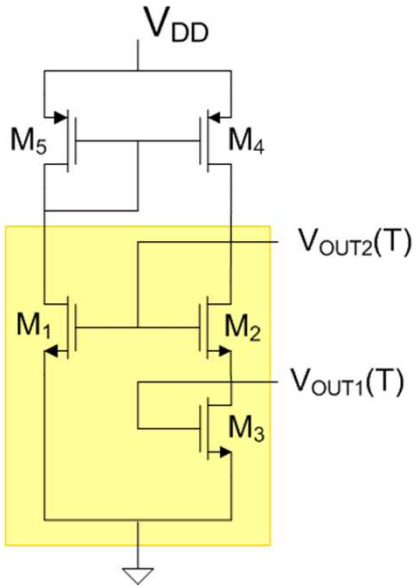



$V_{OUT1}(T)$

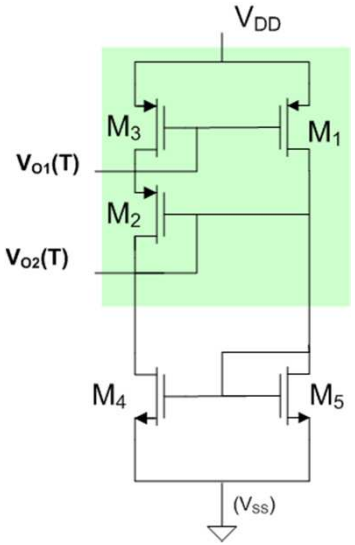



- Over 120°C, INL is about .055°C at TT and about 0.16°C over all corners
- Slope quite independent of process – single batch calibration may be adequate
- Single-point calibration to compensate for process-dependent offset
- Area is very small and power dissipation is very low
- Results based upon simulations in 0.18u process, must verify experimentally

# Voltage Linear to Temperature Sensors




n-type




p-type

Based upon simulations, these circuits appear to be much more linear with T than anything reported

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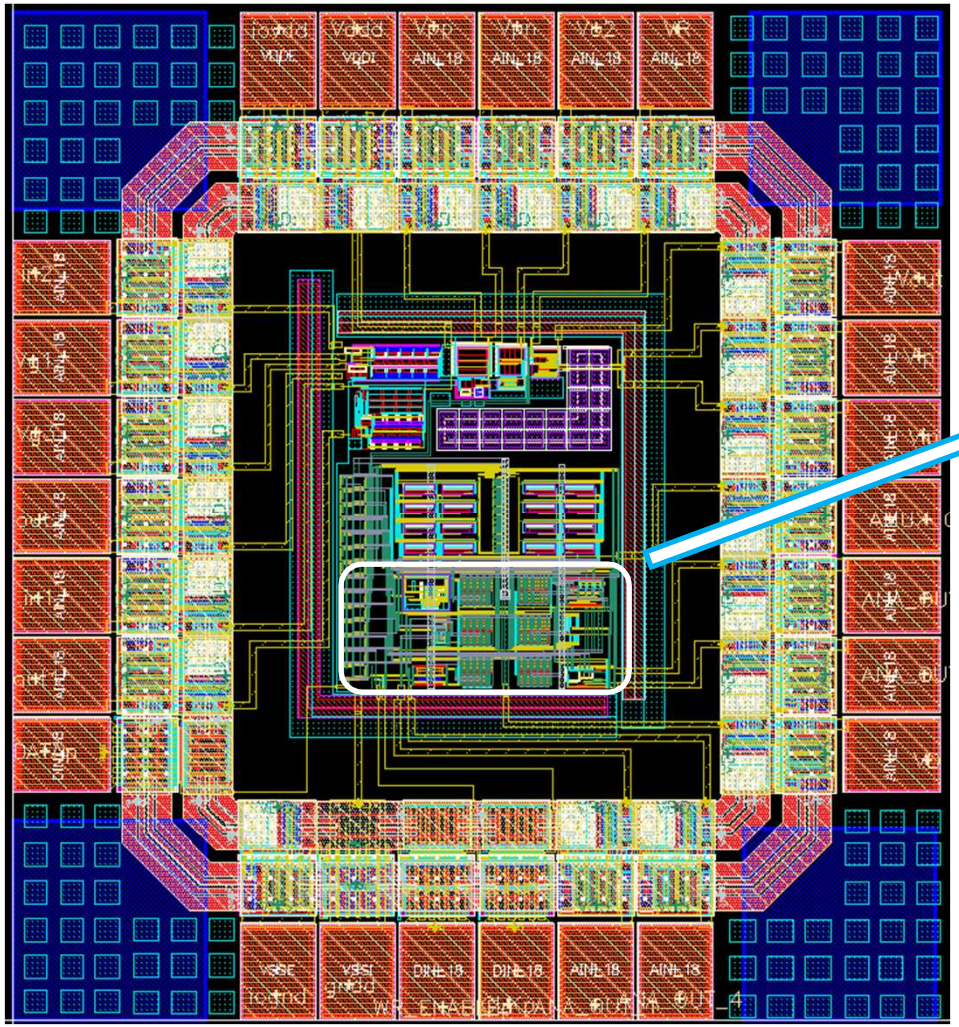
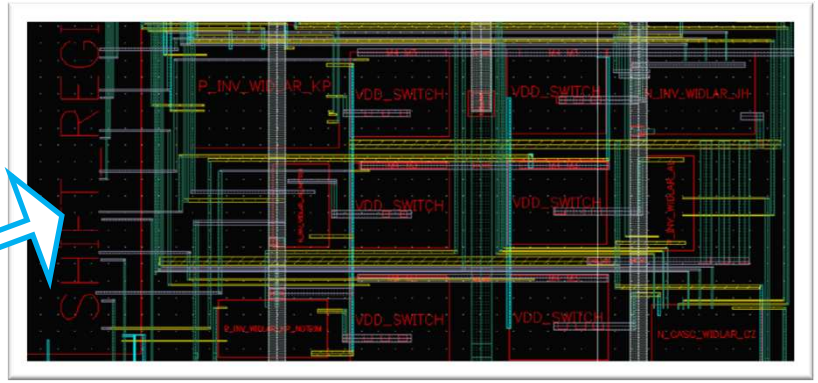
- Summary

# Test Chip Layout

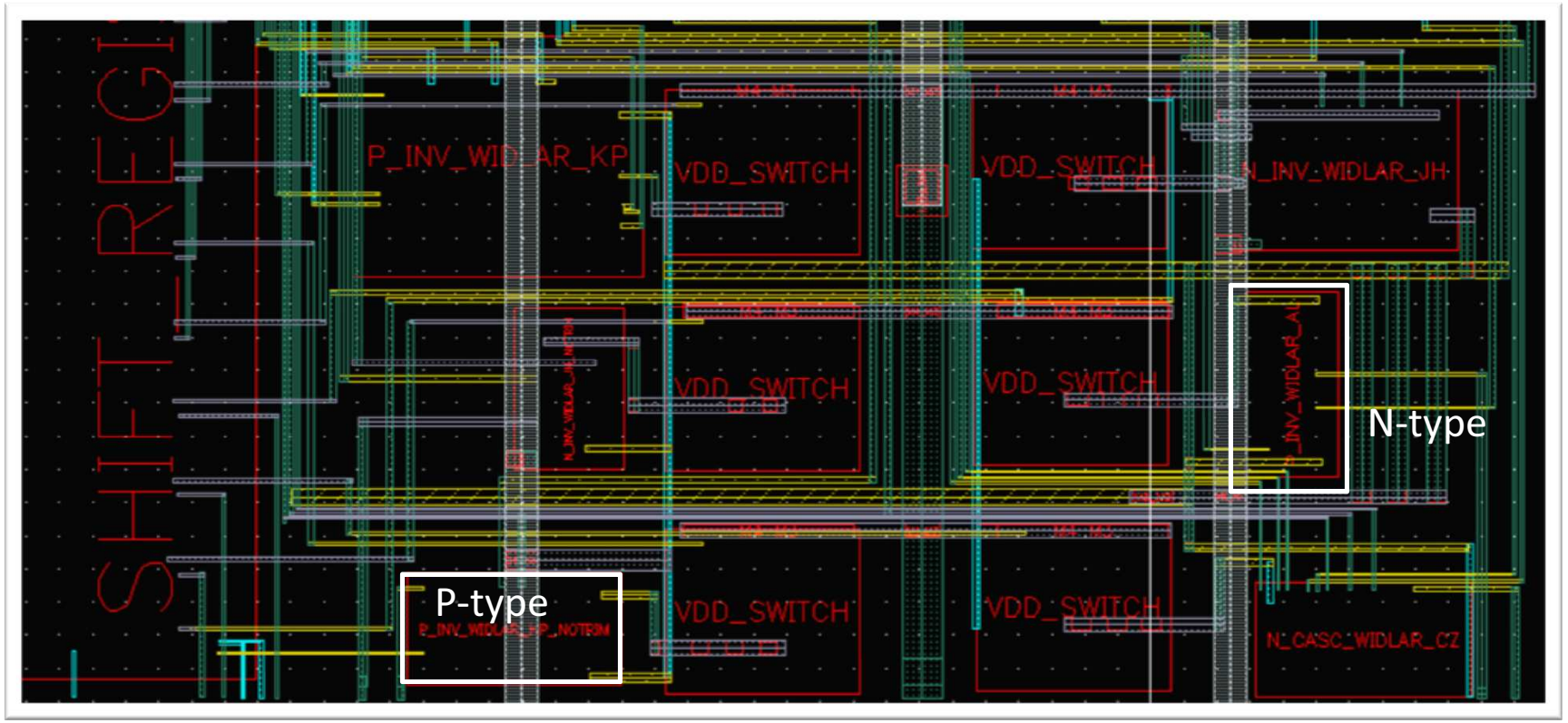
Area:825um*759um (PADs are included)



0.18u CMOS Process

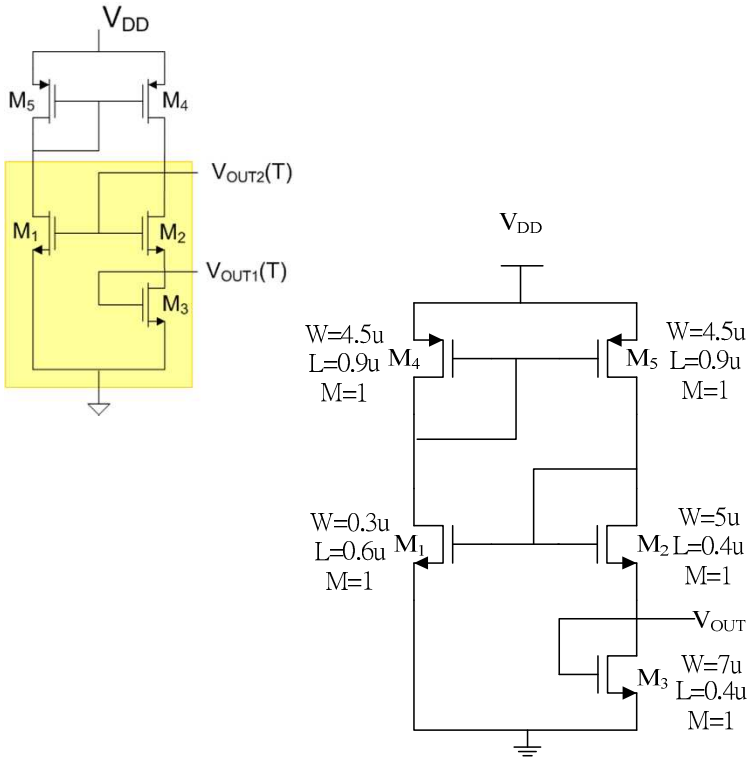


# Different Temperature Sensors on the Die

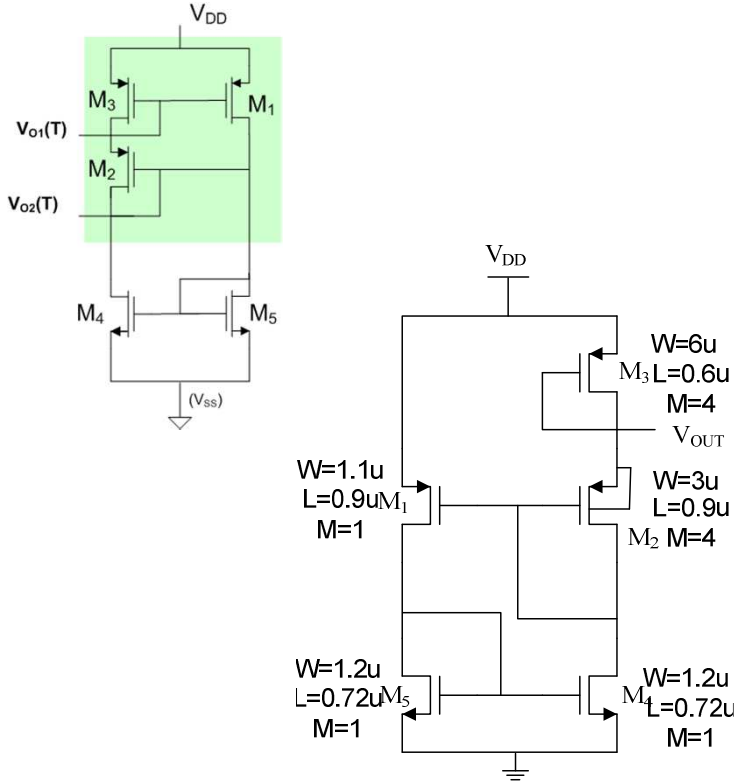



| Circuit | P-type | N-type |
|---|---|---|
| Area(um$^2$) | 24*14.4 | 12*25.5 |

# Test Temperature Sensor Circuits



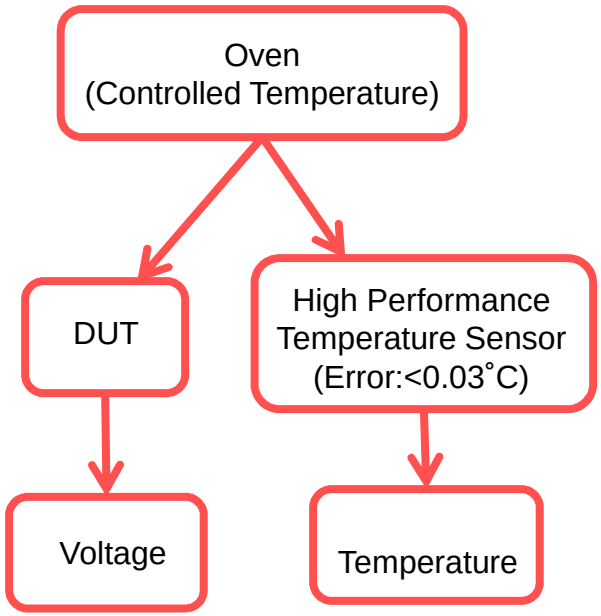

N-type: (NTC)



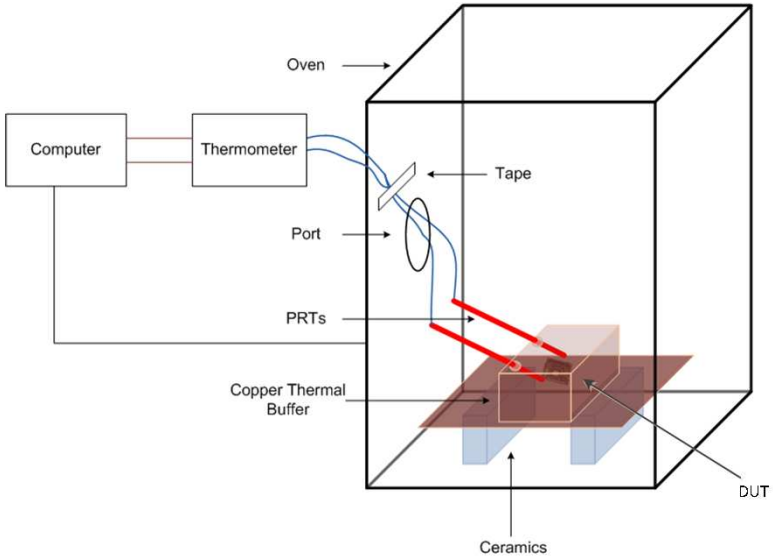

P-type: (PTC)

# Measurement Strategy

- Using high performance platinum RTD temperature sensor as reference




- Testing configuration



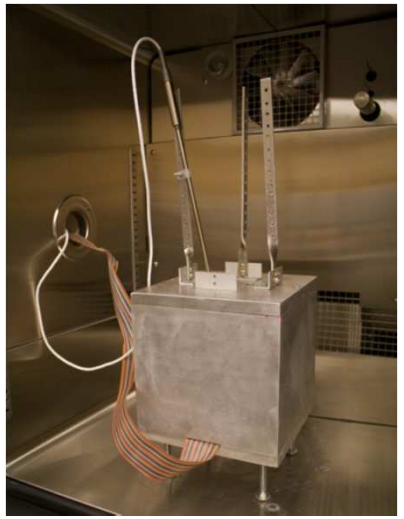
# Measurement Equipment

1. Oven:  ESPEC BTL-433
   - Thermal controller : Watlow F4 connected with computer by RS-232.
   - Temperature range : -20℃ to 180℃
   - ±0.5℃ fluctuation at control sensor after stabilization
   - Temperature cycling rate :
     - 1.5℃/m heating
     - 2℃/m cooling


# Measurement Equipment

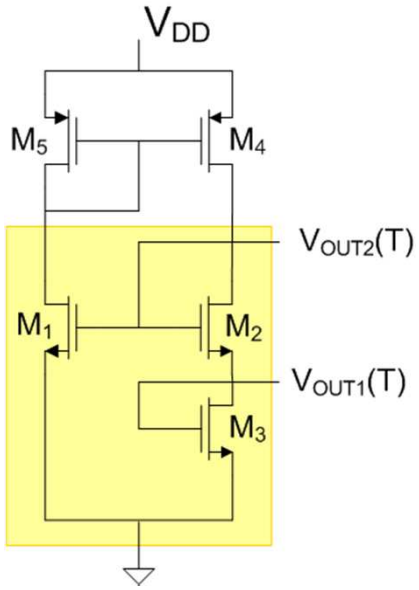
2. Thermometer:
   - F200 thermometer
   - T100-250-18 Platinum Resistance Thermometer

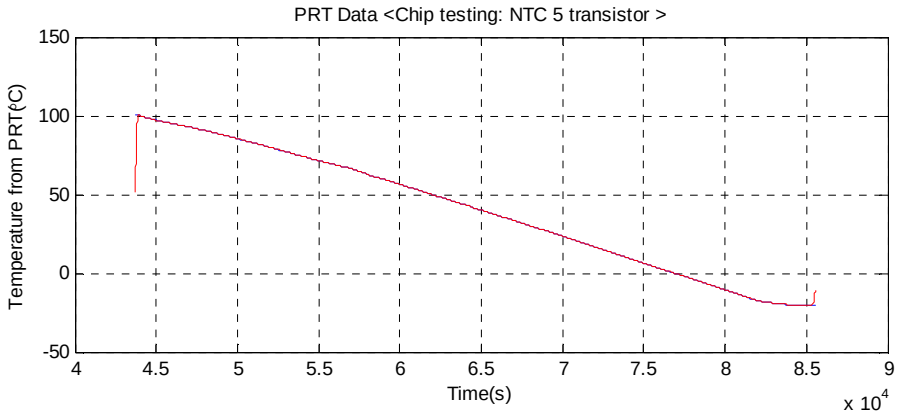

3. Thermal Buffer
   - Achieve Thermal equilibrium

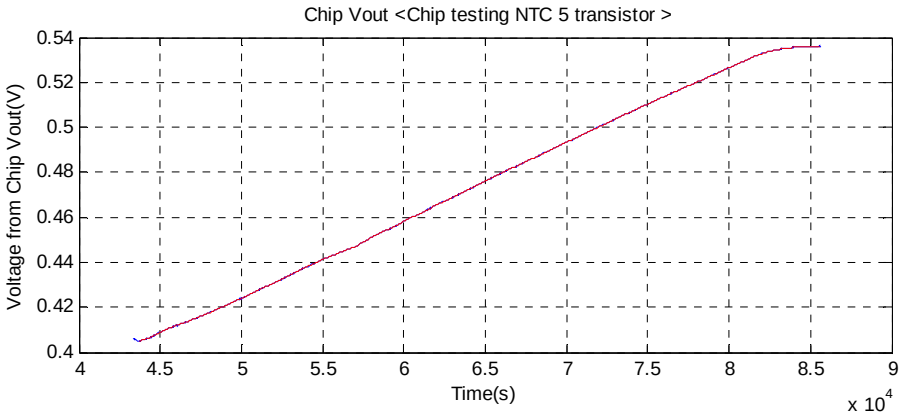


# Measurement Results

- N-type 5-transistor temperature sensor

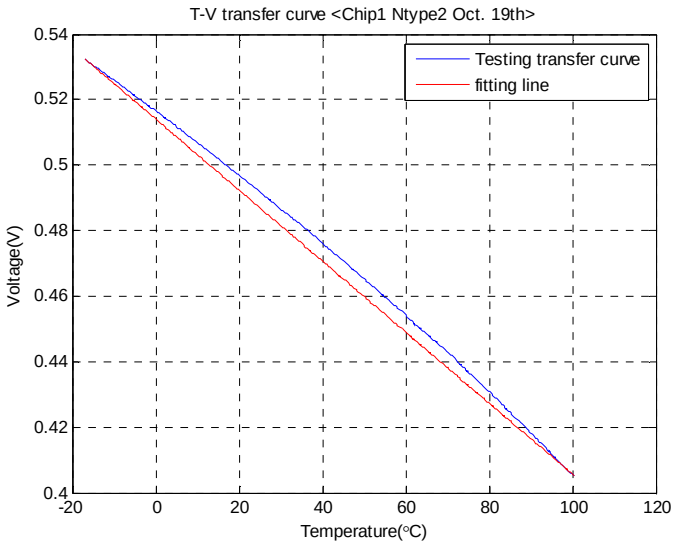


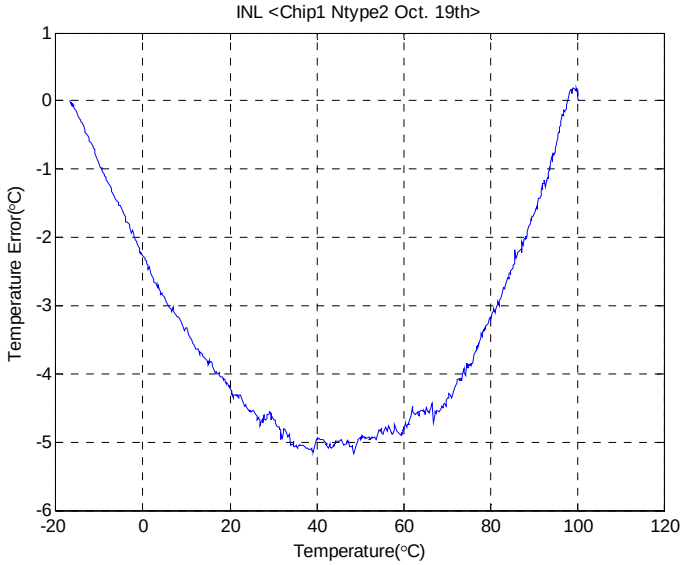




12-hour slow ramp test

# Measurement Results

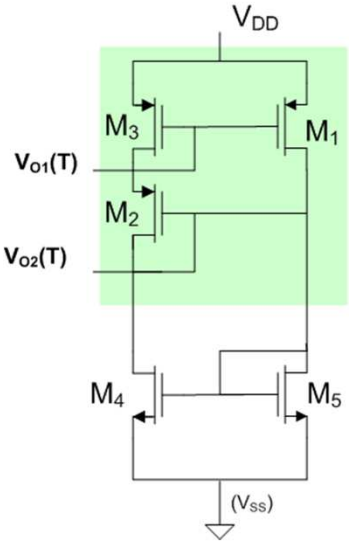


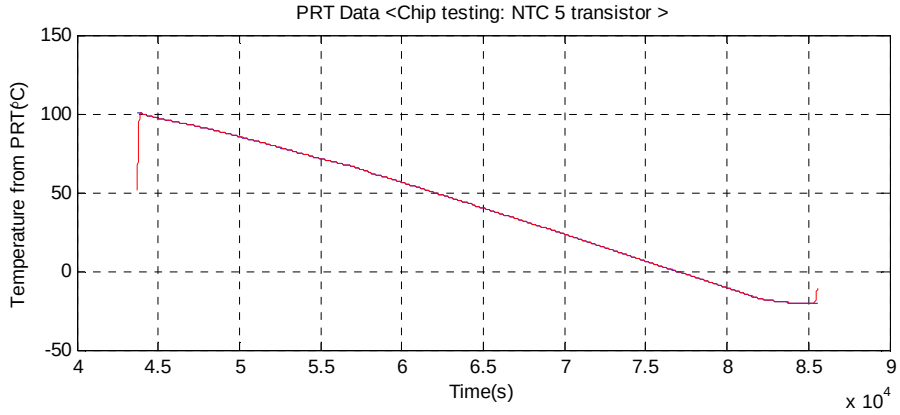



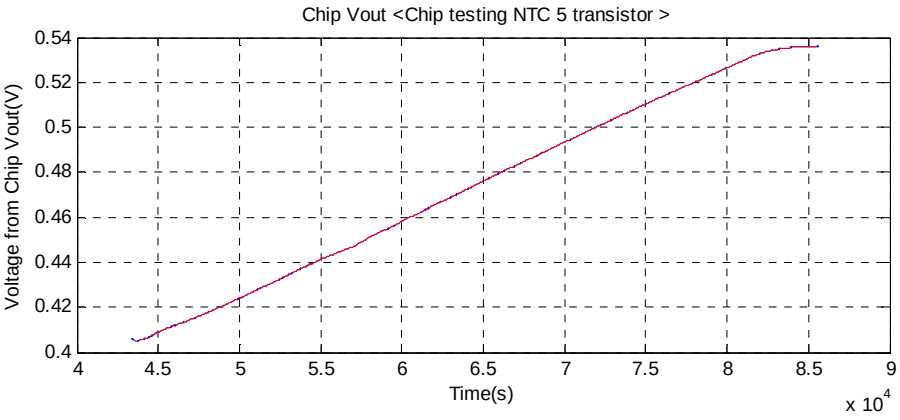

- End-point fitting line shows ± 2.5C linearity error in the measurement results over 120°C range
- Much lower error (100mK) over 30°C range needed for power/thermal management
- Much less linear than simulation results predict but still very useful
- Difference between measurement and simulation attributable to thermal model of $V_T$ used in PDK

# Measurement Results

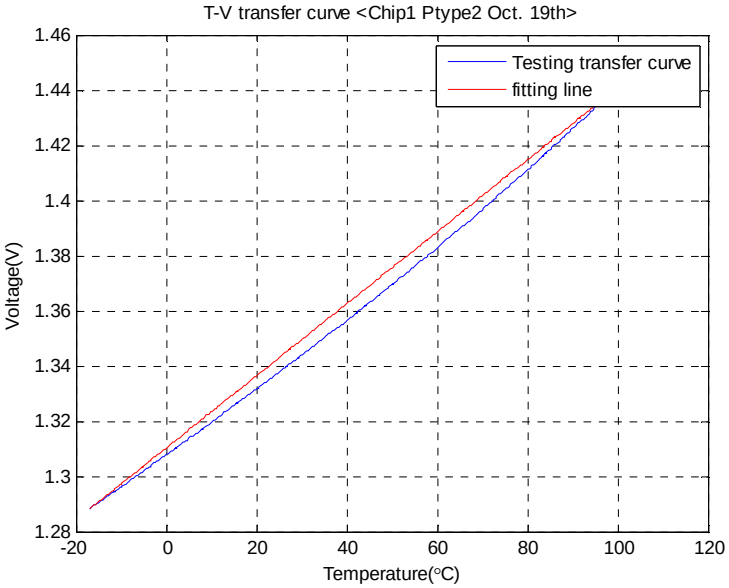
- P-type 5-transistor temperature sensor

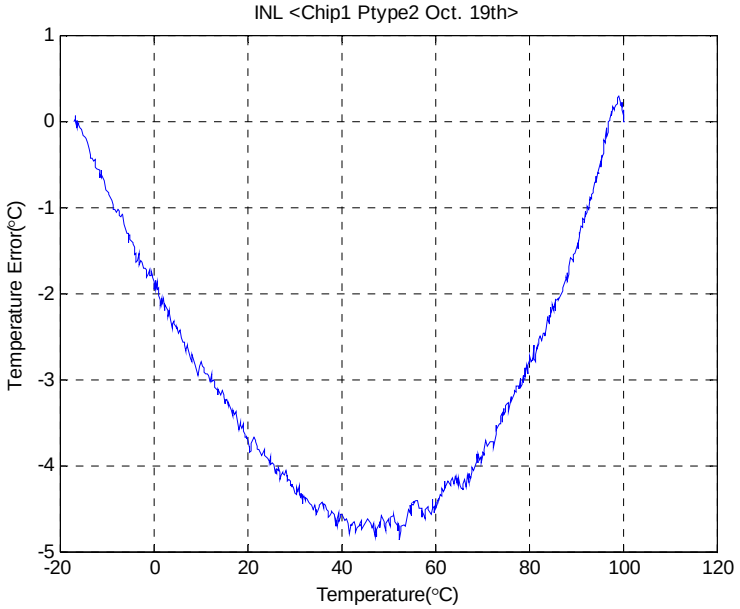


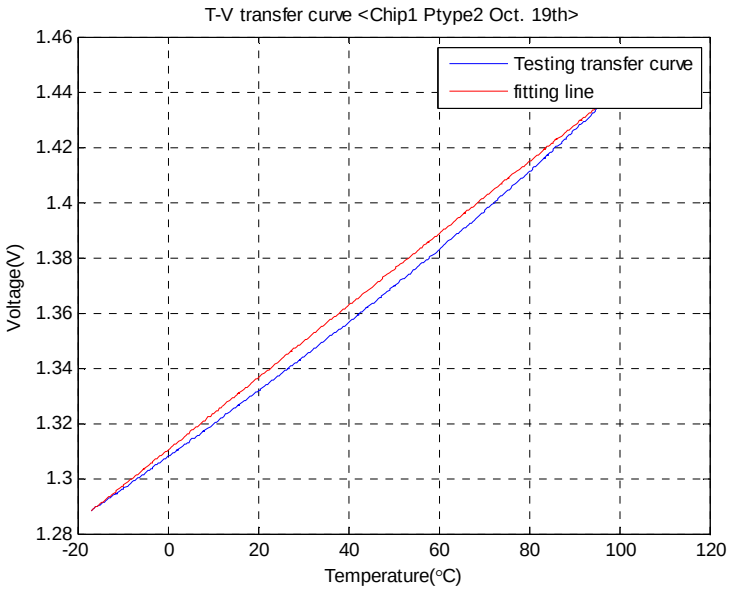
# Measurement Results

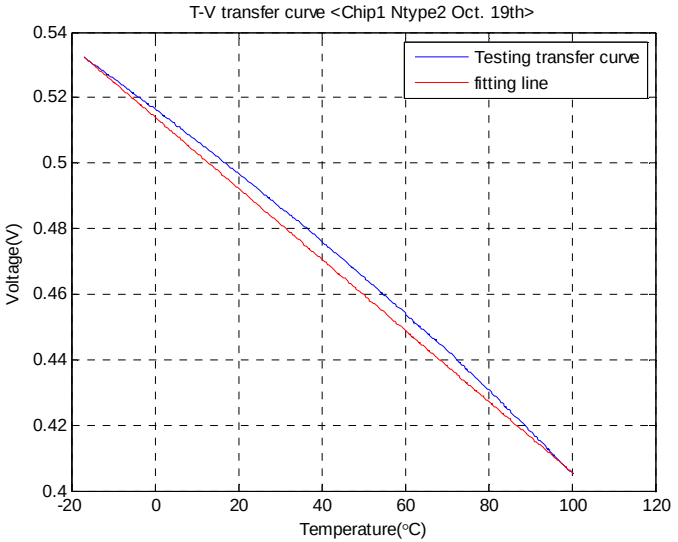



- End-point fitting line shows $\pm$ 2.4C linearity error in the measurement results over 120°C range
- Much lower error over 30°C range needed for power/thermal management
- Much less linear than simulation results predict but still very useful
- Difference between measurement and simulation attributable to thermal model of $V_T$ used in PDK

# Measurement Results




Similar nonlinearity was measured for several other temperature sensors as well !

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# 2nd Order TC

- In the BSIM3 model, the temperature dependence of the threshold voltage of MOS devices is modeled as

$$V_{th}(T) = V_{th}(TNOM) + \left( KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff} \right) \cdot \left( \frac{T}{TNOM} - 1 \right)$$

KT1 is the temperature coefficient

KT1L is the channel length dependence of the temperature coefficient

KT2 is the body-bias coefficient of threshold voltage temperature effect

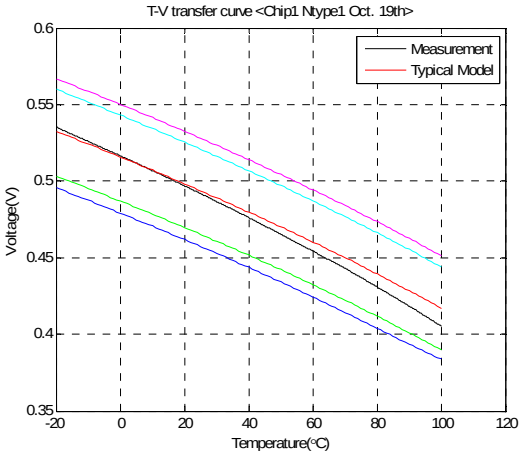
**This is linear in T**

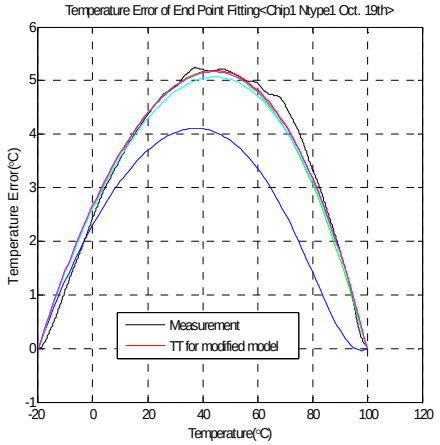
- Second-order temperature coefficient added to BSIM model

$$KT1 = \alpha \left( \frac{T}{Tnom} - 1 \right) - KT10$$

# 2nd Order TC

Simulation results with second-order model for N-Type sensor




$$\text{NMOS: } KT1 = -9.2 \times 10^{-3} \cdot \left(\frac{Temp}{Tnom} - 1\right) - KT1O_n$$

$$\text{PMOS: } KT1 = -9.8 \times 10^{-3} \cdot \left(\frac{Temp}{Tnom} - 1\right) - KT1O_p$$

- Inclusion of the second-order TC provides good agreement between simulation and measured results
- Have been unable to get information from industry on modeling second-order temperature effects of threshold voltage
- Have redesigned sensor to reduce second-order temperatue dependance but no experimental results yet

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# CMOS Temp Sensors with Improved Head Room

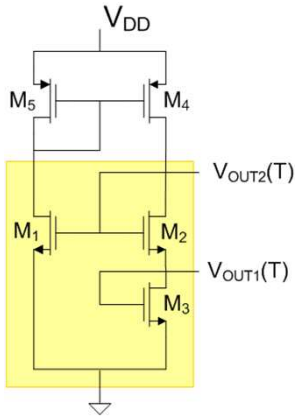
Headroom Requirements to Accommodate for Process and Temperature Variations:

$$HR > s_{V_{Tn}}^{V_o} \times \left( \Delta V_{Tn\ Proc} + \Delta V_{Tn\ temp} \right)$$

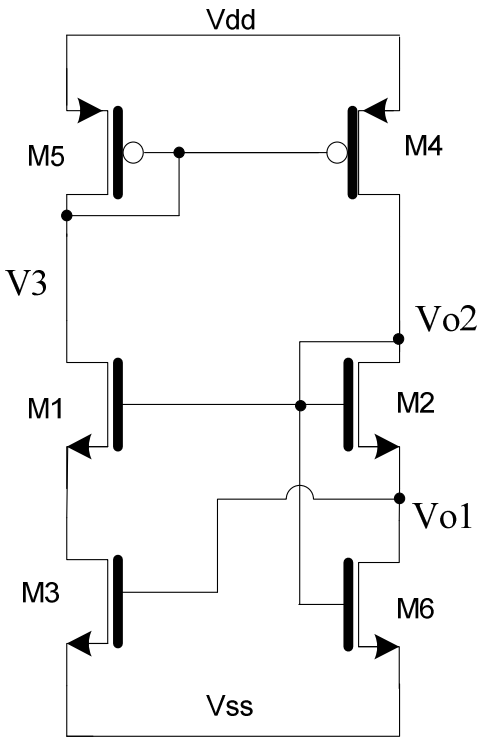
Inverse Widlar Sensor does not have enough headroom at low $V_{DD}$ ($.9V_{DDNOM}$) at the SN,SP process corner

Cascoding is not possible to reduce $V_{DD}$ sensitivity

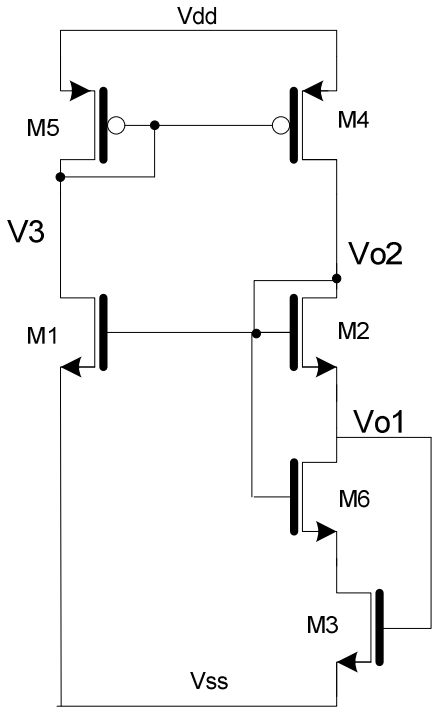
# CMOS Temp Sensors with Improved Head Room




Circuit A




Circuit B

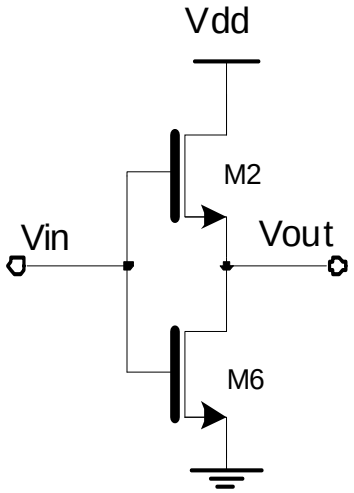



Circuit C

(start-up circuits not shown)

# CMOS Temp Sensors with Improved Head Room

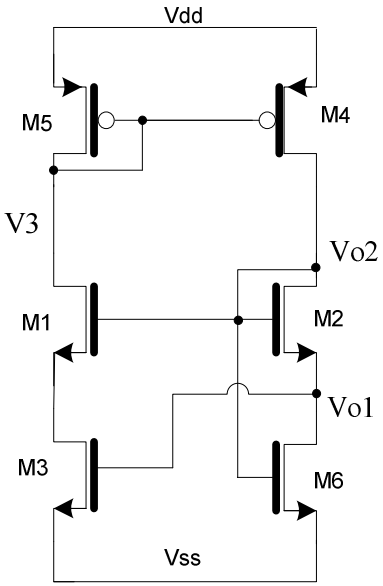
Both improved HR circuits incorporate active attenuator.




$$V_{out} = \theta \left( V_{in} - V_{Tn} \right)$$

For appropriate design, $V_{EB2}$ is very small
Voltage drop from Vin to Vout is approximately $V_{Tn}$.

# Proposed Work 1--- Circuit B




Circuit B

$$V_{o1}=\frac{1}{1-\sqrt{\frac{(W/L)_2}{(W/L)_3}}\left(\frac{1}{\theta}-1\right)}\times V_{Tn3}$$

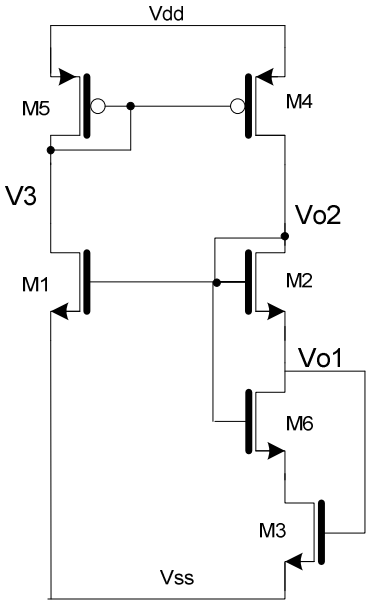
$$V_{o2}=\frac{1}{\theta-\sqrt{\frac{(W/L)_2}{(W/L)_3}}(1-\theta)}\times V_{Tn3}+V_{Tn2}$$

At low $V_{DD}$

$$0.9V_{DD\,nom}-(2V_{Tn}+2V_{EB})>\left|HR\right|$$

- Output is linear with $V_{Tn}$, (thus linear with temperature)
- Output voltage is $V_{DD}$ independent
- HR constraint reduced by $V_{EB}$ with attenuator
- Low current consumption and small area

# CMOS Temp Sensors with Improved Head Room




Circuit C

(17)

$$V_{01}=\frac{[(1-\theta)\sqrt{\frac{(W/L)_3}{W_2/(L_2+L_6)}}-\sqrt{\frac{(W/L)_3}{(W/L)_1}}]\times V_{Tn3}+(V_{Tn1}-V_{Tn2})}{(1-\theta)\sqrt{\frac{(W/L)_3}{W_2/(L_2+L_6)}}-\sqrt{\frac{(W/L)_3}{(W/L)_1}}+1}$$

$$V_{02}=\frac{V_{01}-V_{Tn3}}{\sqrt{\frac{(W/L)_1}{(W/L)_3}}}+V_{Tn1}$$

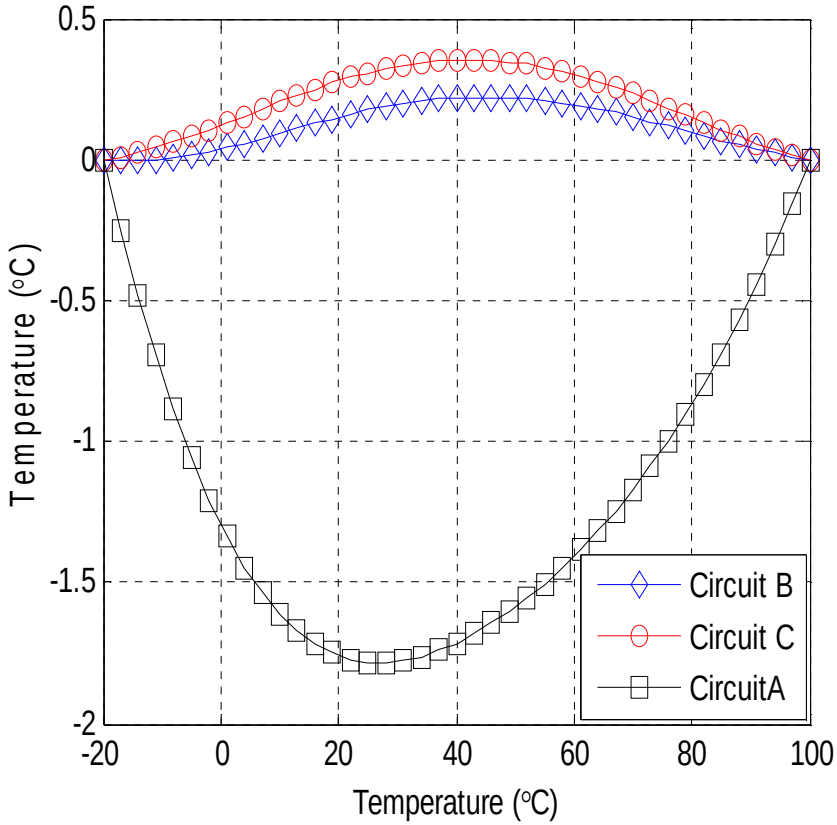
At low $V_{DD}$

$$0.9V_{DD\,nom}-(2V_{Tn}+2V_{EB})>|HR|$$

- Output is linear with $V_{Tn}$, (thus linear with temperature)
- Output voltage is $V_{DD}$ independent
- HR constraint reduced by $V_{EB}$ with attenuator
- Low current consumption and small area

# Simulation Results at Slow n Corner at Low $V_{DD}$

Simulations at $0.9*V_{DD\ Nom}$ at slow n corner




Circuits B and C maintain temperature error within 80mK while Circuit A has more than 900mK temperature error

# Simulation Results Summary

| *Parameters* | *Performance of Circuit B* | *Performance of Circuit C* |
|---|---|---|
| Process | 0.18 μm | 0.18 μm |
| Temperature Range | -20°C~100°C | -20°C~100°C |
| Maximum Temp Error at typical condition | 0.23°C | 0.1°C |
| Maximum Temp Error at worst condition | 0.38°C | 0.65°C |
| Total area | 270 $\mu m^2$ | 185 $\mu m^2$ |
| Output Voltage Coefficient | -2.39 mV/°C | -2.11 mV/°C |
| Power consumption | 95μW | 65μW |

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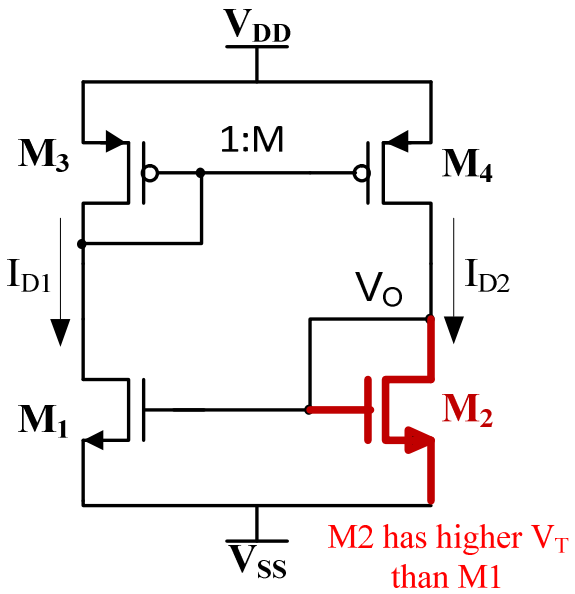
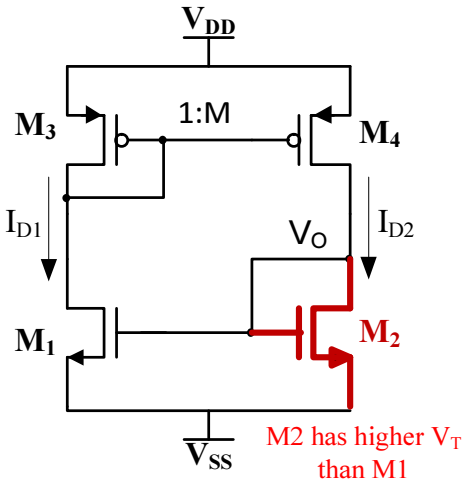
# Low voltage dual-threshold temperature sensor

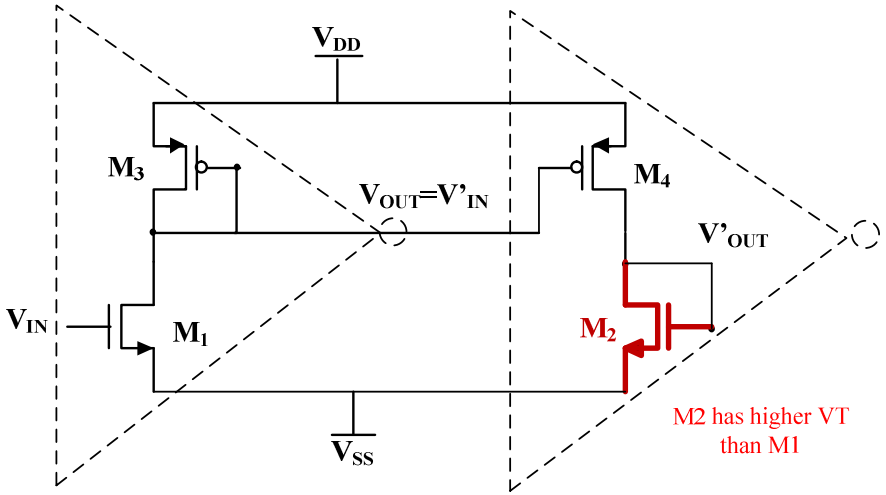



$$V_O = \frac{\sqrt{W_1/L_1}}{\left(\sqrt{W_1/L_1} - \sqrt{M\,W_2/L_2}\right)} V_{Tn1} - \frac{\sqrt{M\,W_2/L_2}}{\left(\sqrt{W_1/L_1} - \sqrt{M\,W_2/L_2}\right)} V_{Tn2}$$

Enough headroom for full cascoding even with low supply voltages!

# Low voltage dual-threshold temperature sensor

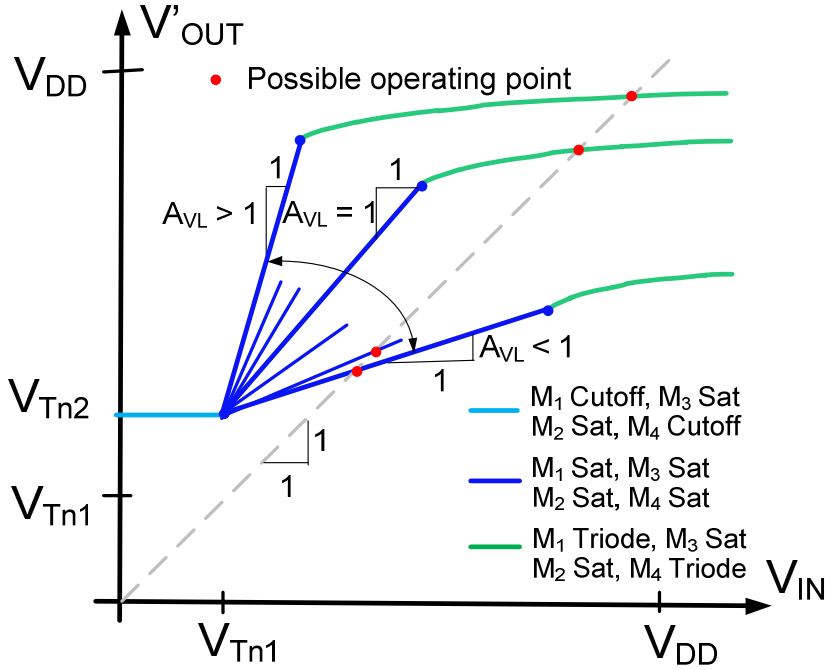



- Can be viewed as 2-cascaded inverters in a loop
- Must have single operating point with all devices in saturation to obtain $V_{DD}$ insensitivity

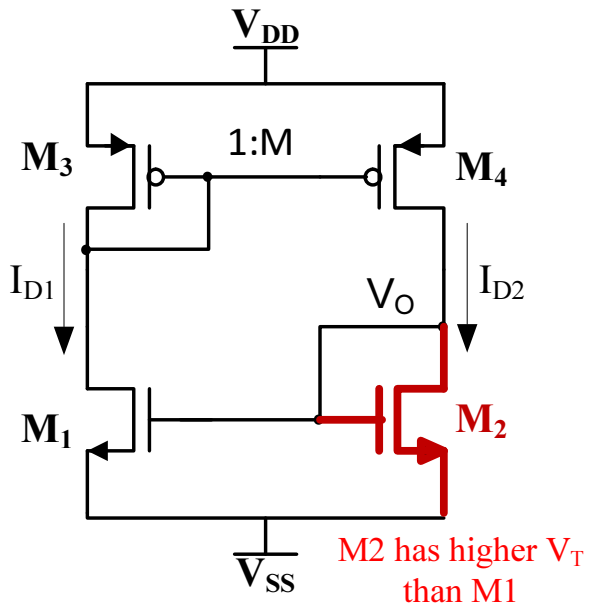
# Low voltage dual-threshold temperature sensor

Basic Operation:




If $V_{Tn2} > V_{Tn1}$ will have a single stable equilibrium point (requires no startup)
If $A_{VL}<1$, all devices will be operating in saturation
It $V_{Tn1}>V_{Tn2}$, will not operate as a $V_{DD}$-independent temperature sensor

# Low voltage dual-threshold temperature sensor




- Circuit has been designed in a 65nm process and is in fabrication
- Simulation results suggest INL well under 0.5°C over temperature range needed for power management
- Can not discuss simulation results at this time

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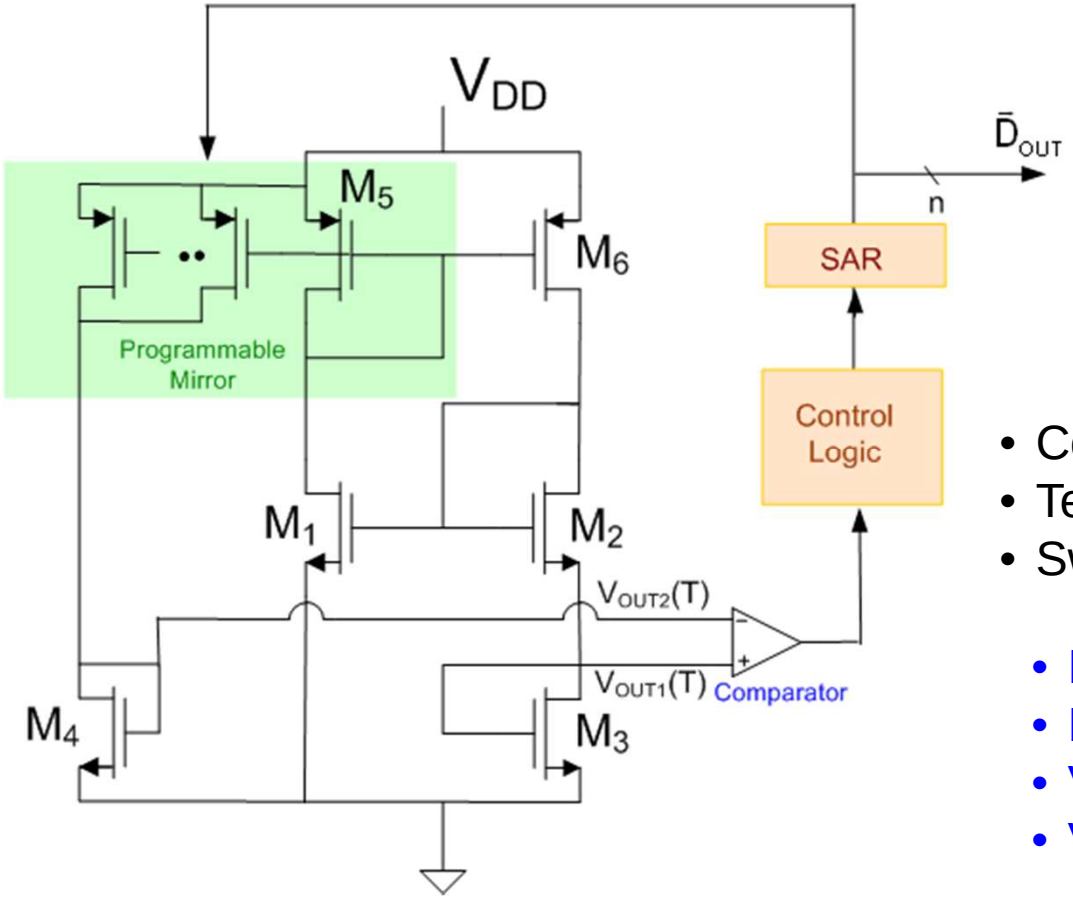
# Direct Temp to Digital Converter

One implementation to demonstrate concept



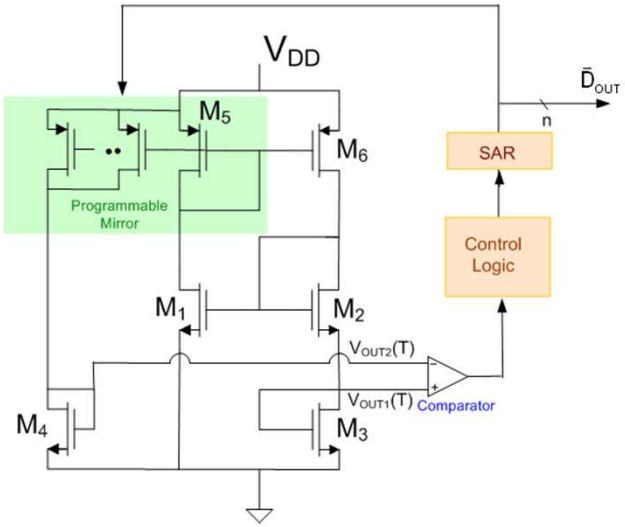

- Control logic forces $V_{OUT1}=V_{OUT2}$
- Temperature encoded in $D_{OUT}$
- Switches on mirror not shown

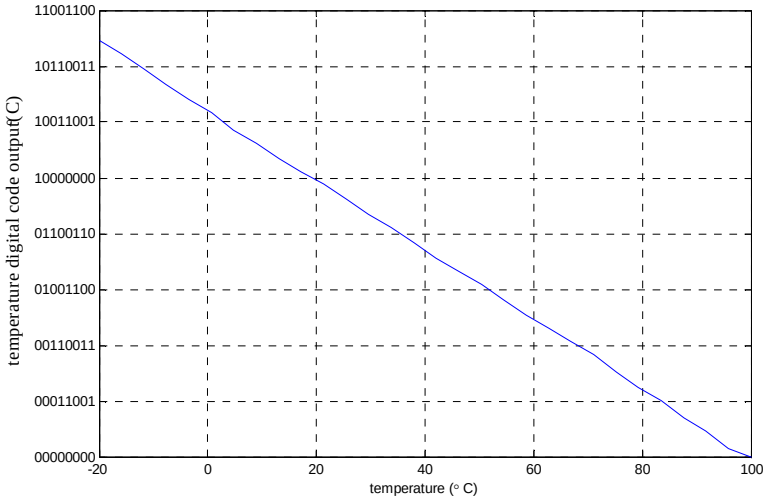
  - No ADC (just SAR register)
  - No $V_{REF}$ or $I_{REF}$
  - Very simple logic
  - Very low power

# Direct Temp to Digital Converter

One implementation to demonstrate concept

Simulation results – TSMC 0.18u with 2nd order model



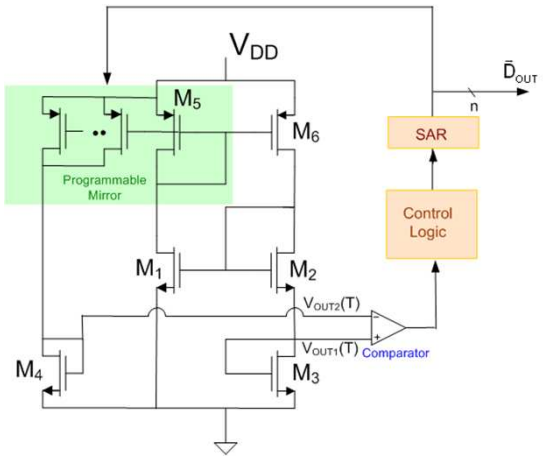



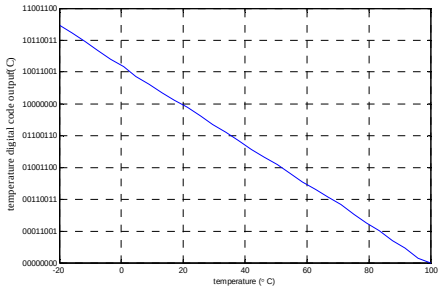

Output code varies linearly with T

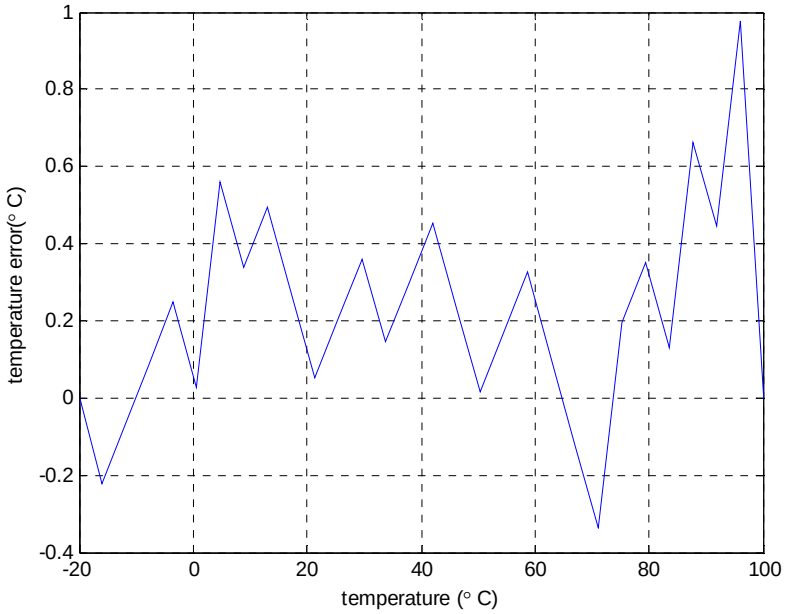
# Direct Temp to Digital Converter

One implementation to demonstrate concept

Simulation results – TSMC 0.18u with 2nd order model




INL bound by 1°C

# Outline

- Review of Temperature Sensor Approaches
- Goal and Motivation
- Inverse Widlar Temperature Sensor
  - Description
  - Measured Results
- Second-Order Temperature Dependence to $V_T$
- Temperature Sensor with Improved Headroom
- Four-Transistor Dual-$V_T$ Temperature Sensor
- Temperature to Digital Converter
- Summary

# Summary

Many different approaches have been proposed for building integrated temperature sensors but limited results have been reported that fairly compare the different approaches

Temperature sensors based upon the temperature dependence of the threshold offer potential for implementation of low-power low-area accurate temperature sensors

Improved models for temperature  higher-order temperature dependence of threshold voltage would be quite useful

New method of designing temperature sensor that does not require either a stable reference or an ADC was introduced.

Thank you for your attention !