Extending HyperTransport™ Technology to 8.0 Gb/s in 32-nm SOI-CMOS Processors

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Advanced Micro Devices, Inc.
Motivation

- High demand for multi-socket processor systems from explosive growth in server market
  - Cores per die increasing faster than I/O capability
  - Server performance increasingly limited by I/O bandwidth between sockets
- I/O technology shifts (e.g., PCIe-3) revolutionary in architecture & design, introduces product risk
- Evolutionary enhancements to existing I/O design can improve server system performance without revolutionary shifts
Evolution of AMD Server Processors

- **Shanghai**
  - 45nm
  - 4 cores & 4 HT I/O

- **Magny Cours**
  - 45nm
  - 6 cores & 4 HT I/O

- **Orochi**
  - 32nm
  - 8 cores & 4 HT I/O

**GOAL:** 6.4Gb/s $\rightarrow$ 8.0Gb/s through modest improvements with jitter ↓, return loss ↓ & constant power

+25% I/O aggregate BW $\rightarrow$ up to +8% system performance !!
Outline

- Motivation
- HyperTransport™ Overview
- Extending HT to 8Gb/s
  - Forwarded Clock Jitter Filtering
  - Wideband Digital Clean-Up PLL
  - Power & Performance Optimization
- Silicon Results
- Conclusion
Outline

- Motivation
- **HyperTransport™ Overview**
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Processor-to-Processor Link

100Ω Differential Channels

Cores
Cache Memory
DDR Port
Embedded NorthBridge (NB)

HT Port
PLL
CDR

200MHz SSC
Forwarded Clock
Data

Cores
Cache Memory
DDR Port
Embedded NorthBridge (NB)
HT Link Characteristics

- Source synchronous
  - Forward half-rate clock for RX data retiming
  - Common-mode jitter rejection, low latency
- NRZ PAM-2 signaling
- 2.4 to 6.4Gb/s per lane
- 2 sublinks of 1 CLK lane + 9 data lanes
- DLL-based CDR
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Jitter in Forwarded Clock Links

TX

Data In

\(TJ_{tx}\)

PLL

Data Lane

Forwarded Clock Lane

RX

Data Out

DATA

CLK

CDR
Jitter in Forwarded Clock Links

\[ TJ_{tx} = \tau_c + \tau_{rx} \]

\[ TJ_{tx} = \tau_c + \tau_{rx} + \tau_{dis} + \tau_{cdr} \]
\[ \phi_{data}(t) = 2\pi f_c t + A_m \sin(2\pi f_m t) \]

\[ \phi_{data}(t) - \phi_{clock}(t) \]

\[ \phi_{clock}(t) = \phi_{data}(t - \tau) \]
Sampling Jitter vs. Delay Mismatch

\[ J_{\text{sample}} = 2 \cdot |\sin(\pi f_m \tau)| \]

\( \tau = 0 \)

Jitter Transfer (dB)

Jitter Modulation Frequency, \( f_m \) (MHz)
Sampling Jitter vs. Delay Mismatch

\[ J_{\text{sample}} = 2 \cdot \left| \sin(\pi f_m \tau) \right| \]

\[ \tau = 160 \text{ps} \]

Jitter Modulation Frequency, \( f_m \) (MHz)

Jitter Transfer (dB)

jitter amplification
Sampling Jitter vs. Delay Mismatch

\[ J_{\text{sample}} = 2 \cdot \left| \sin(\pi f_m \tau) \right| \]

\( \tau = 5.0 \text{ns} \)

jitter amplification

Jitter Transfer (dB)

Jitter Modulation Frequency, \( f_m \) (MHz)

\( \tau = 5.0 \text{ns} \)
Desired Jitter Filtering Behavior

\[ f_m < \frac{1}{6\tau} \]

\[ \phi_{data}(t) = \phi_{clock}(t) + 2\pi f_c \tau \]

- No sampling jitter

\[ f_m \geq \frac{1}{6\tau} \]

Doubling of sampling jitter
Desired Jitter Filtering Behavior

\[ f_m < \frac{1}{6\tau} \]

\[ \phi_{data}(t) = \phi_{clock}(t) + 2\pi f_c \tau \]

- **Phase, \( \phi \)**
- **Time, \( t \)**

- **No sampling jitter**
- **Sampling jitter transfer bounded to unity**
Jitter Filtering Example ($\tau = 2\text{ns}$)

- **Without Jitter Filtering:**
  - 6dB peaks at 250 & 750MHz

- **With Jitter Filtering:**
  - 6dB peaks at 250 & 750MHz
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HT I/O with Clean-Up PLL

Processor 1

Cores
Cache Memory
DDR Port

Embedded NorthBridge (NB)

HT Port

PLL

Clean-Up PLL

CDR

100Ω Differential Channels

Data
Forwarded Clock

200MHz SSC

Processor 2

Cores
Cache Memory
DDR Port

Embedded NorthBridge (NB)

HT Port

PLL

Clean-Up PLL

CDR

Data
Forwarded Clock
Wideband Digital Clean-Up PLL

- Adjustable bandwidth for jitter shaping (200MHz default)
- Variable bang-bang rate ($f_{bb1}$ to $f_{bb1} + f_{bb2}$)
- Coarse frequency calibration to local REFCLK for PVT
- Low loop latency
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TX Output Driver

45nm Hybrid Mode ➔ 32nm Voltage Mode

- Power ↓ 20%
- Return loss & DCD ↓
RX 4:1 Deserializer

Shift Register  Sample/Hold

45nm

B1
B0
A1
A0

32nm  1:2 Deserializers

A1
B1
A0
B0

- Power ↓ 35%, latency ↓
RX Front End

- AC coupling to reduce CLK DCD
- 1-bit speculative (loop-unrolled) DFE
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- HT I/O configured in NB loopback mode
- Test overage of full I/O subsystem
Measured TX Eye – 8Gb/s PRBS-15
RX Eye with Jitter Modulation

inject $0.4 \text{UI}_{pp}$ sinusoidal jitter
Impact of Clean-Up PLL

- $0.4\text{UI}_{\text{pp}}$ jitter amplitude
- Clean-up PLL removes $>300\text{MHz}$ jitter
## Measured Power Consumption

<table>
<thead>
<tr>
<th>SOI-CMOS Technology</th>
<th>Data Rate (Gb/s)</th>
<th>HT I/O Power (W)</th>
<th>ΔPower</th>
<th>Energy Efficiency (pJ/bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>45nm</td>
<td>6.4</td>
<td>1.62</td>
<td>-</td>
<td>14.1</td>
</tr>
<tr>
<td>32nm</td>
<td>6.4</td>
<td>1.40</td>
<td>-13.6%</td>
<td>12.2</td>
</tr>
<tr>
<td></td>
<td>8.0</td>
<td>1.70</td>
<td>+4.9%</td>
<td>11.8</td>
</tr>
</tbody>
</table>

→ 25% higher data rate with only 5% more power
Conclusion

- Achieved higher processor link bandwidth through *evolutionary* enhancements in I/O design
  - 25% boost in lane data rate
  - Sampling jitter reduction with clean-up PLL
  - Near constant power consumption for socket compatibility
- Improves server system performance with minimal product risk
감사합니다

THANK YOU