Extending HyperTransport™ Technology to 8.0 Gb/s in 32-nm SOI-CMOS Processors

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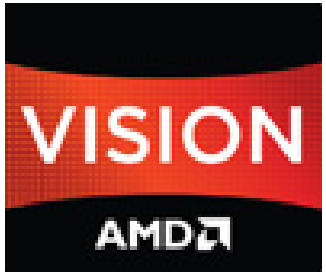
Advanced Micro Devices, Inc.

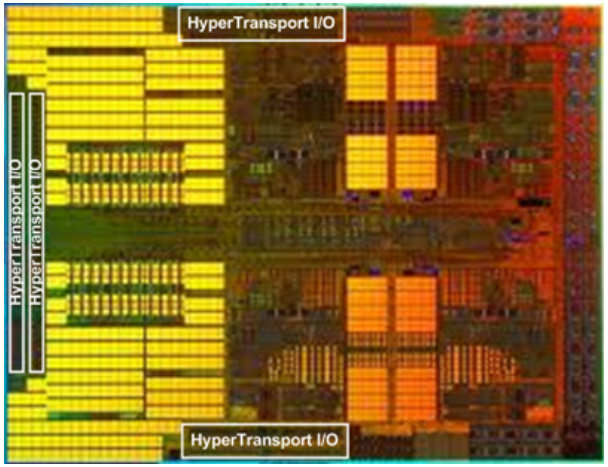


Motivation

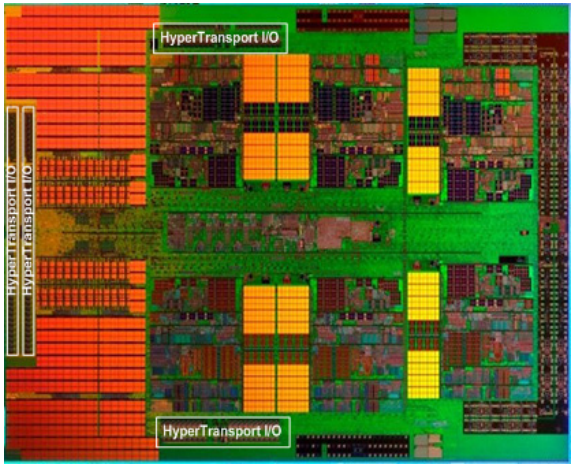
- High demand for multi-socket processor systems from explosive growth in server market
  - Cores per die increasing faster than I/O capability
  - Server performance increasingly limited by I/O bandwidth between sockets
- I/O technology shifts (e.g., PCIe-3) *revolutionary* in architecture & design, introduces product risk
- Evolutionary enhancements to existing I/O design can improve server system performance without revolutionary shifts

Evolution of AMD Server Processors

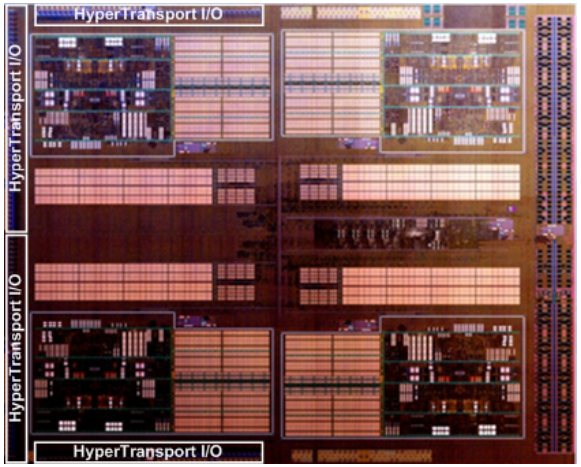
Shanghai
45nm
4 cores & 4 HT I/O



Magny Cours
45nm
6 cores & 4 HT I/O



Orochi
32nm
8 cores & 4 HT I/O



GOAL: **6.4Gb/s → 8.0Gb/s through modest improvements with jitter ↓, return loss ↓ & constant power**

+25% I/O aggregate BW → up to +8% system performance !!

Outline

- Motivation
- HyperTransport™ Overview
- Extending HT to 8Gb/s
  - Forwarded Clock Jitter Filtering
  - Wideband Digital Clean-Up PLL
  - Power & Performance Optimization
- Silicon Results
- Conclusion

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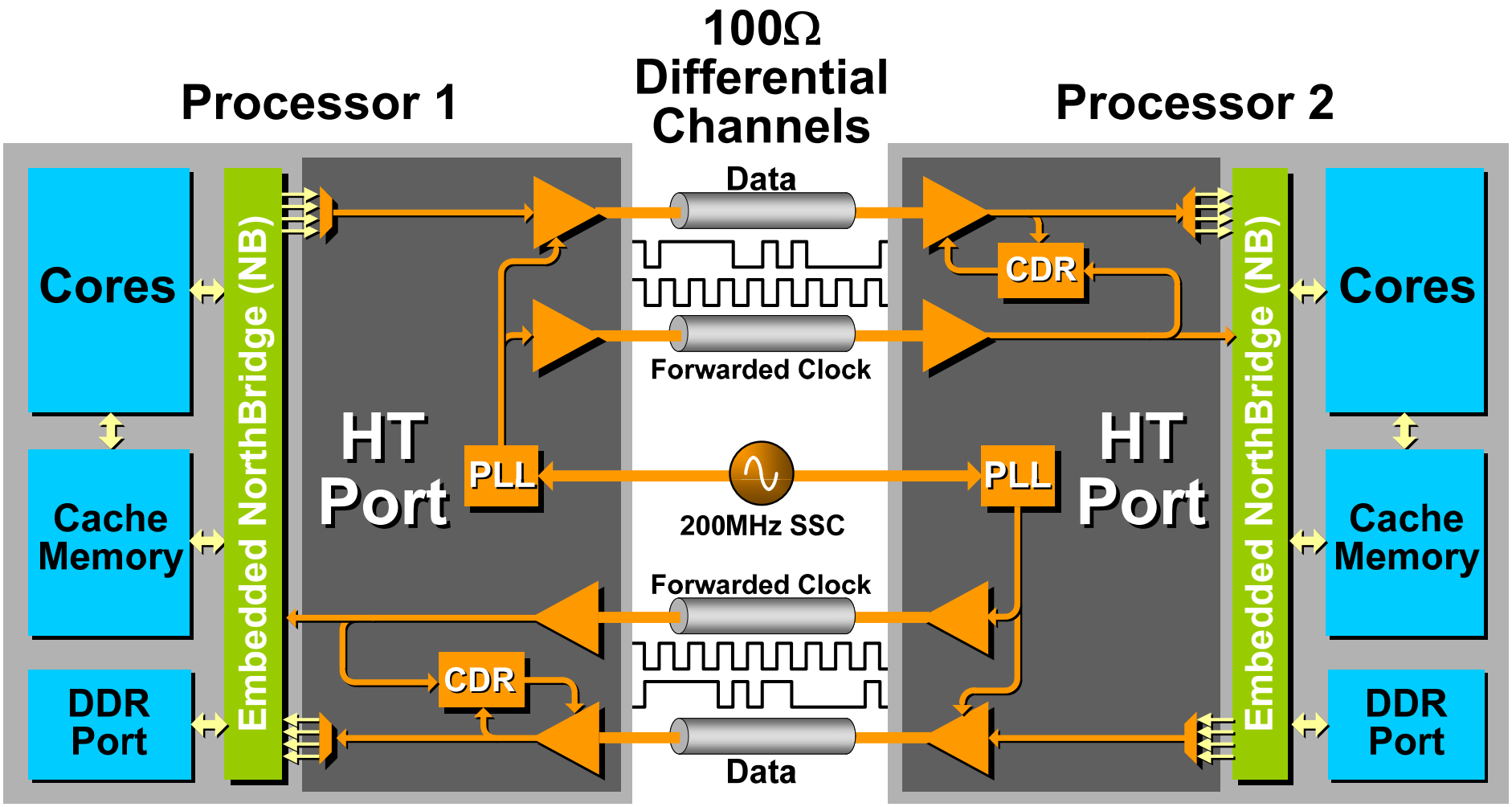
Processor-to-Processor Link



HT Link Characteristics

- Source synchronous
  - Forward half-rate clock for RX data retiming
  - Common-mode jitter rejection, low latency
- NRZ PAM-2 signaling
- 2.4 to 6.4Gb/s per lane
- 2 sublinks of 1 CLK lane + 9 data lanes
- DLL-based CDR

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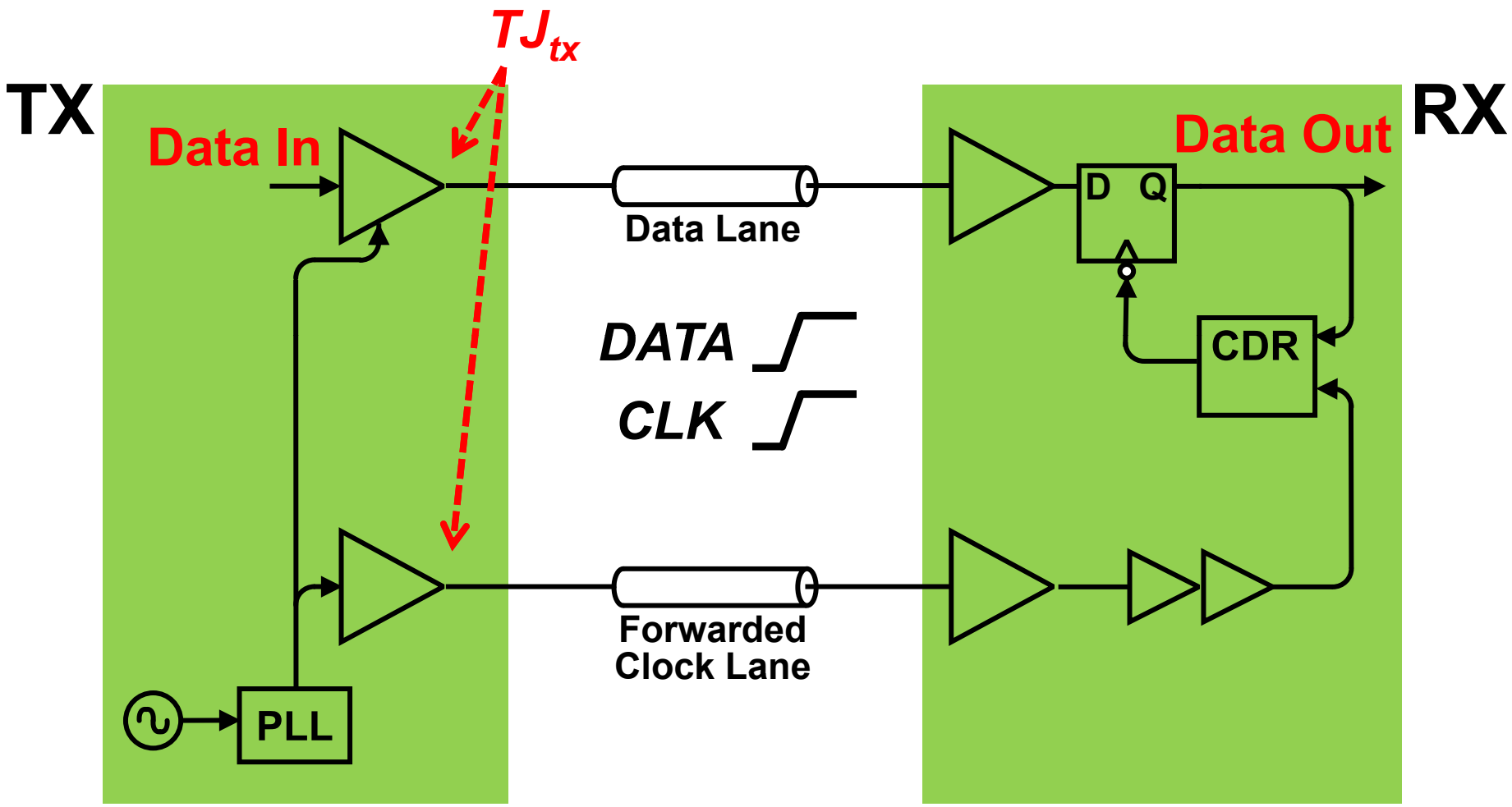
Jitter in Forwarded Clock Links



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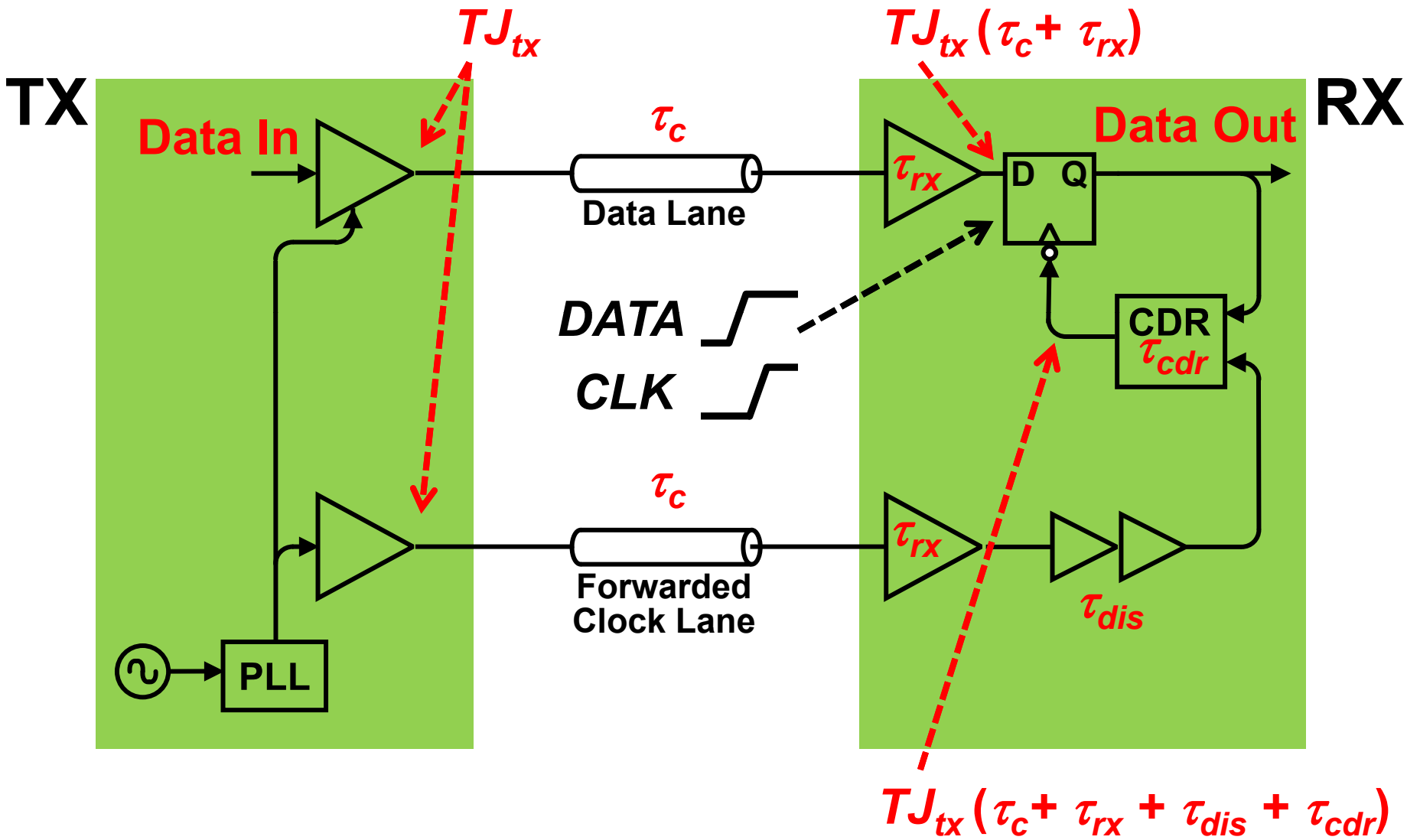
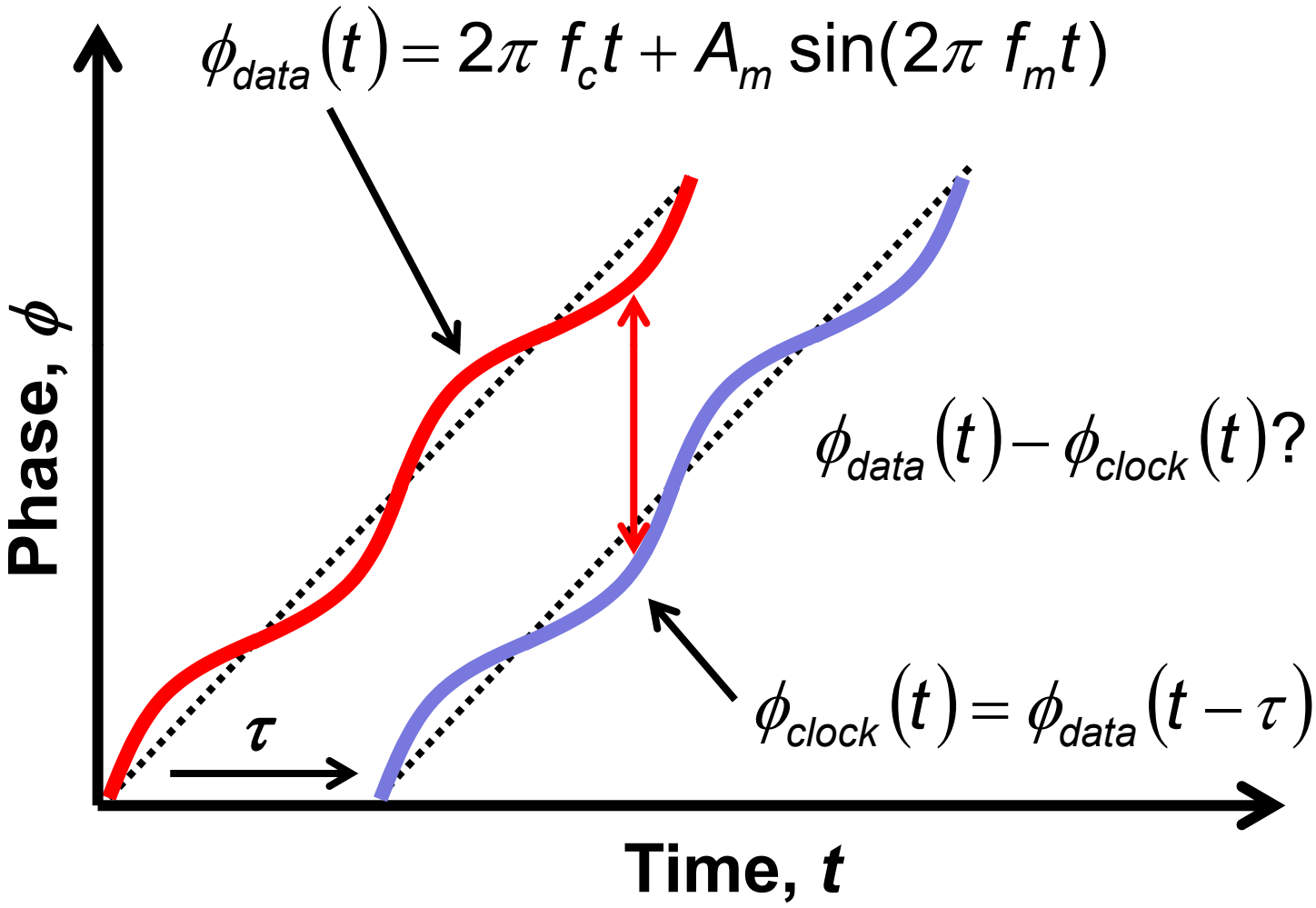
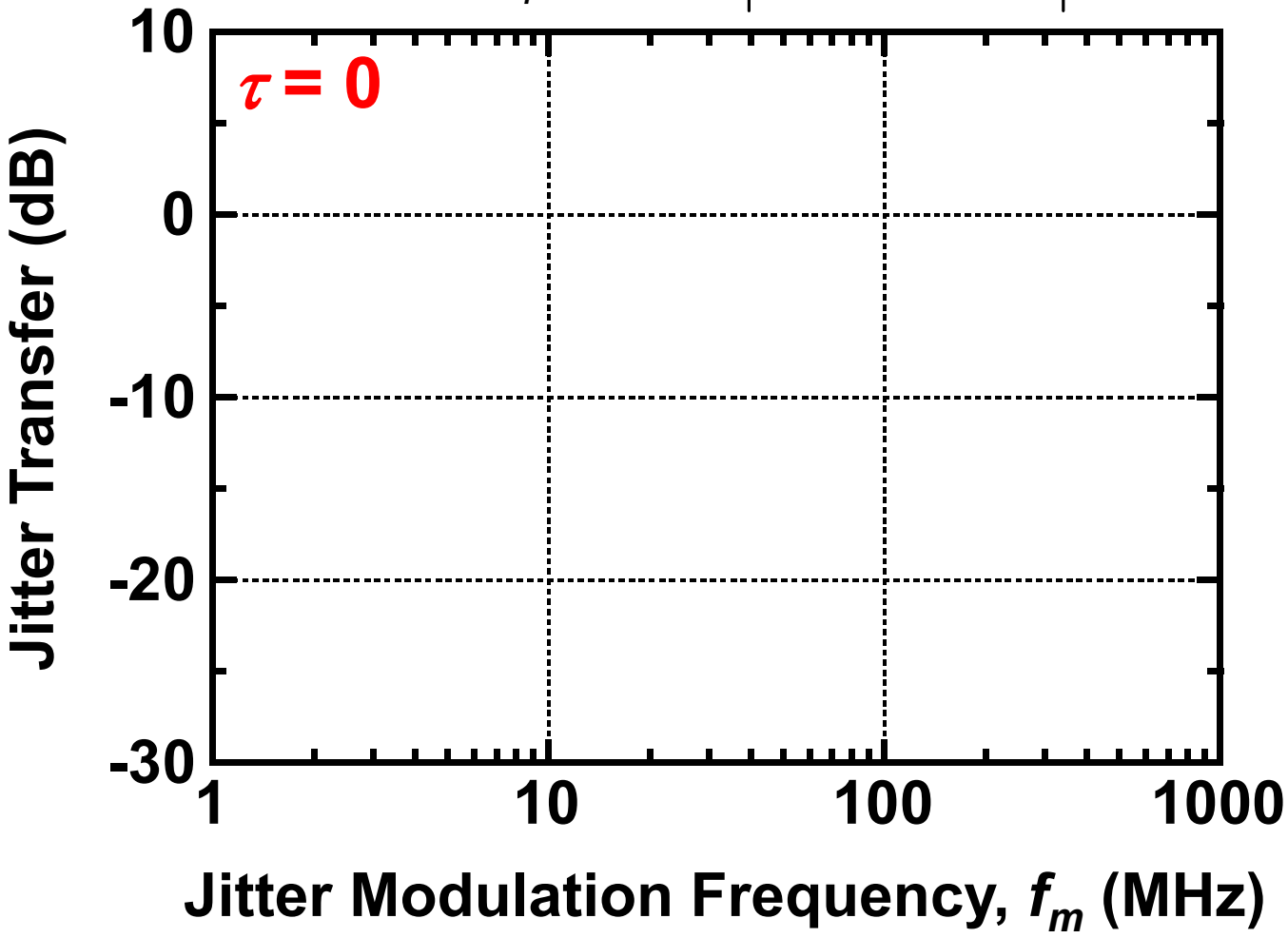


Clock & Data Phase Relationship



Sampling Jitter vs. Delay Mismatch

$$J_{sample} = 2 \cdot \left|\sin(\pi f_m \tau)\right|$$



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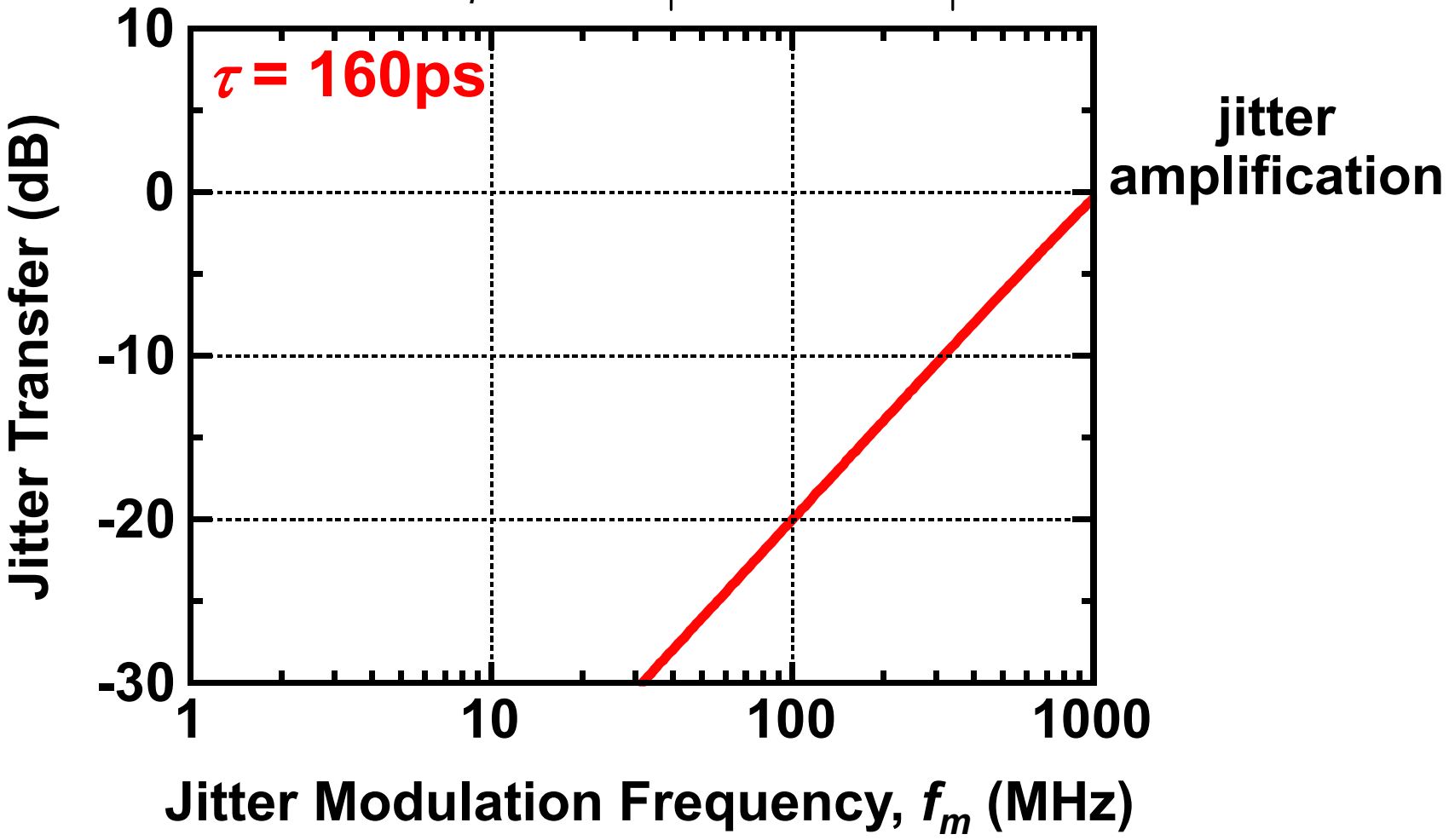

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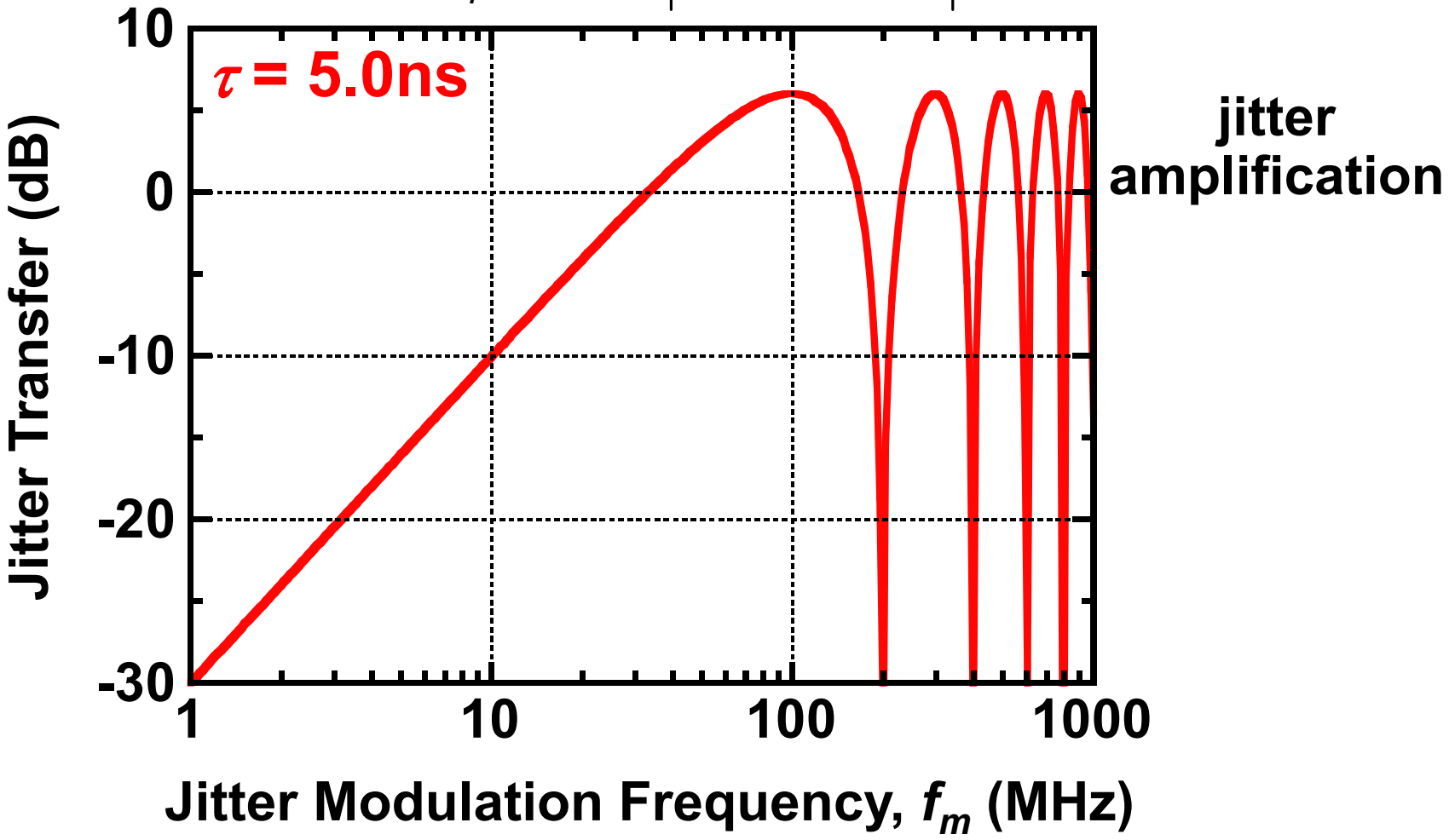
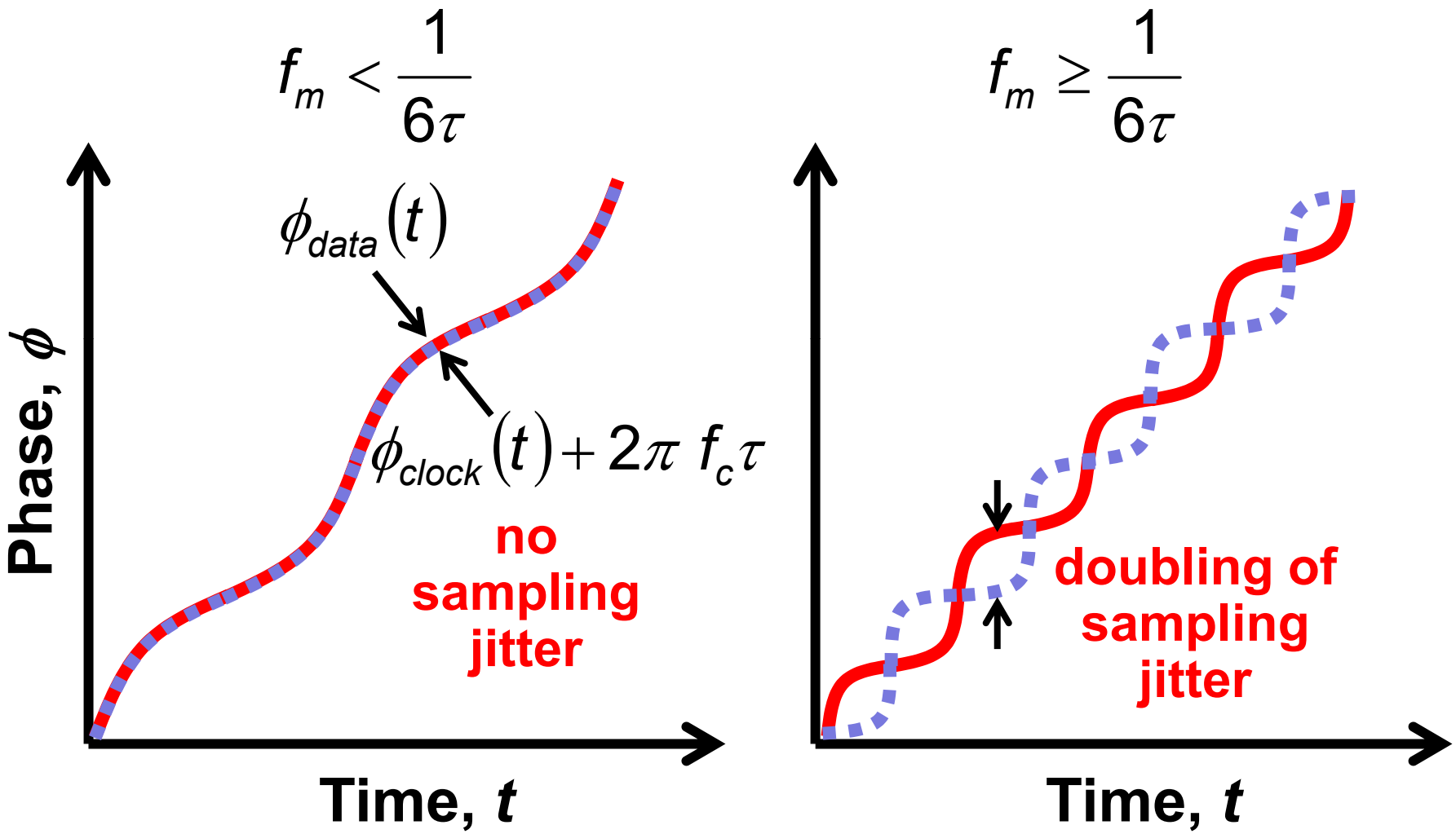


Desired Jitter Filtering Behavior



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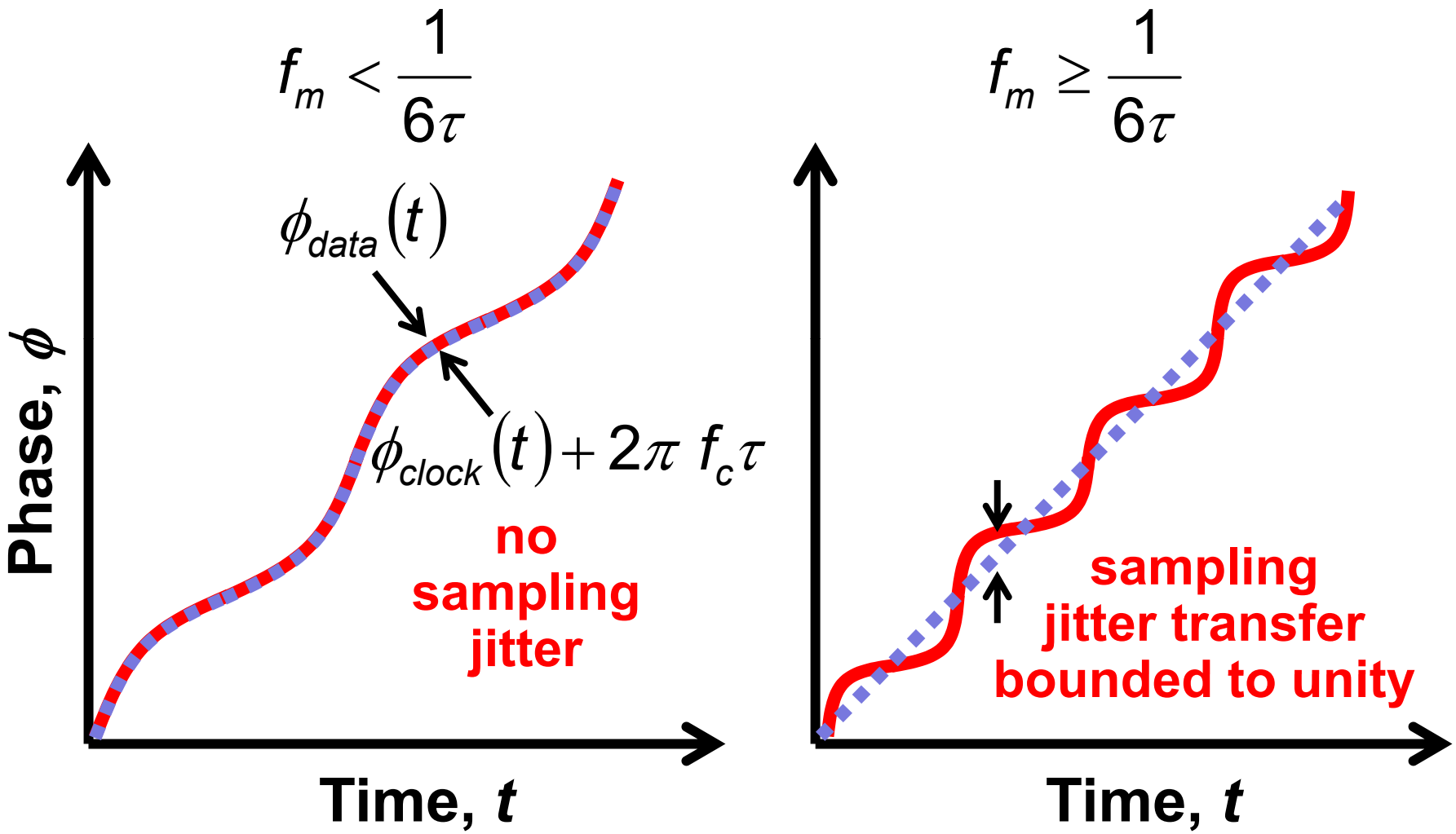
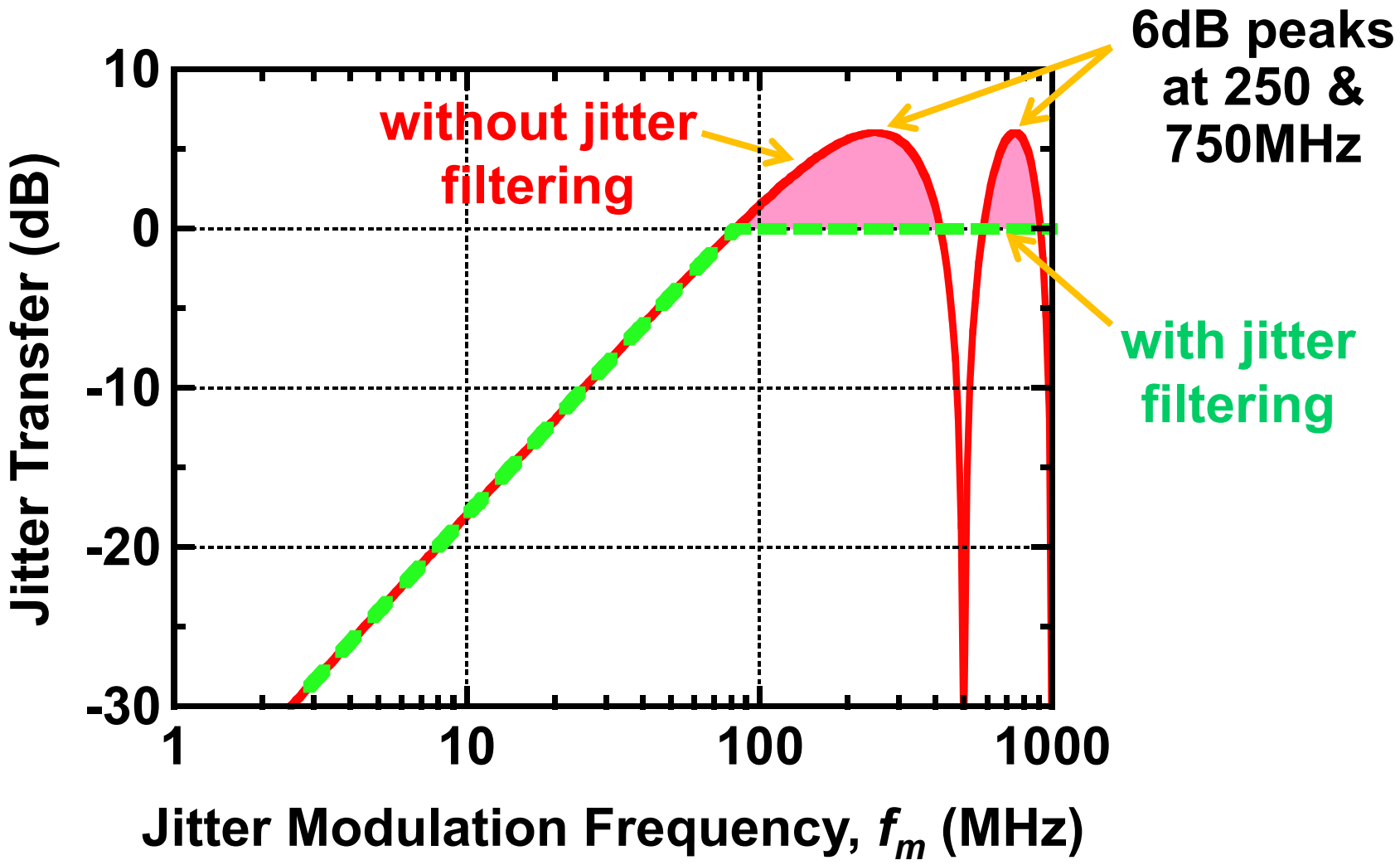


Jitter Filtering Example ($\tau = 2$ns)



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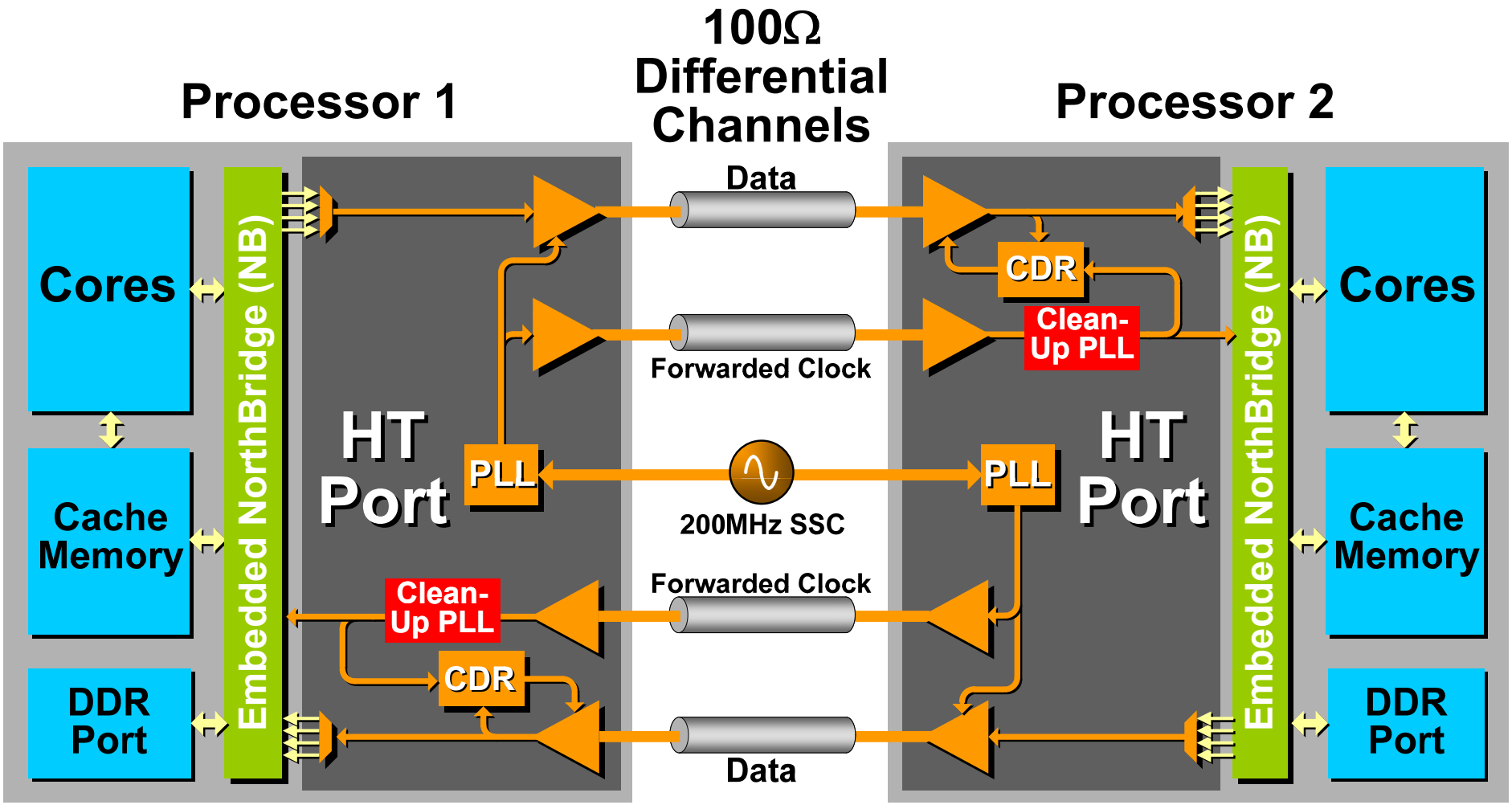
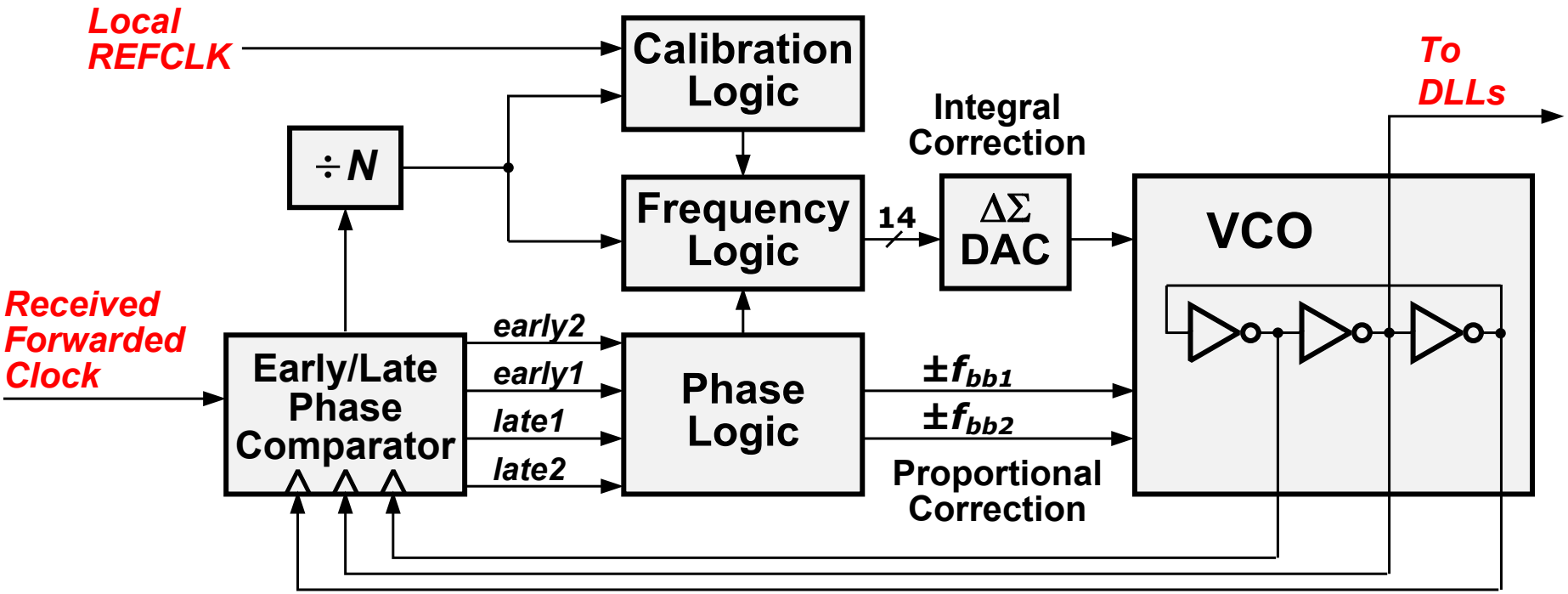
HT I/O with Clean-Up PLL



Wideband Digital Clean-Up PLL



- Adjustable bandwidth for jitter shaping (200MHz default)
- Variable bang-bang rate (f_{bb1} to f_{bb1}+f_{bb2})
- Coarse frequency calibration to local REFCLK for PVT
- Low loop latency

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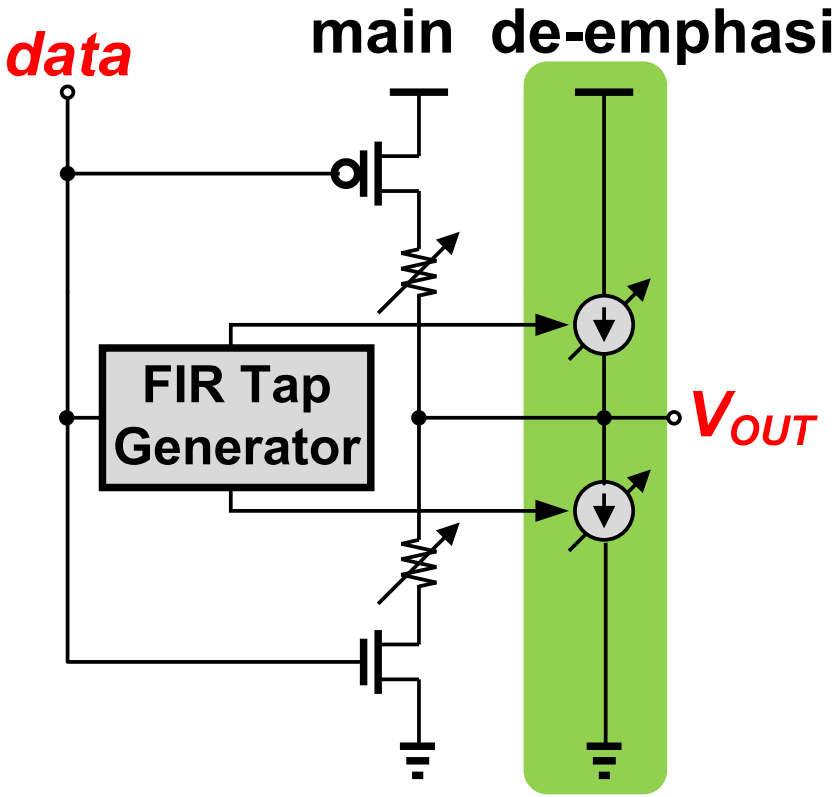
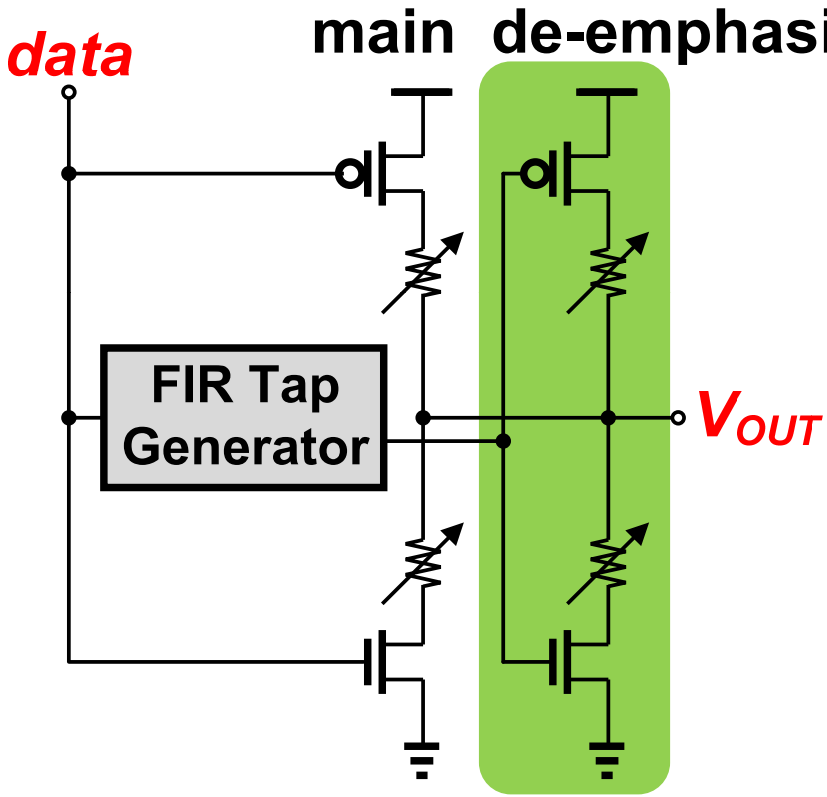
TX Output Driver

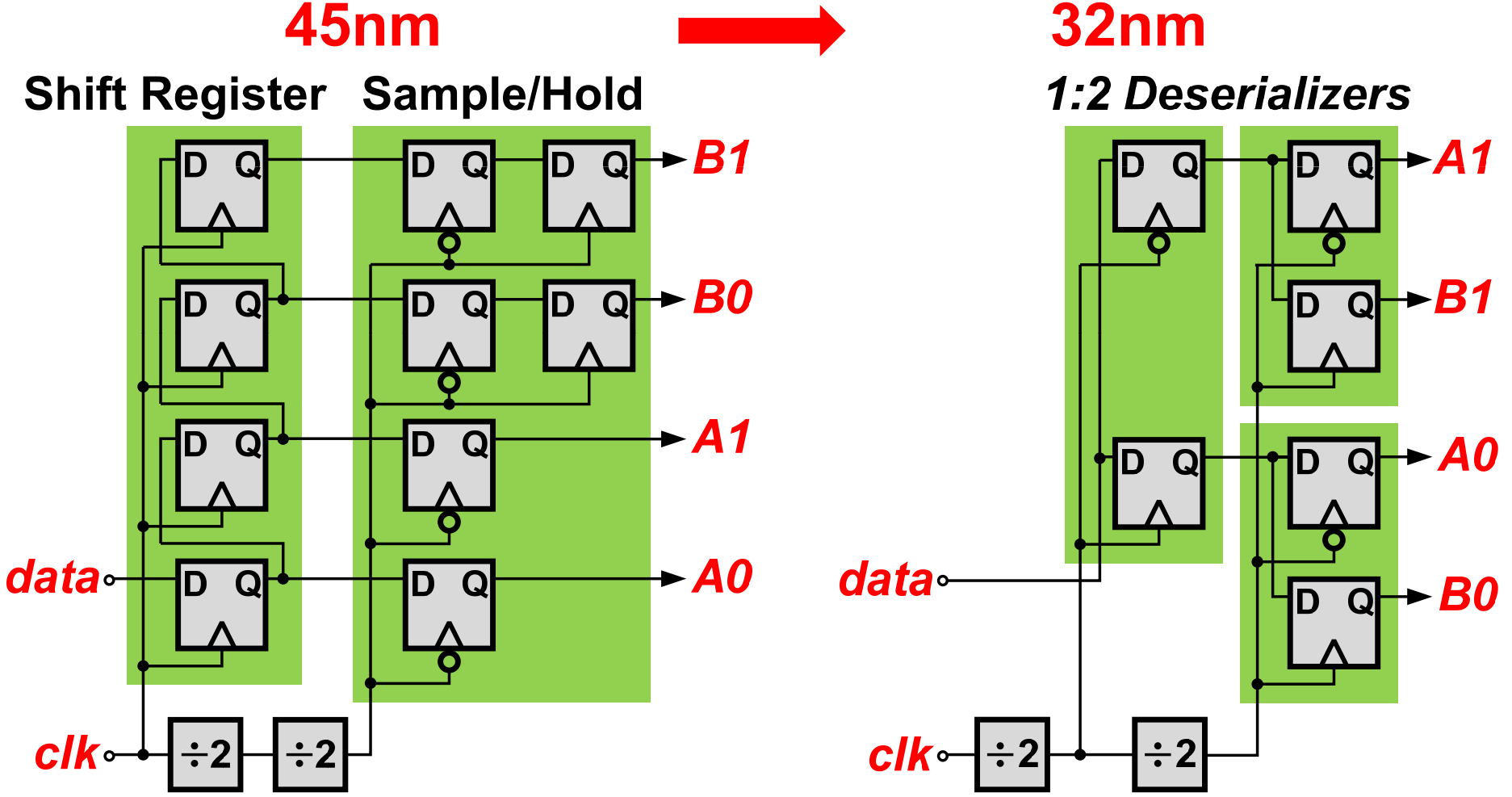
45nm Hybrid Mode → 32nm Voltage Mode





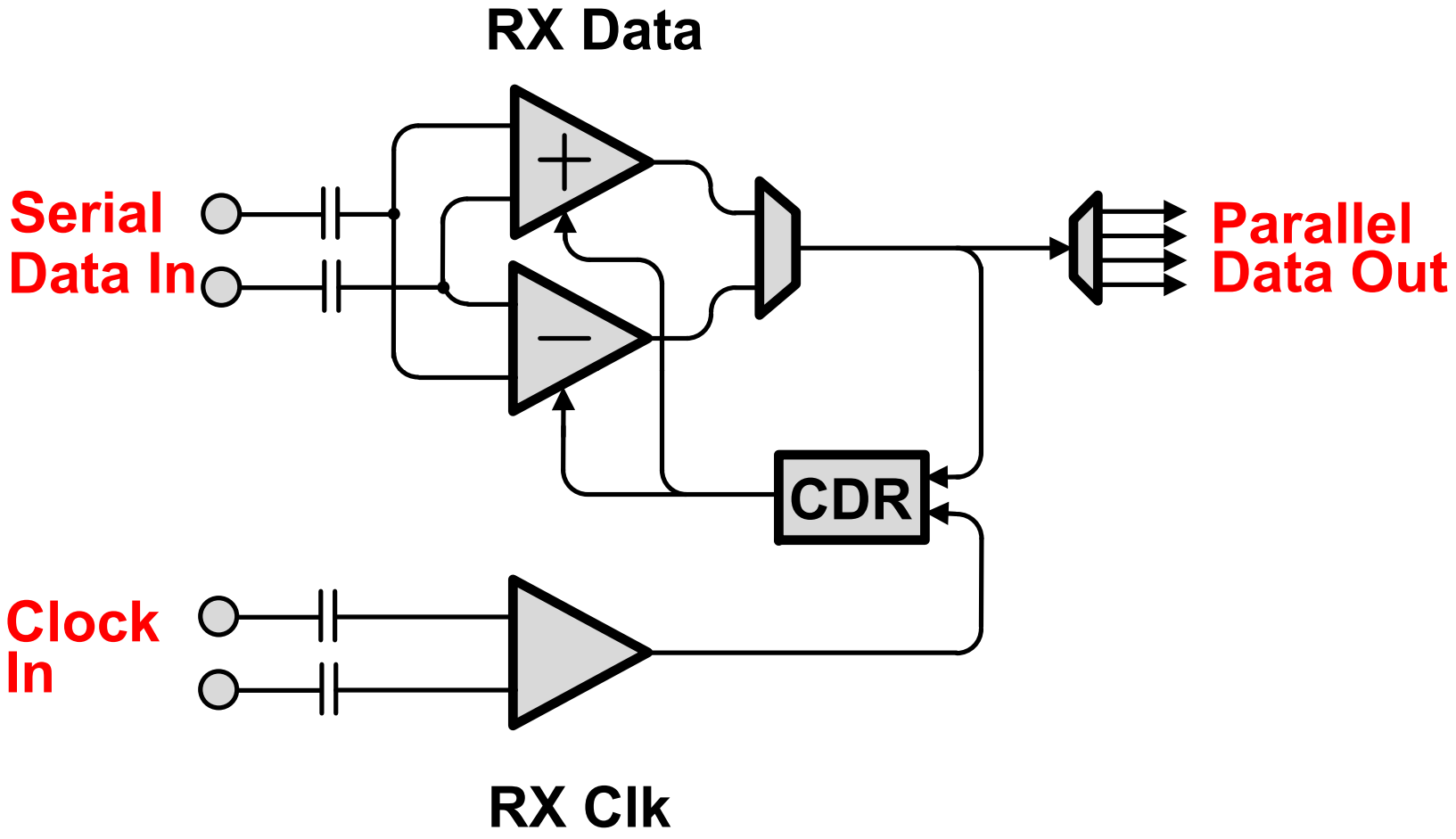
- Power ↓ 20%
- Return loss & DCD ↓

RX 4:1 Deserializer



- Power ↓ 35%, latency ↓

RX Front End



- AC coupling to reduce CLK DCD
- 1-bit speculative (loop-unrolled) DFE

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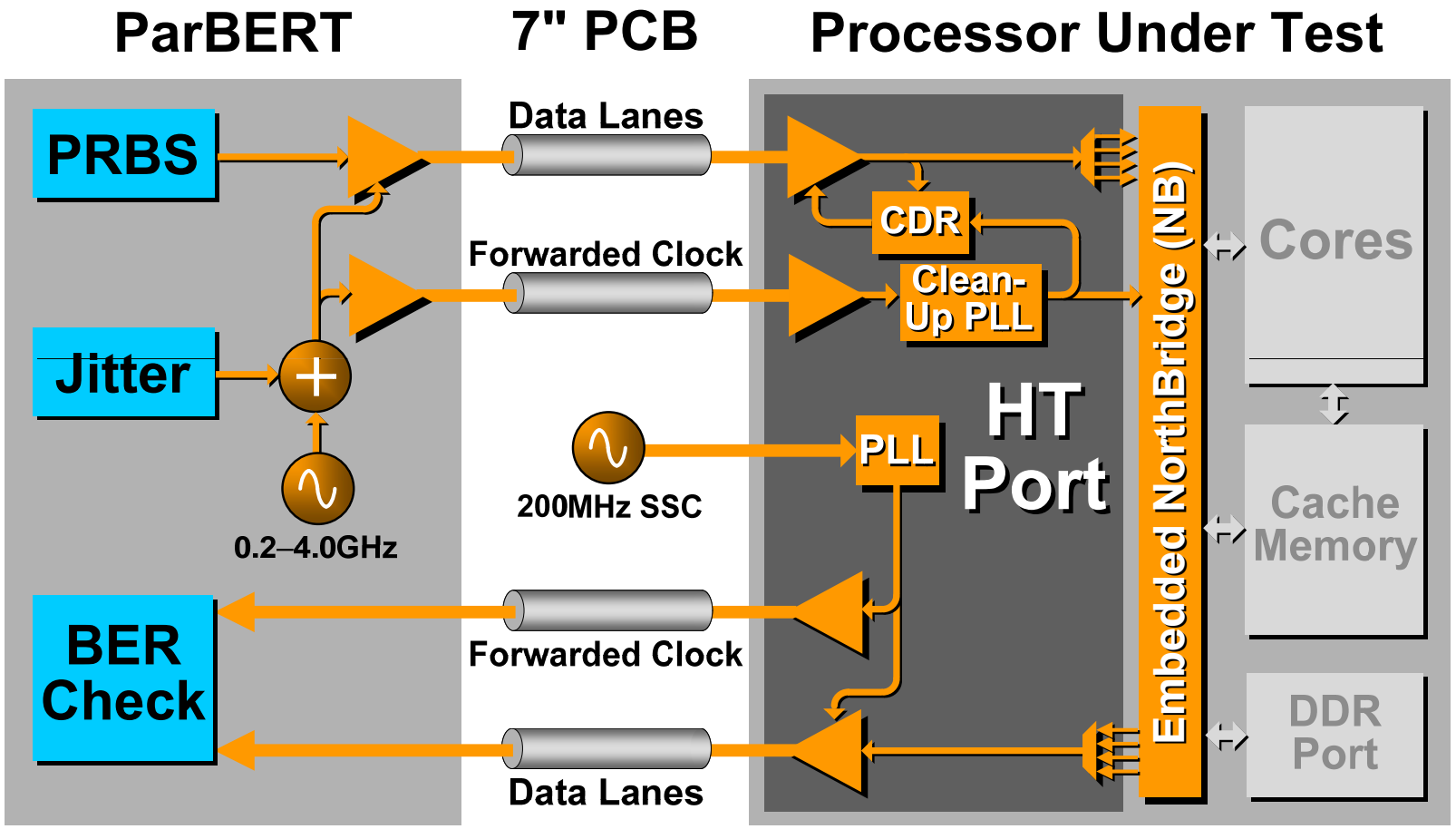
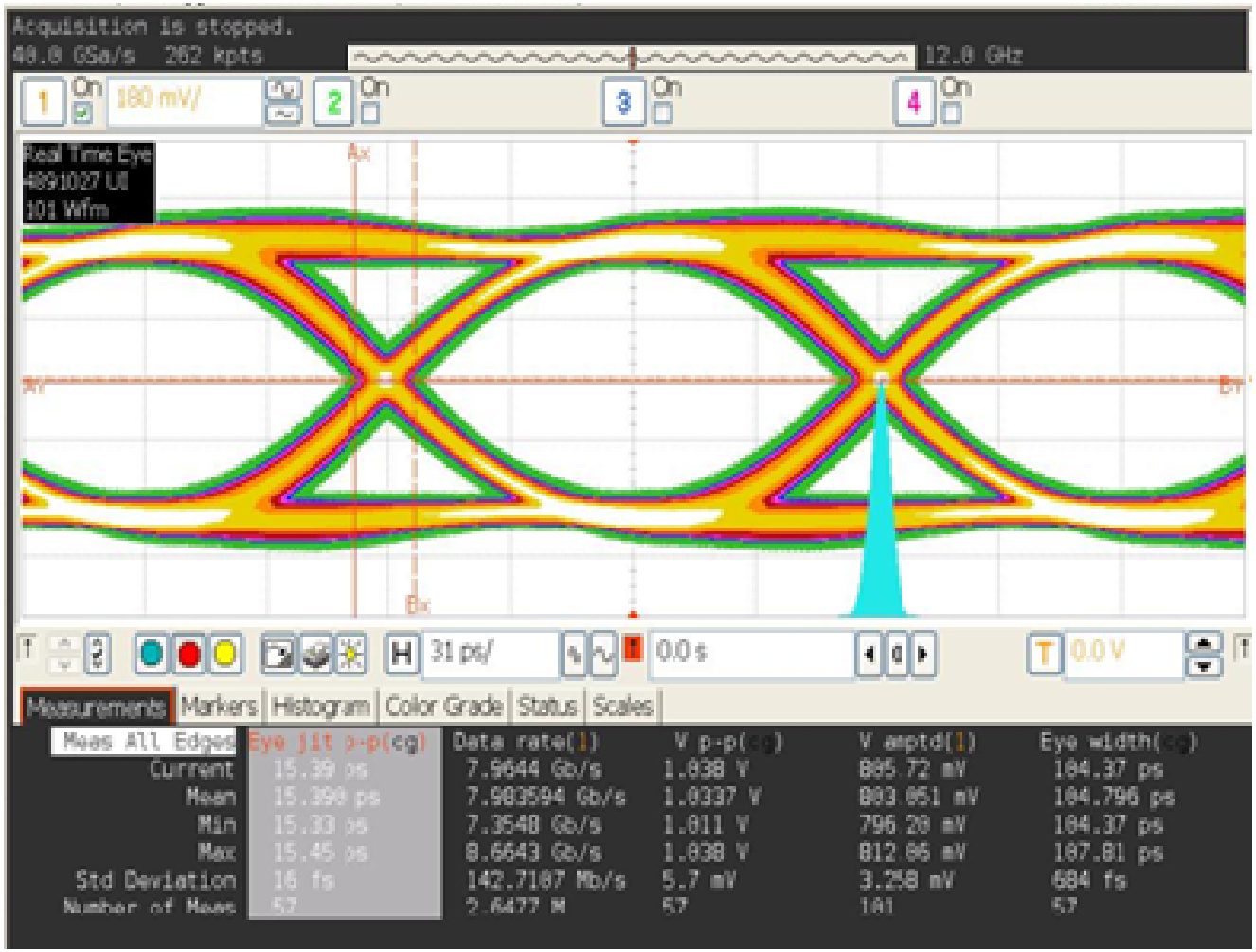
Measurement Setup

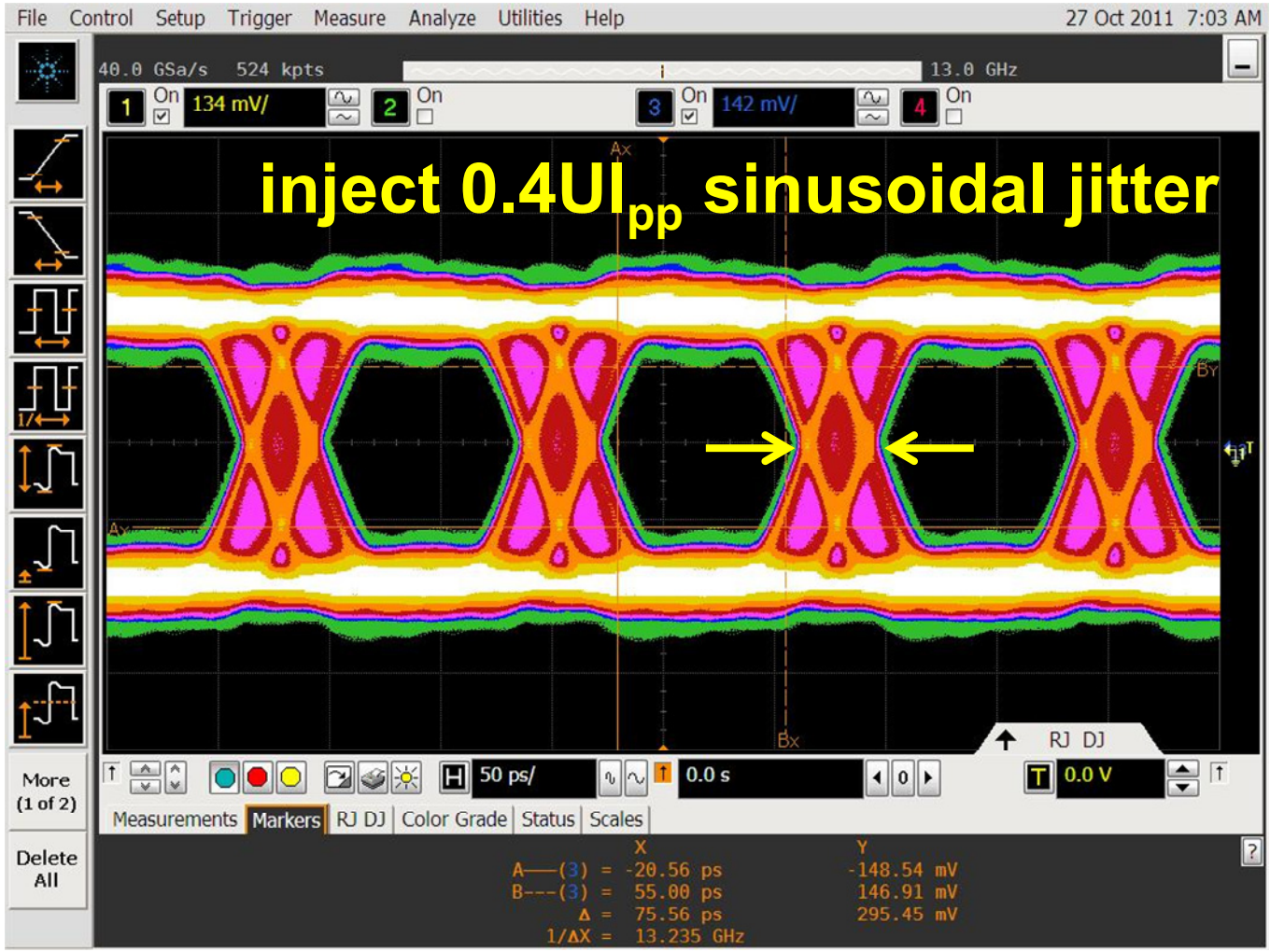


- HT I/O configured in NB loopback mode
- Test overage of full I/O subsystem

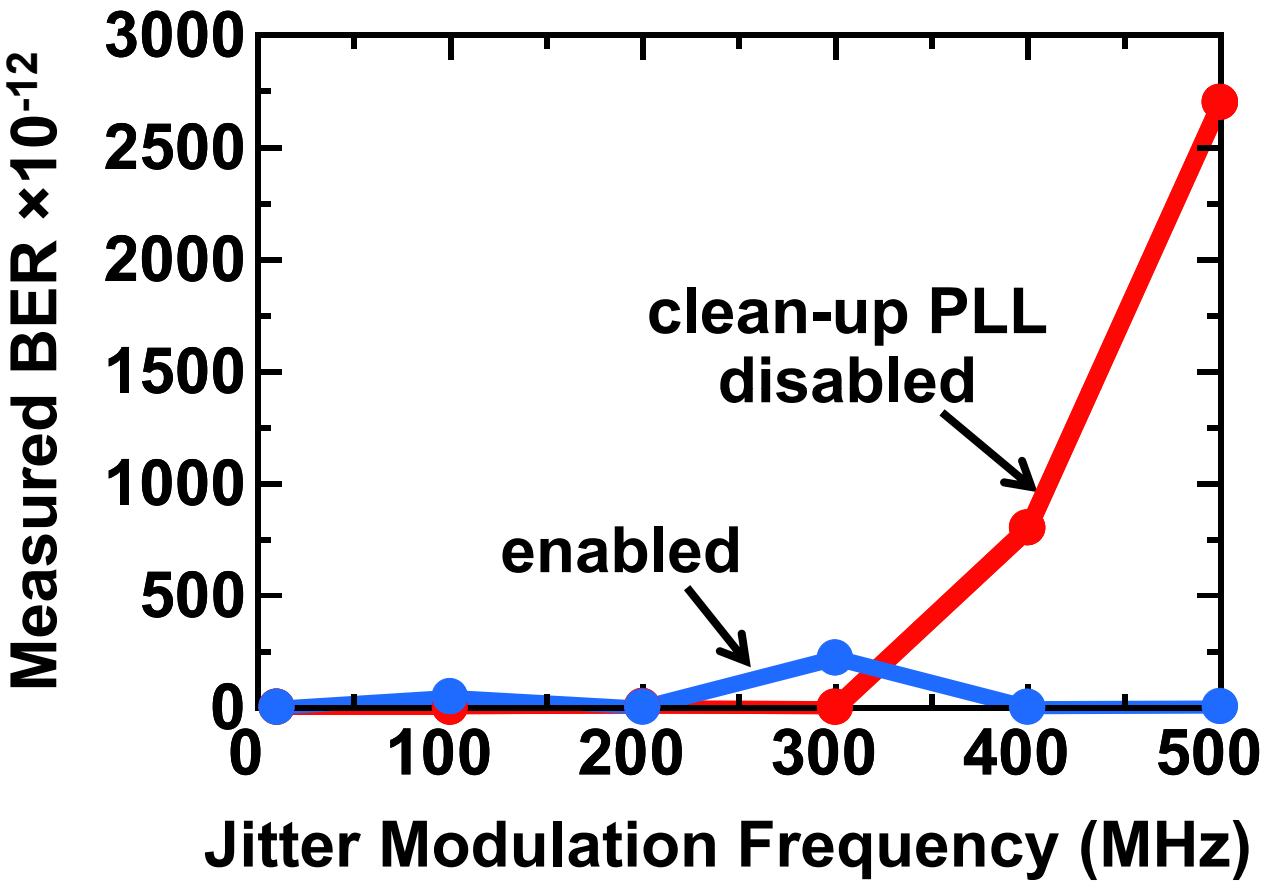
Measured TX Eye – 8Gb/s PRBS-15



RX Eye with Jitter Modulation



Impact of Clean-Up PLL



- $0.4UI_{pp}$ jitter amplitude
- Clean-up PLL removes >300MHz jitter

Measured Power Consumption

SOI-CMOS Technology	Data Rate (Gb/s)	HT I/O Power (W)	ΔPower	Energy Efficiency (pJ/bit)
45nm	6.4	1.62	-	14.1
32nm	6.4	1.40	-13.6%	12.2
	8.0	1.70	+4.9%	11.8

→ 25% higher data rate with only 5% more power

Conclusion

- Achieved higher processor link bandwidth through *evolutionary* enhancements in I/O design
  - 25% boost in lane data rate
  - Sampling jitter reduction with clean-up PLL
  - Near constant power consumption for socket compatibility
- Improves server system performance with minimal product risk

감사합니다

THANK YOU