Equalization for High-Speed Serdes:

System-level Comparison of Analog and Digital Techniques

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Outline

- High-Speed Serdes Channels
- Overview of Equalization Techniques
- Performance & Cost Comparisons
- Future Directions

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Serdes Channel Examples

- Copper Backplane
- Twinax Copper Cable
- Twisted Pair Copper Cable
- MultiMode Fiber/Single Mode Fiber
- PCB Trace

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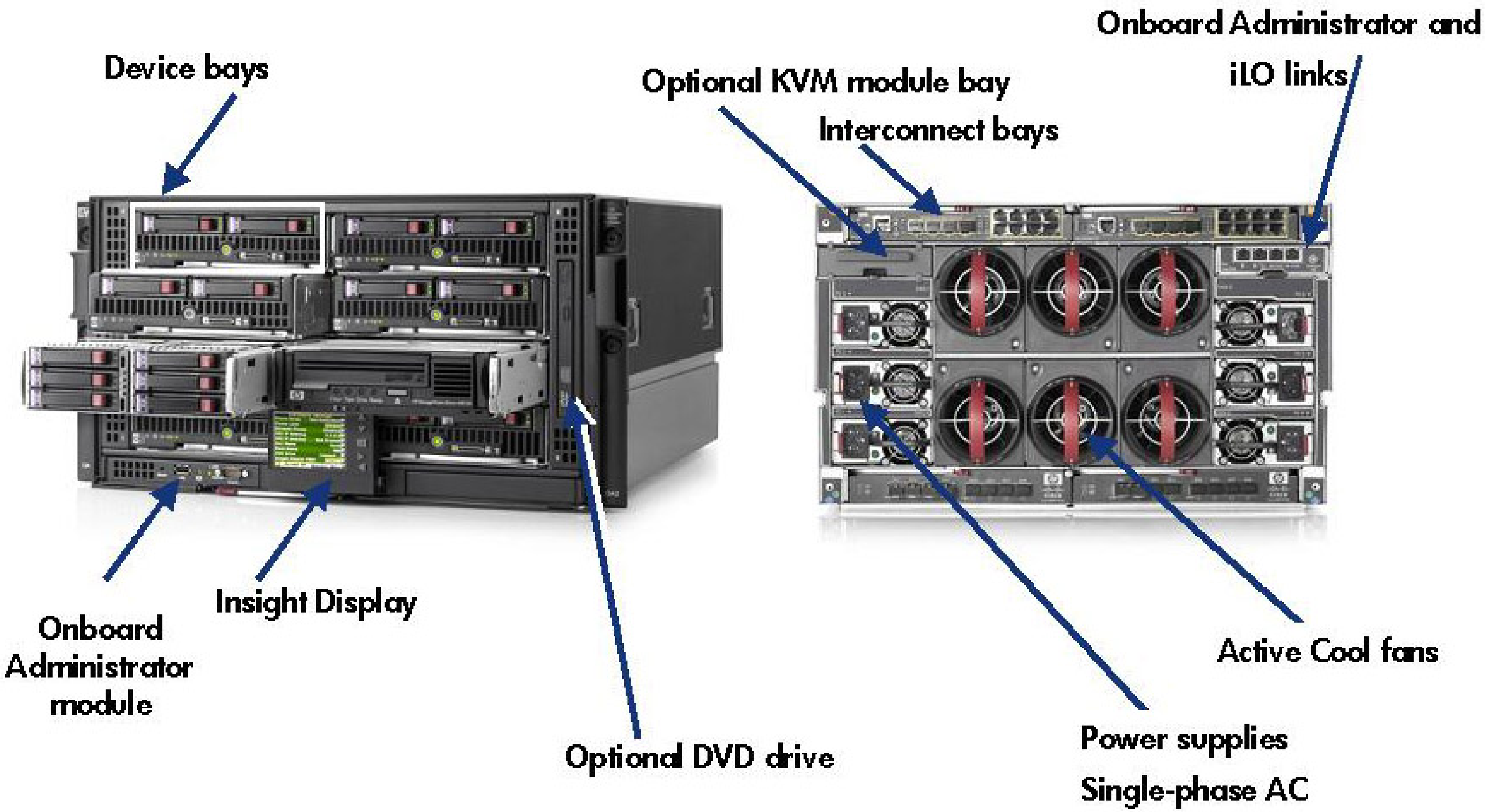
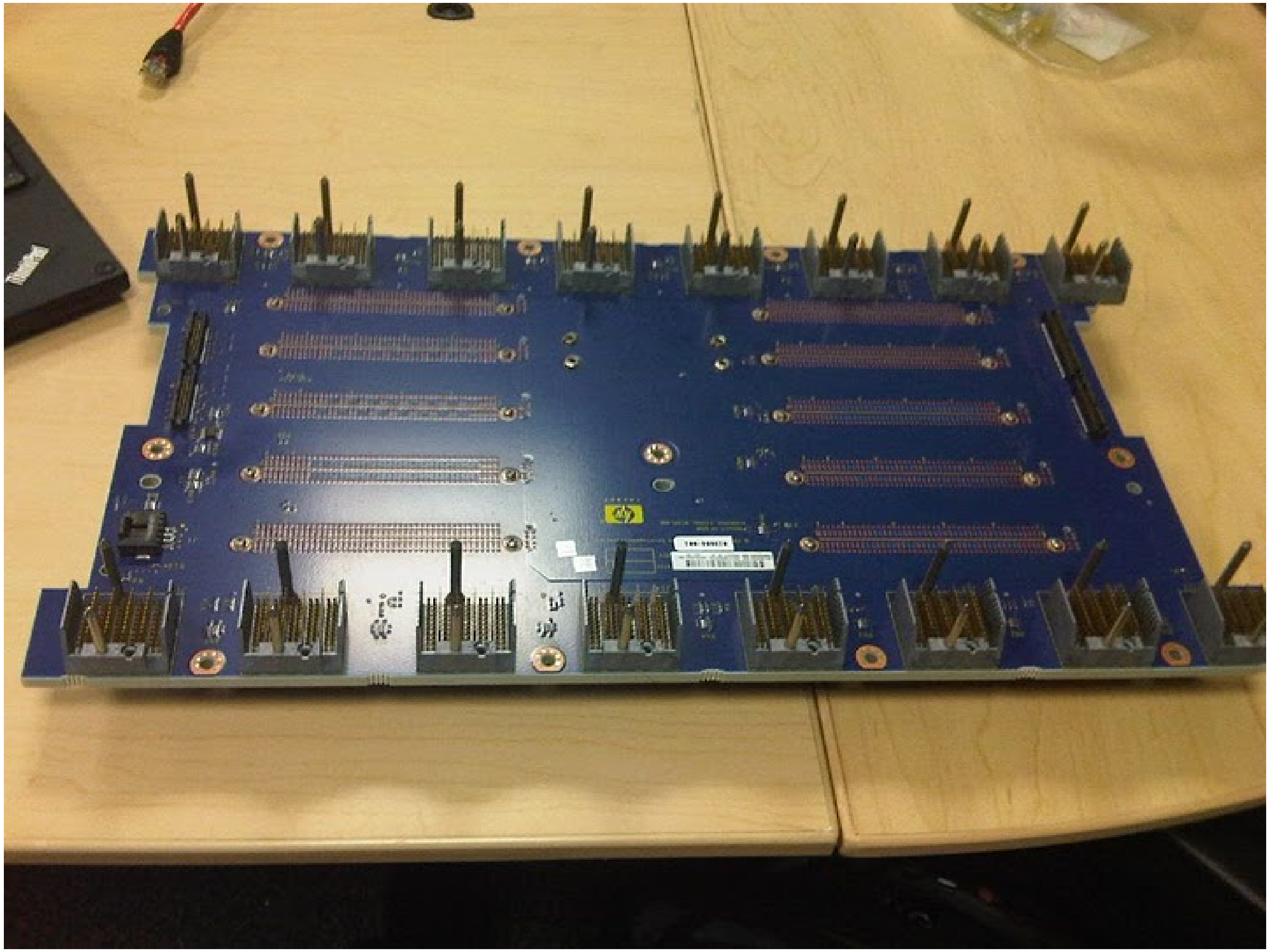
Backplane Enclosure



Midplane



Backplane Channel Overview

- 40in trace end-to-end + 2-3 connectors

- Bandwidth Limited Channels
  - Channel is reasonably well behaved
  - No sharp nulls or peaks

- Key challenge: High Signaling Rate (~25 GBd)

- BER Target is 10^{-12} - 10^{-15}

Channel Types

- "Legacy" backplanes using older PCB material, e.g., FR4, Nelco4000-13
- "Next Generation" backplanes newer PCB material, e.g., Megtron-6 and ISOLA-680

Channel Impairments

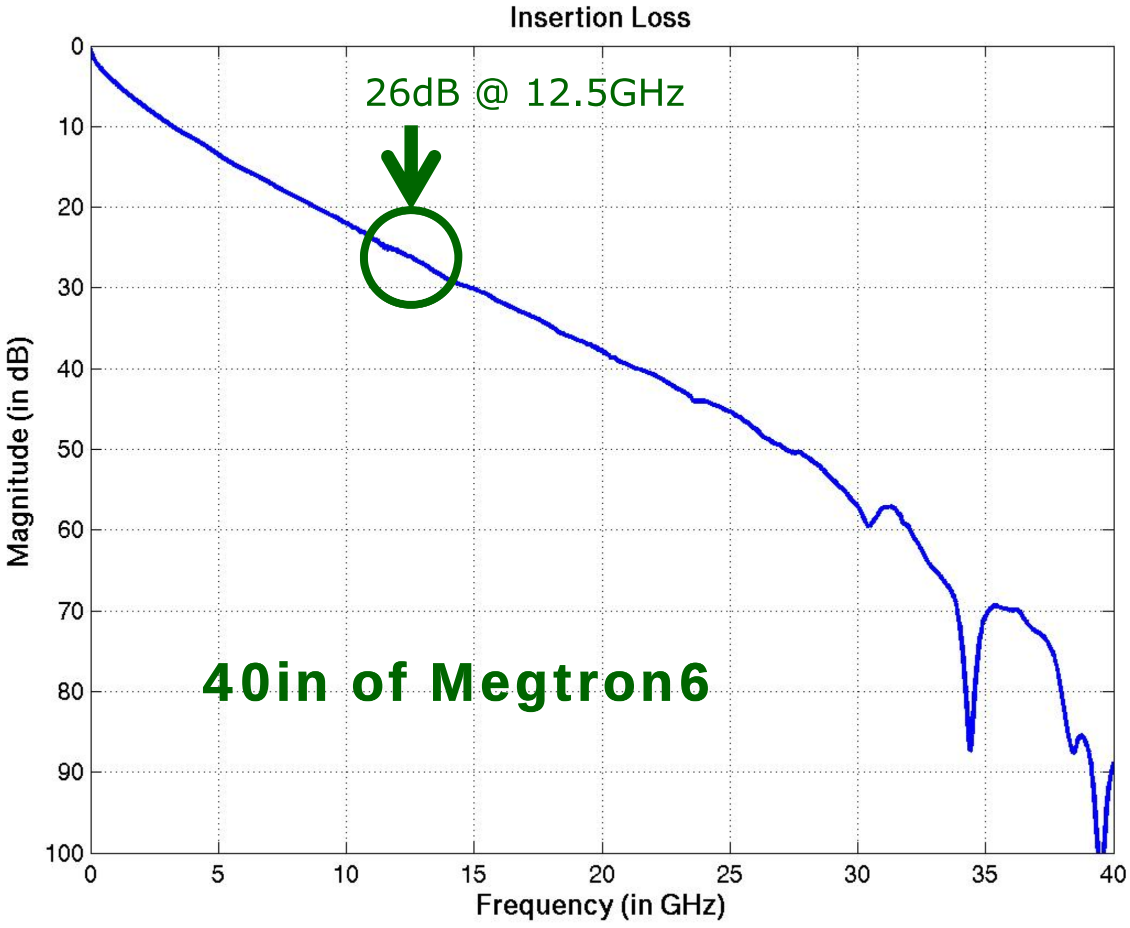
- Attenuation (resistive loss)
- InterSymbol Interference (ISI) caused by bandwidth limitation
- Reflections (Return Loss) caused by impedance discontinuities
- Crosstalk caused by coupling between traces and in connector
  - Near End CrossTalk (NEXT)
  - Far End CrossTalk (FEXT)
- Jitter (Tx and Rx)
- Thermal Noise

Backplane Example

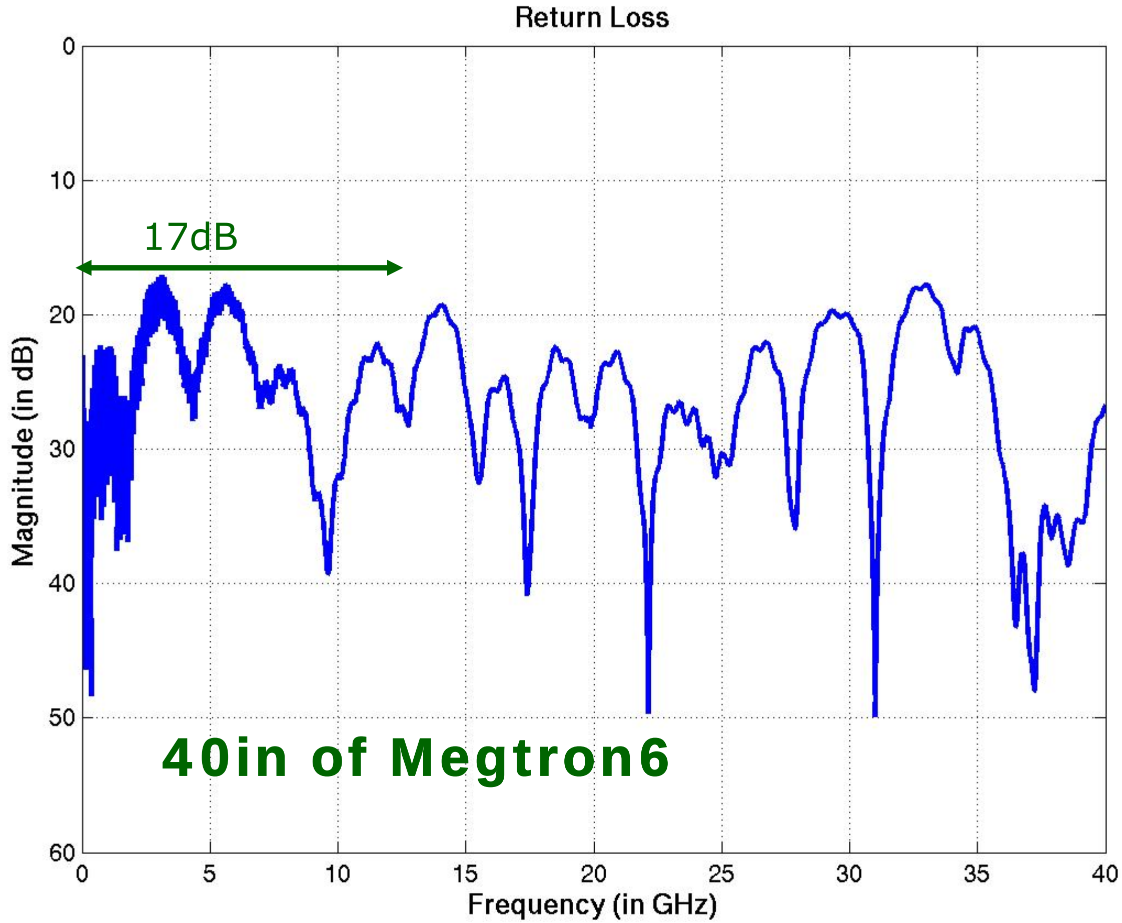
- 40in Total Length
  - Footprint traces add 2.8in additional length
- 30 in Backplane
- 2 Daughter Cards, 5 in trace each
- 2 connectors – STRADA Whisper*
- **25Gbit/s data rate!**

*TE Connectivity Trademark

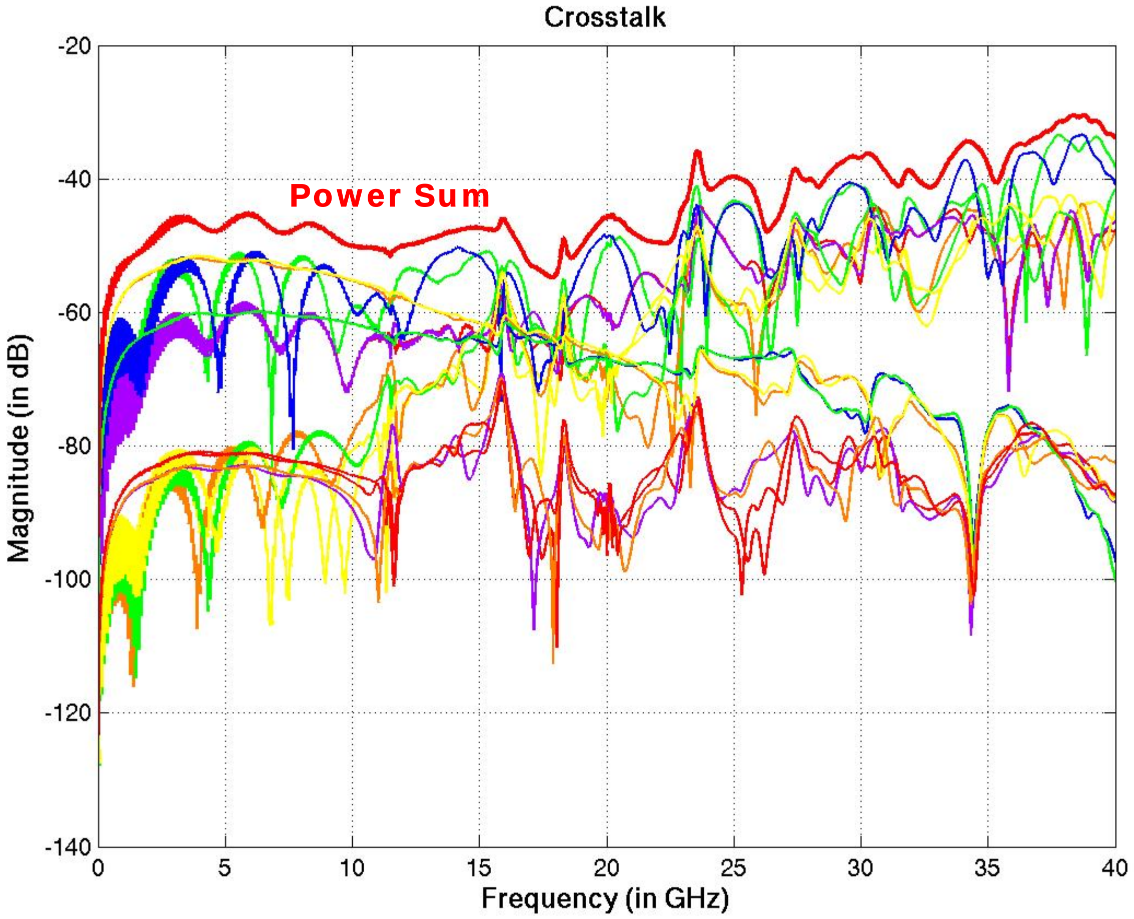
Insertion Loss of 40in Backplane



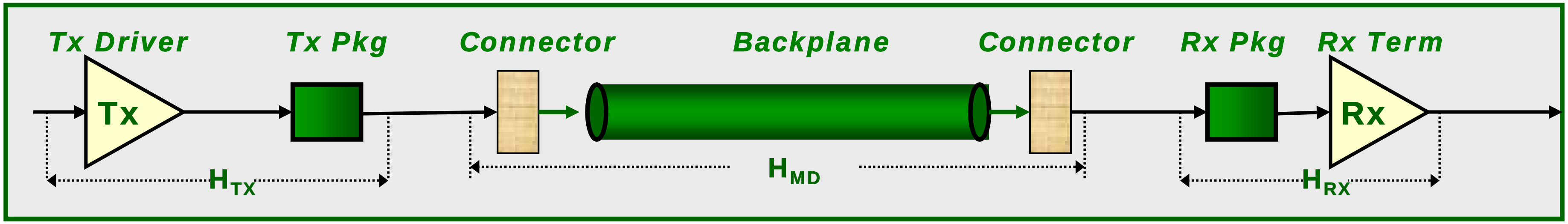
Return Loss of 40in Backplane



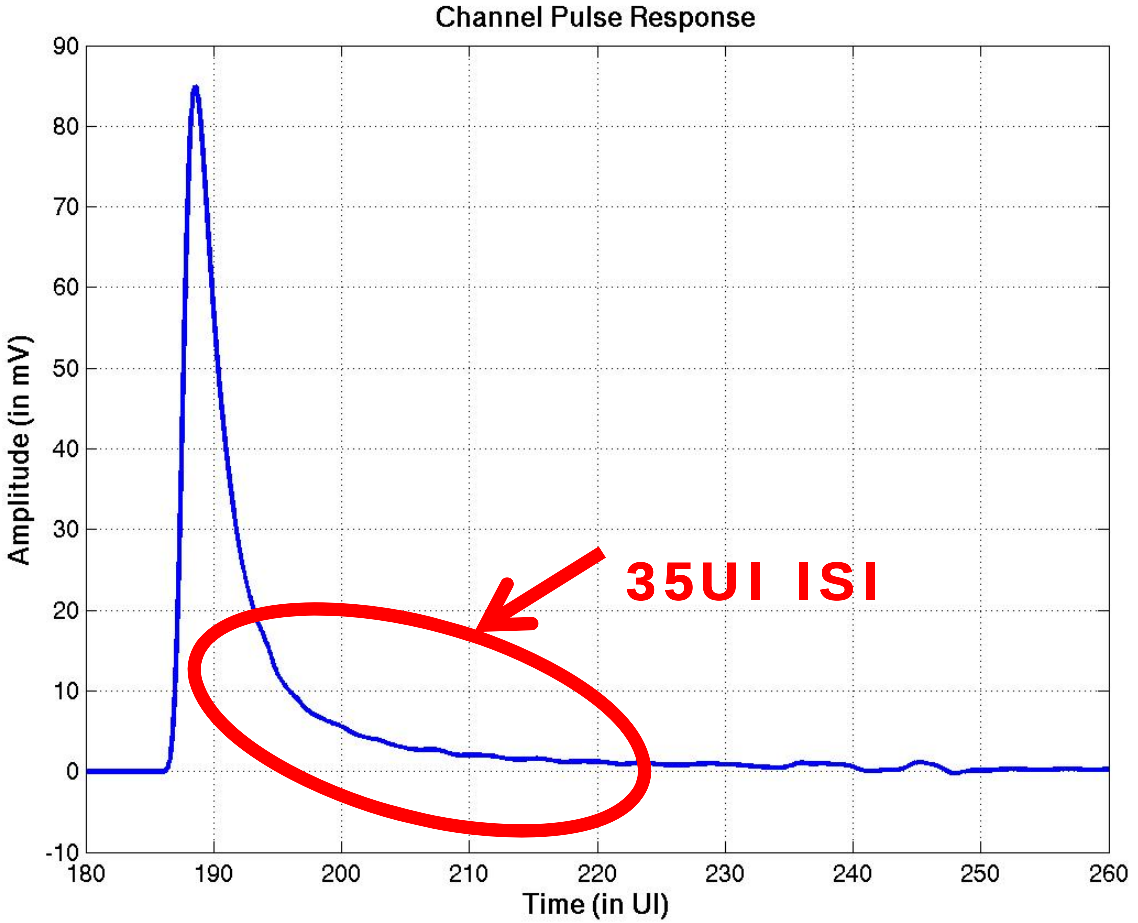
Crosstalk – 8 NEXTs, 8 FEXTs



End-to-End Channel



Channel Impulse Response



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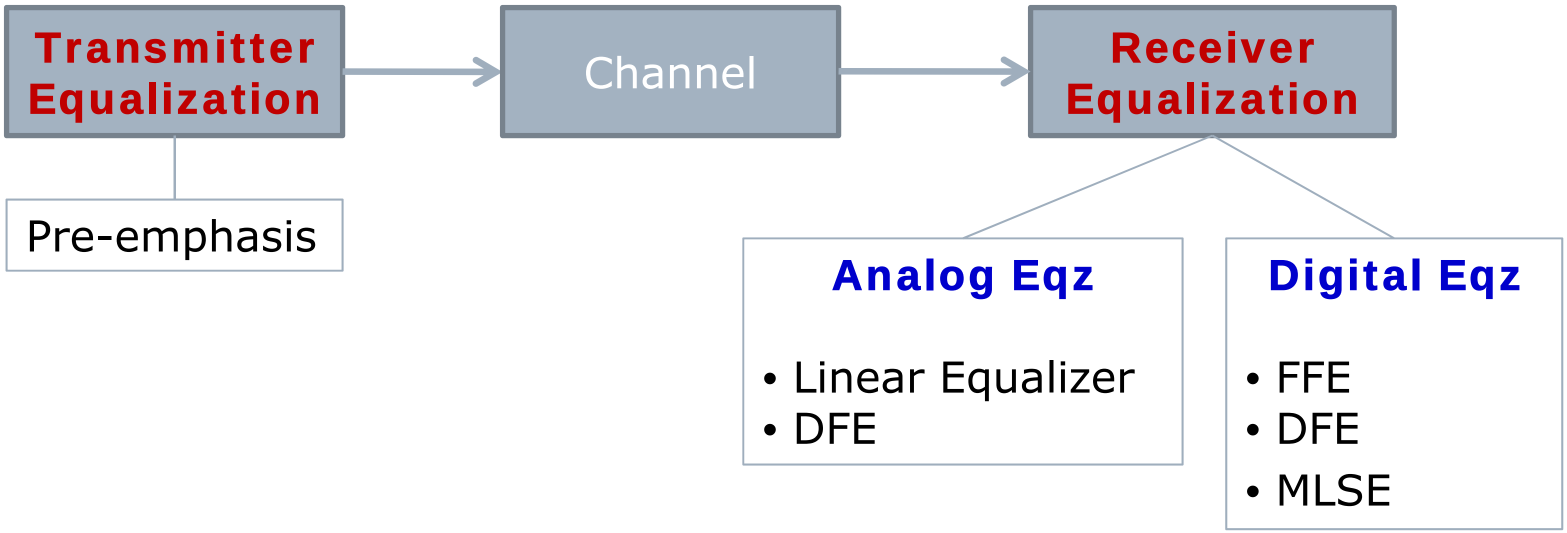
- High-Speed Serdes Channels
- Overview of Equalization Techniques
- Performance & Cost Comparisons
- Future Directions

Equalizer Architecture Options

- Many different ways to equalize the channel
  - Tradeoff between power/area and performance

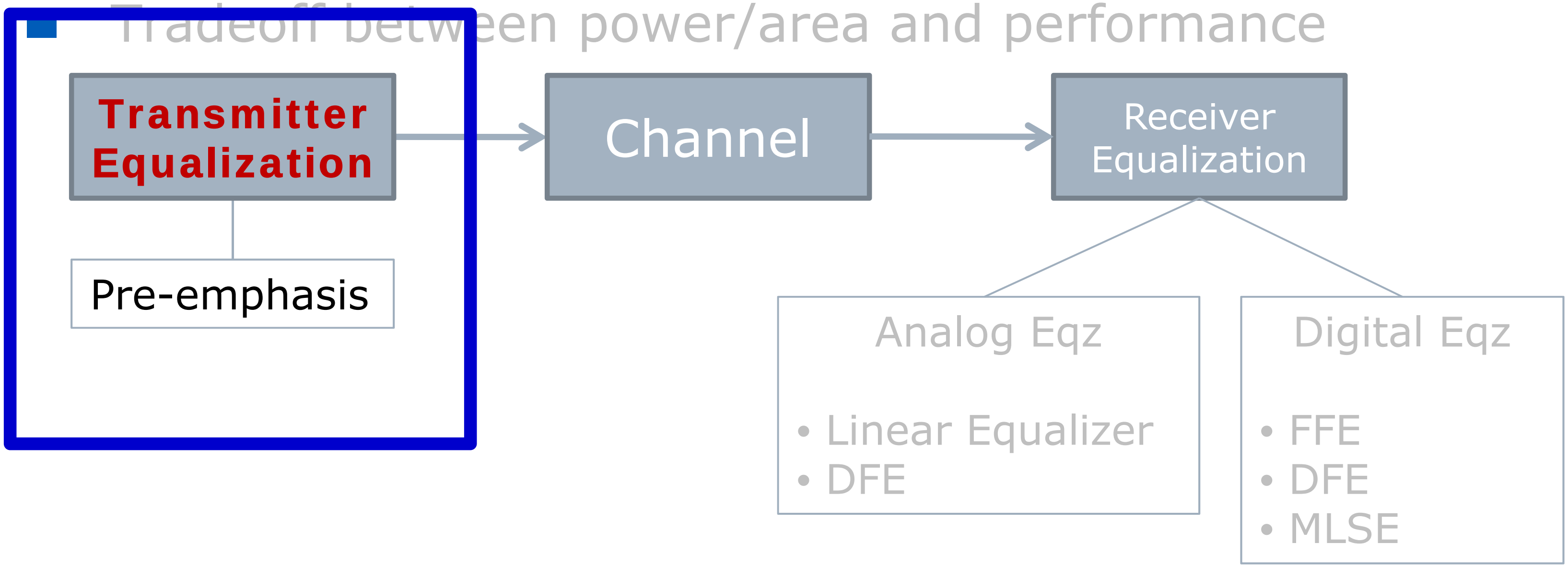


Equalization Overview

	Pros	Cons
Transmit Pre-emphasis	• Low complexity	• Non-adaptive • Amplifies crosstalk
Linear Equalizer	• Adaptive	• Noise enhancement
DFE	• No noise enhancement	• Implementation Difficulty • Error propagation
MLSE	• Optimal Performance	• Implementation Cost

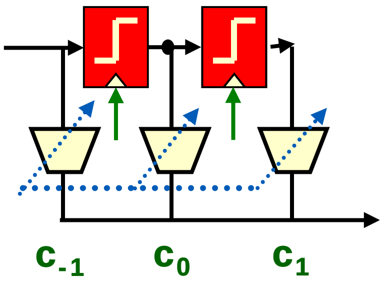
Equalizer Architecture Options

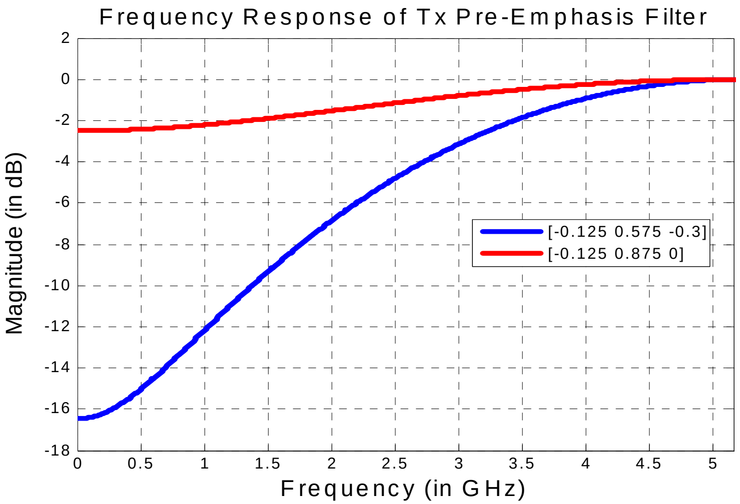
- Many different ways exist to equalize the channel
  - Tradeoff between power/area and performance



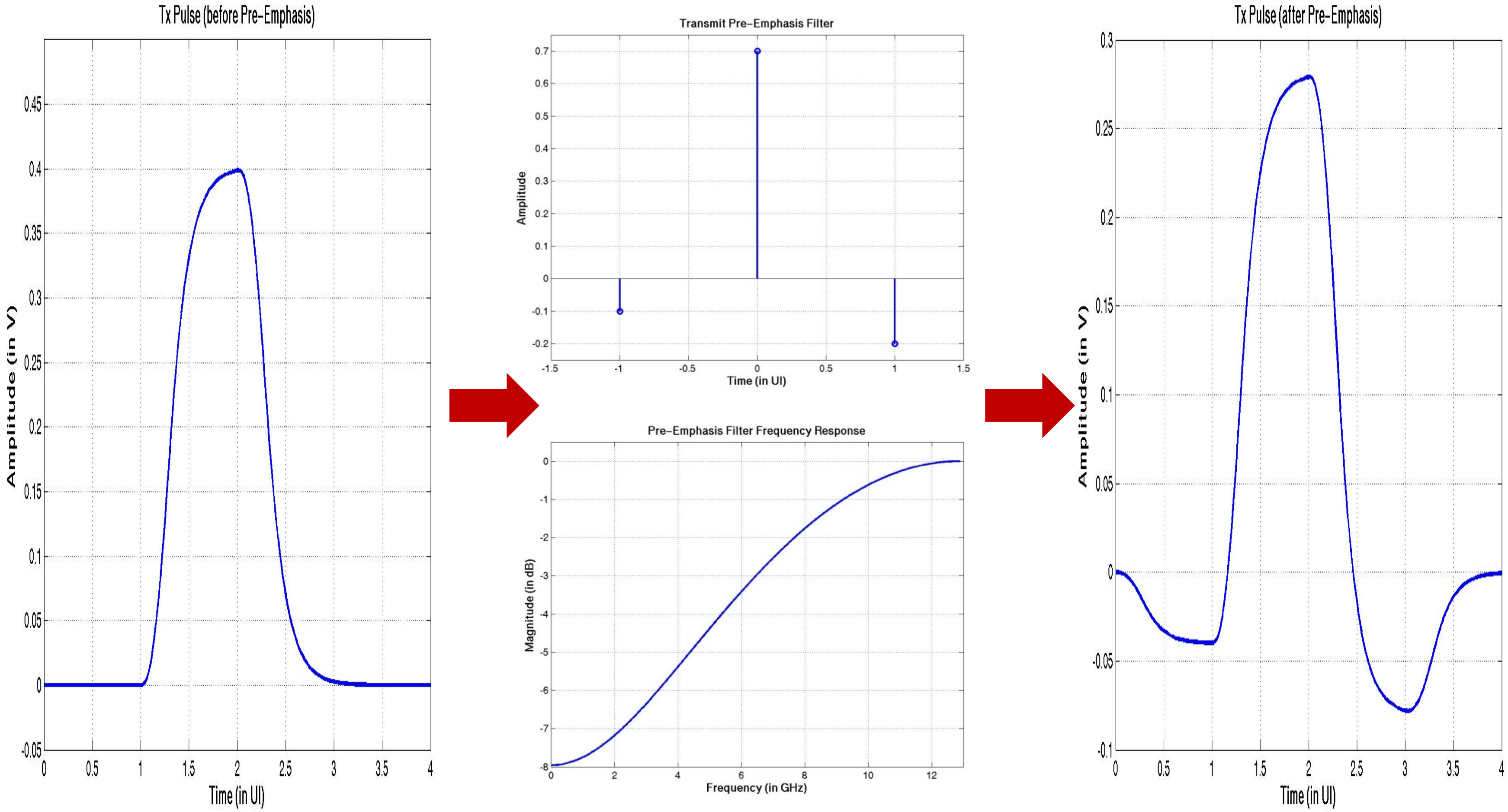
Transmitter Pre-Emphasis

- Pre-distorts the Tx signal to compensate for the channel
  - Simple implementation, but fixed behavior
  - Implemented as de-emphasis, low-freq signal is reduced
- Equalization in Tx is lower complexity than in Rx
- 2 or 3-tap FIR

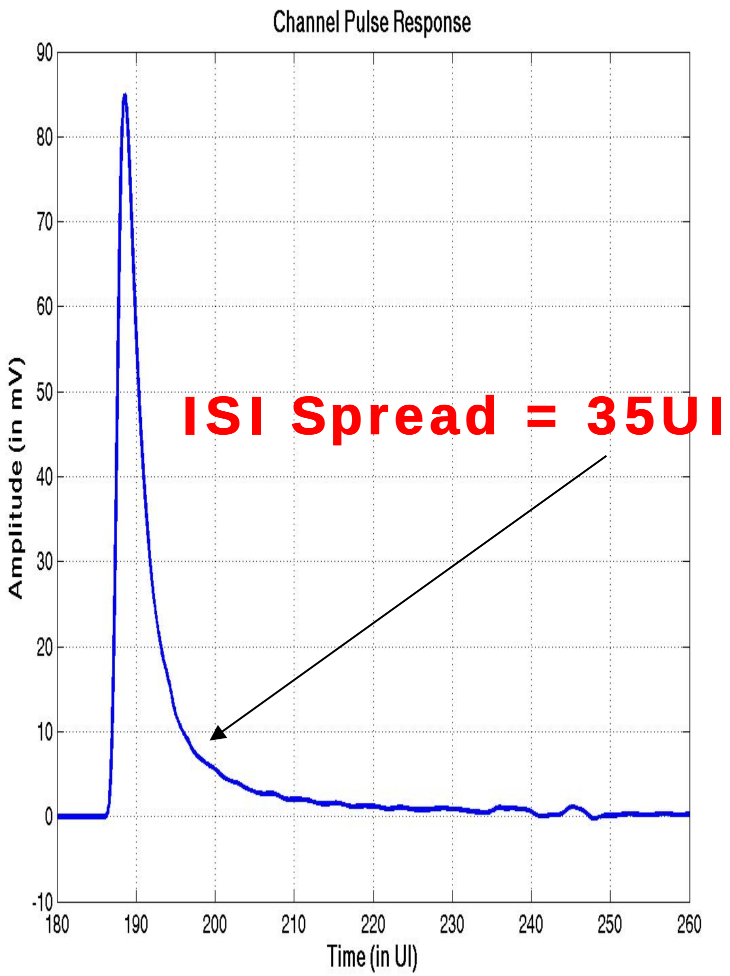


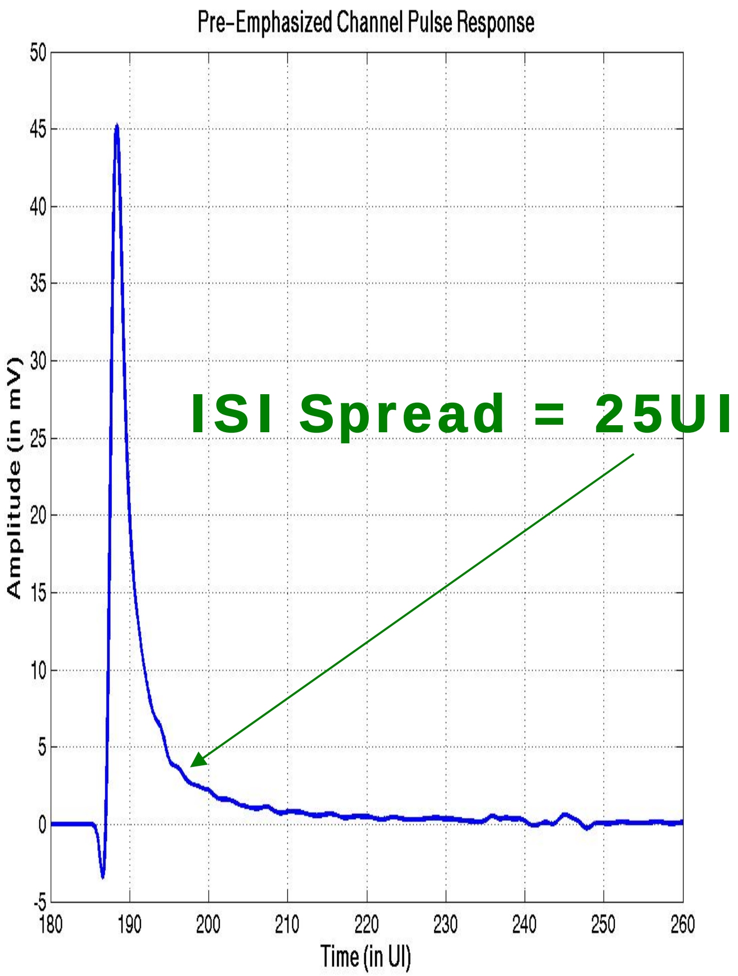


Optimized Tx Pre-Emphasis Filter



Effect of Tx Pre-Emphasis





Equalizer Architecture Options

- Many different ways exist to equalize the channel
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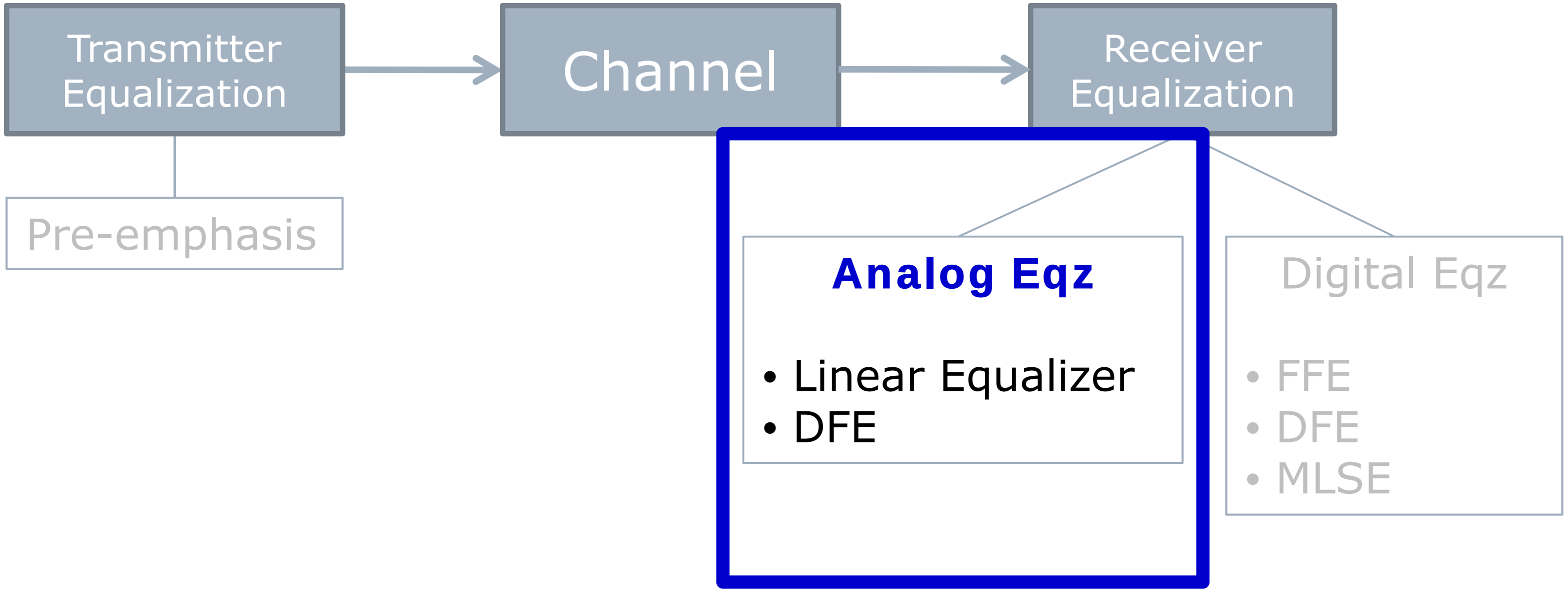


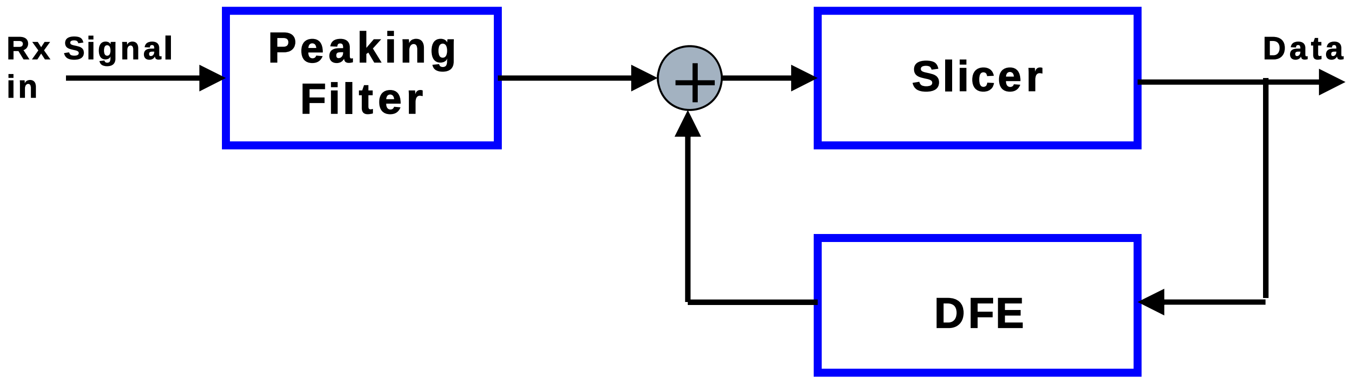
Analog Equalizer Options

- Continuous Time Linear Equalizer (CTLE) is typically implemented as a “Peaking” Filter

- An analog linear equalizer can also be built as an FIR, using continuous-time tapped delay lines, with T-spaced, or T/2 spaced taps

- Analog Decision Feedback Equalizer (DFE)

Peaking Filter + DFE Block Diagram

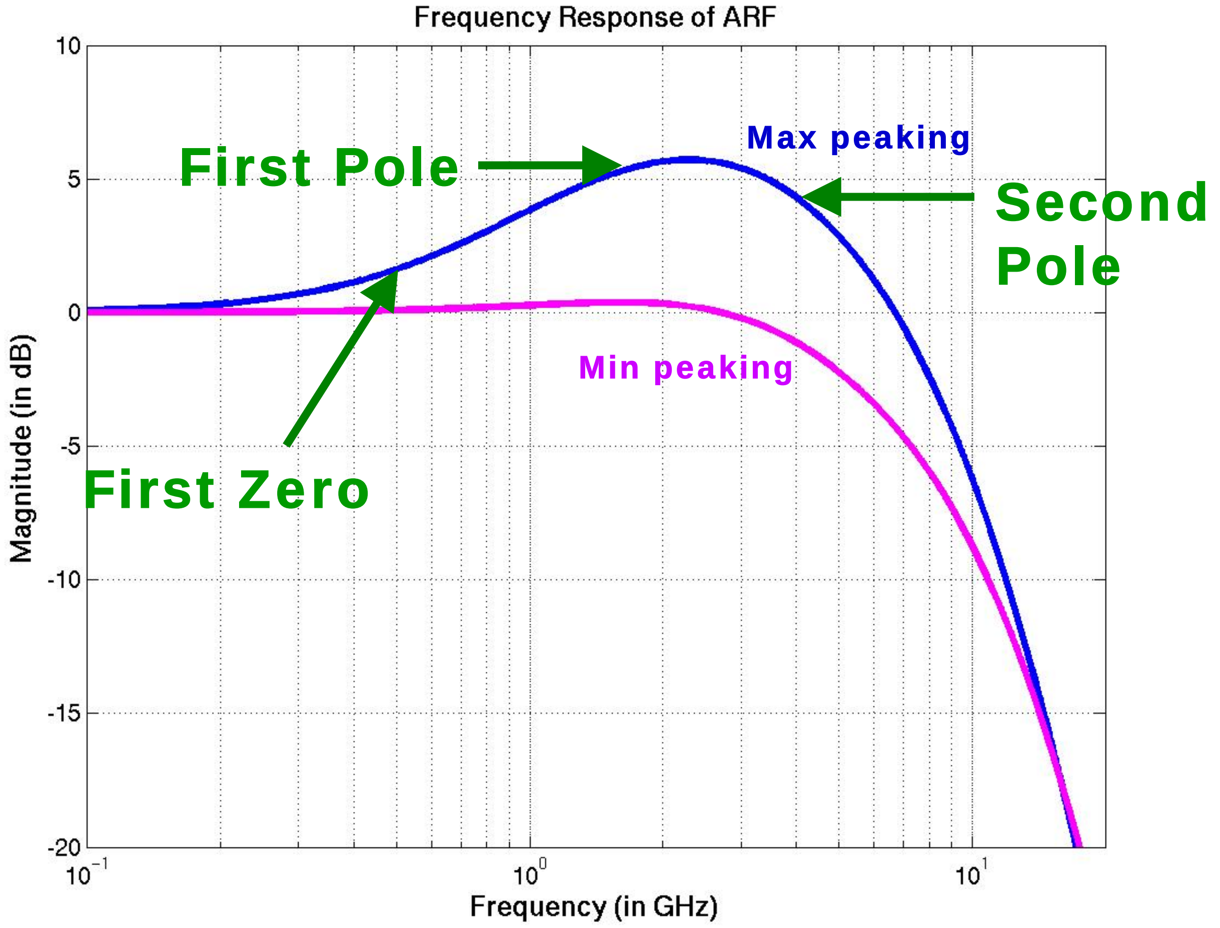


Decision
Feedback
Equalizer

Analog Peaking Filter

- Pole-Zero filter that provides peaking, in order to “invert” the channel
- Typically one low frequency zero followed by two or more poles
- Relative location of zero and first pole determine frequency and magnitude of peaking
- Adjustable peaking levels, e.g., 16 settings
  - LMS-like algorithm can be used to adapt

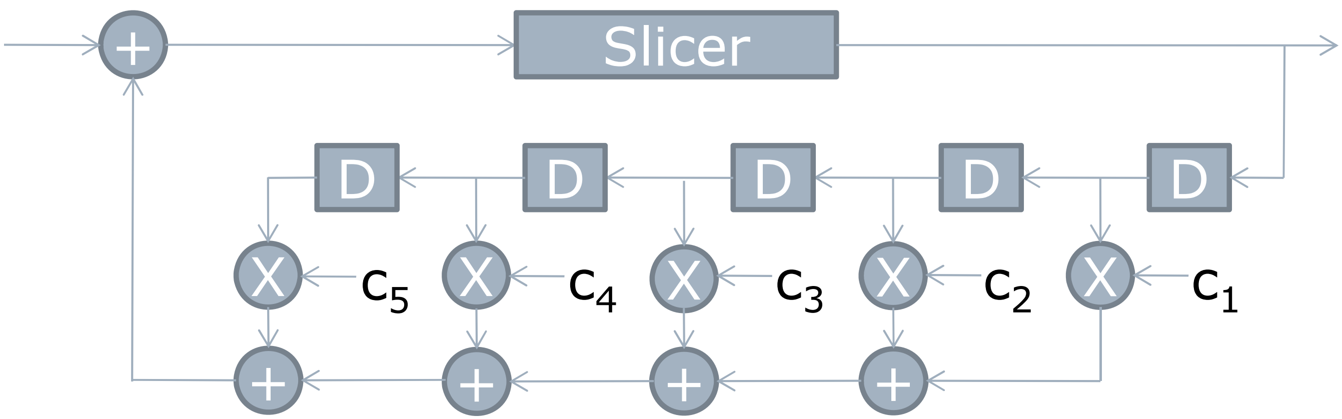
Peaking Filter Freq Response



Decision Feedback Equalizer

- Cancels post-cursor ISI
  - Equalization without noise enhancement
  - Implementation is challenging at high speeds
  - Error propagation can be an issue

- Coefficients are adapted using LMS



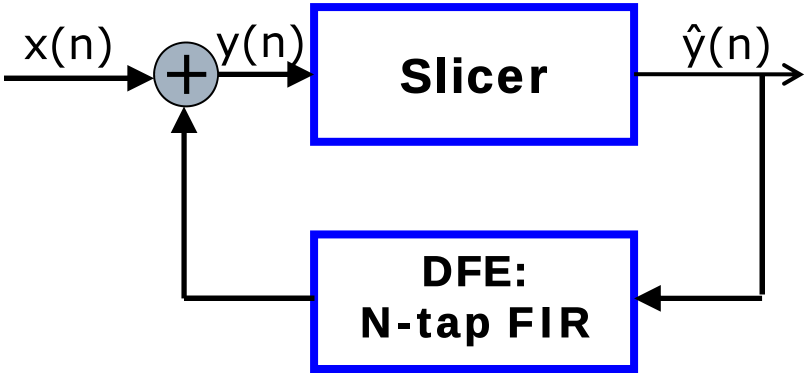
Analog DFE Challenges

- Closing the feedback loop with 1 UI (~40ps)
  - Binary symbols (+/-1) simplify multiply to add/subtract
- Feedback is susceptible to PVT variation
- As the number of taps increases, the capacitive loading on the summing node increases, which leads to reduced BW
- Implementation can be simplified by “unrolling” the DFE, or using tentative decisions
  - Costs additional area and power for parallel calculations

Unrolled DFE : 1-tap Example

- Conventional equation is

  $$y(n) = x(n) - \alpha\, \hat{y}(n)$$



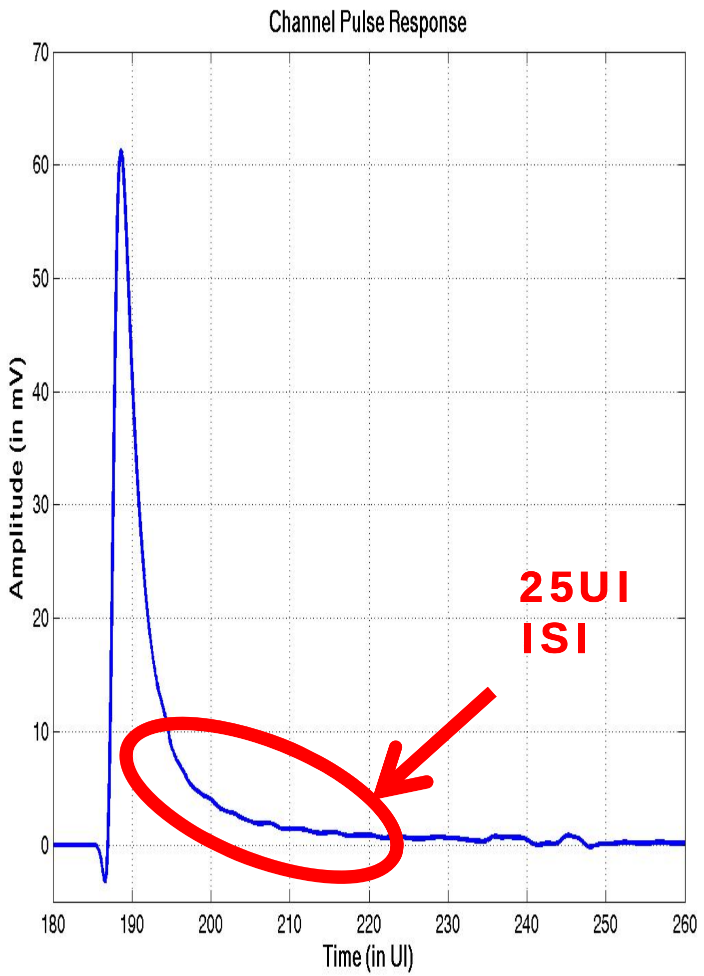
- Instead of subtracting the coefficient
  - Move the slicer level to include the compensation
  - Slice for each possible level, since previous value unknown
- Offset slicer levels by +/- α
  - Previous symbol selects correct value
- 2^L slicers for L taps

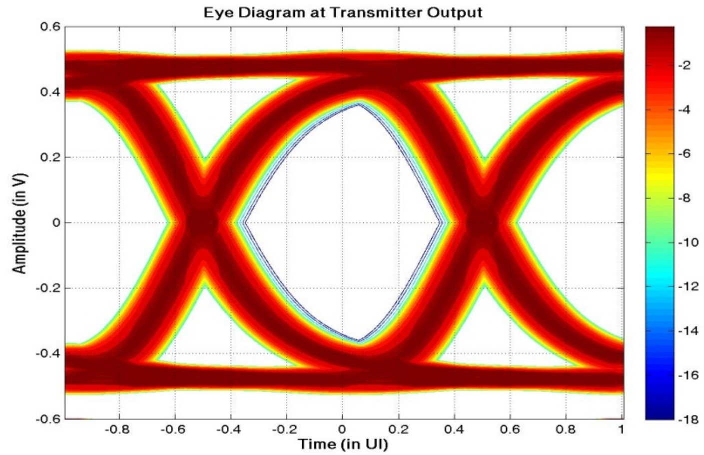
Analog Equalizer for 40in Backplane

- Peaking Filter
  - Peaking location and boost are adaptive
  - Peaking optimized to 12dB boost @ ~9GHz

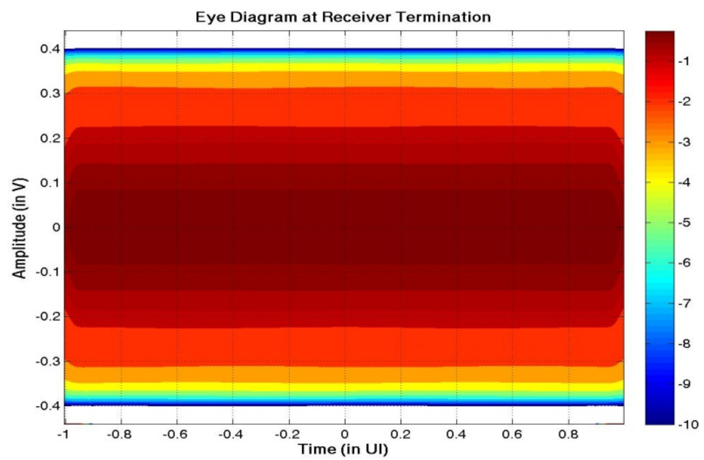
- DFE
  - 10-taps adaptively optimized to cancel postcursor
  - Taps can be constrained to limit error propagation

Pulse Response – At Rx Termination



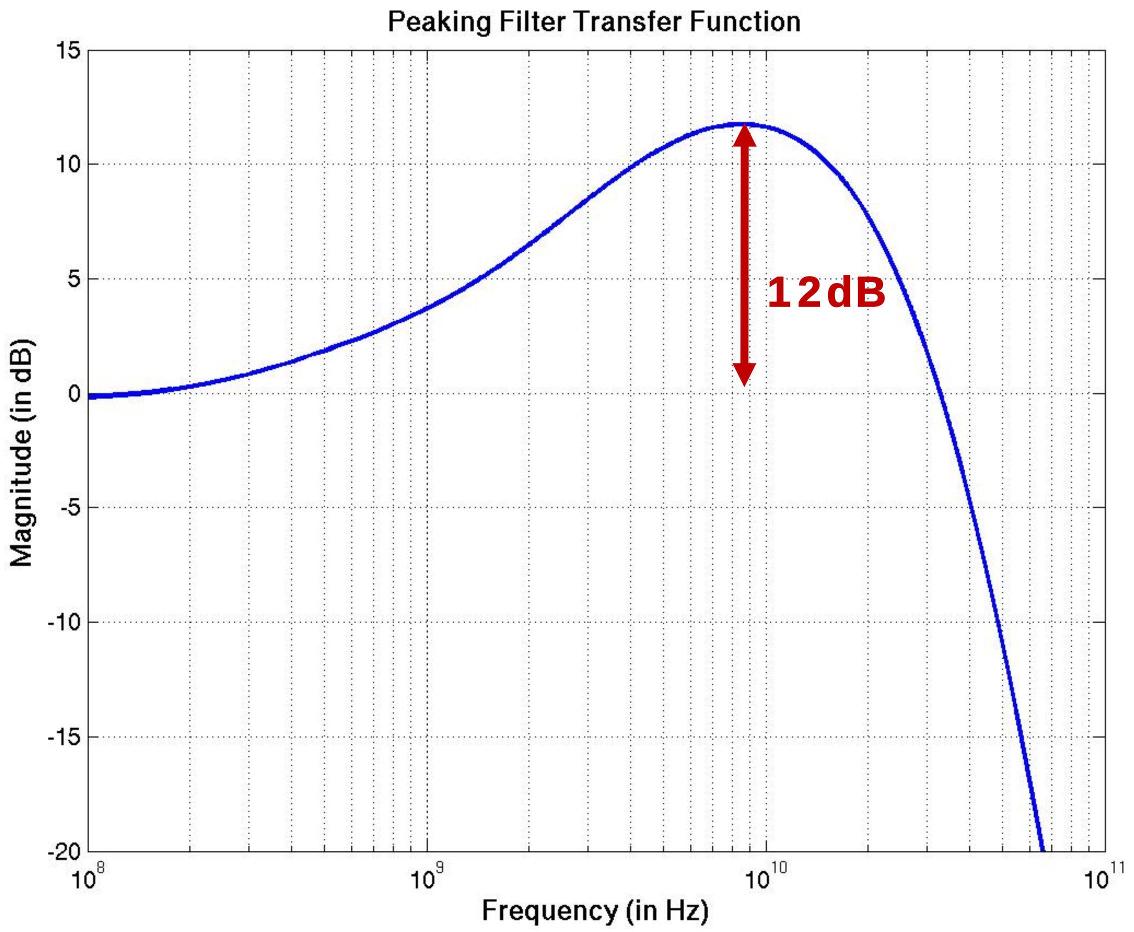


Eye At Tx

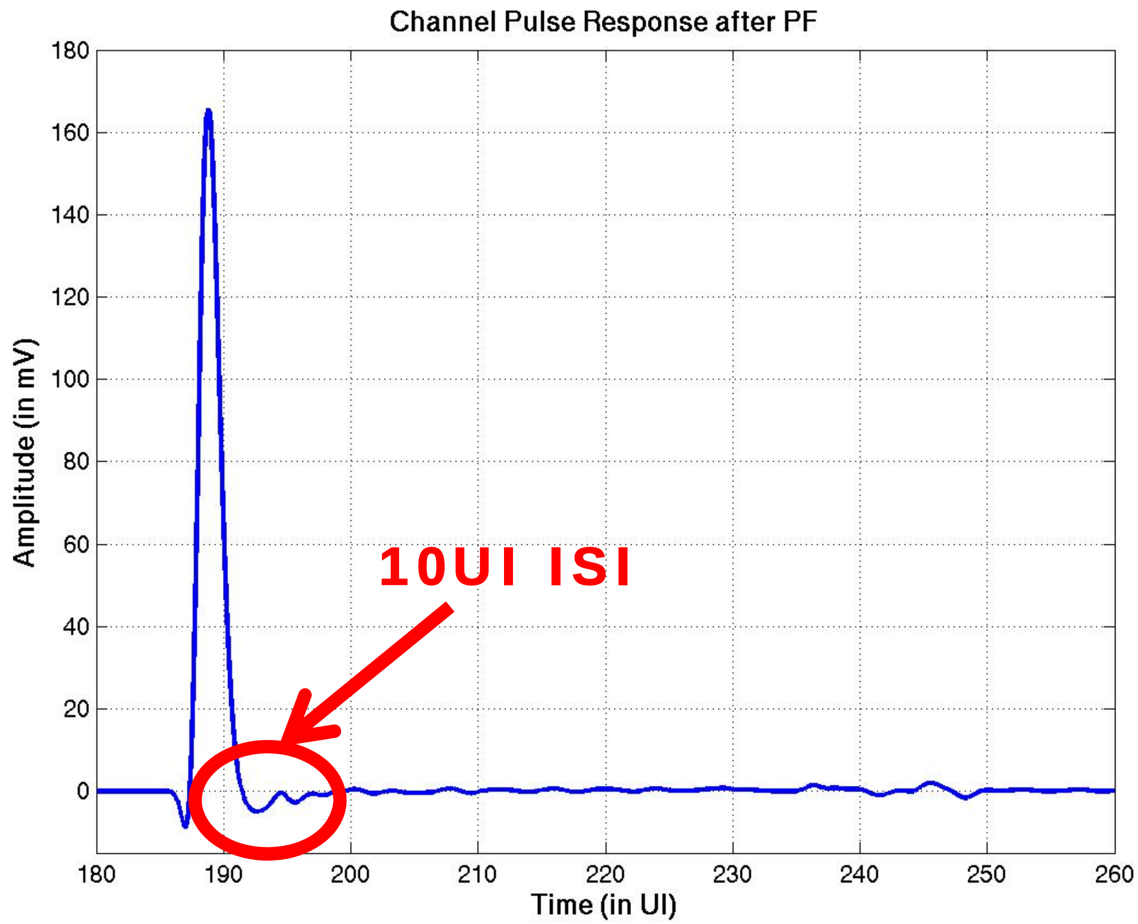


Eye At Rx

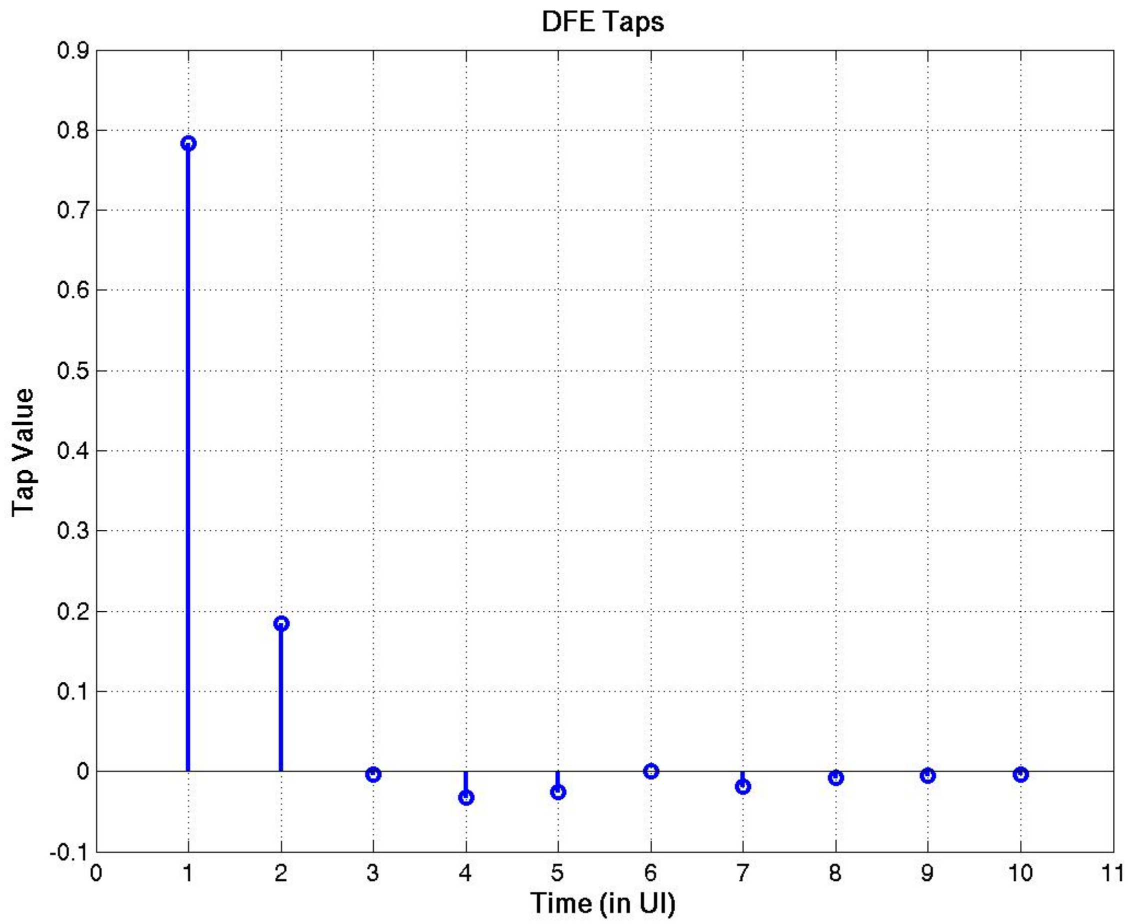
Optimized Peaking Filter



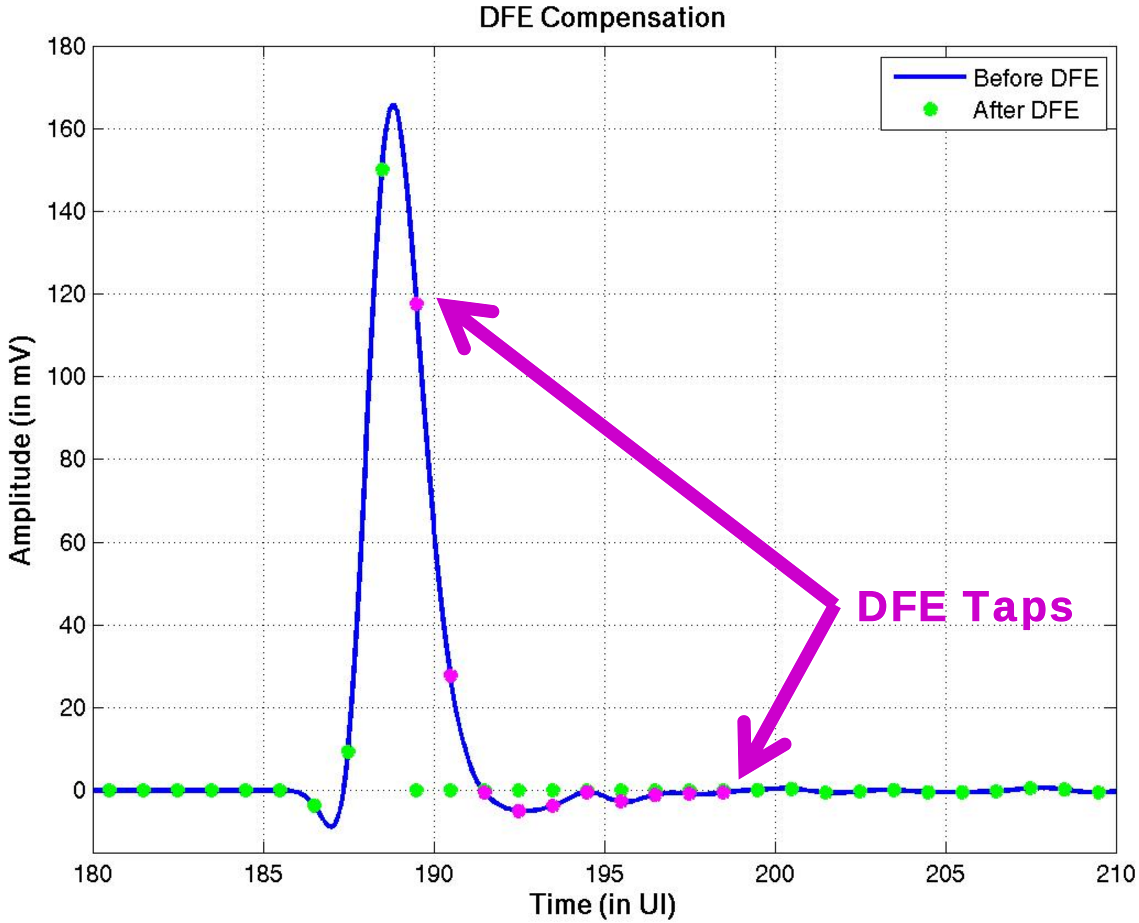
Pulse Response – After Peaking Filter



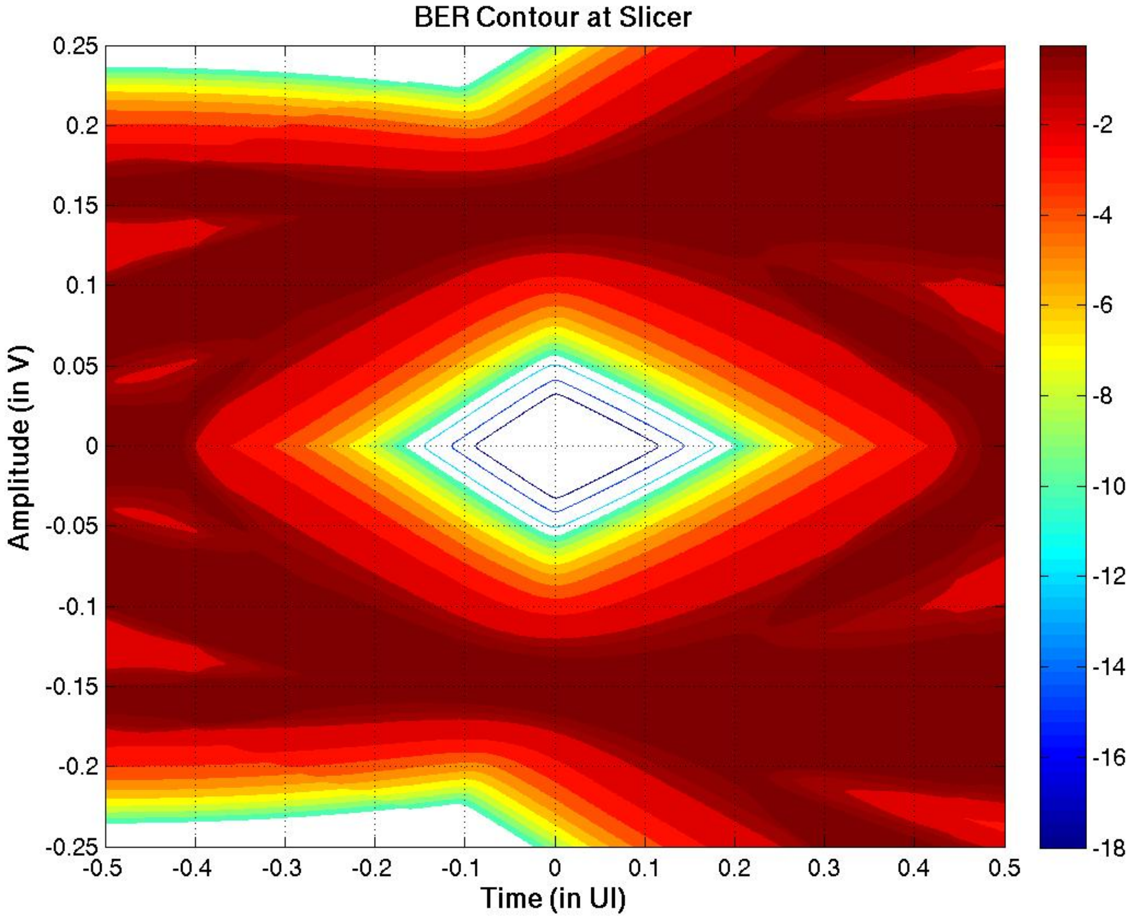
Optimized DFE Filter



Pulse Response – After DFE



Slicer Eye Diagram



VO = 102 mV

HO = 289 mUI

BER = 8×10^{-32}

SNR Margin = 4.4dB

Equalizer Architecture Options

- Many different ways exist to equalize the channel
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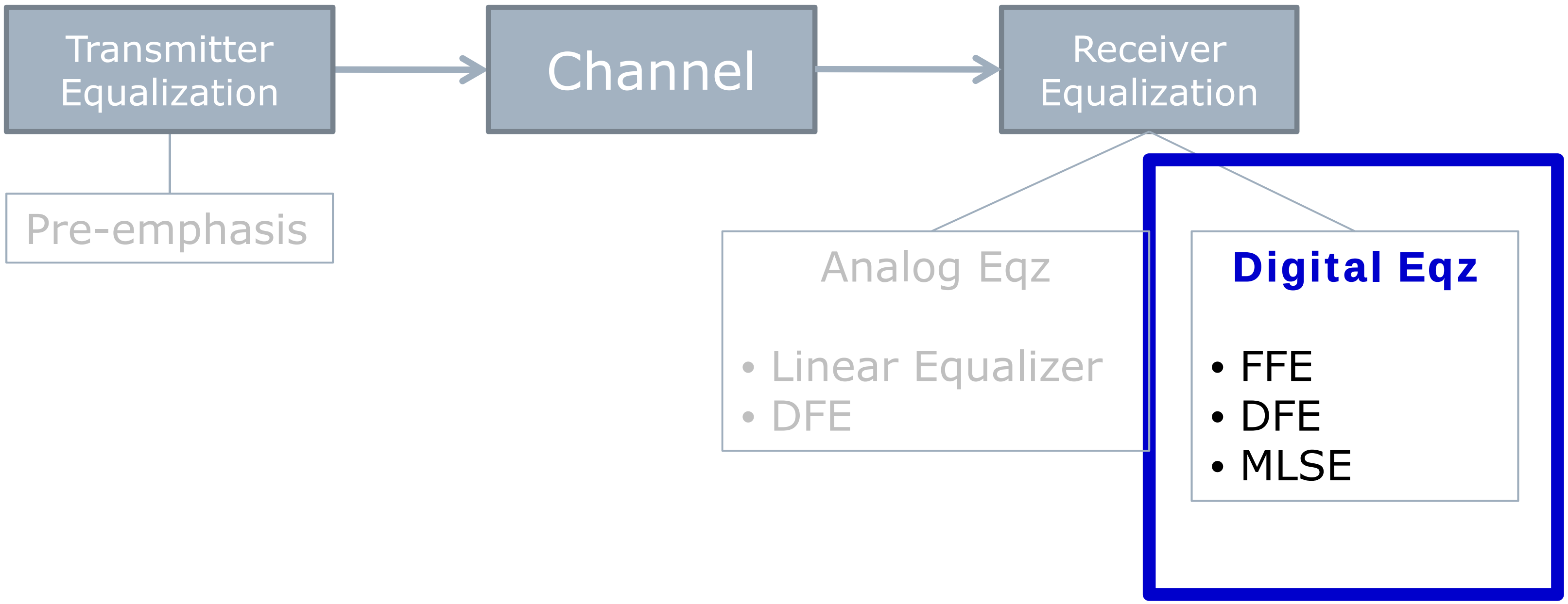
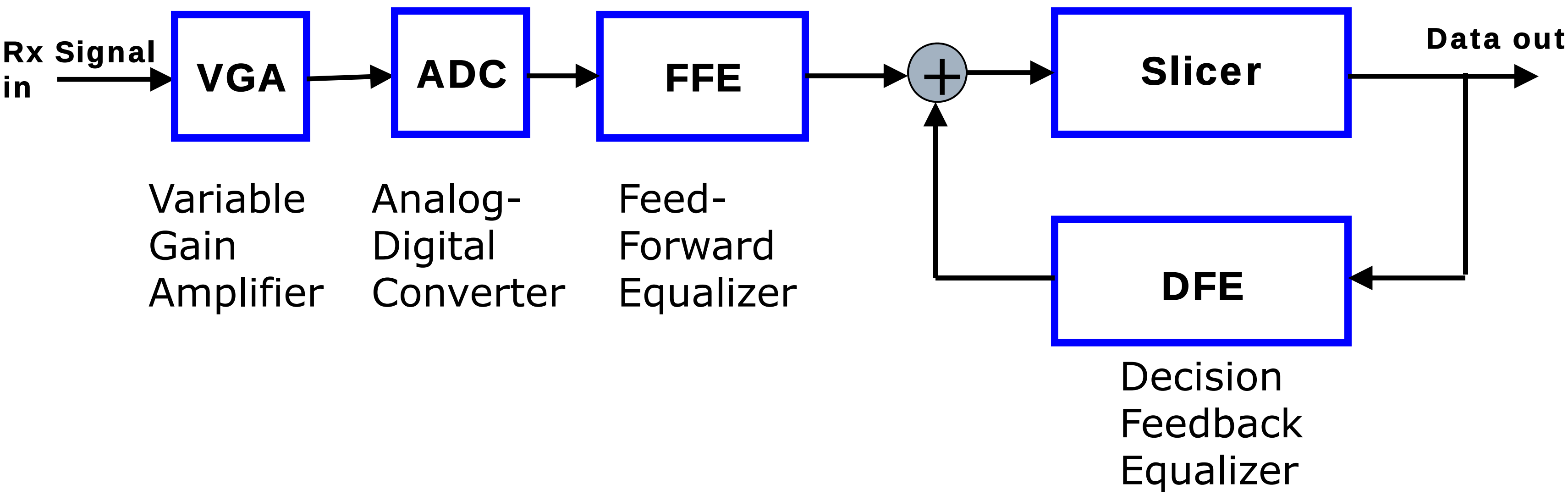


Digital Equalizer Options

- Most commonly used architecture is FFE + DFE
- Non-linear channels can benefit from MLSE equalizers
  - Performance comes at a steep area/power penalty
- Essential building block is Analog-Digital Converter
  - Very high sampling rate, and moderate resolution
  - 25Gsps ADC with ~5 ENOB

Digital Equalizer Architecture



Digital Equalizer Design Challenges

- Entire data path is high-speed and high resolution

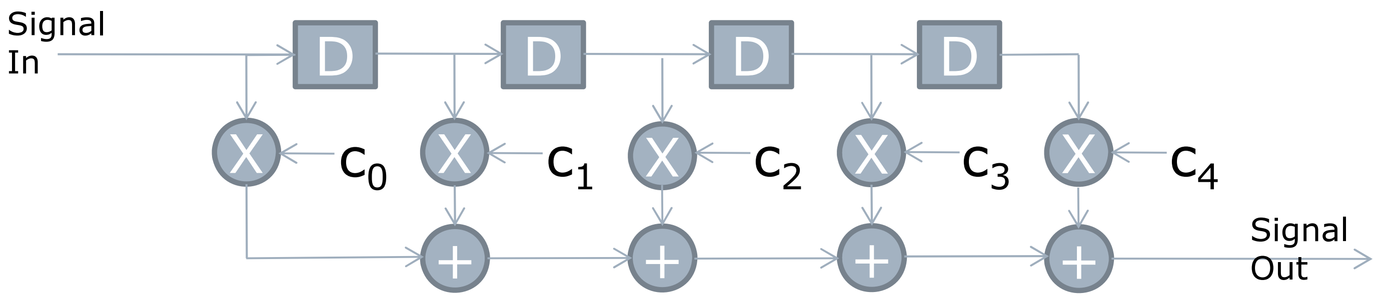
- Parallelized data paths allow efficient CMOS implementation
  - Cost of parallelization is area and latency

- FFE can be pipelined
  - Cost of pipelining is area and latency

- DFE is particularly challenging, cannot be pipelined
  - “Unrolled” architecture is the only option

Feed-Forward Equalizer

- Multi-tap FIR filter, typically spaced one UI apart (T-spaced)
- Goal is to whiten the noise and equalizer precursor ISI
- Coefficients are typically adapted, using Slicer-error based LMS



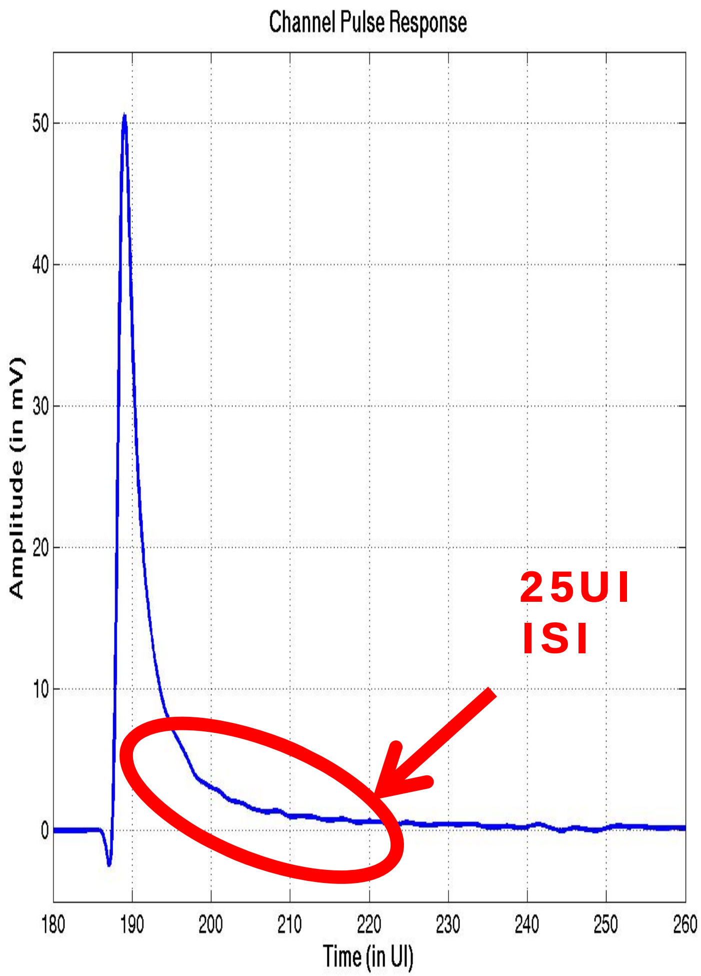
Equalizer Adaptation

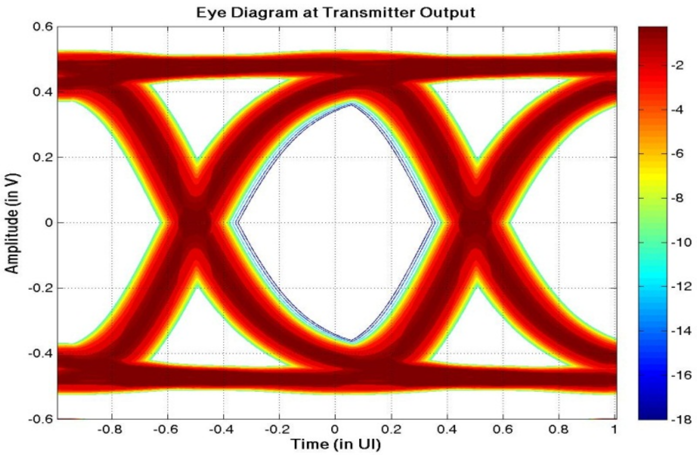
- Channel is not known a priori, and can vary significantly
  - Short backplane trace, long backplane trace
- Equalizer needs to “learn” the channel using “blind” adaptation
- Adaptation techniques are based on the “gradient search” or LMS algorithm
- Requires spectrally rich, scrambled data for stability

Digital Equalizer for 40in Backplane

- ADC
  - ENOB = 4.5
  - Sampling rate = 25 Gsps
- FFE
  - 10 taps adaptively optimized
  - T-spaced
- DFE
  - 10-taps adaptively optimized to cancel postcursor
  - Taps can be constrained to limit error propagation

Pulse Response – At Rx Termination





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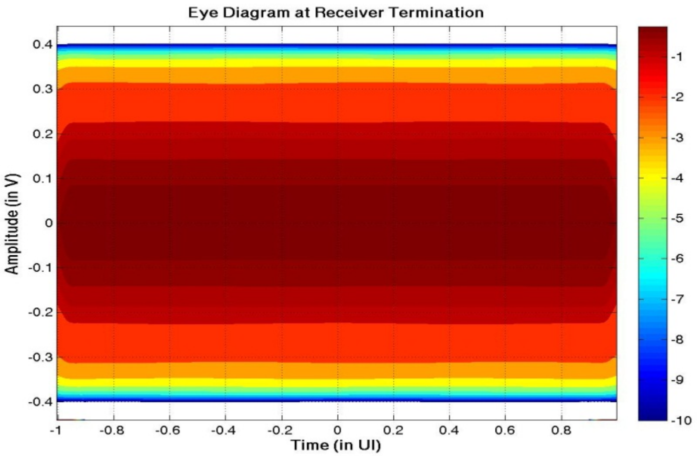
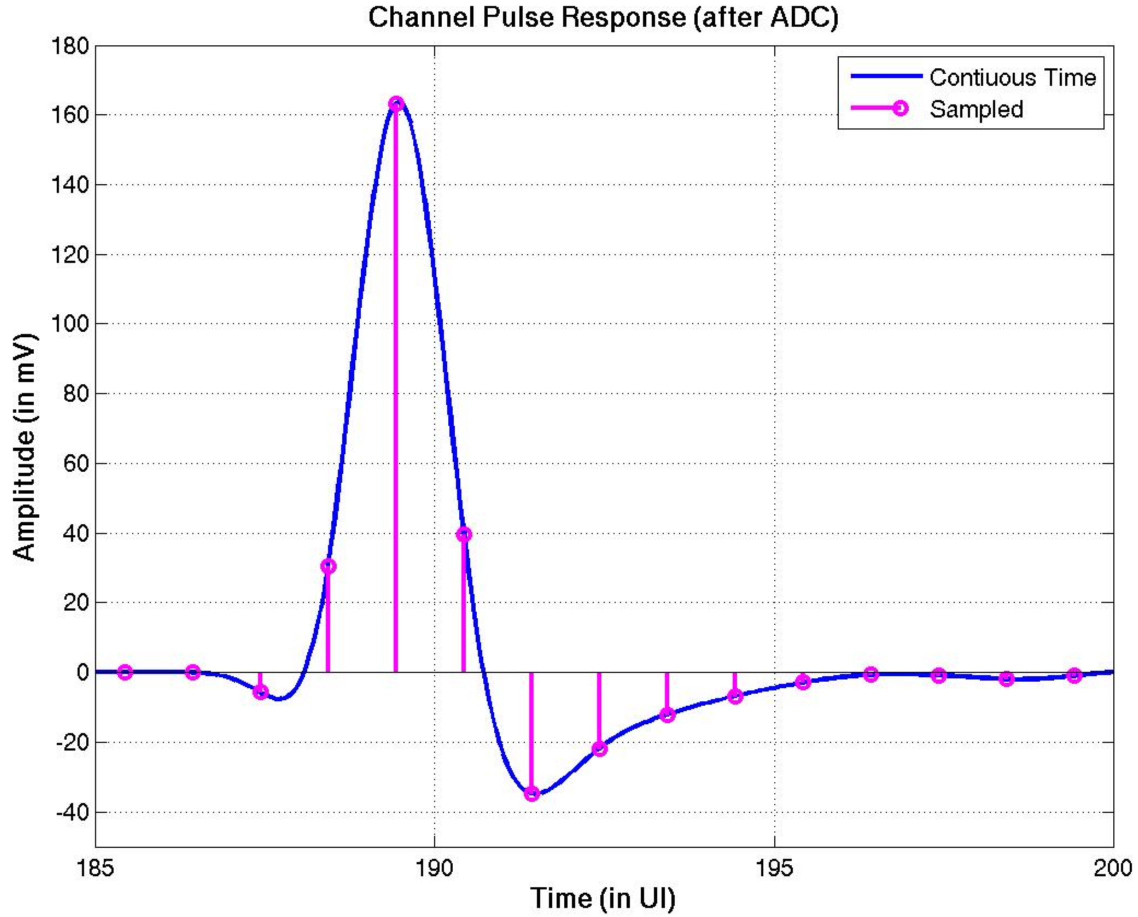
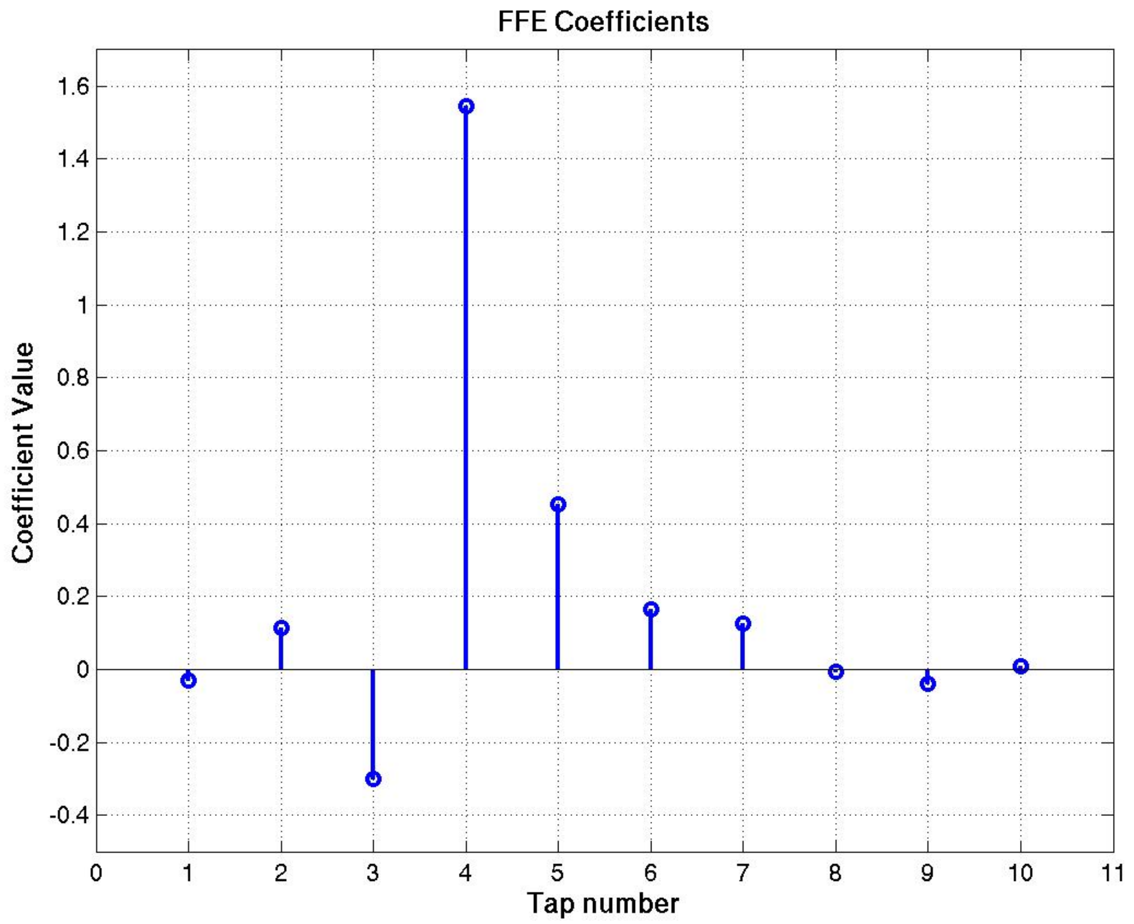


Eye At Rx

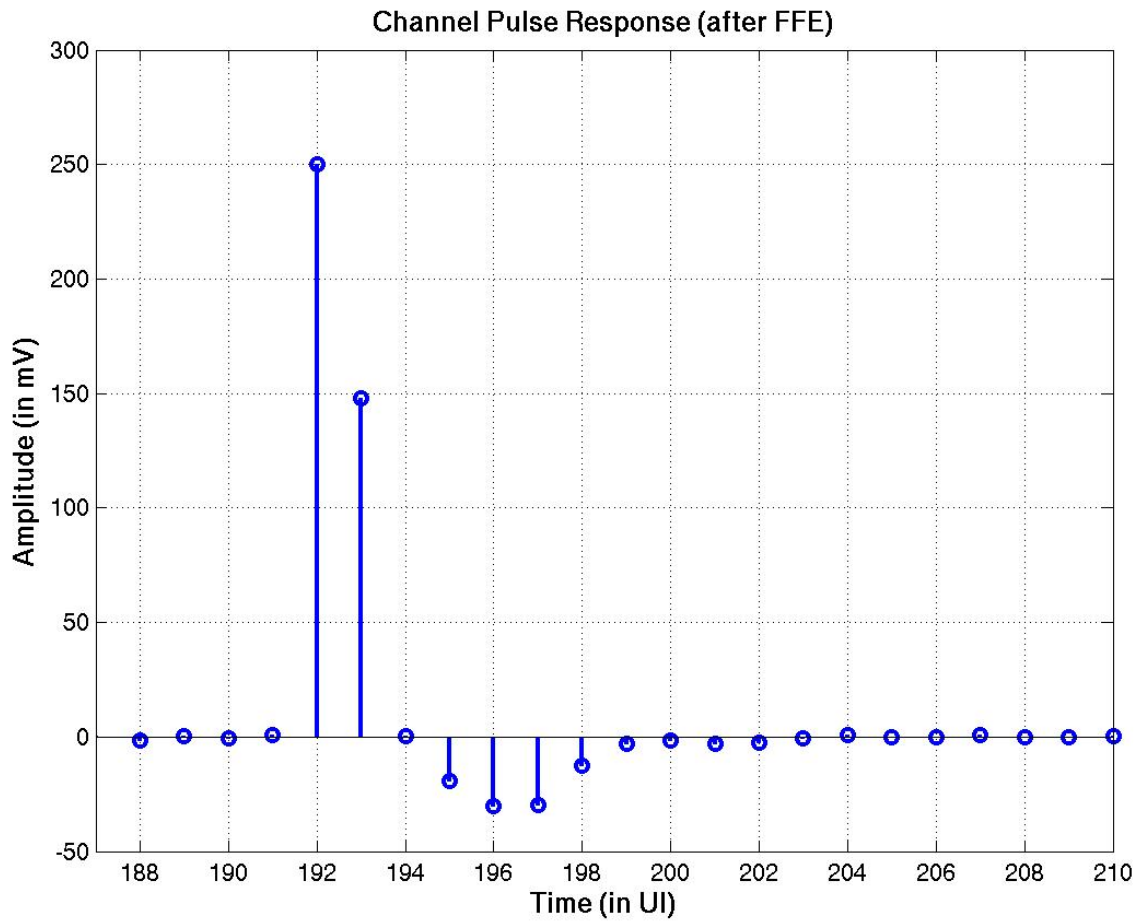
Pulse Response – after ADC sampling



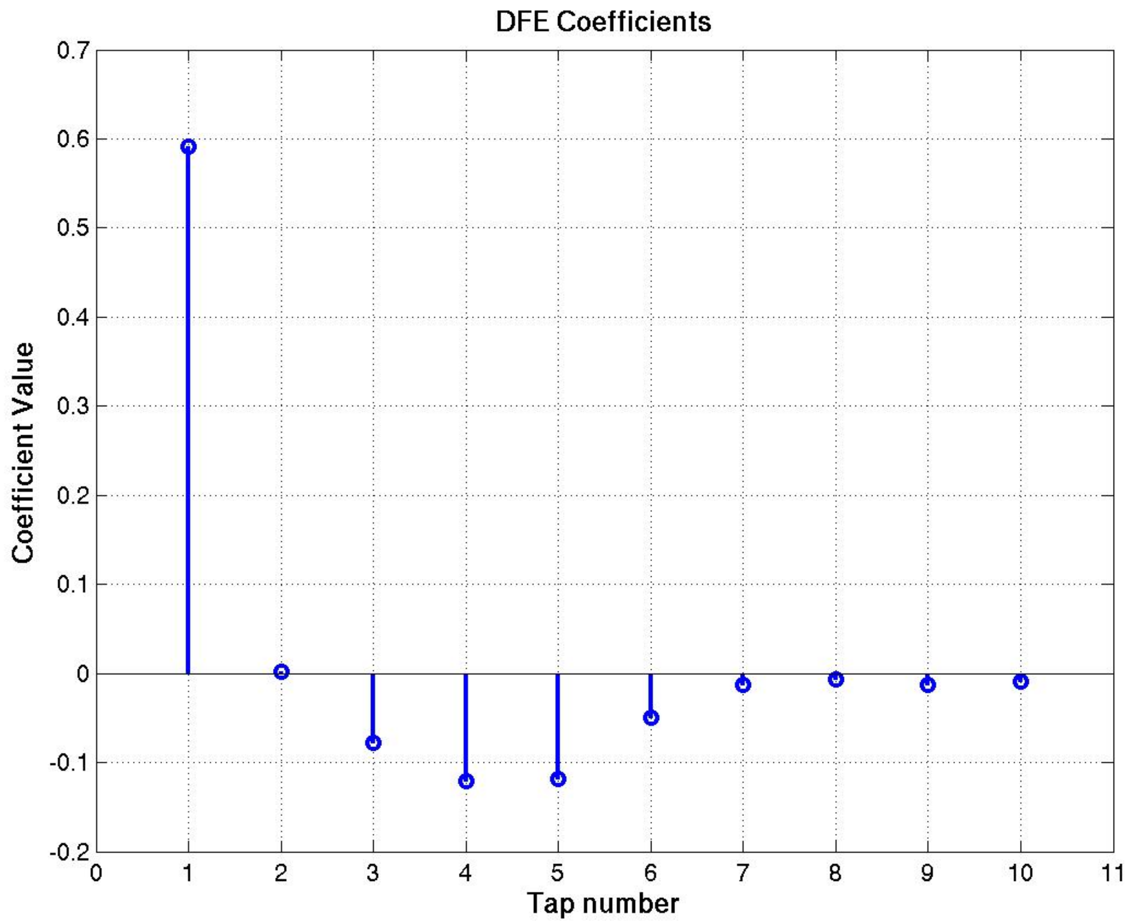
Optimal FFE Filter



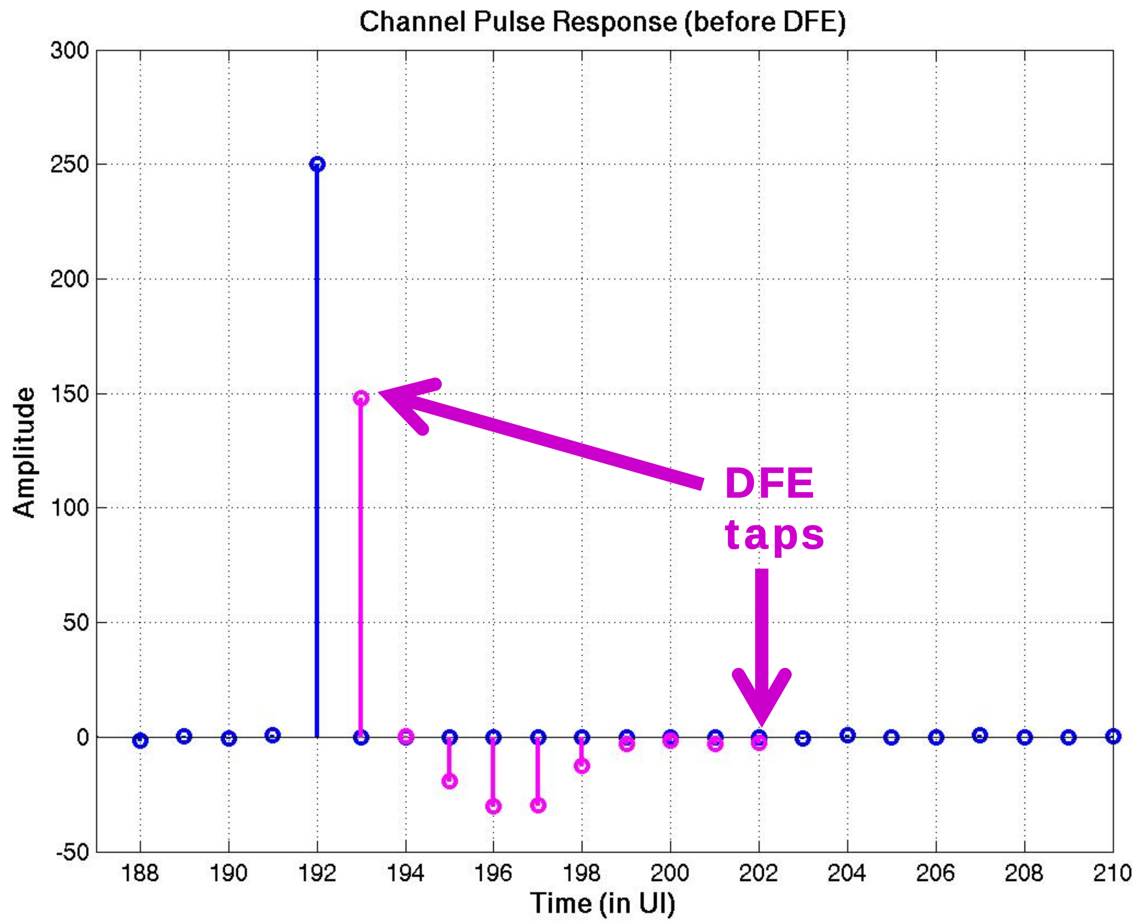
Pulse Response – after FFE



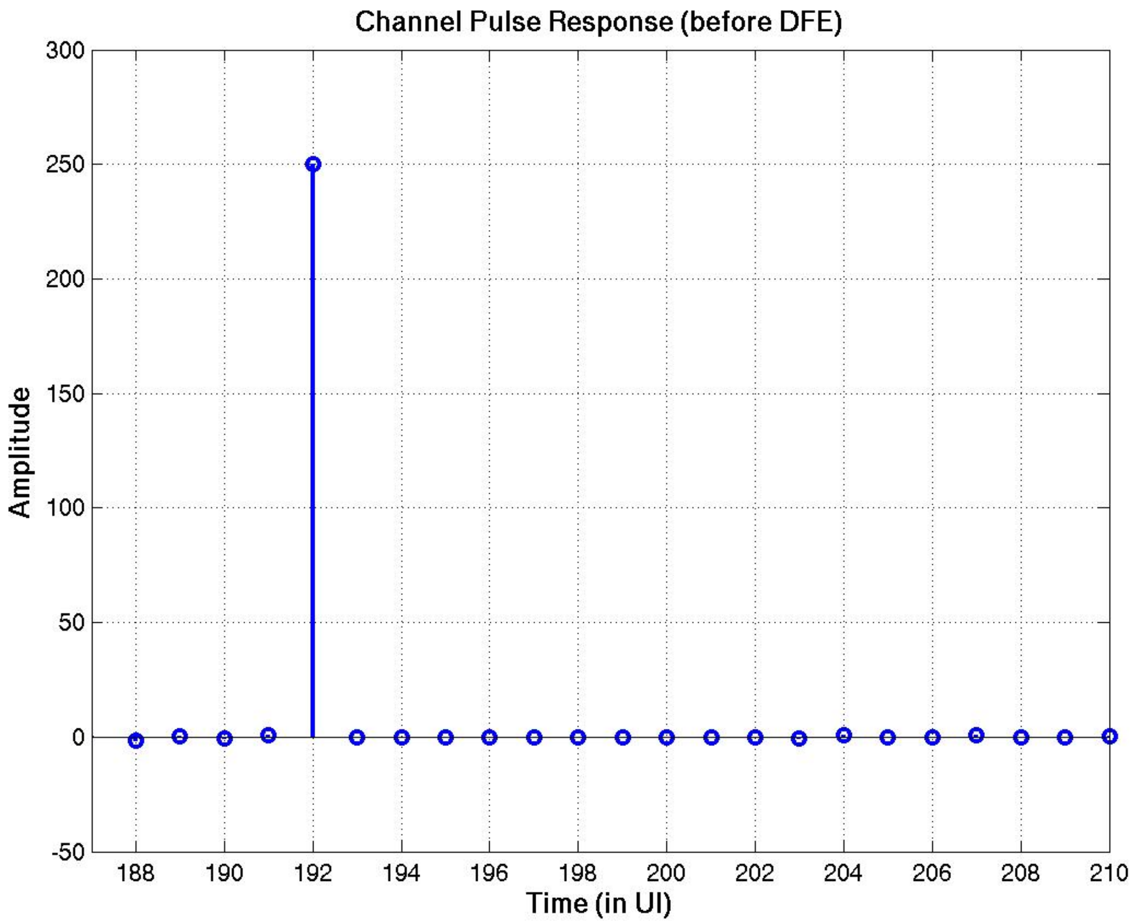
Optimized DFE Filter



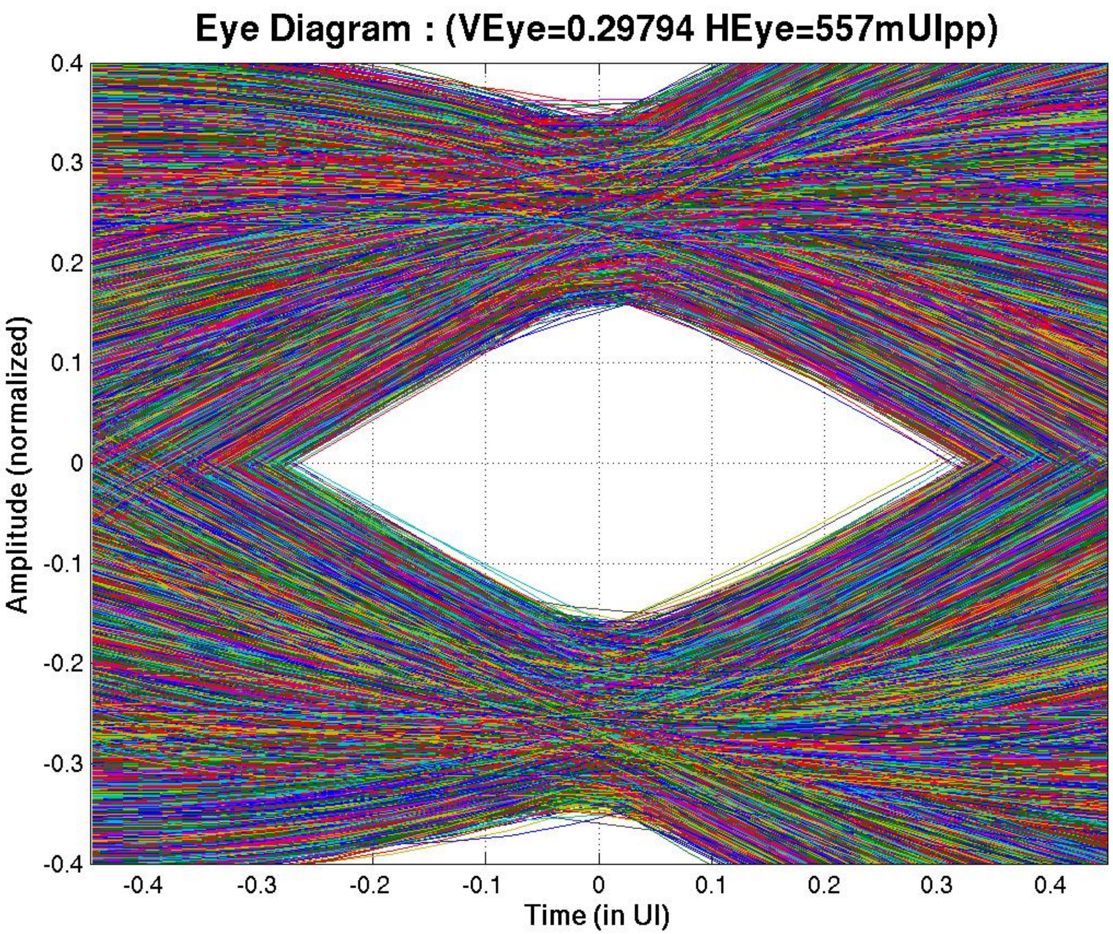
Pulse Response – before DFE



Pulse Response – after DFE



Slicer Eye Diagram



VO = 298 mV

HO = 557 mUI

BER = 8×10^{-36}

SNR Margin = 4.9dB

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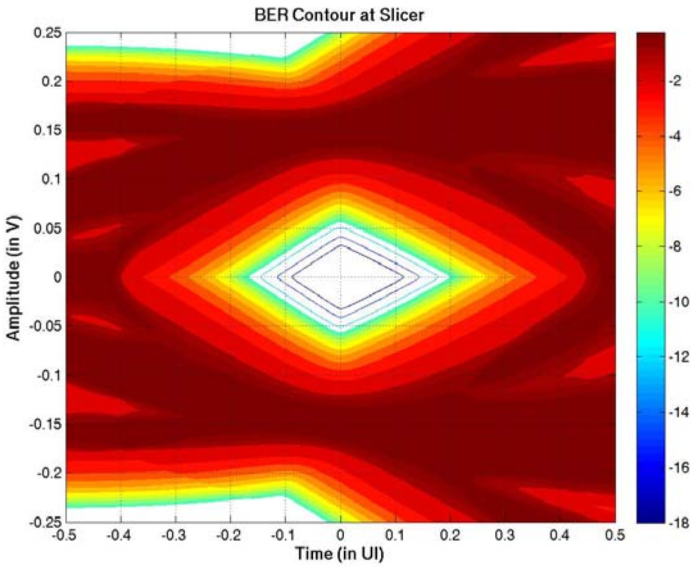
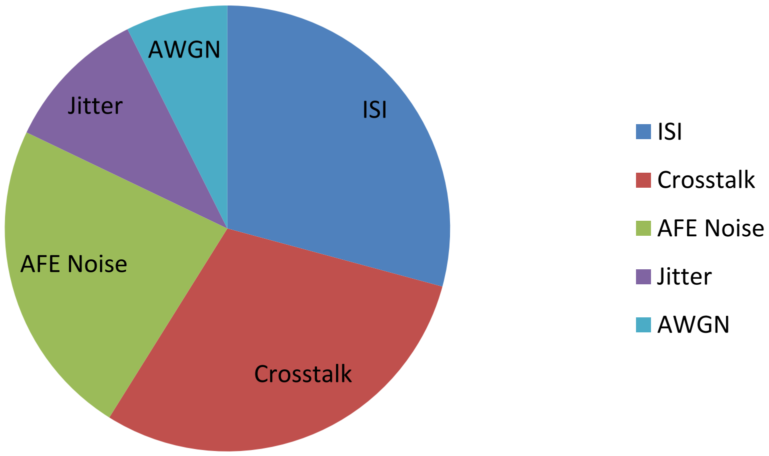
Analog Equalizer Performance

- SNR Margin = 4.4 dB
- BER = 8×10^{-32}

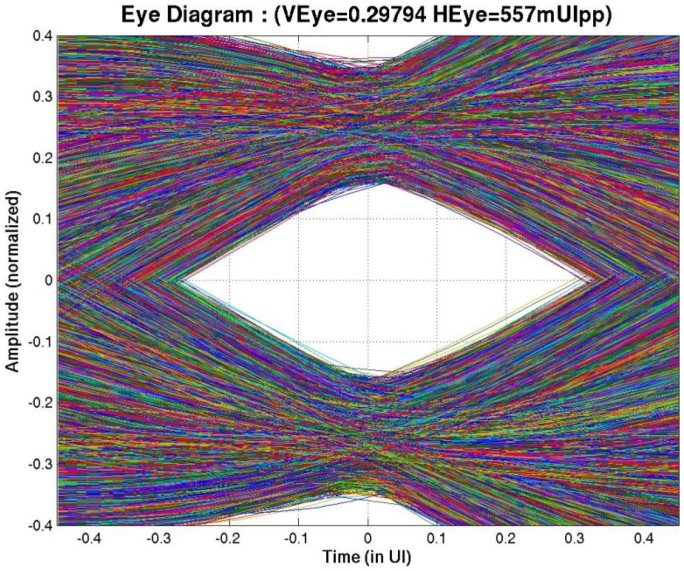


Breakdown of Noise Sources



Digital Equalizer Performance

- SNR Margin = 4.9 dB
- BER = $8x10^{-36}$



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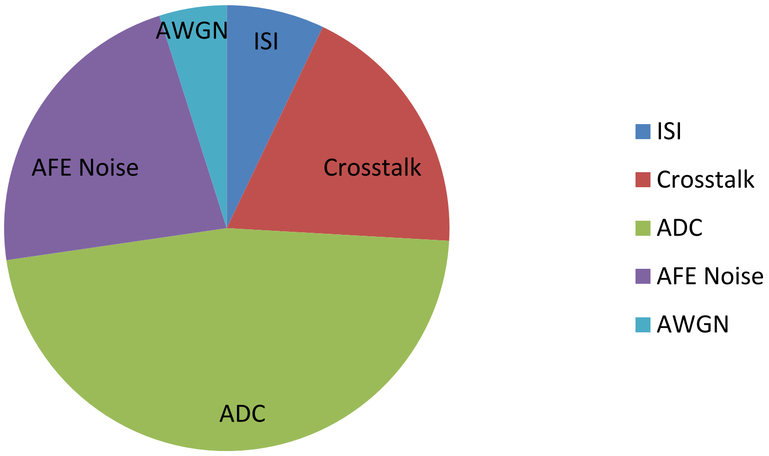


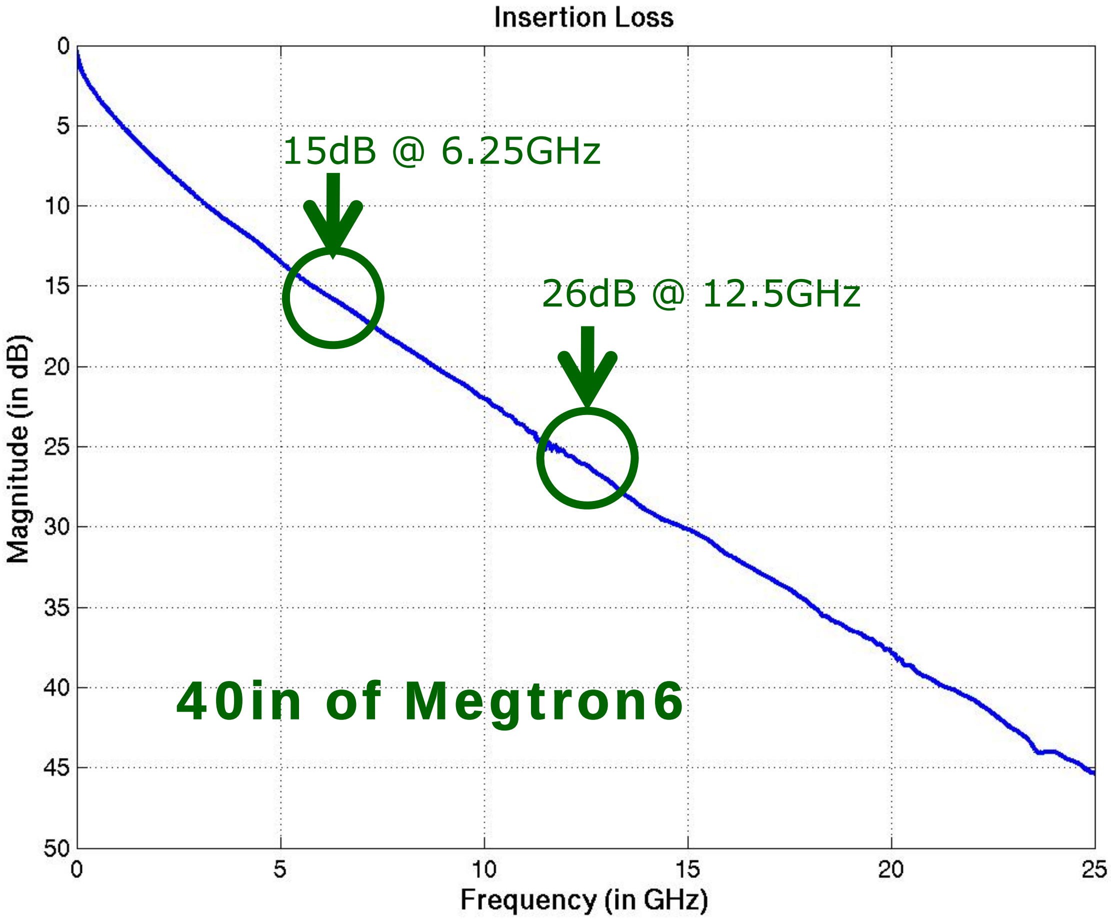
Cost Comparison

	Power	**Area**
10G Analog Serdes: PF + DFE	1	1
25G Analog Serdes: PF + DFE	**1.9**	**1.4**
25G Digital Serdes: ADC + FFE/DFE	2.3	2.4

25G Serdes Line Code Options

	NRZ	PAM-4
Signaling Rate	25 GBd	12.5 GBd
Nyquist Frequency	12.5 GHz	6.25 GHz
IL @ Nyquist	26 dB	15 dB

Insertion Loss Comparison

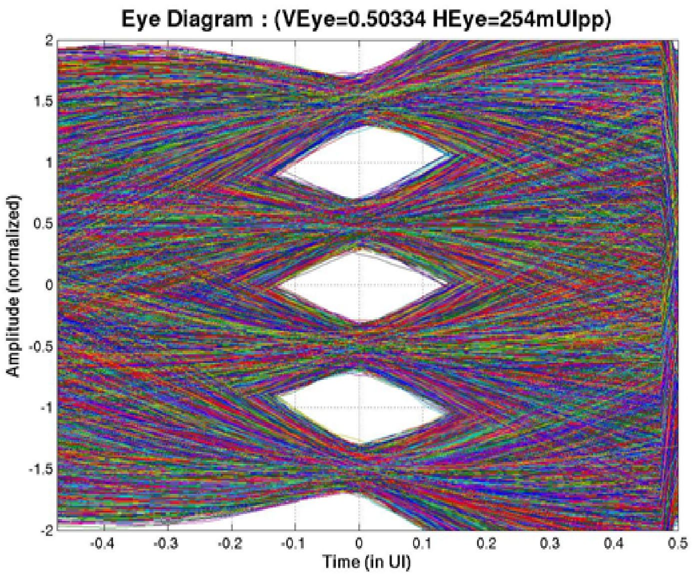


Digital Equalizer Parameters

- ADC
  - ENOB = **5.7**
  - Sampling rate = **12.5 Gsps**
- FFE
  - 10 taps adaptively optimized
  - T-spaced
- DFE
  - **2 taps** adaptively optimized to cancel postcursor
  - Taps can be constrained to limit error propagation

Digital Equalizer Performance

- SNR Margin = 5.4 dB
- BER = 6×10^{-40}



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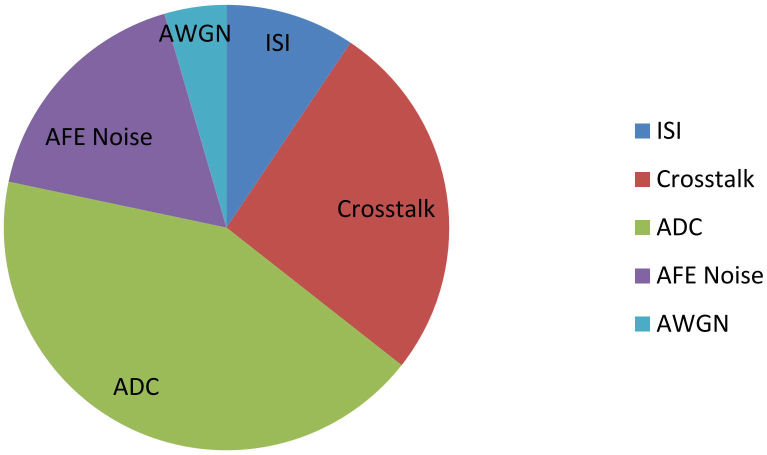

Cost Comparison

	Power	**Area**
10G NRZ Analog Serdes: PF + DFE	1	1
25G NRZ Analog Serdes: PF + DFE	1.9	**1.4**
25G NRZ Digital Serdes: ADC + FFE/DFE	2.3	2.4
25G PAM-4 Digital Serdes: ADC + FFE/DFE	**1.8**	1.5

Analog vs. Digital - Pros and Cons

Analog Equalizer

- Smaller area
- Lower power
- Suitable for high-scale integration in large ASICs

Digital Equalizer

- Higher performance
- Flexible architecture
- Powerful diagnostics
- Easier to port to smaller geometries
- Less susceptible to PVT variations

Future Direction

- Higher Multi-level line coding being investigated – PAM-8, PAM16
  - Signal processing becomes significantly more complex

- For future applications at 100+Gbps, more efficient line coding is a possibility, e.g., DMT

Summary

- Serdes Channels vary widely from application to application
- As data rates increase, sophisticated equalization is necessary
- Wide spectrum of equalization techniques is available
- Choice of optimum equalization method is a tradeoff between power/area and performance

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THANK YOU!

QUESTIONS?

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