Spur-Free Switching Power Converters for Analog and RF Loads

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Ayman Fayed, Assistant Professor
Director, Power Management Research Lab
Electrical & Computer Engineering, Iowa State University

POWER MANAGEMENT RESEARCH LAB

Outline

- Personal Background & Research Group
- Power Management → The story
- The Switching Noise Problem
  - Types of power supplies
  - Spectral characteristics of switching noise
  - Impact on noise-sensitive Analog/RF Loads
- Switching Noise Mitigation Techniques
  - Time-domain Approaches
  - Frequency-domain Approaches
- Constant Cycle Frequency Hopping for Spur-Free Operation
- Power Management and Formal Education → If time permits

Personal Background & Research Group

- M.Sc. and Ph.D. from The Ohio State University, Columbus, Ohio
- Nine years at multiple business units at TI → High-speed wire-line transceivers, ADCs for RF CODECs, PM for multi RF cores SoCs
- Assistant Professor and Director of the Power Management Research Lab (PMRL) at the Dept. of Electrical & Computer Engineering at Iowa State University since Jan. of 2009
- 6 Ph.D. Students working on projects sponsored by NSF, RCI, State of Iowa, TI, and National Semiconductors
- Alumni at TI and Broadcom

Research Interests

- Areas of expertise & Research Interests
  - Embedded Power management circuit and system design for Mixed-signal/RF SoCs and multi-core processors
  - Supply Modulators for RF Polar PAs
  - Class-D Audio Power Amplifiers
  - Energy Harvesting for power-restricted systems
  - Particular emphasis on fully integrated implementations in nanometer CMOS and GaN technologies

Power Management: What is it?

- A System Designer → Task oriented
- A Digital Designer → Dynamic Voltage Scaling
- A Chip Architect → Power Delivery
- Analog/PM Designer → It is not only about "managing" how power is being used, conserved, or distributed

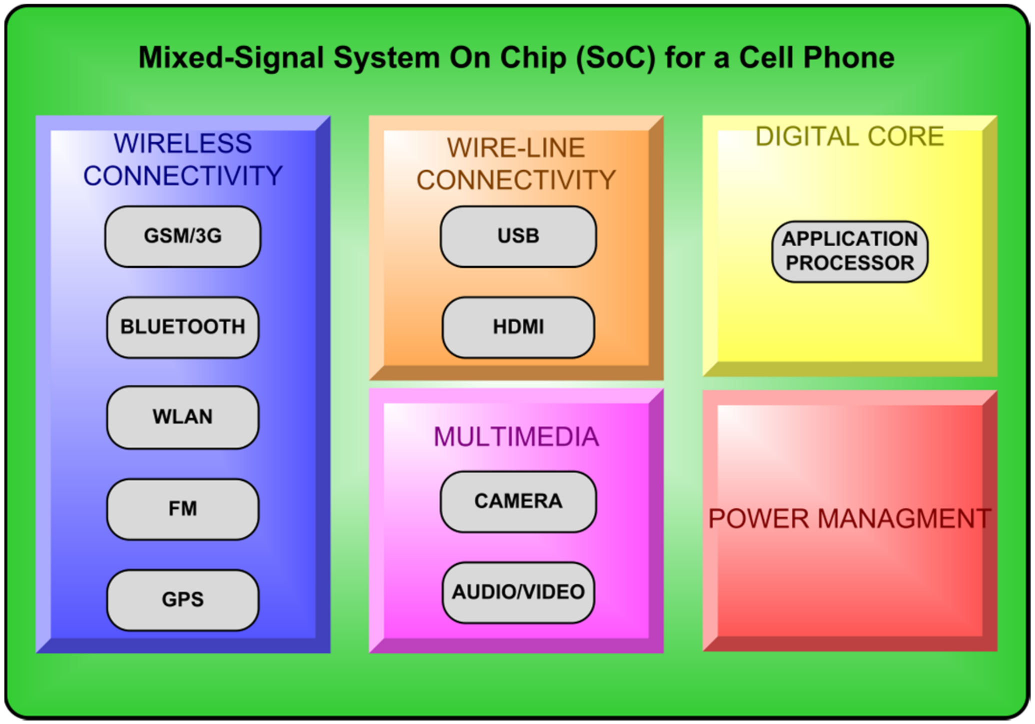
Power Conversion, Regulation, and Monitoring

Reemergence of Power Management

- Gaining a front seat role in VLSI systems today
  - Isn't it just the traditional good old power electronics!! What's new?
- The battery life challenge
  - Slow pace battery technology development
  - Focus has been on power consumption reduction → technology scaling, low voltage/power design → diminishing returns?
  - The efficiency of how power is converted and delivered from the battery to the system must be revisited for any further improvement

Reemergence of Power Management

- Cost & Size challenge → The SoC era
  - Analog/Digital/RF is successfully fully integrated with minimal external components → Cost-effective & Compact
  - Large passive components → Expensive, Bulky, not integrate-able
  - Many package pins are needed



PM is becoming a real cost, size, and performance bottleneck

Reemergence of Power Management

- Design & Performance challenge
  - Adaptability to different power sources
  - Large number of independent on-chip power domains → in order to further reduce power
  - With massive integration, there is no enough package pins to deliver all required power supply domains externally
  - Thermal efficiency
  - Efficiency often contradicts noise → Analog/RF loads are victims

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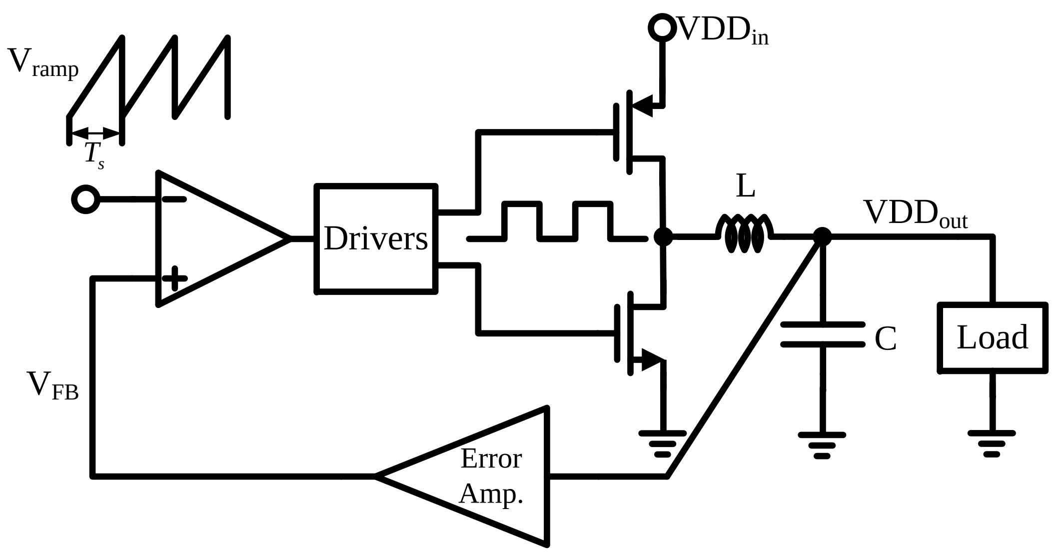
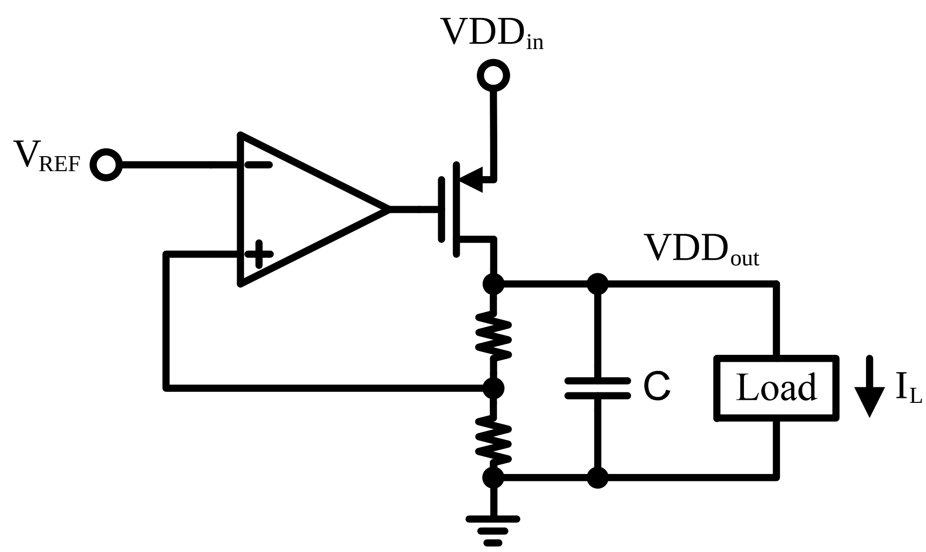
Power Supplies: Basic Circuits



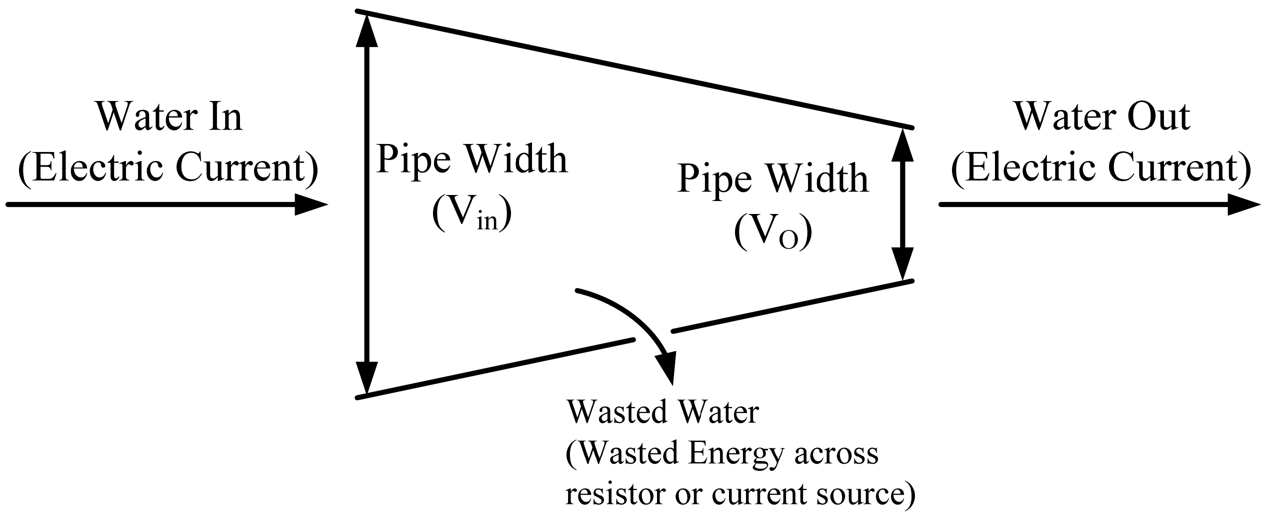


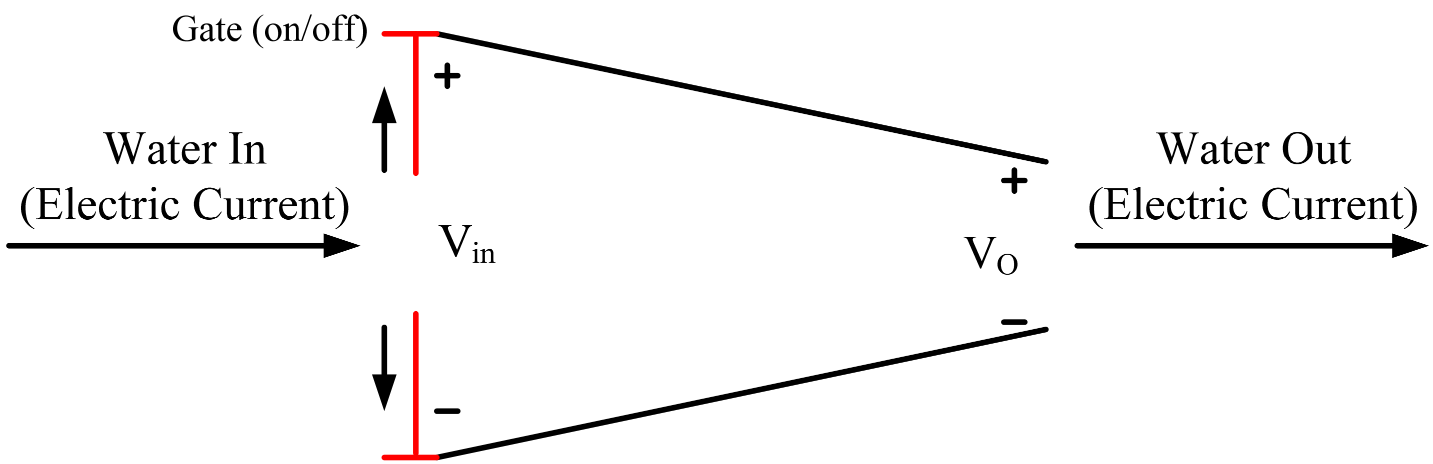
- ◆ **Switching Regulators**
  - Step up, down or both
  - Efficient, noisy, large cost/size overhead

- ◆ **Linear Regulators**
  - Only step-down
  - Inefficient, low noise, relatively small cost/size overhead

Power Supplies: Basic Circuits

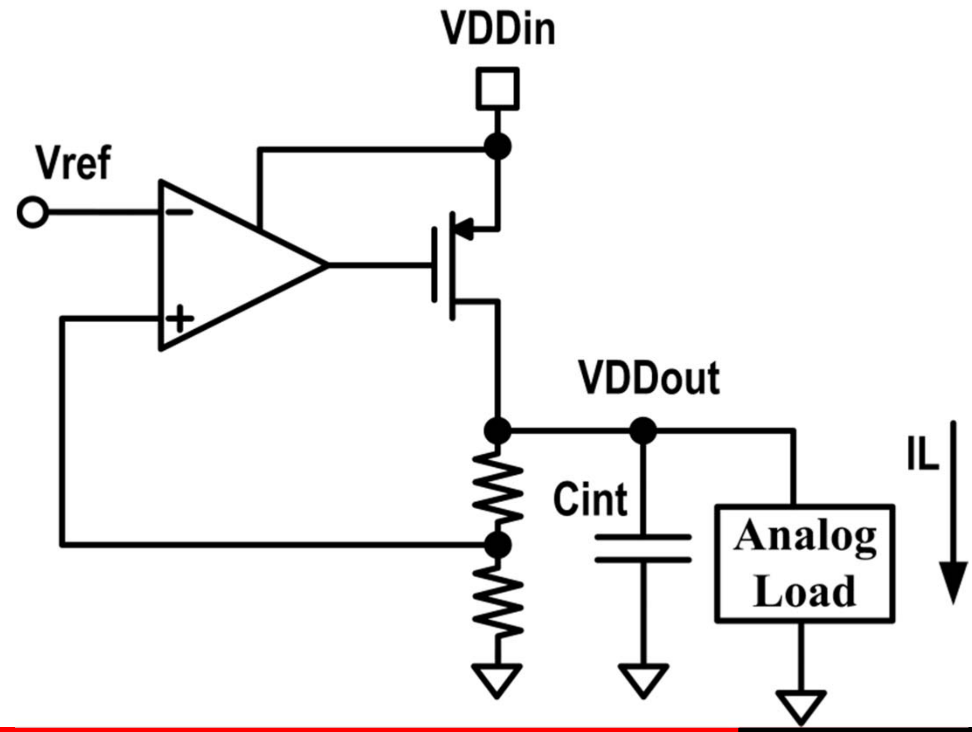
- From efficiency and noise point of view





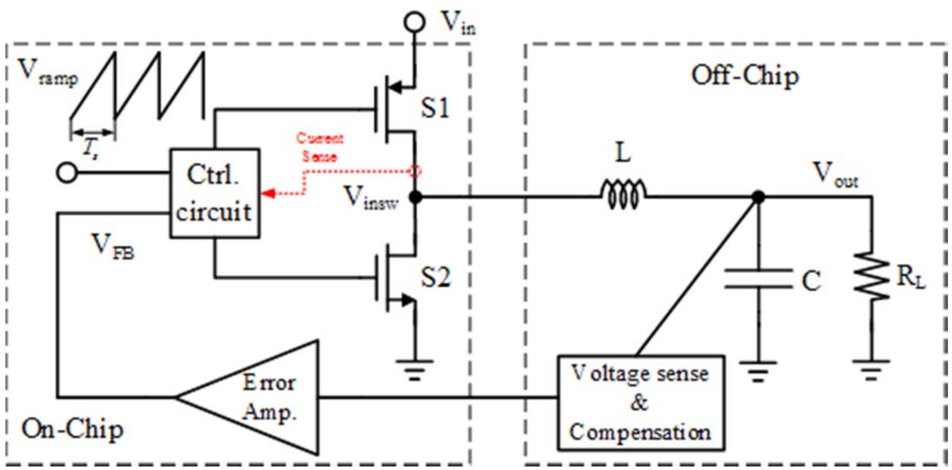
Linear Power Supplies: Efficiency

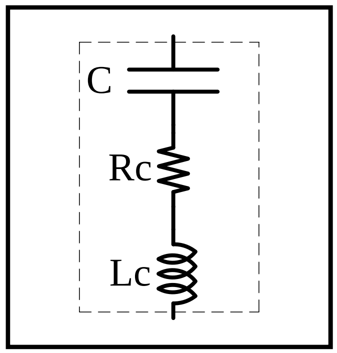
- Voltage scaling is often needed to improve the efficiency of many analog/RF circuits → Supply-switched PAs and polar modulation
- Linear regulators render voltage scaling ineffective for Analog/RF loads

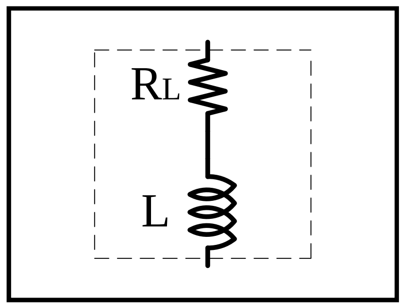


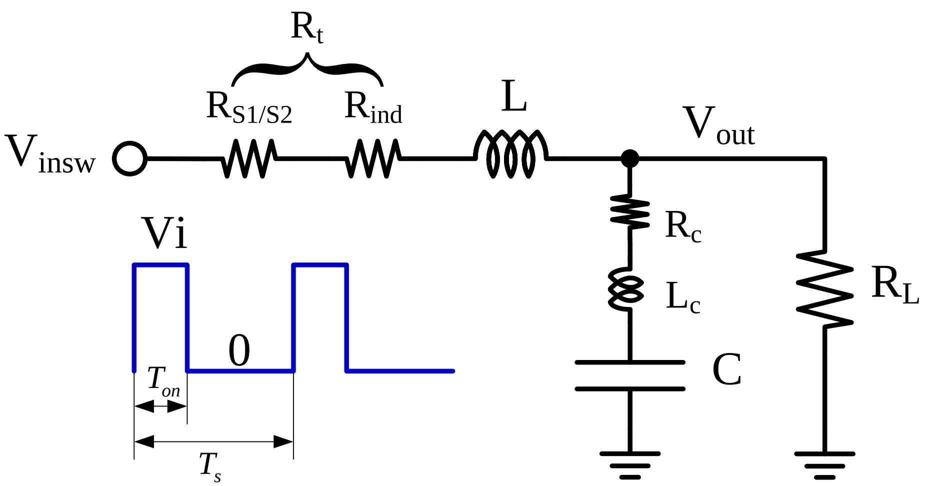
Switching Power Supplies: Noise

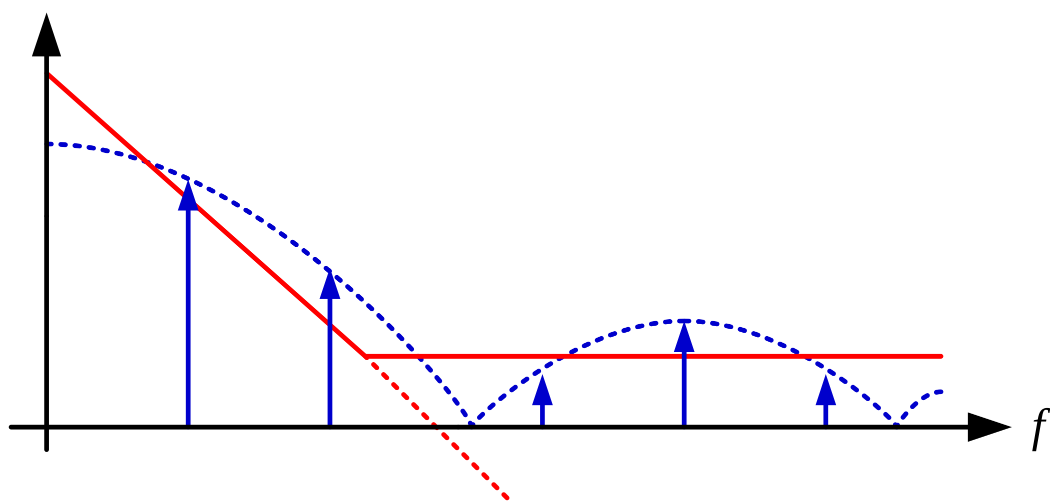
- The switching node is supposed to be filtered out by a sharp second-order low-pass function



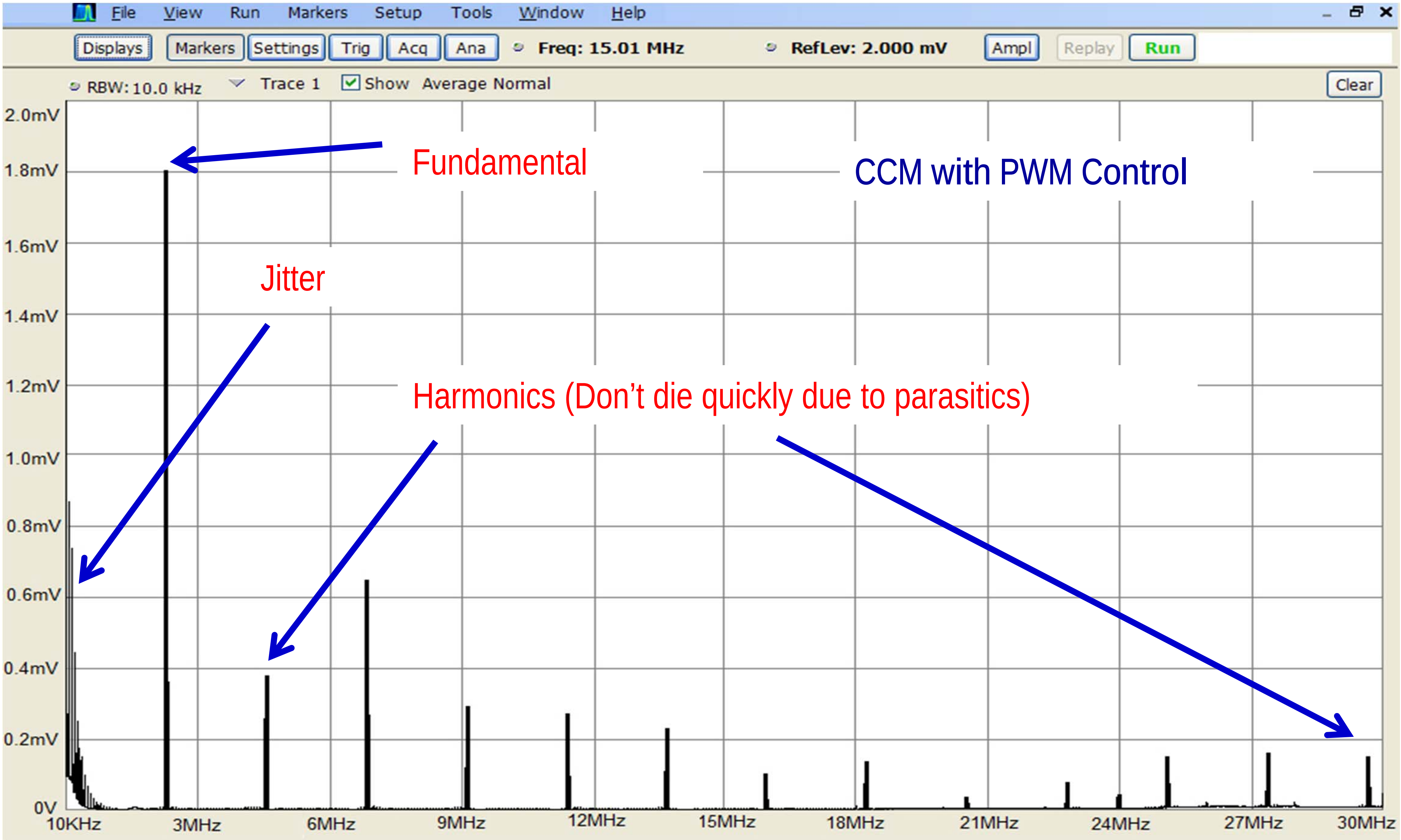




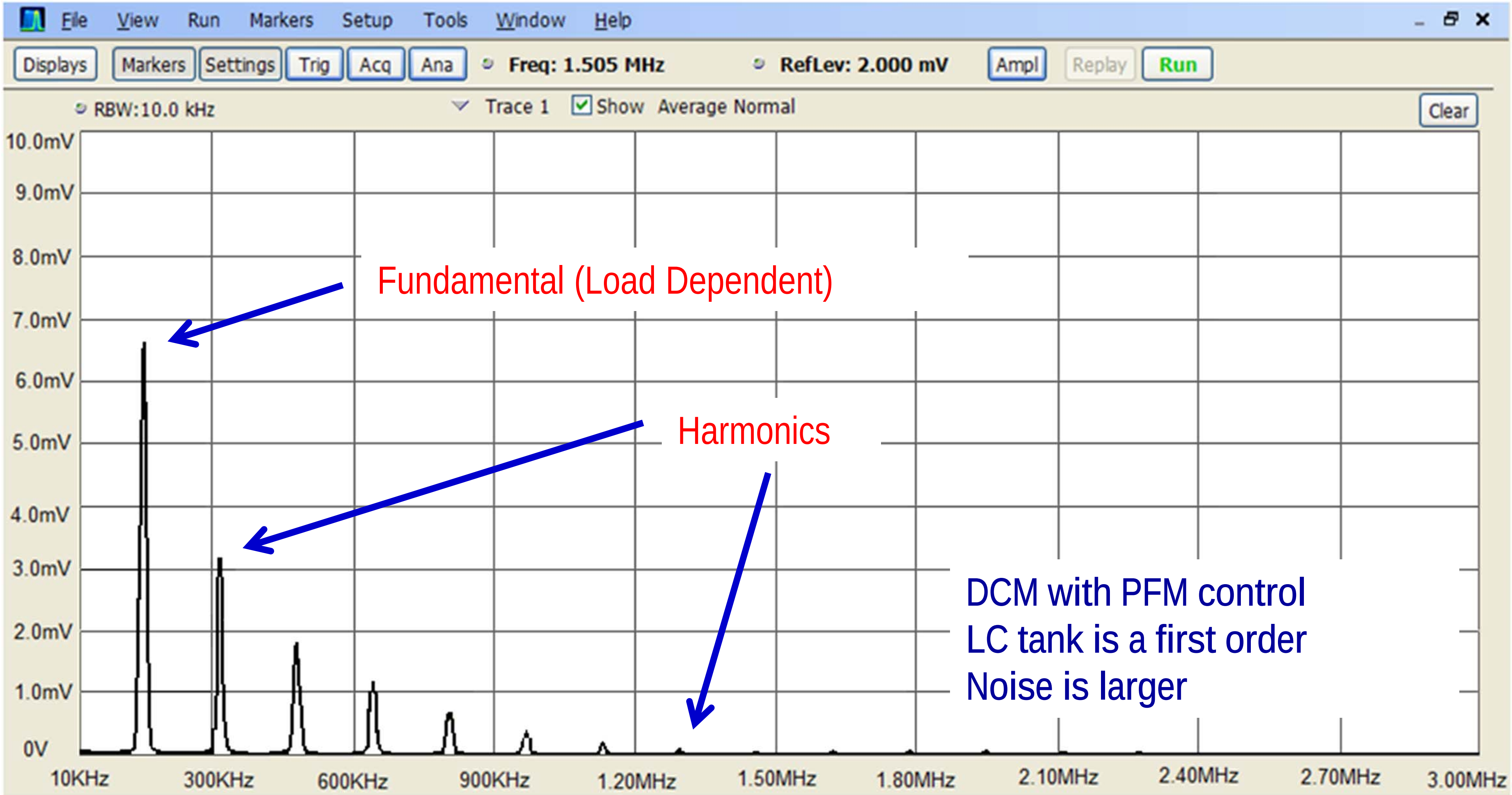




Switching Noise: Frequency-Domain

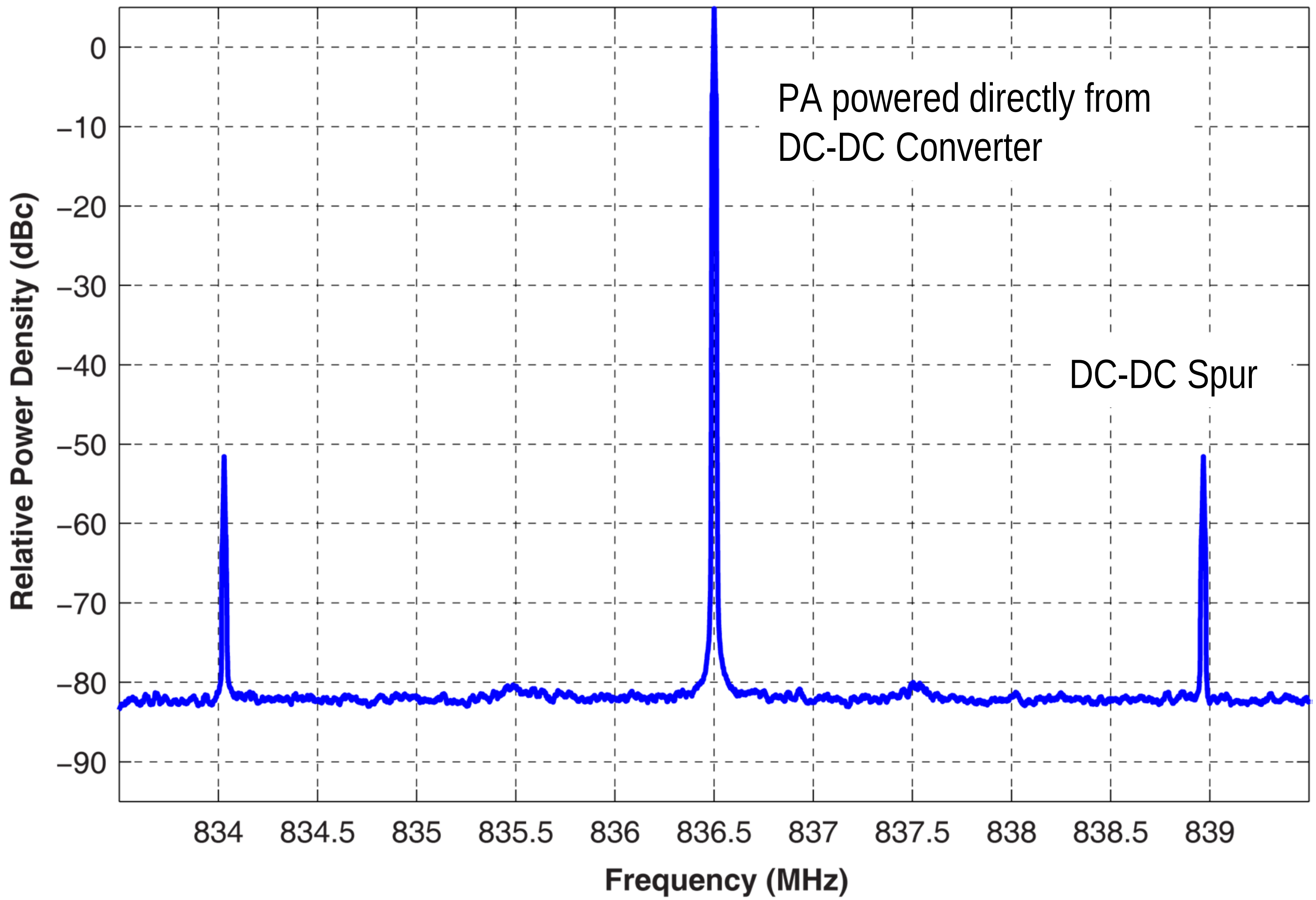


Switching Noise: Frequency-Domain



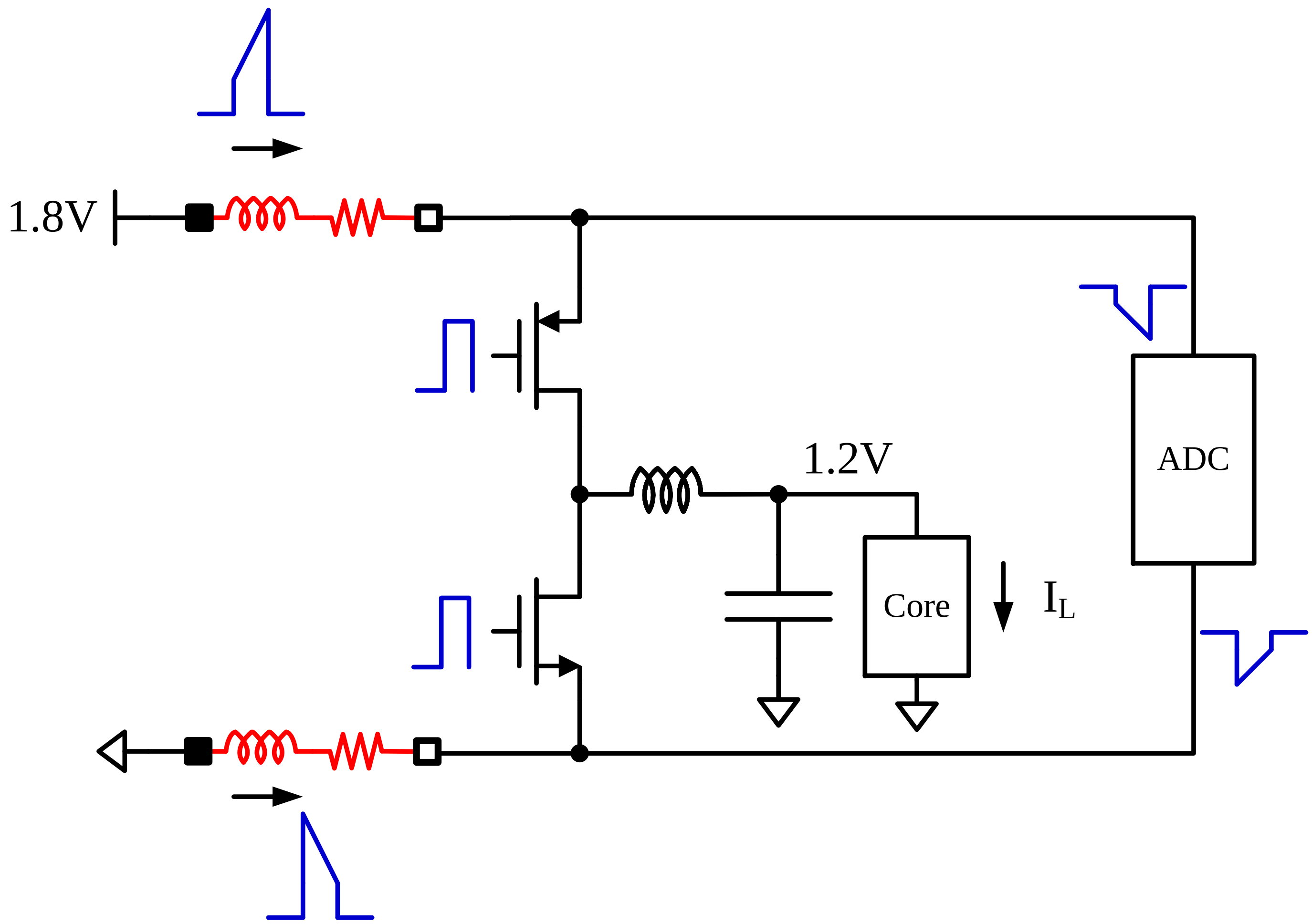
Impact of Switching Noise: Direct Powering

- A GSM PA example



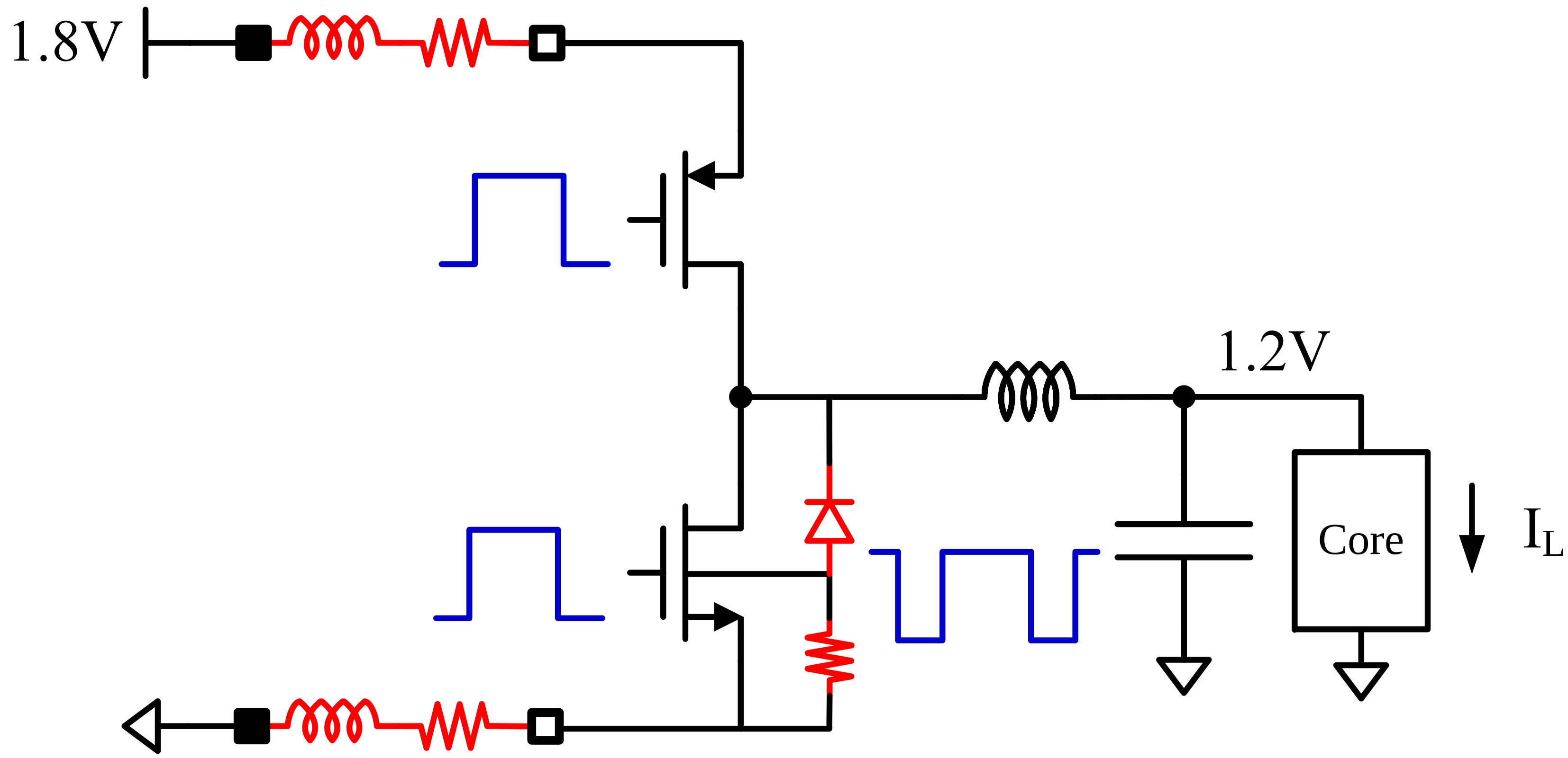
Impact of Switching Noise: Power Rails Sharing

- Problematic in pin-limited applications → Low-power DSPs



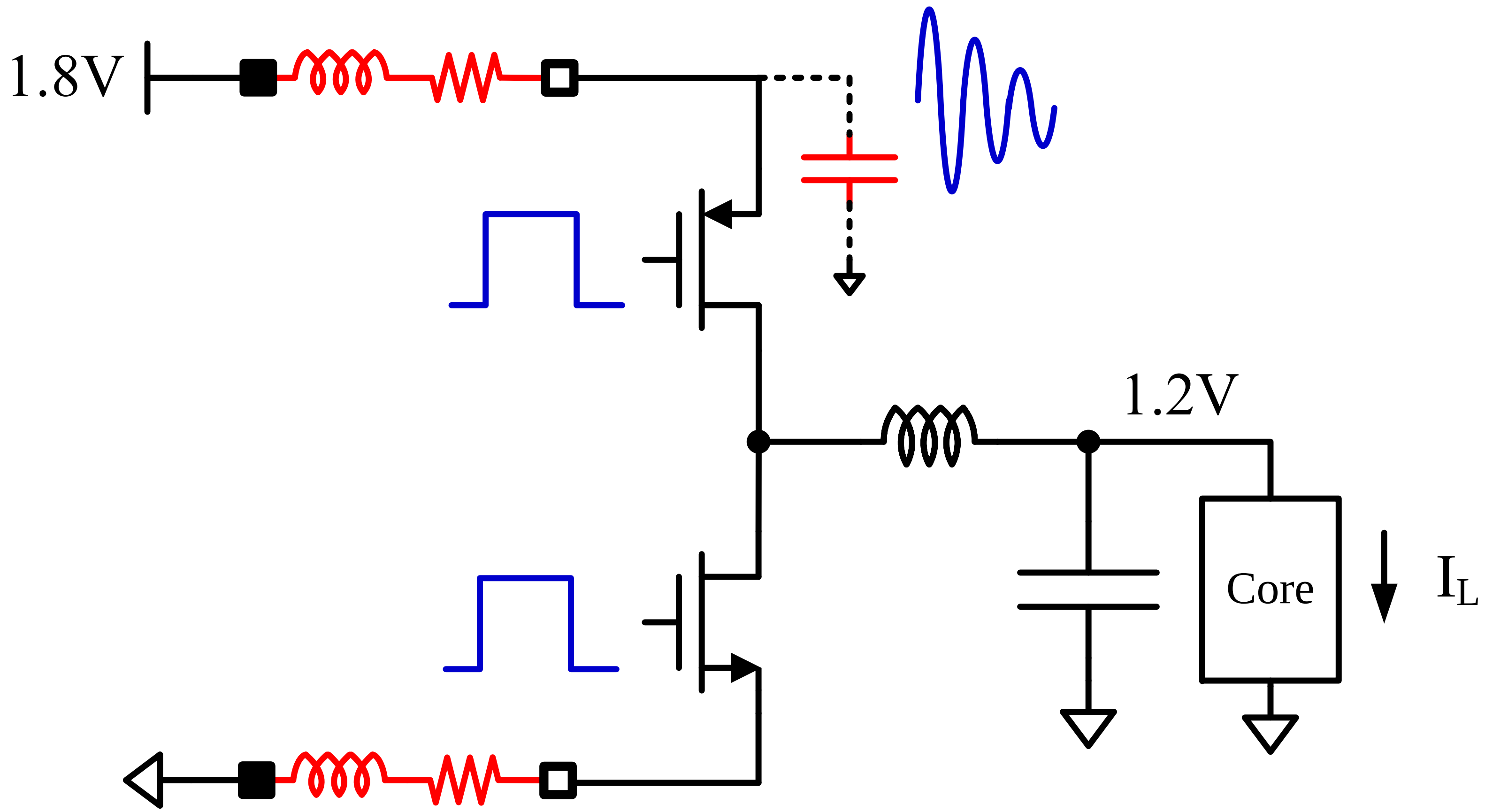
Impact of Switching Noise: Substrate Sharing

- Quite problematic when integrated in an SoC



Impact of Switching Noise: EMI & Reliability

- EMI is an issue and also device reliability in low-voltage CMOS



Accommodating Switching Noise

- Switching noise is spurious → It is arguable whether this is better or worse than random
- Spurious → Self/Cross mixing, Interference, Folding
- Random → SNR degradation
- But we know where the spurs are, isn't that good?
  - Not if they continue to exist with a significant magnitude up to very high frequencies
  - Location my be known with PWM control, but not PFM → Often need to tolerate both

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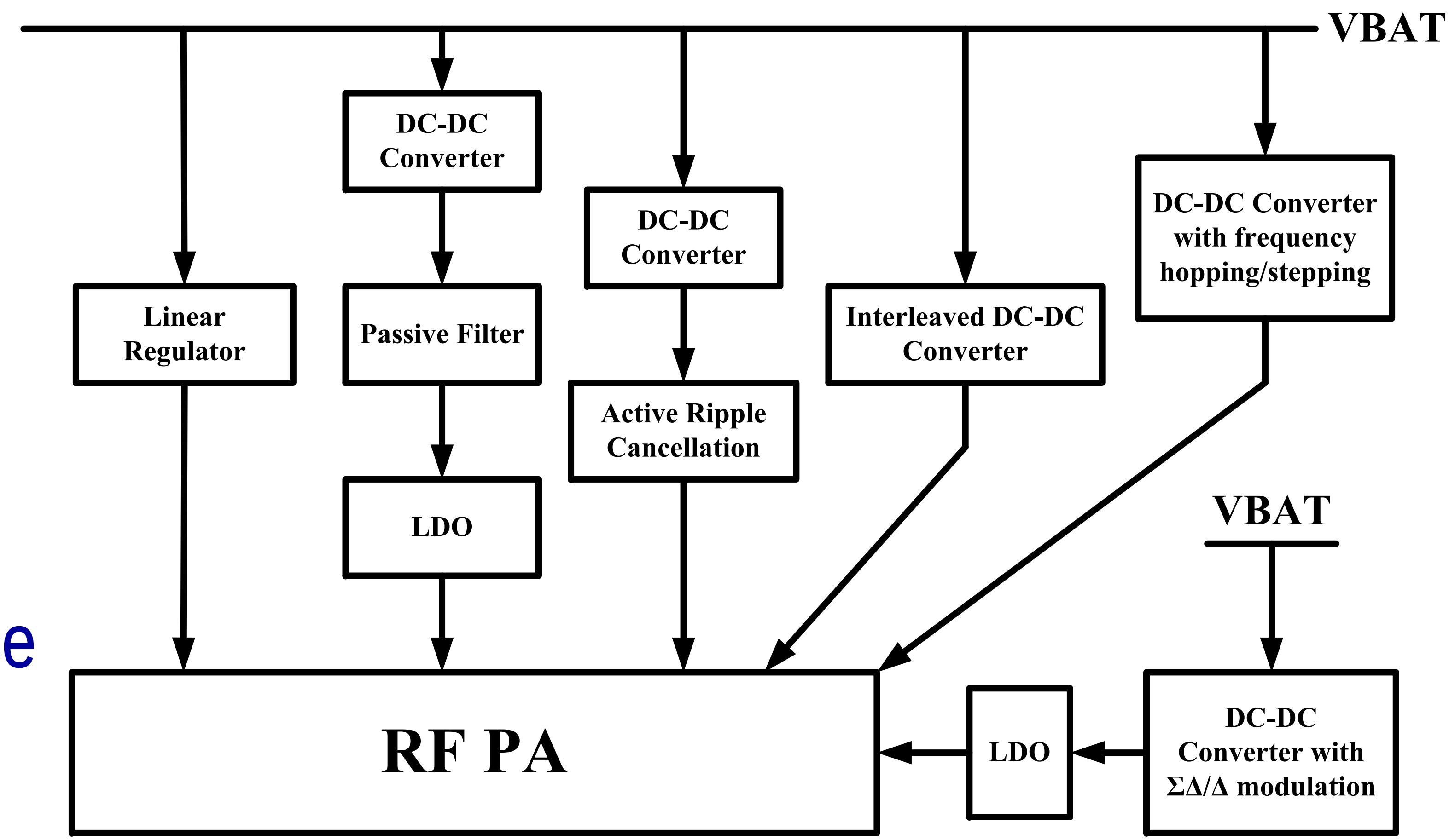
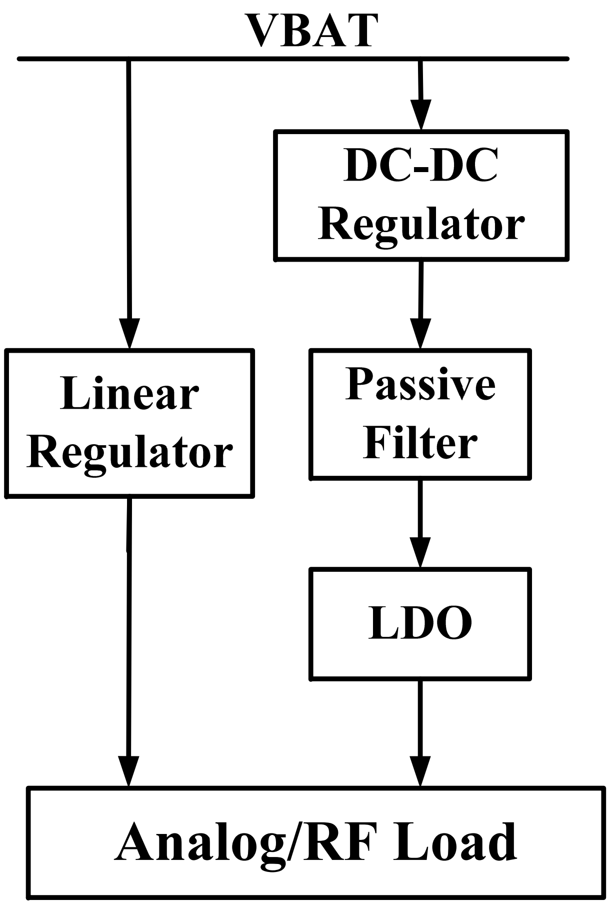
Switching Noise: Mitigation Techniques

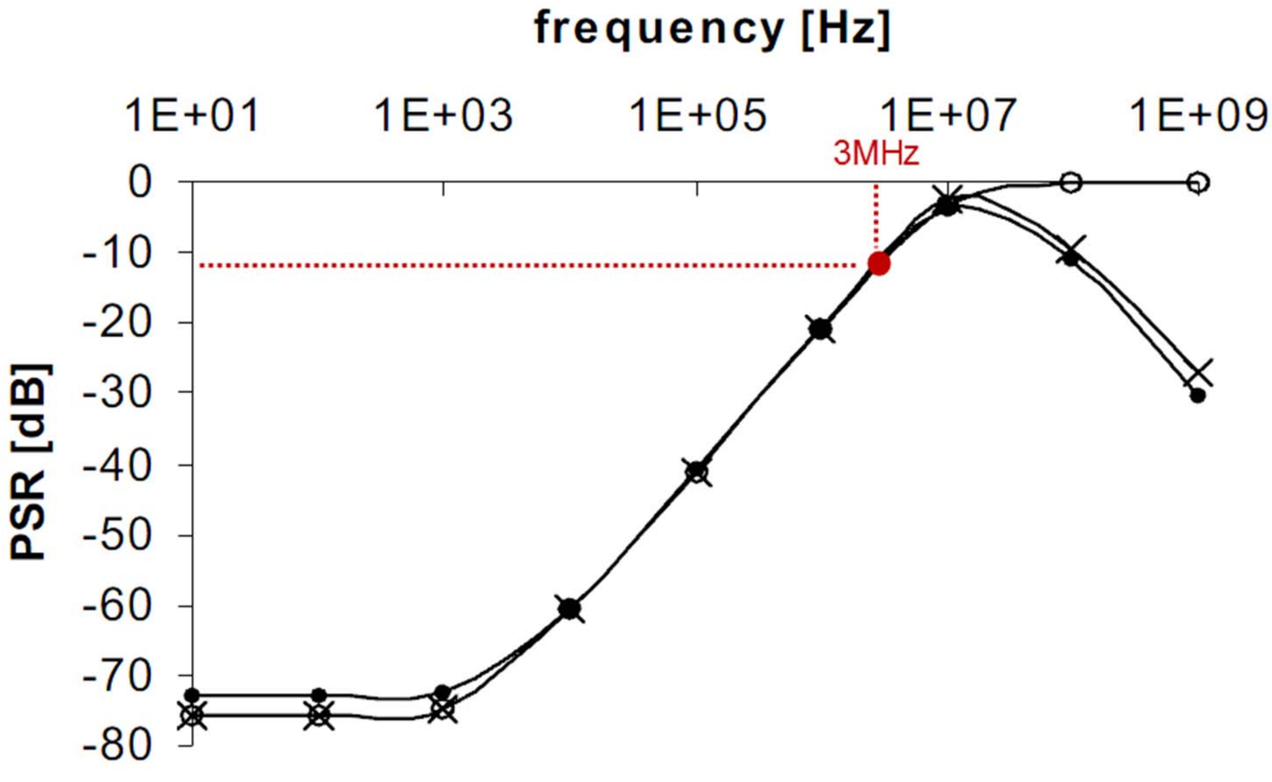
- Brute force time-domain techniques versus smart frequency-domain techniques

- Efficiency
- Cost
- Performance



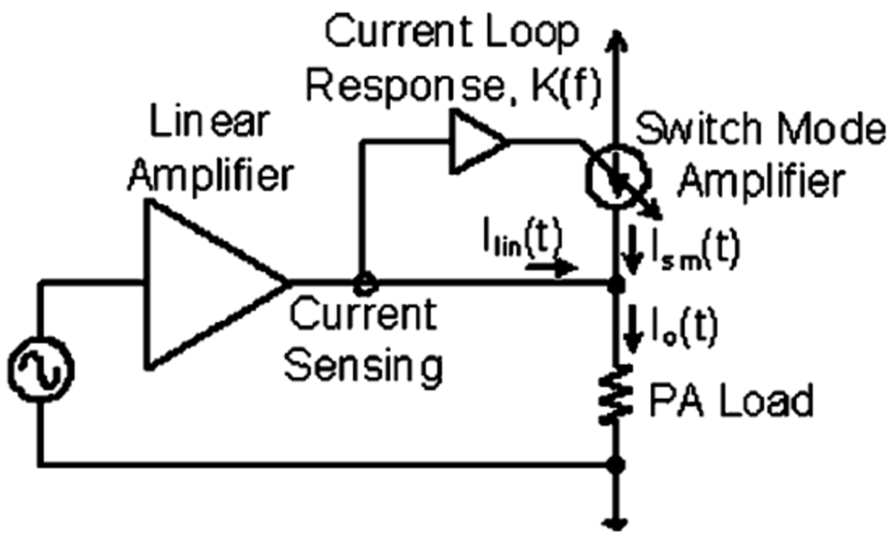
Do LDOs Really Help?

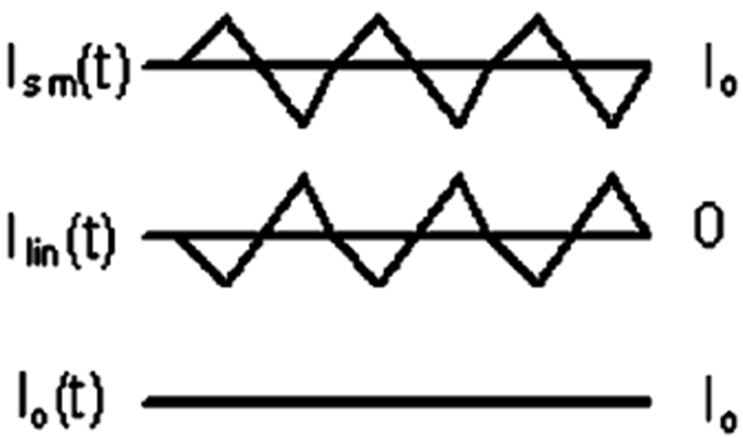




V. Gupta, G. A. Rincon-Mora, P. Raha, "Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications", IEEE International SOC Conference, 2004.

Brute Force: Time-Domain Approaches



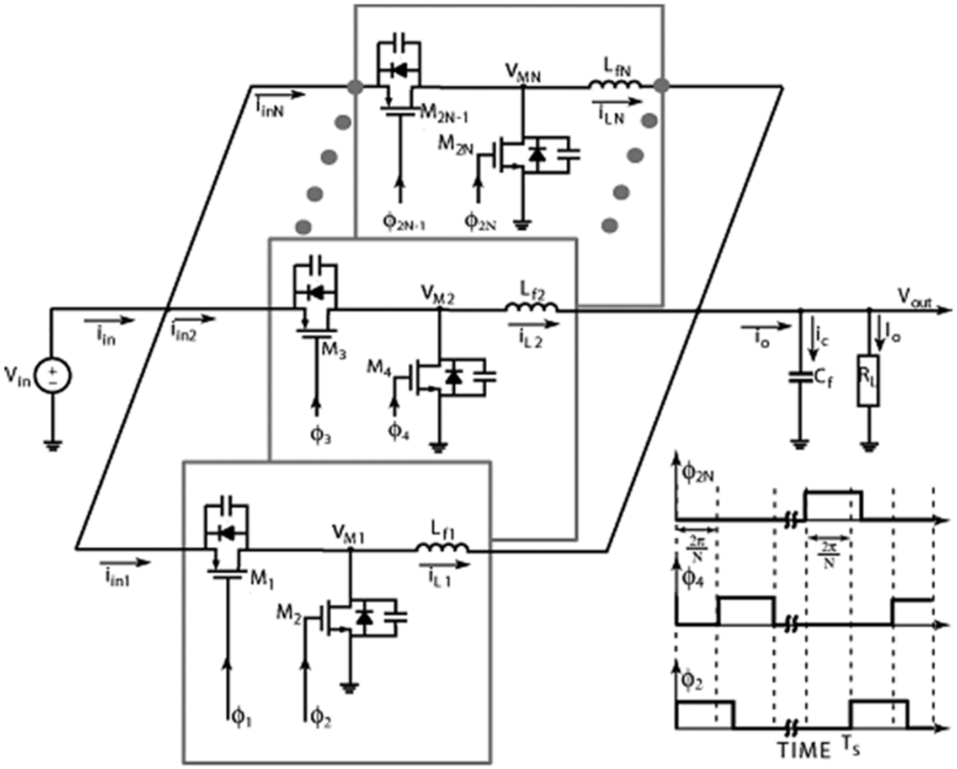


Wing-Yee Chu, Bertan Bakkaloglu, and Sayfe Kiaei, "A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters," *IEEE JSSC*, vol. 43, no. 12, pp. 2809-2819, Dec. 2008.

Active Ripple Cancellation

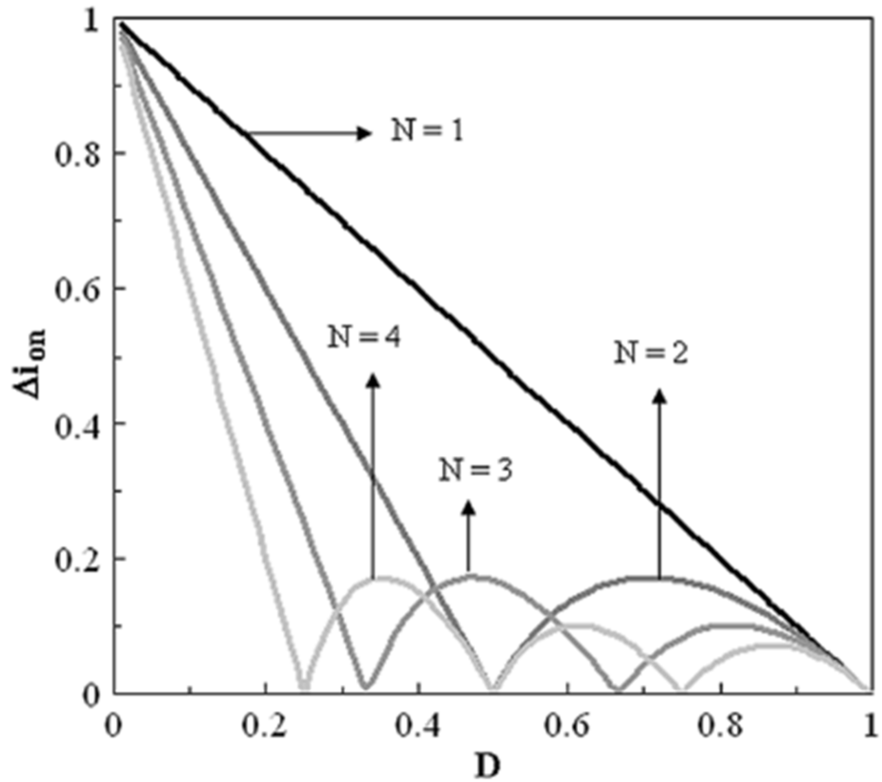
- Cancel the voltage ripple by compensating for inductor current ripple
- A class AB Linear amplifier is needed → source and sink current
- Amplifier has to be as fast as the switching frequency of the switching regulator → Power consumption
- Sensing inductor current is not simple
- Can result is significant efficiency loss if the inductor used is not large specially at low load conditions

Brute Force: Time-Domain Approaches



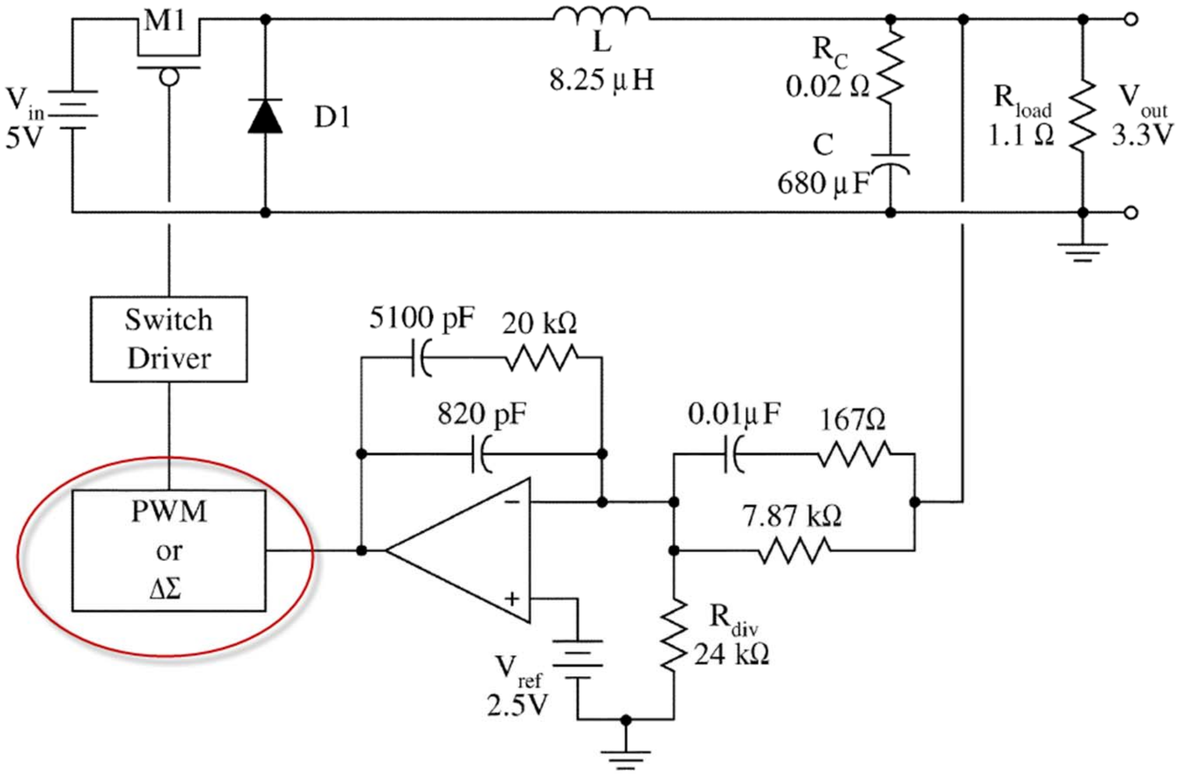
Siamak Abedinpour, Bertan Bakkaloglu, and Sayfe Kiaei, “A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 um SiGe Process,” IEEE Tran. on Power Electronics, vol. 22, no. 6, pp. 2164-2175, Nov. 2007.

Interleaved Regulators



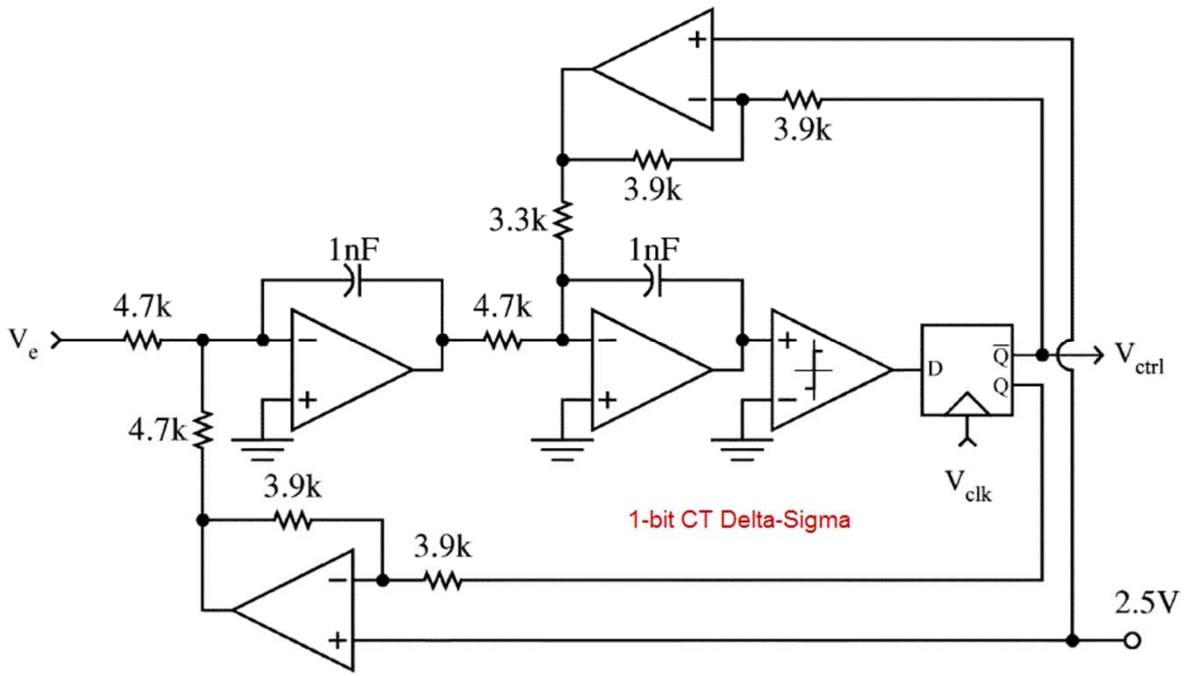
- Cancel the voltage ripple by switching multiple inductors with different switching phases to reduce overall current ripple
- Very expensive due to the inductors
- Complex to design due to accurate phase relation requirements

Spectrum Manipulation: Delta-Sigma



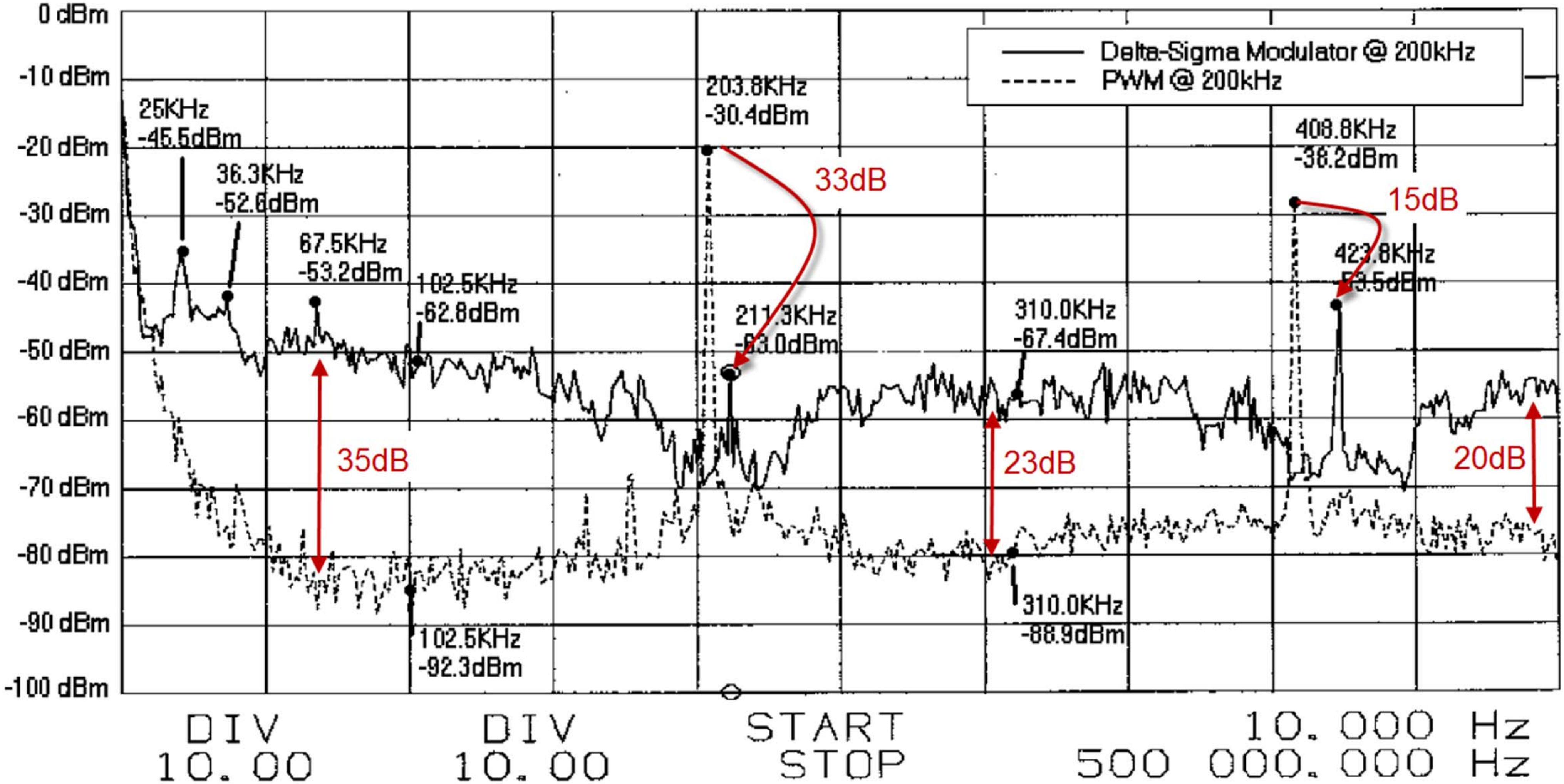
Steven K. Dunlap, and Terri S. Fiez, “A Noise-Shaped Switching Power Supply Using a Delta-Sigma Modulator,” *IEEE TCAS-I*, vol. 51, no. 6, pp. 1051-1061, Jun. 2004.

- Replace PWM with a single-bit Delta-Sigma

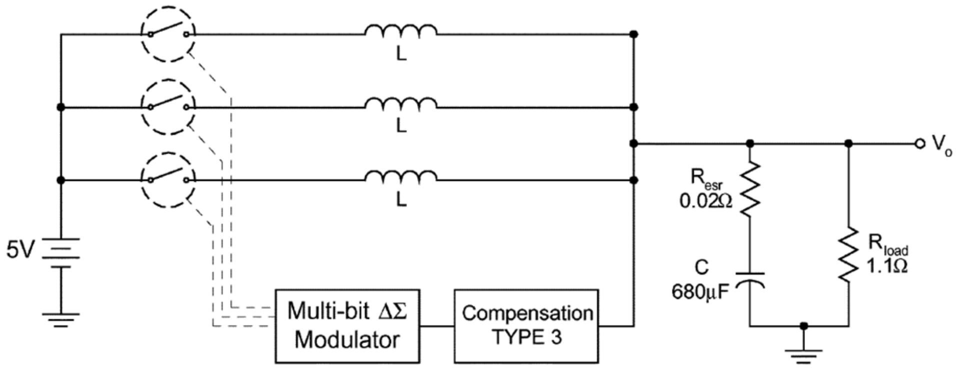


Spectrum Manipulation: Delta-Sigma

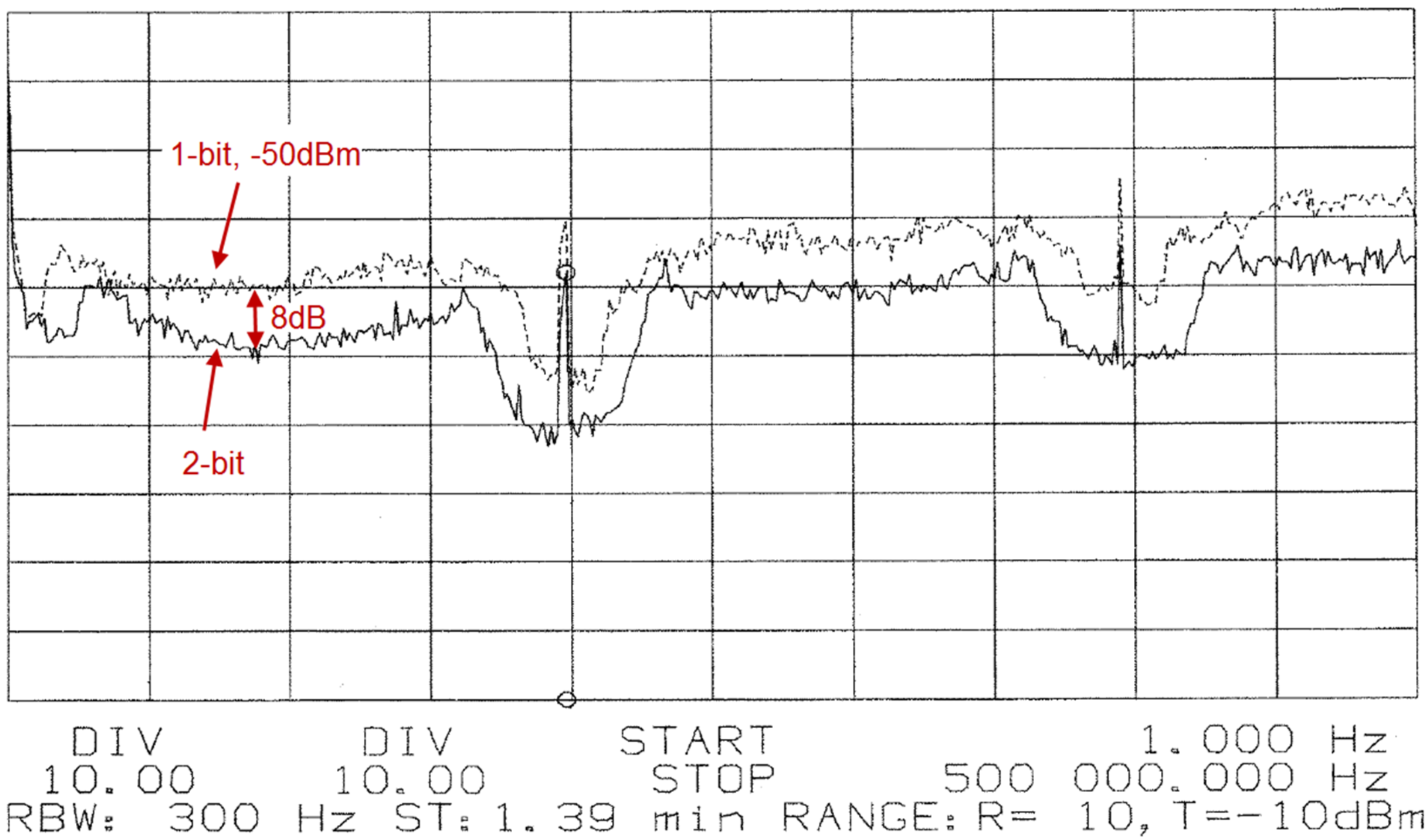
- Spurs are much lower, but still Spurs → Large broadband increase in the noise floor
- LDOs are still required but with relaxed PSR specs



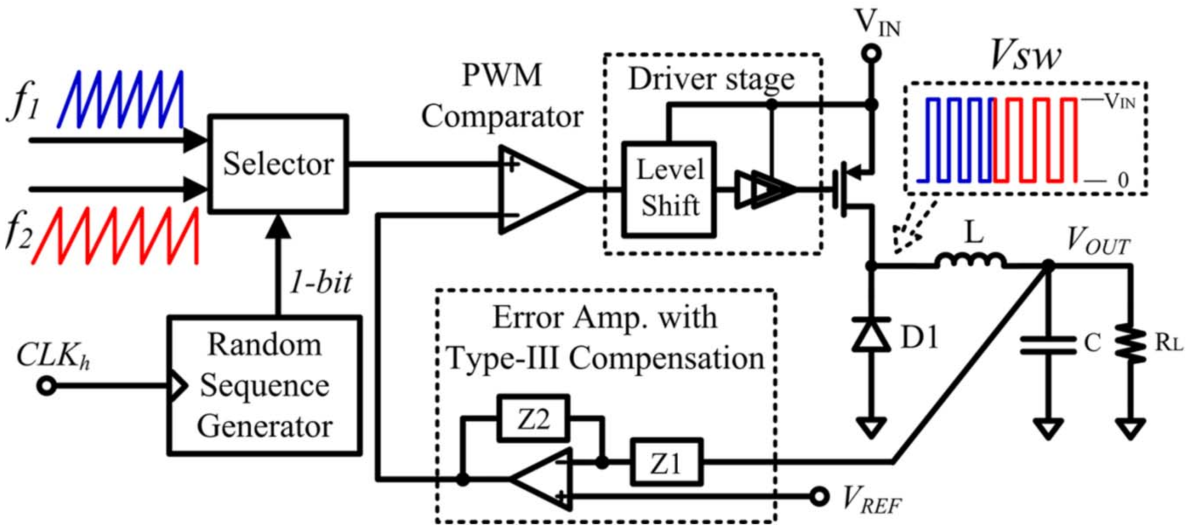
Spectrum Manipulation: Delta-Sigma



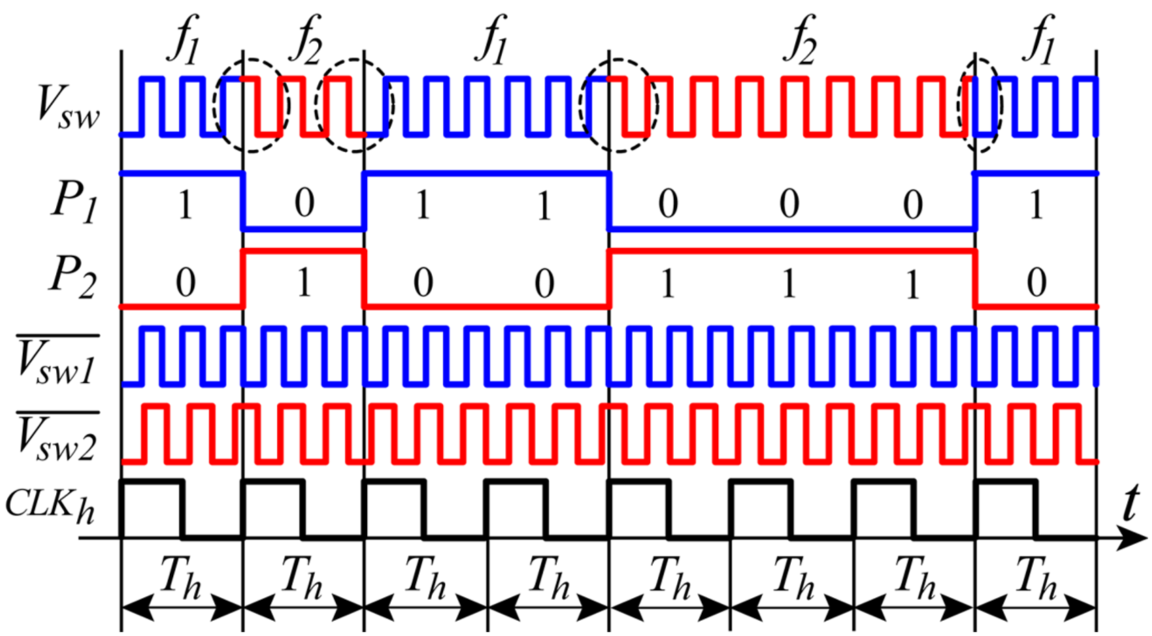
- Multi-bit Delta-Sigma
- Better Noise Floor, but several Inductors

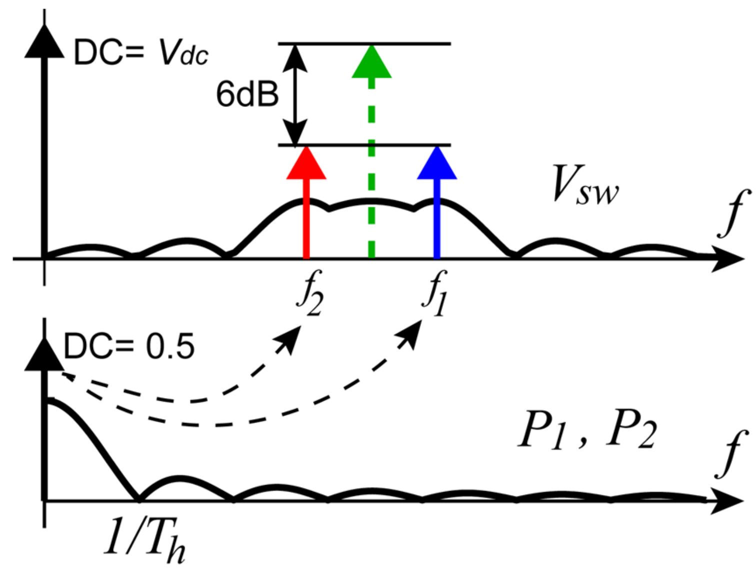


Spectrum Manipulation: Frequency Hopping



Chengwu Tao and Ayman Fayed, "PWM Control Architecture for Spur-Free Operation in Buck Regulators," IEEE Transactions on VLSI, Accepted.





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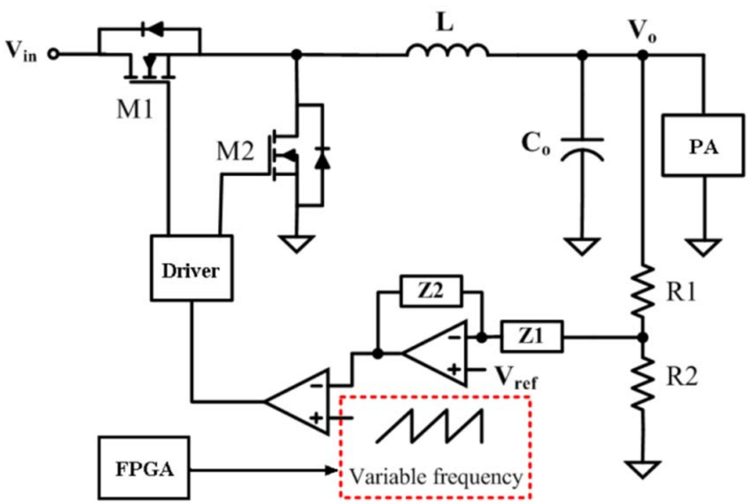
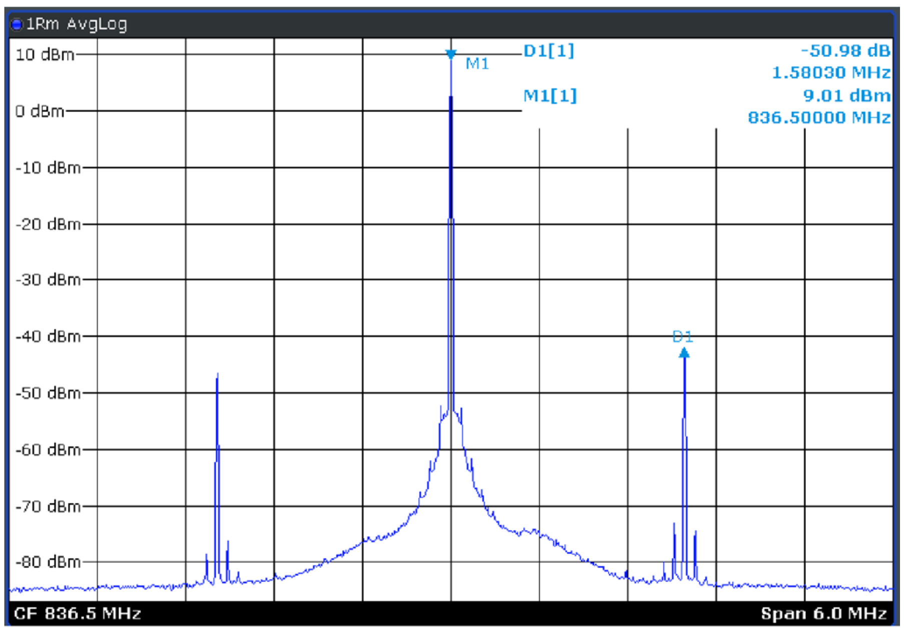
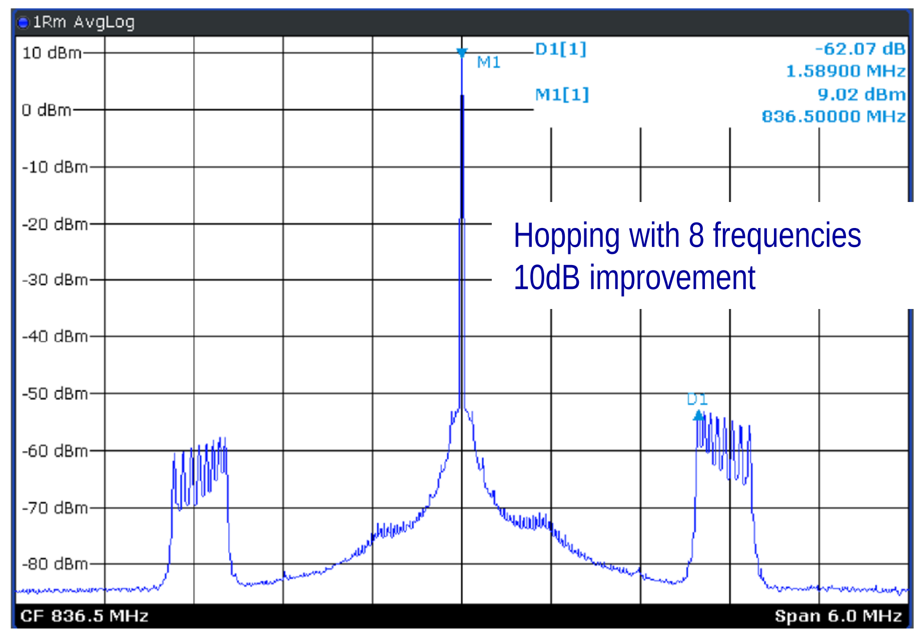


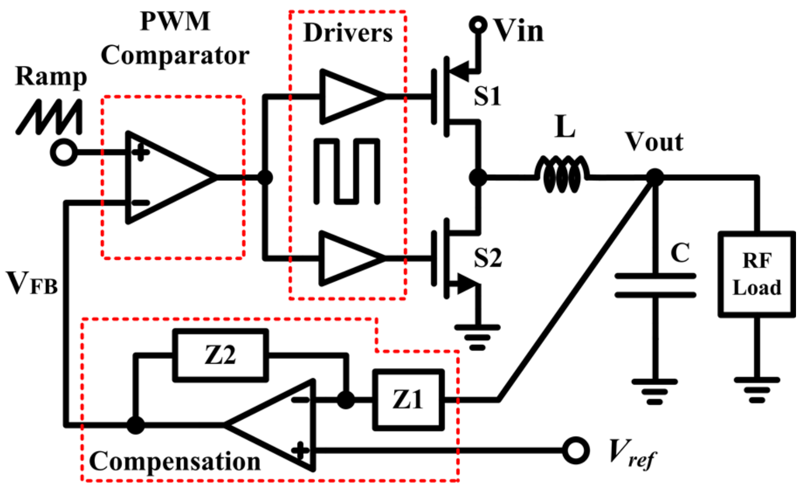
Jau-Horng Chen, Pang-Jung Liu, Y.-J.E. Chen "A spurious emission reduction technique for power amplifiers using frequency hopping DC-DC converters," IEEE RFIC, pp. 145-148, Jun. 2009.

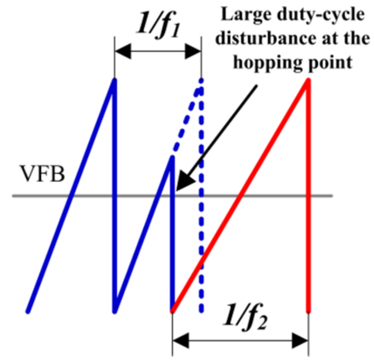
- Traditional random frequency hopping (Constant hopping rate)
- Spurs are lower, but still Spurs
- Large number of frequencies is needed to get significant reduction



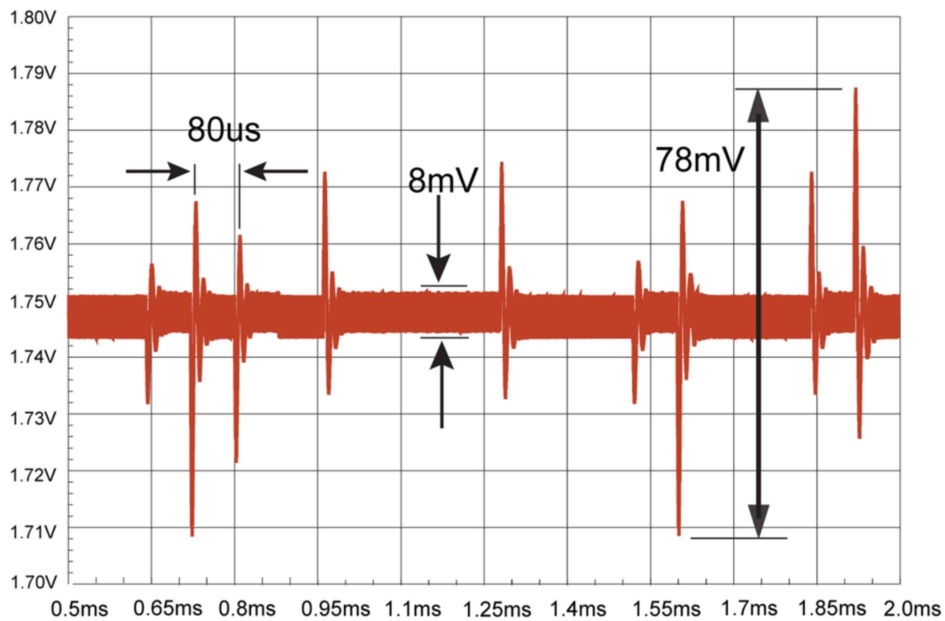


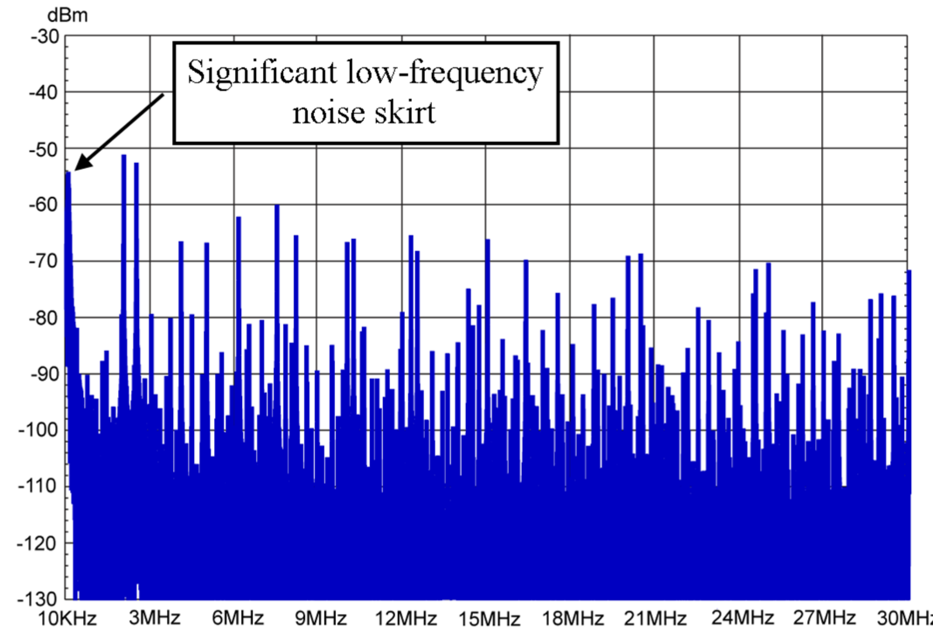
Spectrum Manipulation: Frequency Hopping



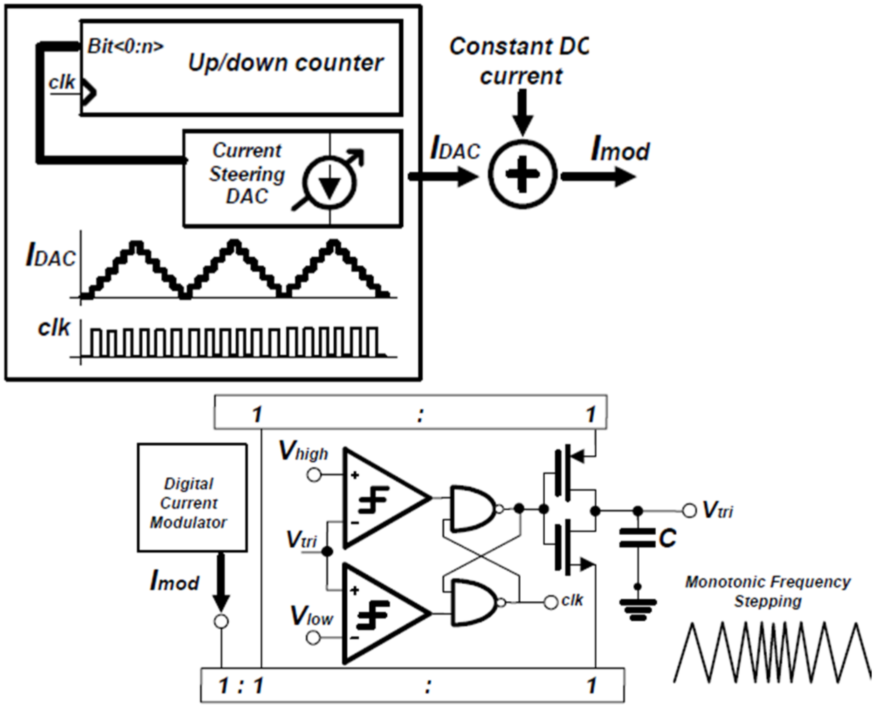


- Duty Cycle disturbance is problematic for low frequency spectrum
- Can be mitigated by using a long hopping period → less spreading at high frequency



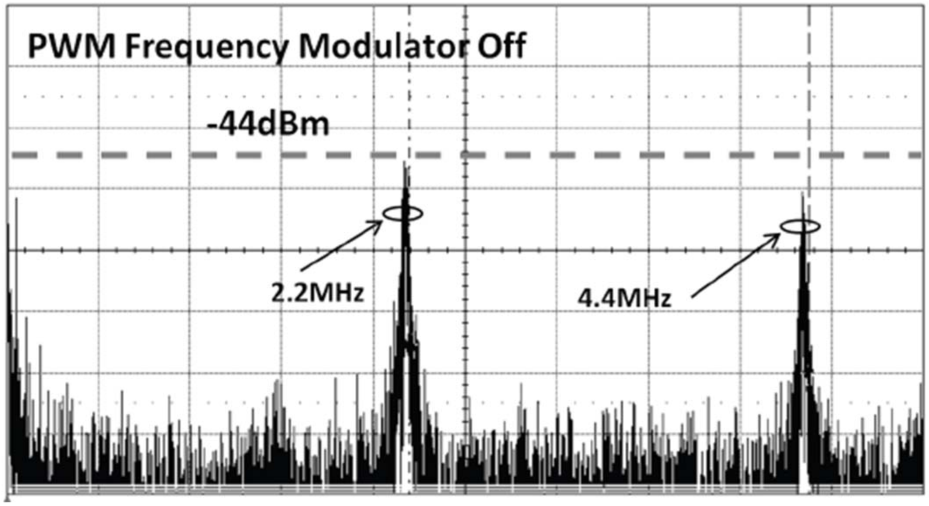


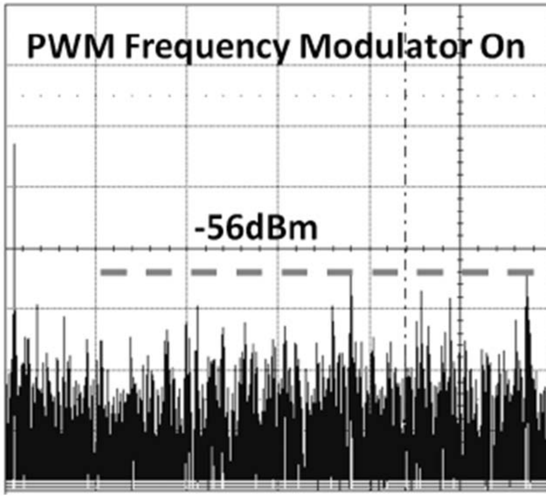
Spectrum Manipulation: Frequency Stepping



Eung Jung Kim, Chang-Hyuk Cho, Woonyun Kim, Chang-Ho Lee, and Joy Laskar, "Spurious Noise Reduction by Modulating Switching Frequency in DC-to-DC Converter for RF Power Amplifier," IEEE RFIC Symposium, pp. 43-46, May 2010

- Monotonic periodic frequency stepping
- Resolves the issue of duty-cycle distortion
- Spurs are lower, but still Spurs
- Large number of frequencies is needed and many spurs are generated





Frequency Stepping with 64 frequencies
12dB improvement

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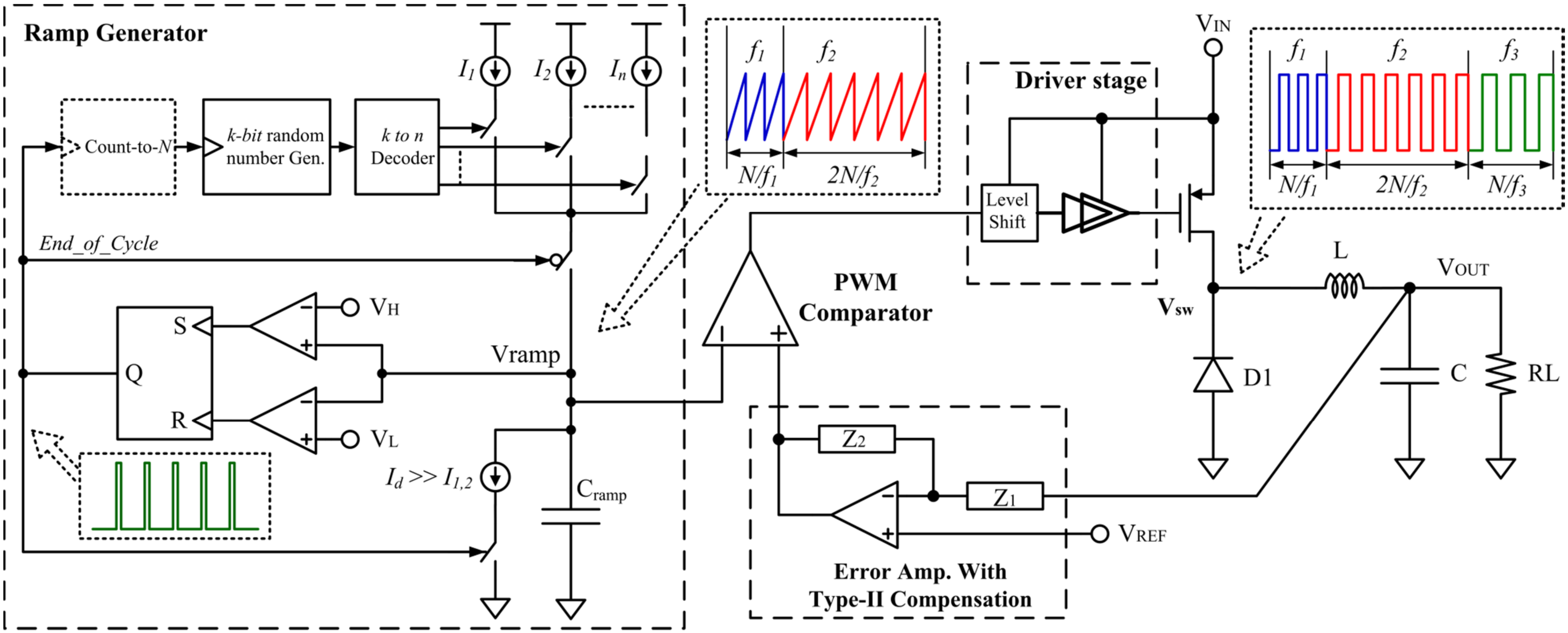
Constant Cycle Frequency Hopping (CCFH)

- Adopt random frequency hopping to avoid injecting extra noise in the system and to minimize the number of hopping frequencies needed

- CCFH (Variable Hopping Rate)
  - Minimizes duty-cycle disturbance during hopping
  - Maximizes hopping rate without transients
  - Maximum spur reduction with minimum noise floor peaking

- Add random phase chopping
  - Fully eliminates switching spurs at the output

CCFH: PWM Architecture

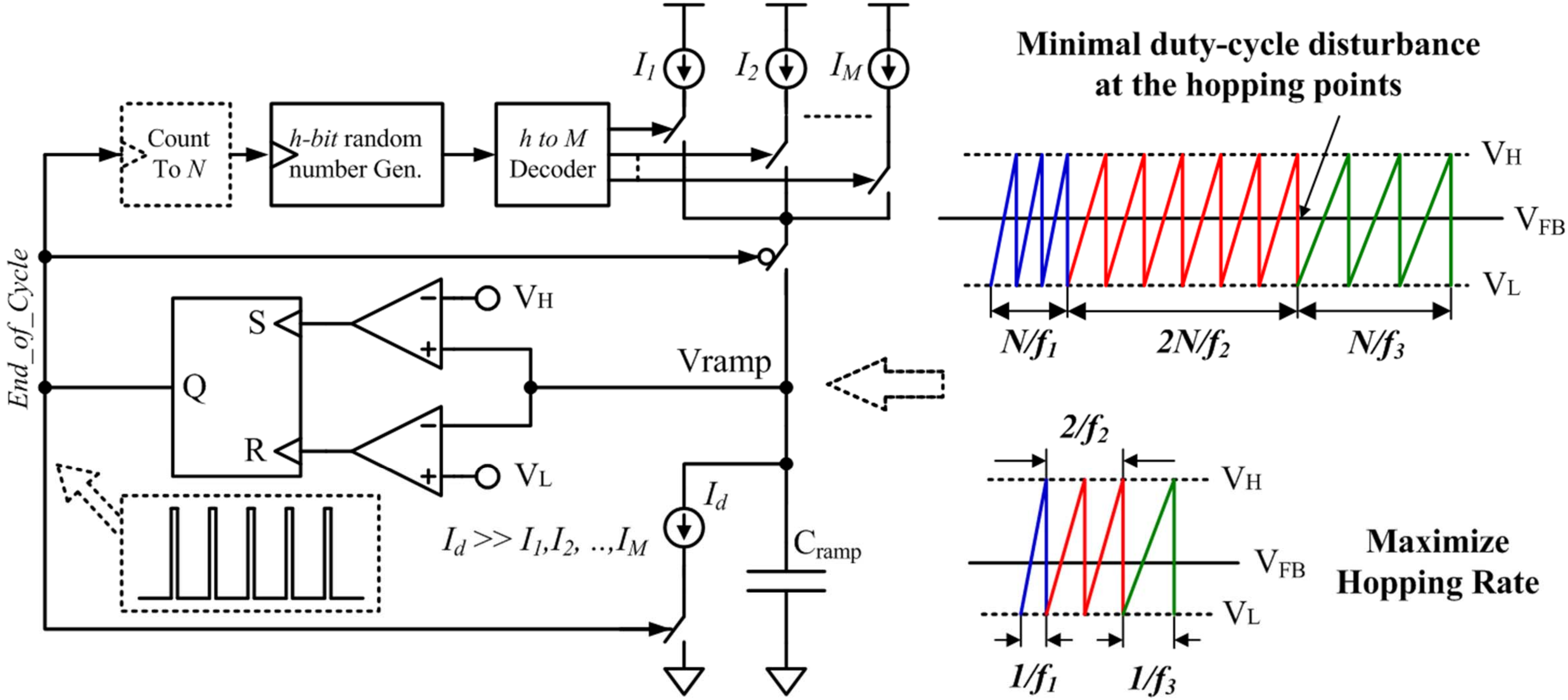


[1] Ayman Fayed and Chengwu Tao, “System and Method for Providing Power via a Spurious-Noise-Free Switching Device”, US Patent Pending, Application # 13/397,251 Feb. 2012.

[2] Chengwu Tao, and Ayman Fayed, “Spurious-Noise-Free Buck Regulator for direct-powering of Analog/RF loads using PWM Control with Random Frequency Hopping and Random Phase Chopping,” IEEE International Solid-State Circuits Conference (ISSCC 2011), pp. 396-397, Feb. 2010. Feb. 2011.

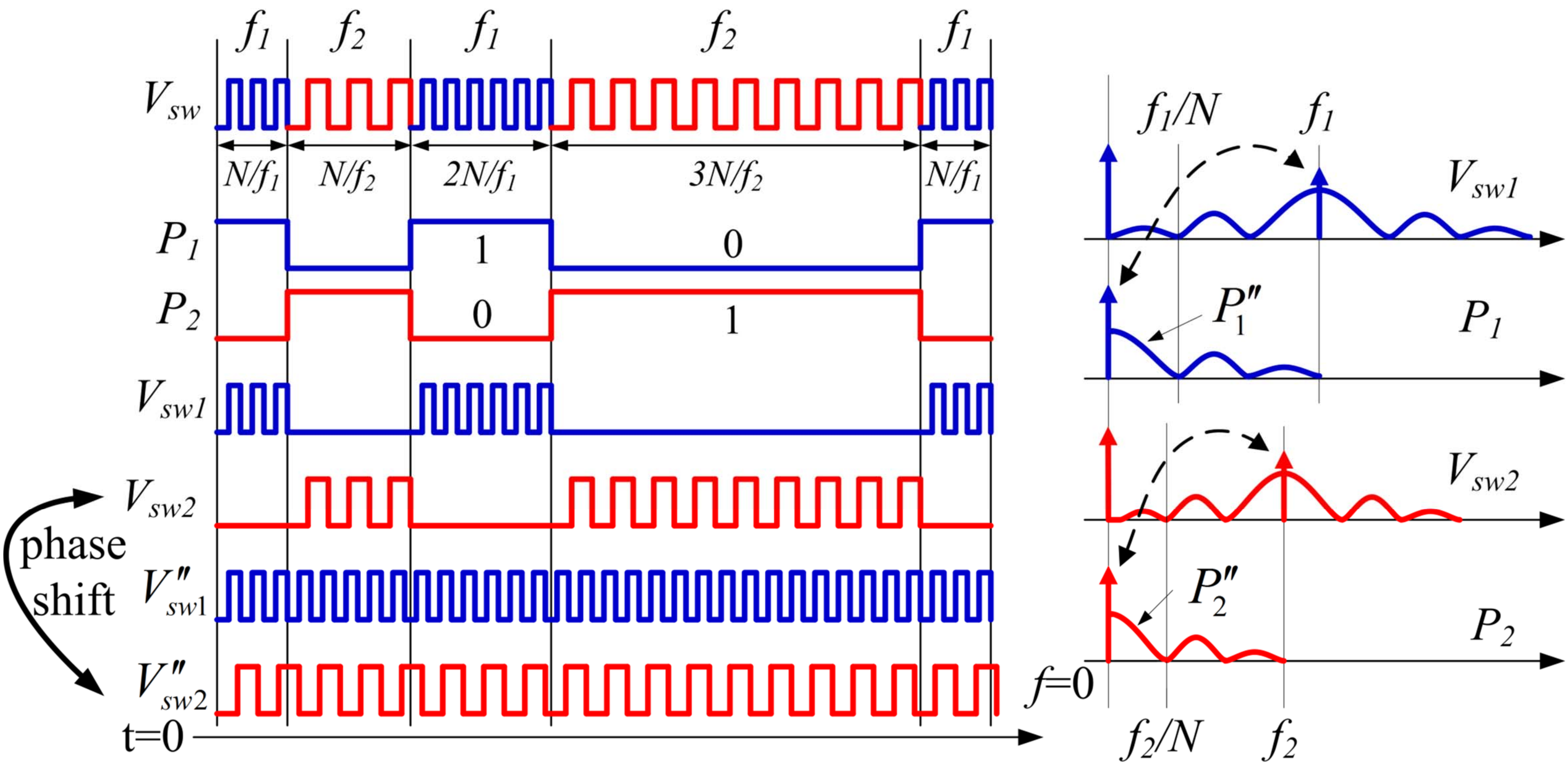
[3] Chengwu Tao and Ayman Fayed, “PWM Control Architecture for Spur-Free Operation in Buck Regulators,” IEEE Transactions on VLSI, Accepted.

CCFH: Maximizing Hopping Rate



- Minimize duty-cycle disturbance
  - Maintain ramp range regardless of frequency
  - Custom-tailored hopping period → Constant-Cycle

CCFH: Spectral Analysis



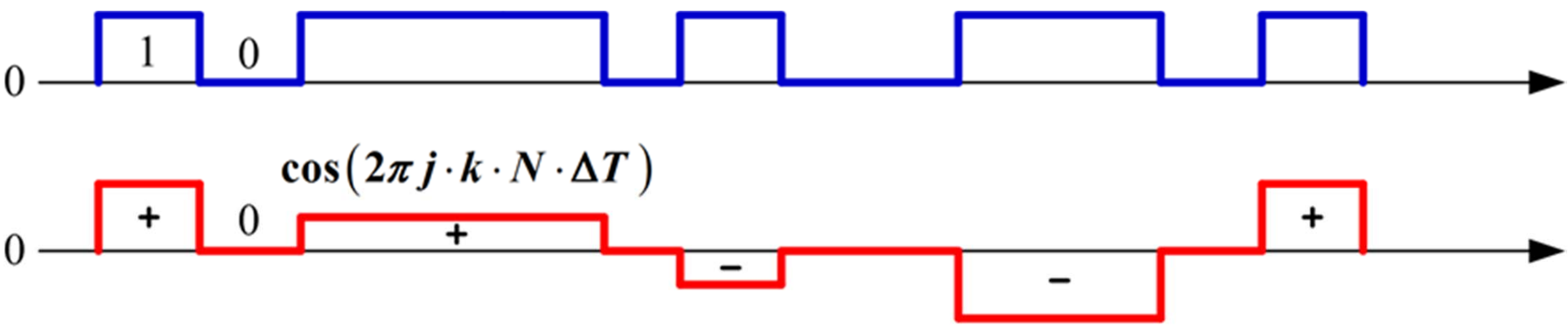
- Freq. hopping alone won't eliminate spurs
  - Phase chopping → $k \cdot f_1 \cdot N \cdot (1/f_1 - 1/f_2) = k \cdot f_1 \cdot N \cdot \Delta T$

CCFH: Phase Chopping

$$V_{sw1}(\mathrm{t}) = \left[\left(\frac{f_2}{f_1 + f_2}\right) + P_1''(\mathrm{t})\right] \times \left[(V_{in} \cdot dc) + \sum_{j=1}^{\infty} \gamma_j \sin\left(2\pi j \cdot f_1\left(\mathrm{t} - \boldsymbol{k} \cdot \boldsymbol{N\Delta T}\right) + \phi_j\right)\right]$$

$$\left(\frac{f_2}{f_1 + f_2}\right) \times \sum_{j=1}^{\infty} \gamma_j \times \begin{bmatrix} \cos\left(2\pi j \cdot k \cdot f_1 N\Delta T\right) \times \sin\left(2\pi j f_1 \mathrm{t} + \phi_j\right) - \\ \sin\left(2\pi j \cdot k \cdot f_1 N\Delta T\right) \times \cos\left(2\pi j f_1 \mathrm{t} + \phi_j\right) \end{bmatrix}$$

- Phase chopping modulates the gating function



CCFH: Eliminating Spurs

- To achieve zero average

$$\sum_{k} \cos\left(2\pi j \cdot k \cdot f_1 N \Delta T\right) = \sum_{k} \sin\left(2\pi j \cdot k \cdot f_1 N \Delta T\right) = 0$$

- But k increases indefinitely → zero average requires infinite period of time?
- Fortunately the modulating terms are periodic

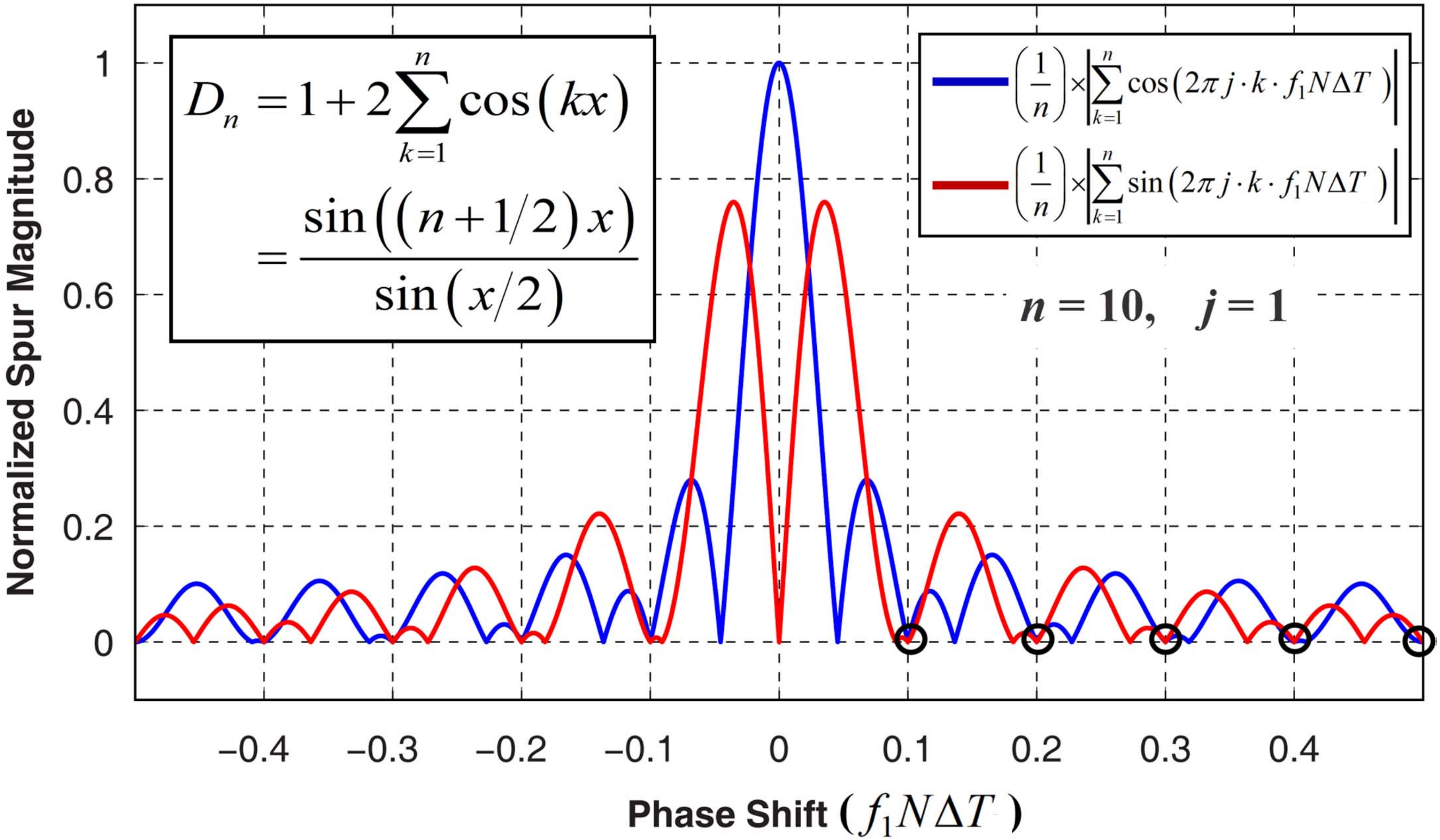
$$f_1 N \Delta T = \frac{m}{n}$$

$$\downarrow$$

$$\sum_{k=1}^{k=n} \cos\left(2\pi j \cdot k \cdot f_1 N \Delta T\right) = \sum_{k=1}^{k=n} \sin\left(2\pi j \cdot k \cdot f_1 N \Delta T\right) = 0$$

CCFH: Eliminating Spurs

- Average = Zero → Dirichlet kernel



CCFH: Eliminating Spurs

- Condition for Spur Elimination → Two Frequencies

$$f_1 N \Delta T = \frac{m}{n} \neq Integer \qquad f_2 N \Delta T = \frac{Nm}{Nn+m} \neq Integer$$

$$N = 1$$

$$f_1 N \Delta T = (m/n) \neq Integer$$

$$f_1 / f_2 = \frac{n+m}{n}$$

- Condition guaranteed at maximum hopping rate N=1
  - Easily implemented with segmented current mirrors → Current Steering DAC

CCFH: Eliminating Spurs

- Condition for Spur Elimination → Multiple Frequencies

$$f_i N \Delta T_{ji} = \frac{m}{n} \neq Integer \qquad f_j N \Delta T_{ji} = \frac{Nm}{Nn + m} \neq Integer$$

$$N = 1$$

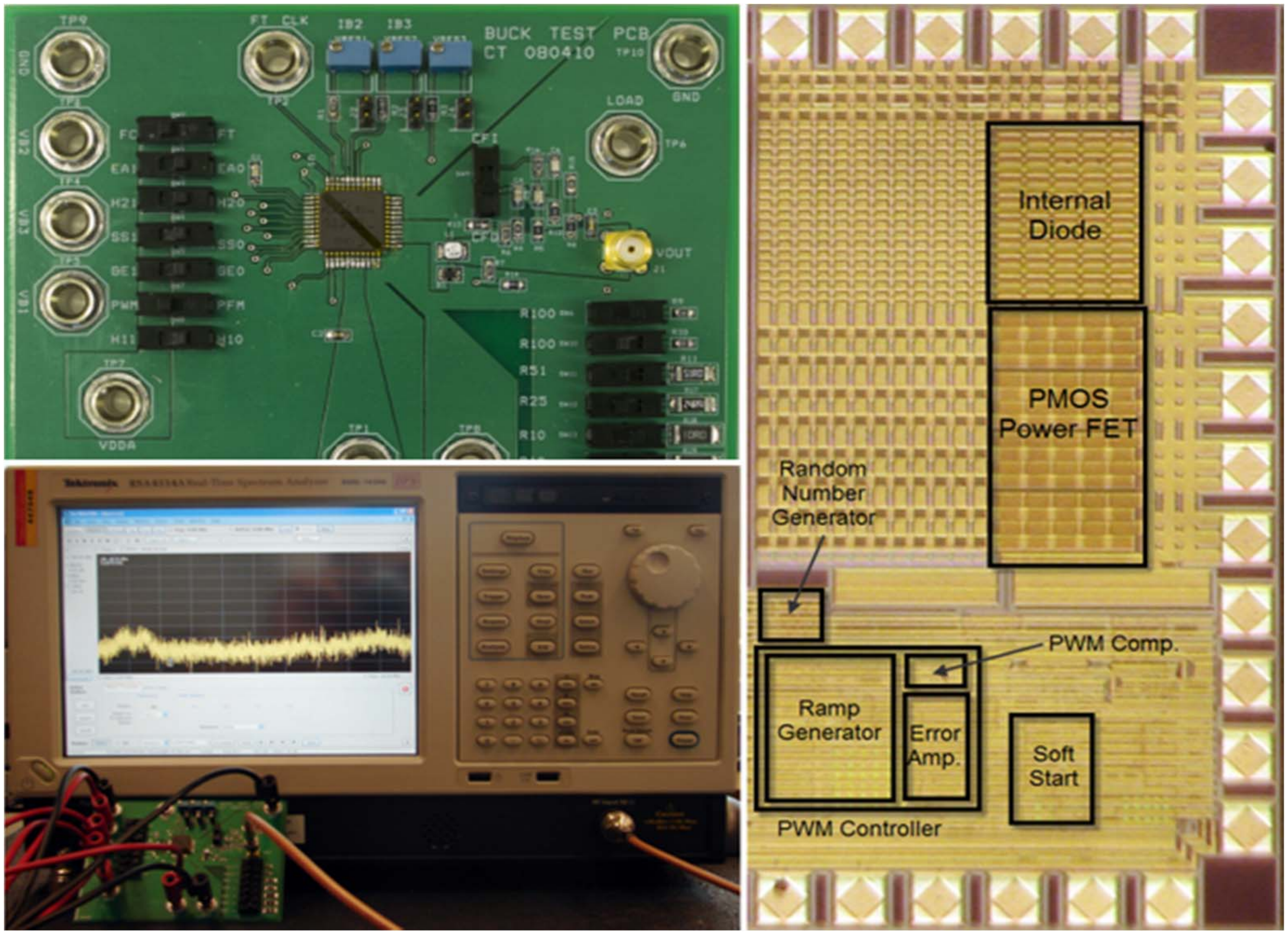
$$f_M N \Delta T_{iM} = \left(m_i / n_i\right) \neq Integer$$

$$f_M / f_i = \frac{n_i + m_i}{n_i}$$

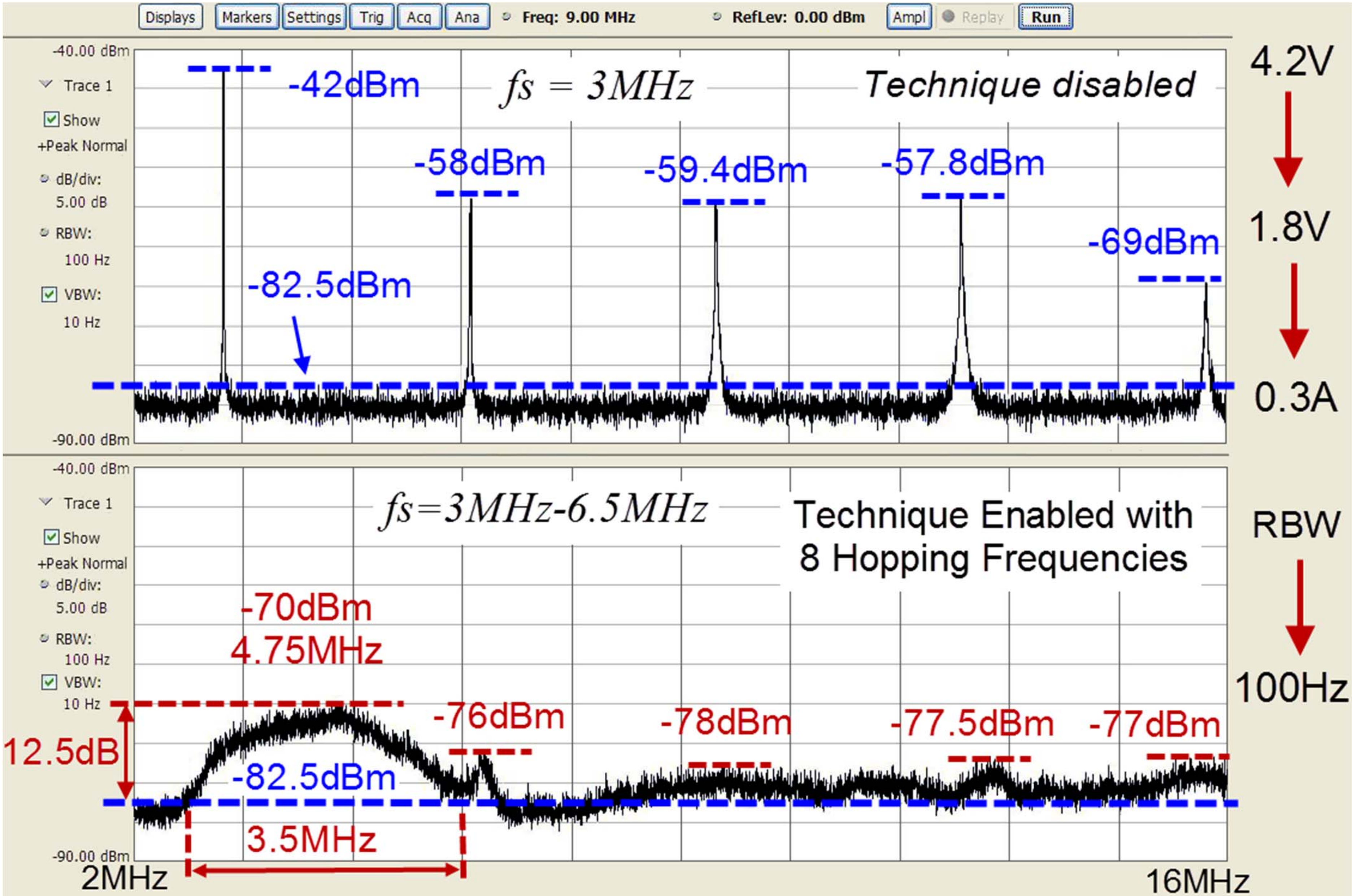
- It is sufficient for the condition to be met between each frequency and at least one other frequency in the set

Implementation

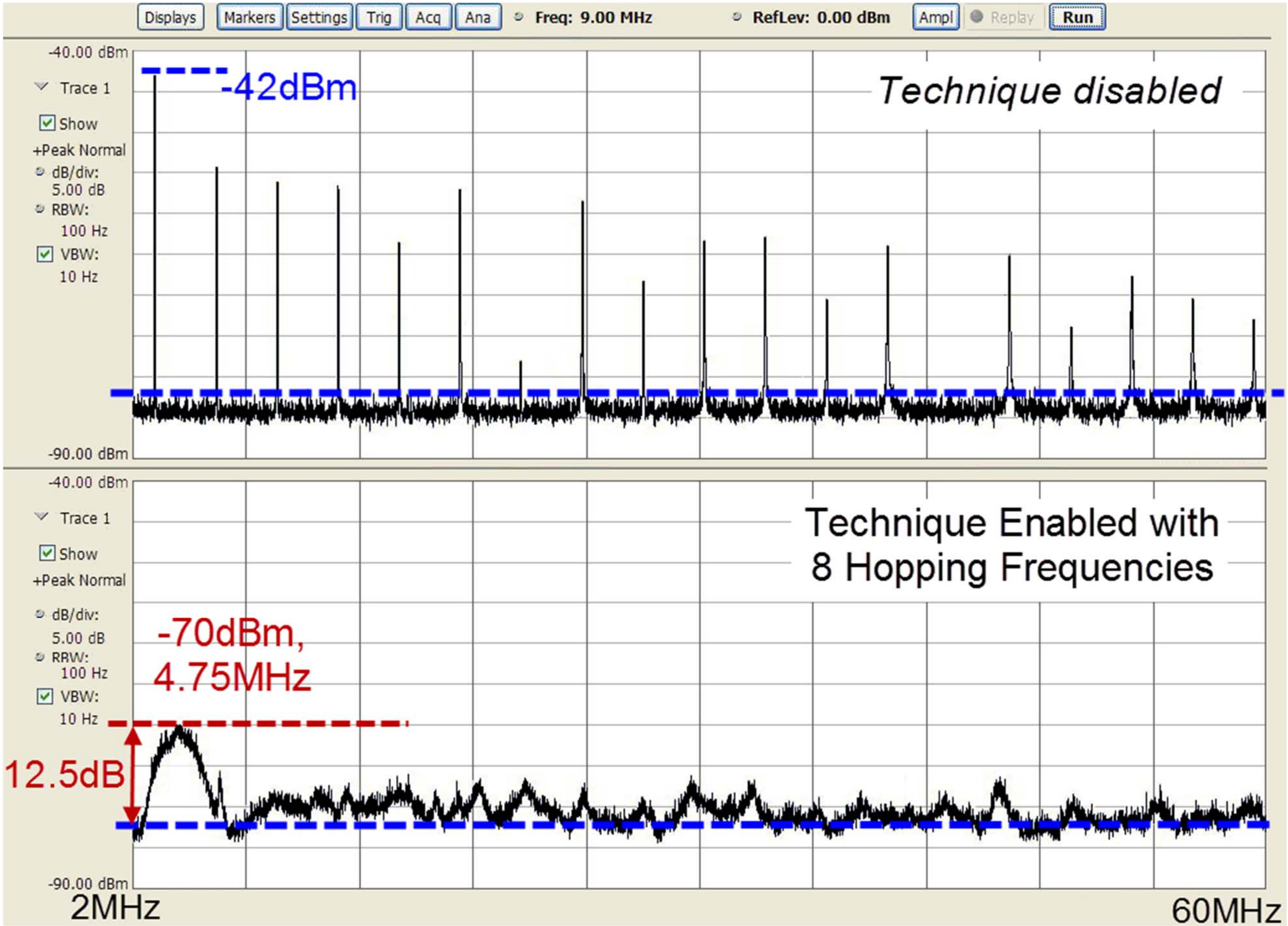
- In 0.35-µm → Single Switching Frequency Mode, and CCFH mode with 2, 4, or 8 frequencies



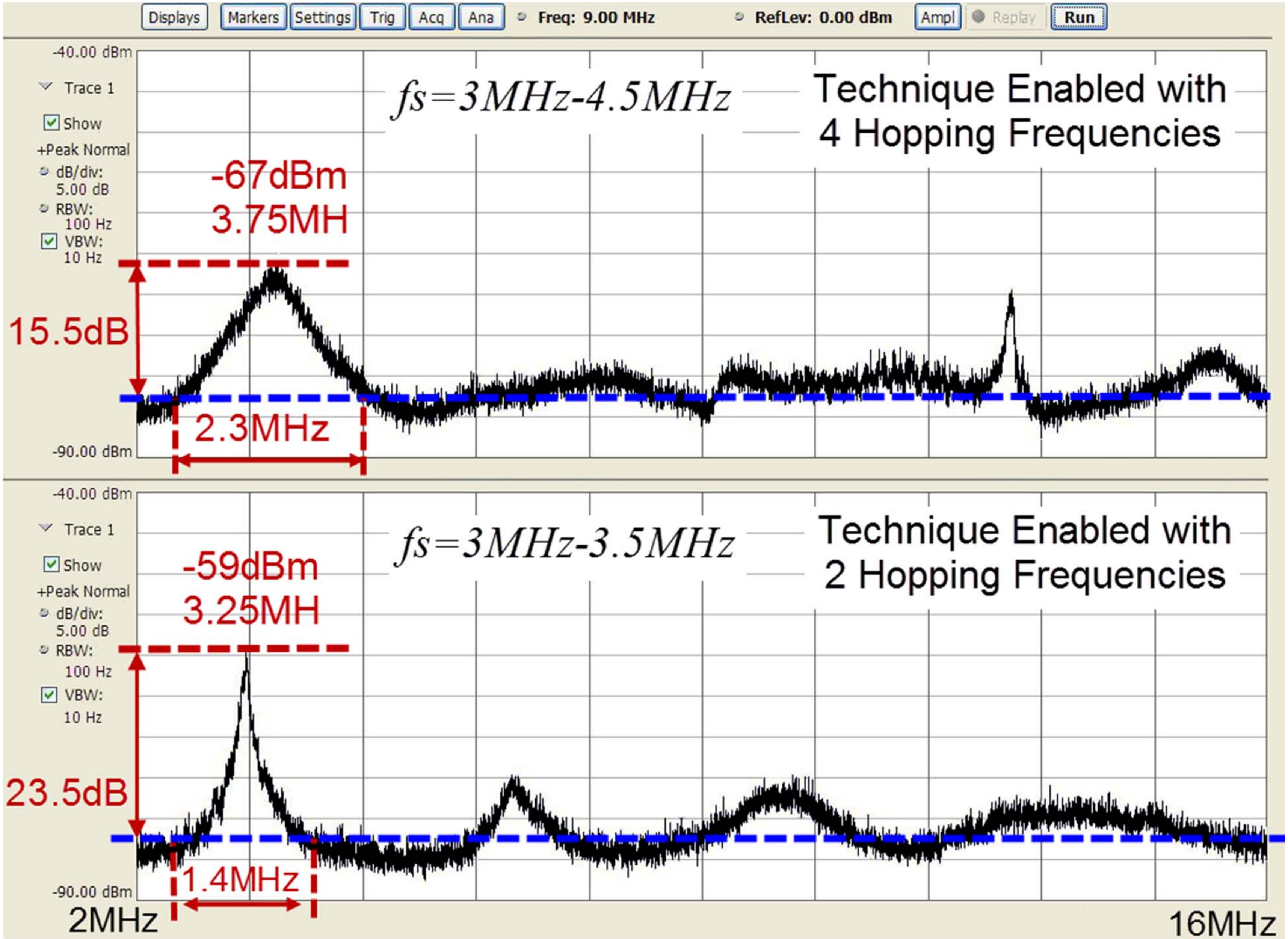
Output Spectrum: 16MHz (8 Frequencies)



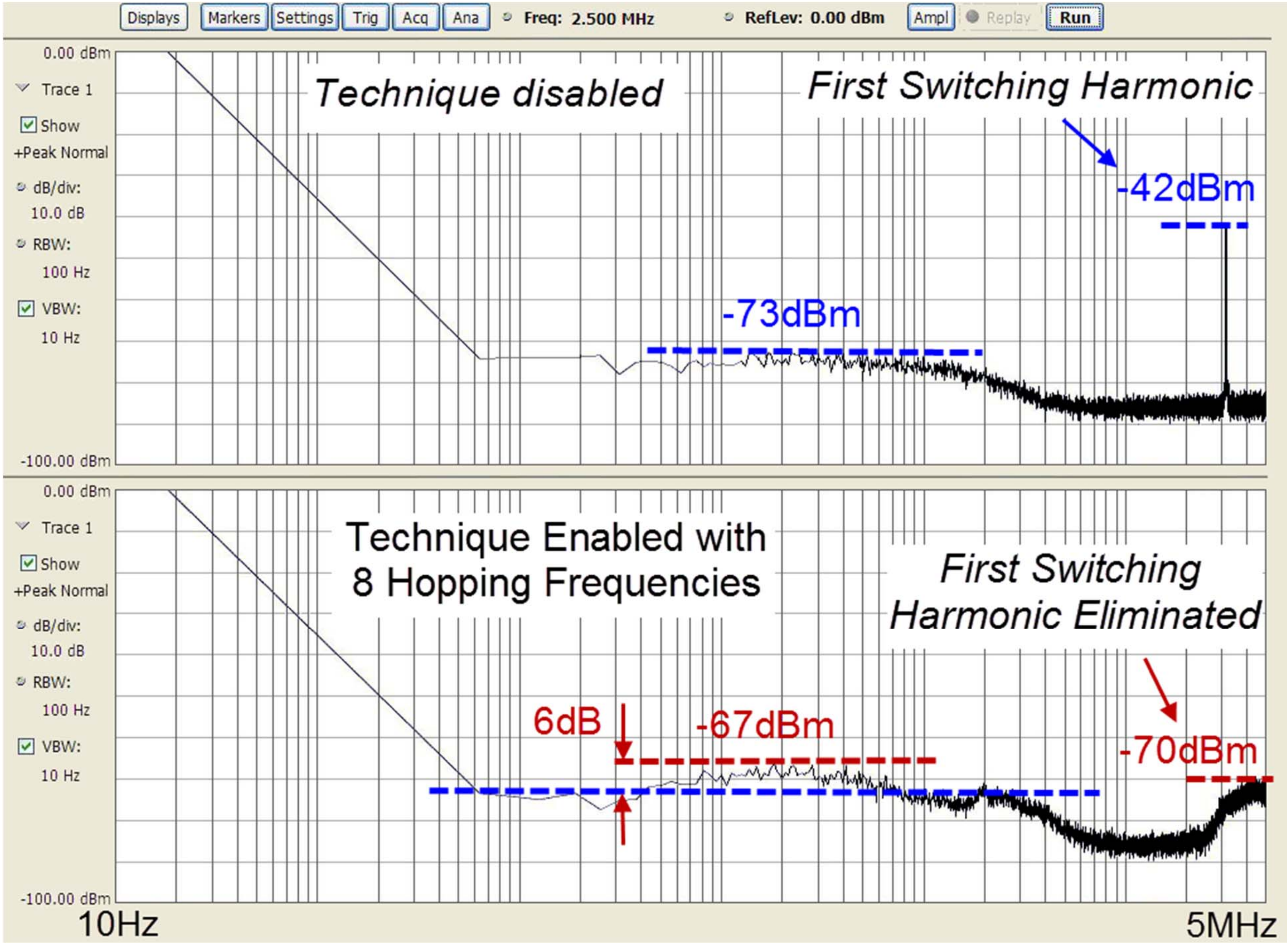
Output Spectrum: 60MHz (8 Frequencies)



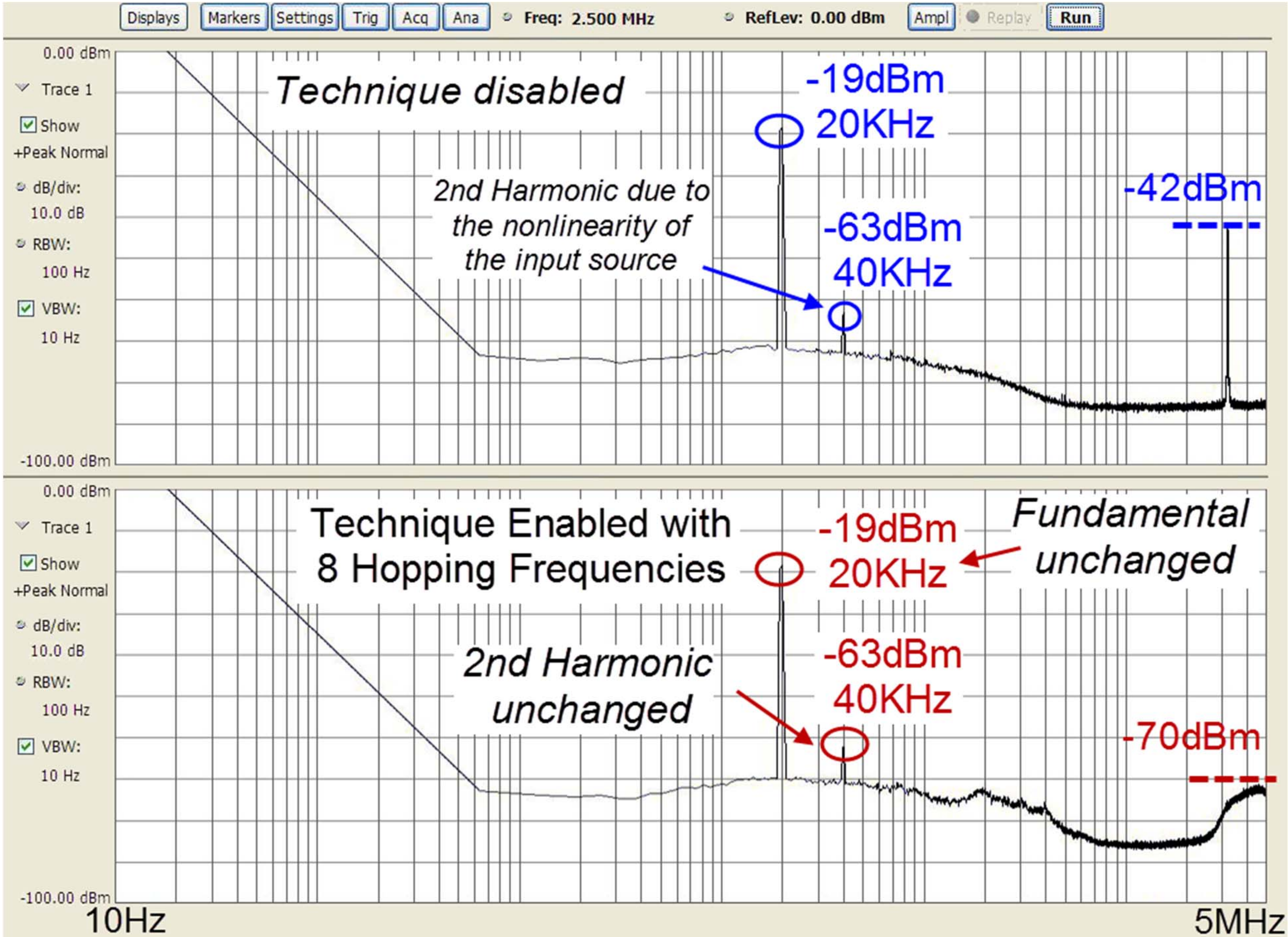
Output Spectrum: 16MHz (2,4 Frequencies)



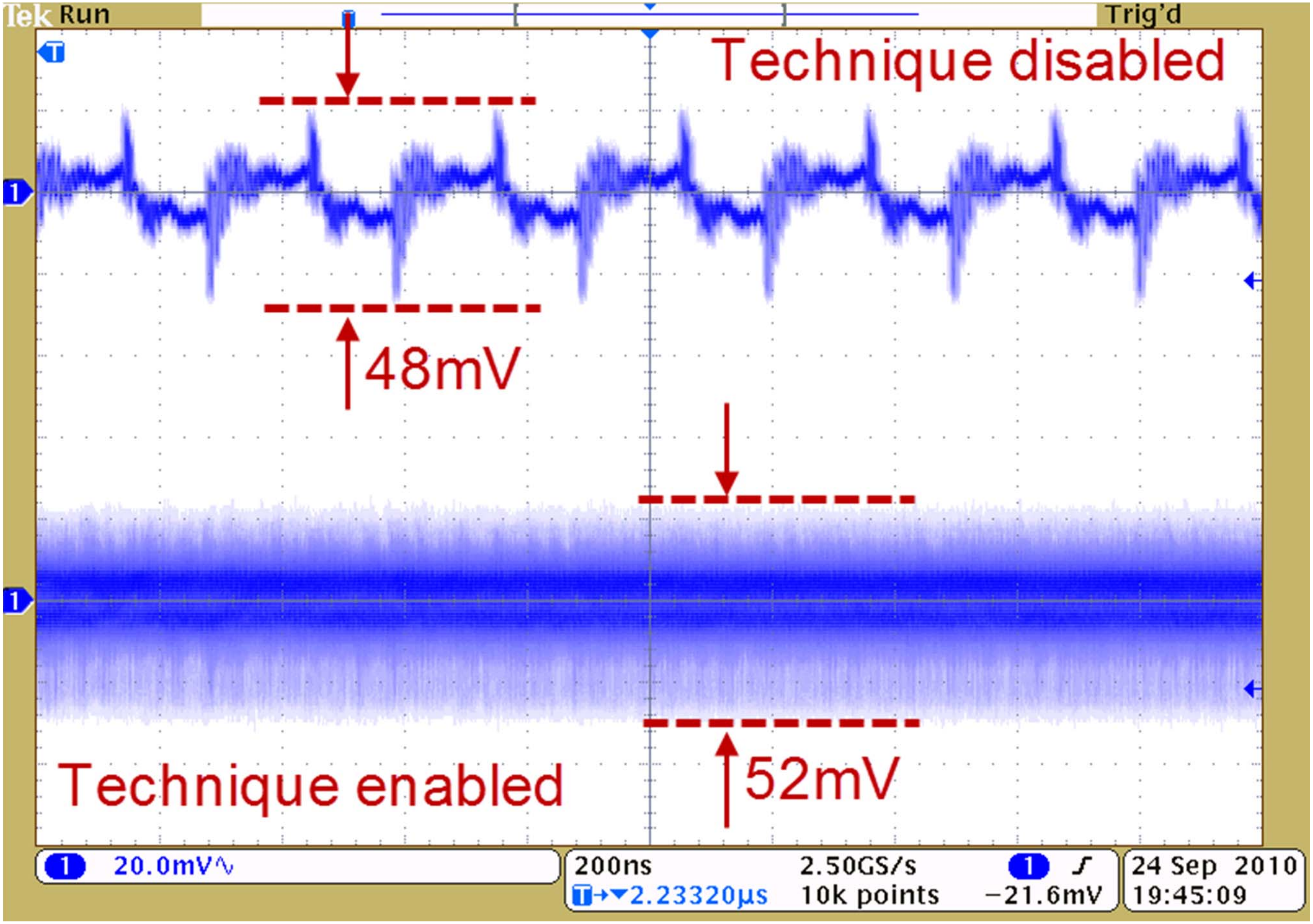
Output Spectrum: Low Frequency



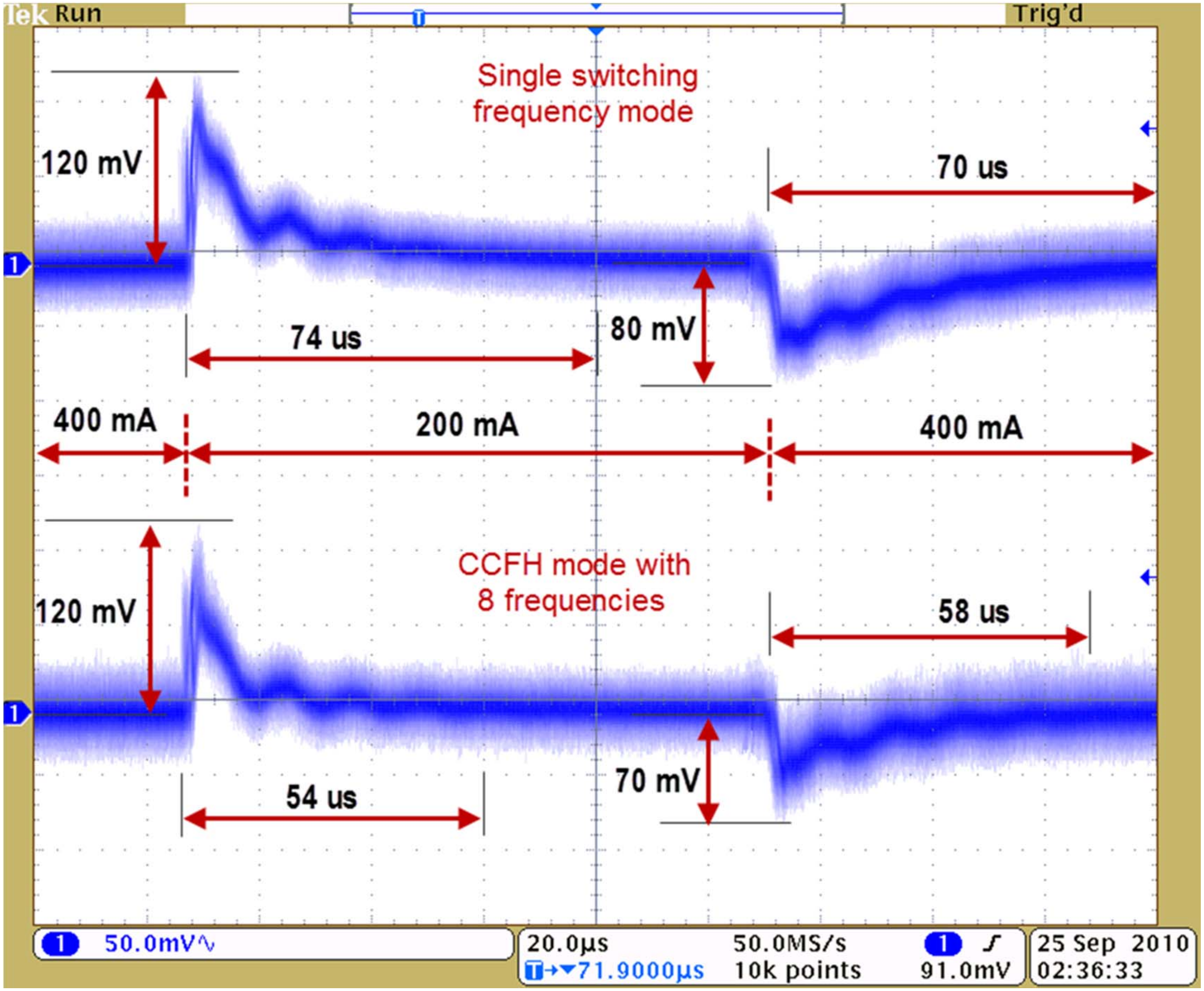
CCFH: Distortion



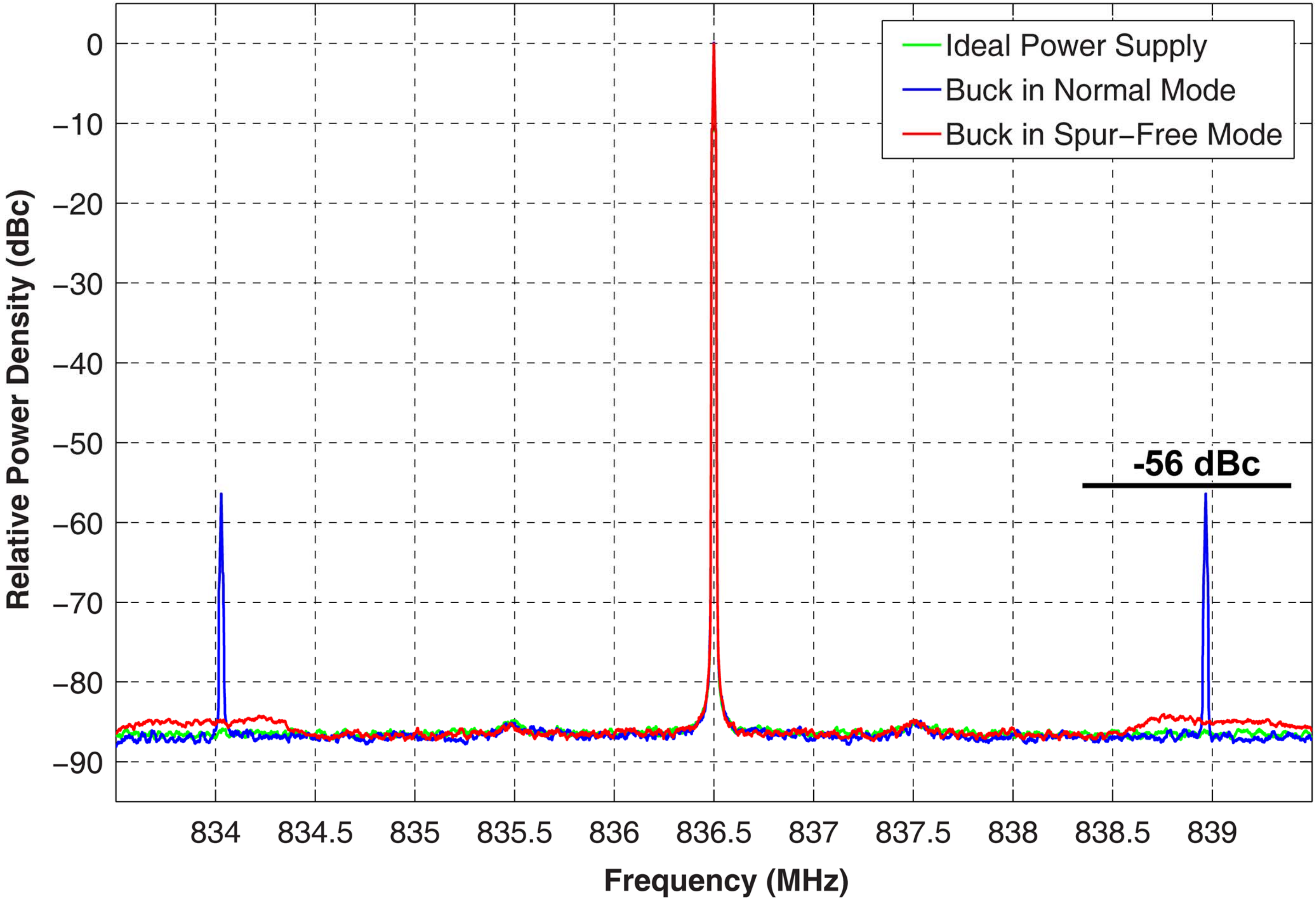
CCFH: Output Ripple



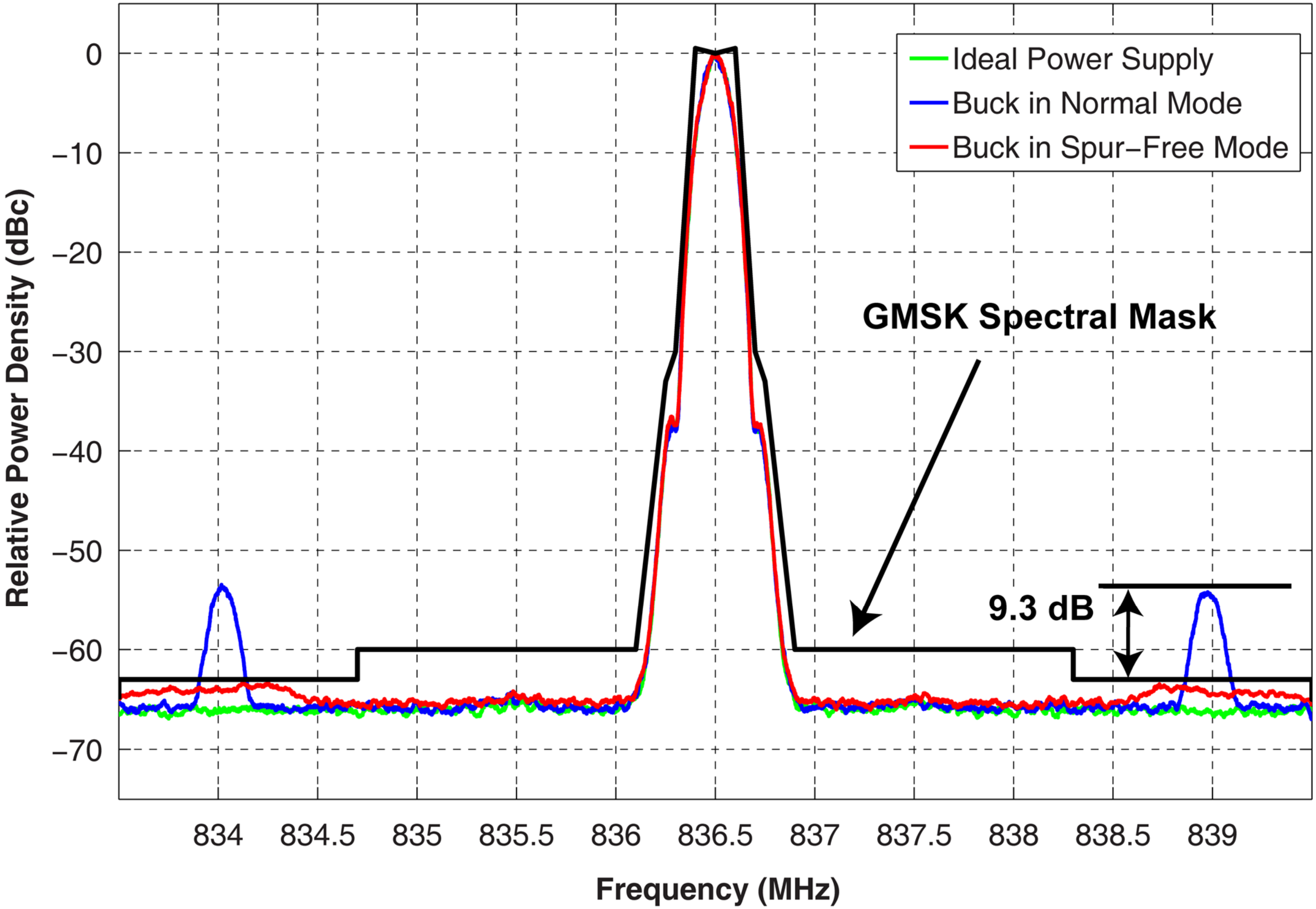
CCFH: Transient Response



Verification with a GSM PA



Verification with a GSM PA



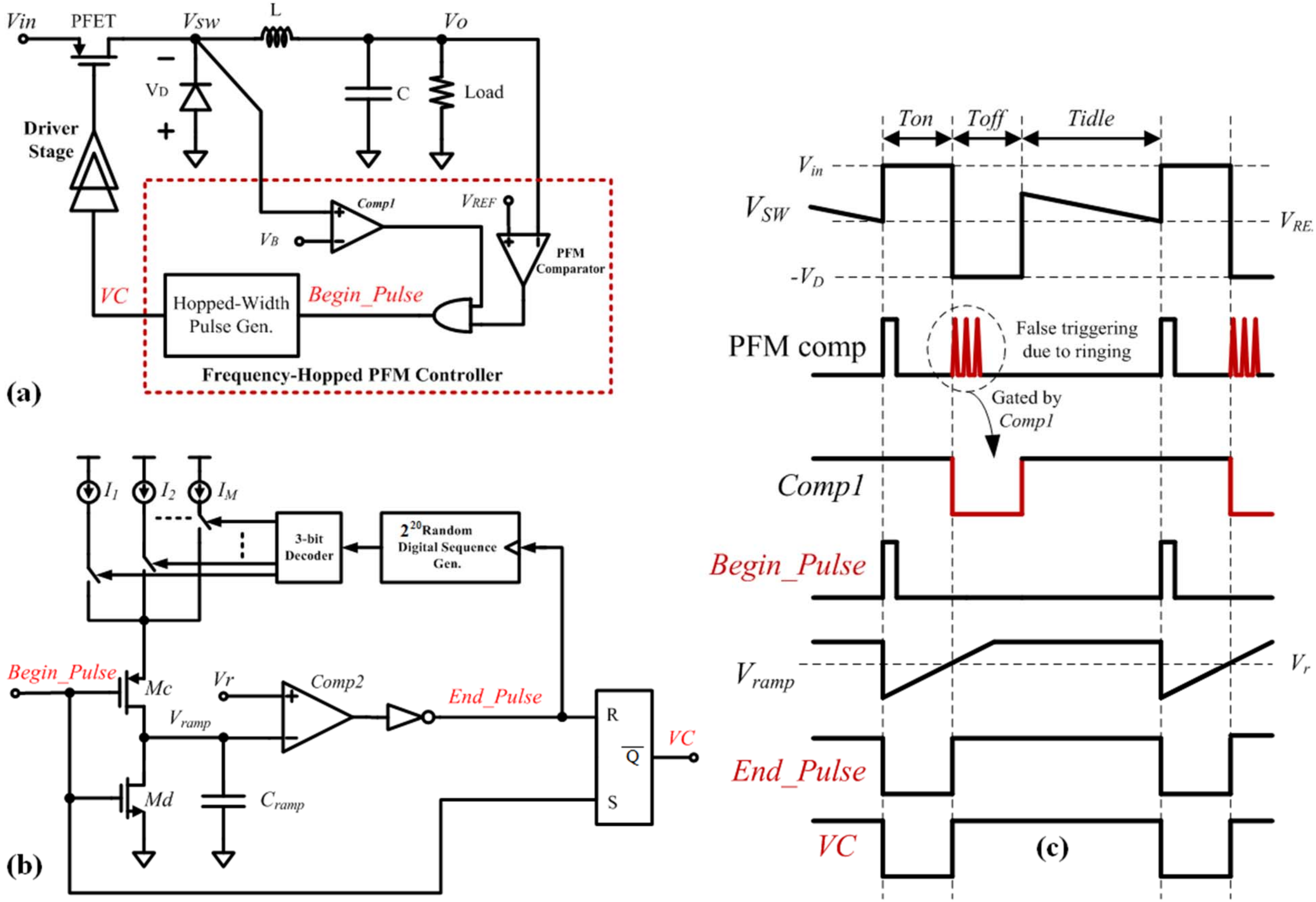
Chengwu Tao and Ayman Fayed, "A GSM Power Amplifier Directly-Powered from a DC-DC Power Converter," IEEE Microwave and Wireless Components Letters, vol. 22, no. 1, pp. 38-40, Jan. 2012.

CCFH in PFM Architectures

- PFM is popular at light load to improve efficiency
- Not immediately obvious how to meet spur-elimination condition → Frequency varies with the load → No direct control over it!
- One must observe, though, that the spur-elimination condition is relative in nature and not absolute
- Meeting the condition between hopped on-times in COT topologies leads to meeting it between the frequencies → Despite the nonlinear relationship!

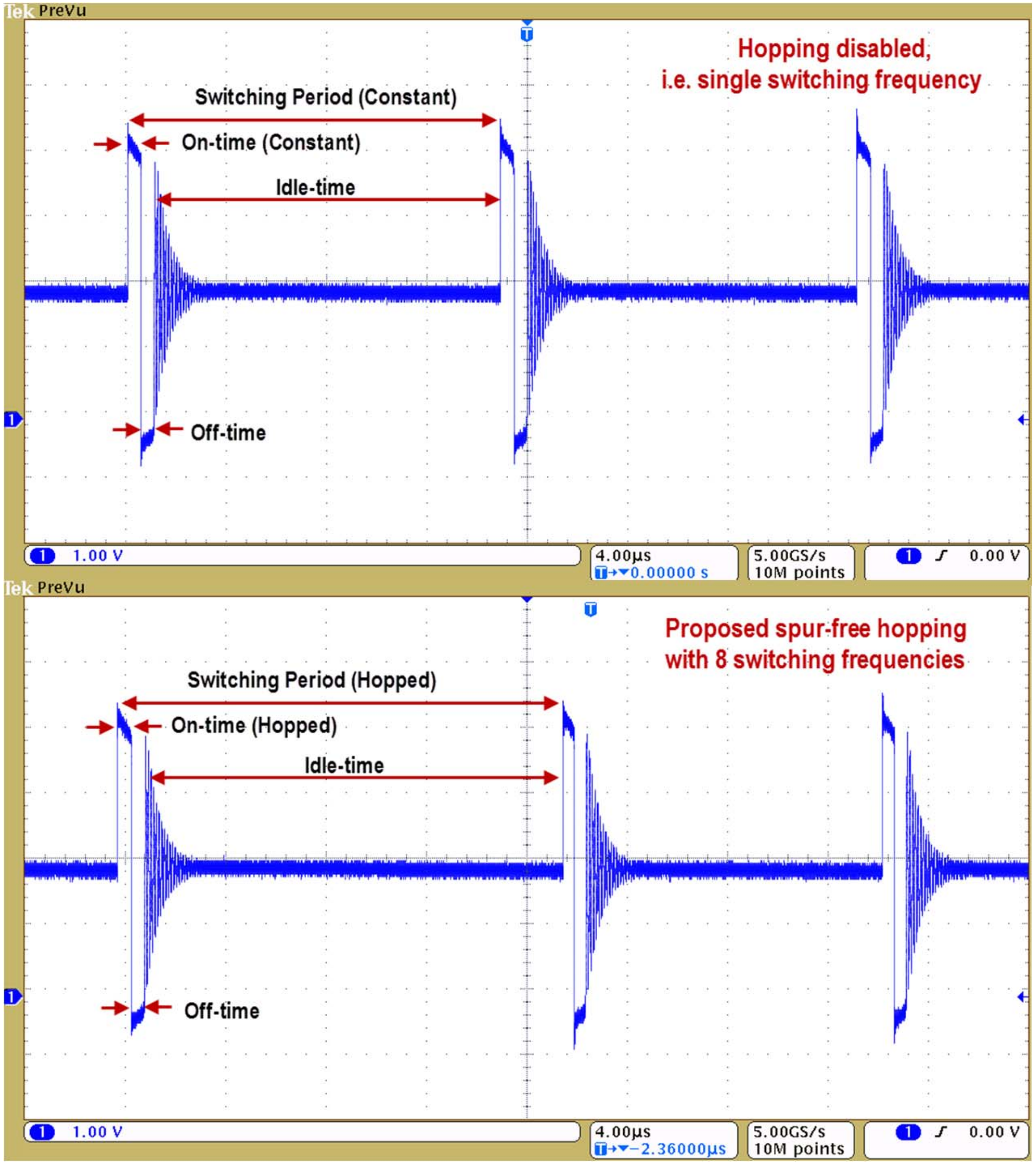
$$f_s = \frac{2 \times V_o \times L \times I_L}{V_{in} \times \left(V_{in} - V_o\right) \times T_{on}^2}$$

CCFH: PFM Architecture - COT

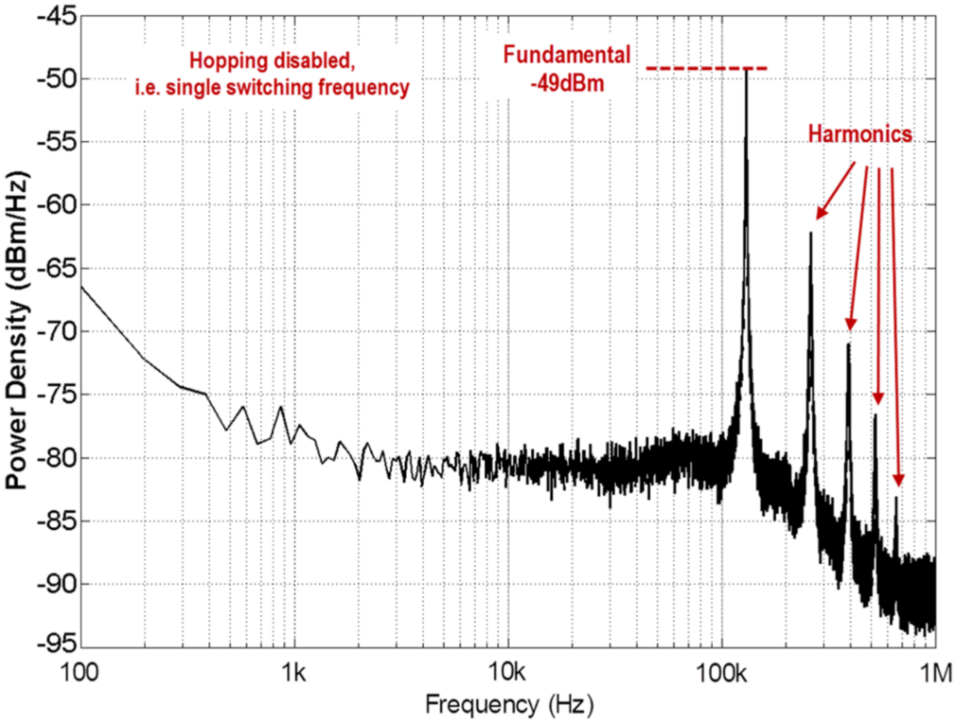


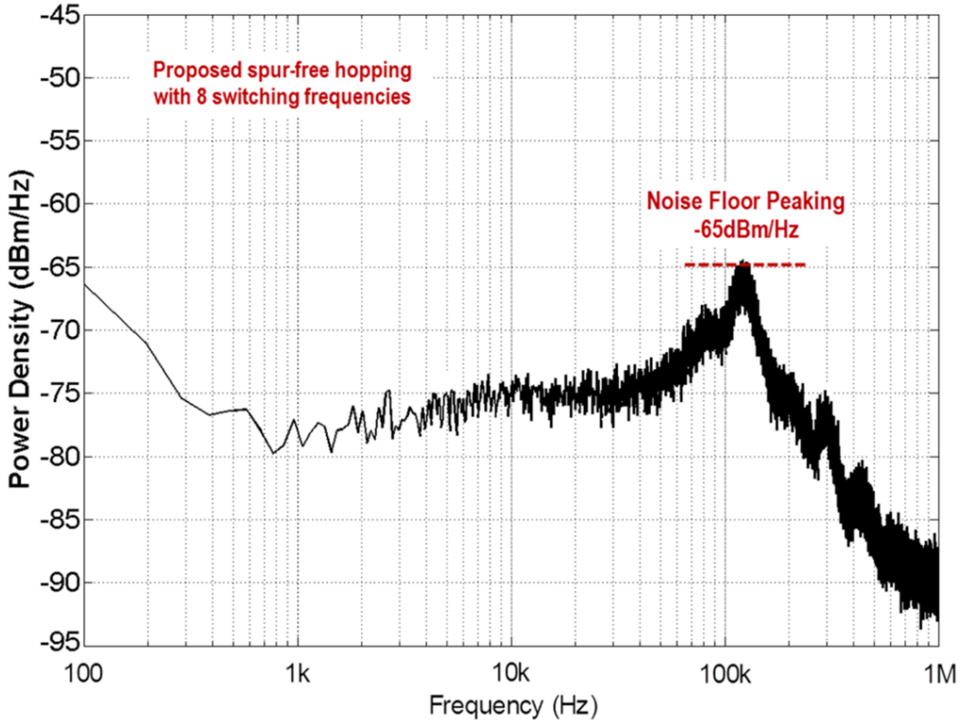
[1] Chengwu Tao and Ayman Fayed, "A Low-Noise PFM-Controlled Buck Converter for Low-Power applications," IEEE Transactions on Circuits and Systems I, vol. 59, no. 12, pp. 3071-3080, Dec. 2012.

CCFH-PFM-COT: Transient Performance



CCFH-PFM-COT: Output Spectrum





CCFH: Summary

- DC-DC Converters
  - Spur-Free with minimum noise floor increase
  - Minimal low-frequency noise impact
  - Maintain time-domain ripple magnitude
  - Spur-Free performance at every node → Integration and rail-sharing
  - Works with both PWM and PFM Control
- Applications
  - Direct powering of Analog/RF (e.g. PAs)
  - Polar PAs and Class-D Amps
  - Improvement in EMI