

# Delta-Sigma Modulation in Fractional- $N$ Frequency Synthesis

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**Abstract**—This paper describes a delta-sigma ( $\Delta$ - $\Sigma$ ) modulation and fractional- $N$  frequency division technique to perform indirect digital frequency synthesis based on the use of a phase-locked loop (PLL). The use of  $\Delta$ - $\Sigma$  modulation concepts results in a beneficial noise shaping of the phase noise (jitter) introduced by fractional- $N$  division. The technique has the potential to provide low phase noise, fast settling time, and reduced impact of spurious frequencies when compared with existing fractional- $N$  PLL techniques.

## I. INTRODUCTION

USE of a phase-locked loop (PLL) with arbitrary frequency division ( $\div N$ ) is a well-known method for synthesizing desired frequencies [1]. The underlying interest in this paper is to establish a technique for monolithic frequency synthesizers which maximizes the frequency achievable in a given technology. A goal, for instance, would be to synthesize frequencies required for mobile radio applications in the 1- to 2-GHz frequency range using a short-channel BiCMOS technology with minimal or no external components.

Fractional- $N$  indirect digital frequency synthesis, i.e., using a PLL, is particularly well suited to integrated circuit applications. The technique allows very narrow channel spacing relative to the output frequency, large bandwidth in the PLL relative to the channel spacing, and high output frequency relative to the processing technology used in the IC. Consequently, the availability of a low-noise, low-spurious-frequency form of fractional- $N$  division can, in our view, have a significant impact on the performance of low-cost frequency synthesizers for use in consumer products.

This paper describes a new method of implementing the fractional- $N$  function ( $\div N$ ) in the feedback loop of the PLL, where  $N$  is a rational number rather than an integer. By using fractional- $N$  division, the wider loop bandwidth for a given channel spacing allows faster settling time [1] and reduced phase noise requirements to be imposed on the voltage-controlled oscillator (VCO) [2]. With reduced phase noise requirements, lower cost, possibly on chip, VCO's might be used. The faster settling time, resulting from broader loop bandwidth of a PLL-based fractional- $N$  frequency synthesis, has the potential to eliminate additional hardware

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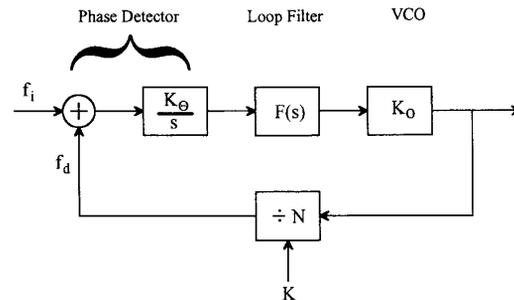


Fig. 1. Use of a phase-locked loop for indirect digital frequency synthesis.

typically included in a PLL to provide fast settling. Thus, a high-performance fractional- $N$  frequency synthesizer technique could lead to a complete high-performance synthesizer on a chip.

Typically, single-loop indirect digital frequency synthesis is accomplished as indicated in Fig. 1. The term indirect is used to signify a closed-loop context. This should be compared to direct synthesis where it is required to have a clock frequency and accumulator operating at higher than the synthesized frequency in the case of direct digital synthesis [3], or analog mixers and filters in the case of direct analog synthesis [3] or multiple-loop synthesis.

With indirect digital synthesis, the upper limit of the synthesized frequency depends mainly on the design of the voltage- or current-controlled oscillator (VCO or CCO) and the initial stage of the  $\div N$  function. This in turn depends on the frequency capability of the fabrication technology used. Two examples are 200 MHz in a 2- $\mu$ m CMOS process [4] or 1 GHz in a silicon bipolar process [5]. The reference frequency and the divided down VCO frequency, being much lower, do not present significant implementation problems.

A brief overview of indirect digital synthesizers is presented here to allow comparison with the new technique. As indicated in Fig. 1, the action of the PLL drives frequency  $f_d$  to be equal to the input reference frequency  $f_i$ , and the output frequency is thus given by  $f_o = N f_i$ . Since frequency  $f_i$  is fixed, the desired synthesized output frequency  $f_o$  is controlled by  $N$ . Other symbols introduced in Fig. 1 follow those used in [1].

Three techniques to implement the  $\div N$  function indicated in Fig. 1 have been identified in the literature [3] namely: pulse swallowing, phase interpolation, and Wheatley random jittering. Each of these techniques has advantages and disadvantages as summarized in Table I. The new technique,

TABLE I  
EXISTING TECHNIQUES COMPARED TO NEW TECHNIQUE

Technique	Pulse Swallowing	Phase Interpolation	Wheatley Random Jittering	$f-d$ Modulated Jittering
Prone to Spurious Frequencies	Yes	No	No	No
Precision Analog Components Required	None	D/A Converter or Delay Generator	None	None
Minimum Complexity of Digital Hardware	1 accumulator	1 accumulator	1 accumulator + random number generator	2 accumulators
Introduces Broad Band Noise in $f_d$	No	No	Yes	No

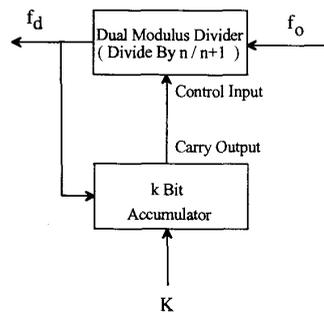


Fig. 2. Detailed view of the pulse swallowing approach to the  $\div N$  block in Fig. 1.

described in the following sections of this paper, is also included in Table I for comparison.

## II. FIRST-ORDER $\Delta$ - $\Sigma$ MODULATION FOR FRACTIONAL- $N$ DIVISION

We will discuss pulse swallowing in some detail to provide the terminology needed. Fig. 2 shows some detail of the pulse swallowing approach to performing the  $\div N$  function shown in Fig. 1. The point of view presented in this paper is the association of the accumulator in Fig. 2 with a first-order  $\Delta$ - $\Sigma$  modulator, also known as a  $\Sigma$ - $\Delta$  modulator [6], as shown in Fig. 3(a). The background drawn on in this paper is  $\Delta$ - $\Sigma$  modulation as used in the realization of oversampled A/D converters (OSAD's) [6]. In the context of the OSAD application, a body of experience has been developed about the use of the noise-shaping properties of  $\Delta$ - $\Sigma$  modulators to obtain a high dynamic range for narrow-band signals. The parallels we will now discuss allow carryover of that knowledge to frequency synthesis.

The premise of the pulse swallowing approach is that by dividing by  $n$  sometimes and  $n+1$  at other times, one can, on average, divide by a fractional  $N$  such that  $n < N < n+1$ , where  $n$  and  $n+1$  are the two moduli by which the dual-modulus divider divides. The  $k$ -bit accumulator shown in Fig. 2 has its value  $R$  modified periodically by the addition of a control word  $K$  to the value  $R$  stored in the accumulator. The condition of overflow in the accumulator is used to shift the division to  $n+1$ , effectively swallowing a pulse and dynamically increasing the division ratio. Hence, the average

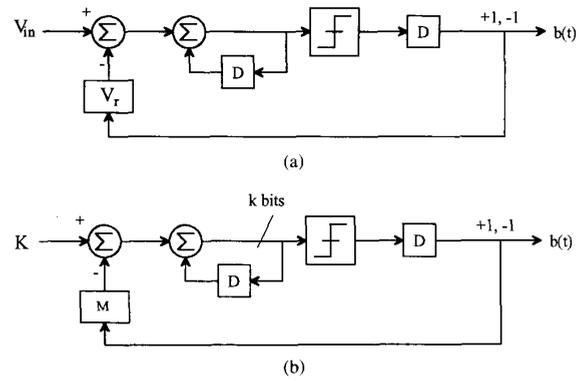


Fig. 3. (a) An analog  $\Delta$ - $\Sigma$  modulator used as an OSAD. (b) A model for the OSAD as a  $\Delta$ - $\Sigma$  modulator.

$\div N$  ratio is controlled by  $K$ . It can be seen that, for a  $k$ -bit accumulator, the accumulator will produce an overflow on average every  $K/2^k$  cycles of the  $f_d$  clock. The average division ratio of the dual-modulus divider following the carry output (bit stream) generated in Fig. 2 is then

$$N = n + \frac{K}{2^k}. \quad (1)$$

The detailed operation of the accumulator is now explained to show its similarity to the block diagram of the analog first-order  $\Delta$ - $\Sigma$  modulator in Fig. 3(a). On every cycle of the  $f_d$  signal, in Fig. 2, the variable  $R$  in the accumulator is assigned the value  $R + K$  unless the accumulator overflows, when the value assigned to the accumulator is  $R + K - 2^k$  and a carry output is generated. In this way, the accumulator overflow is equivalent to a comparator decision. The value stored in the accumulator is then essentially the integral of the frequency error between the desired frequency  $K$  and the actual frequency control input (the carry output bit stream). This is exploited by the digiphase principle [3] where the integral of the frequency error is used as a measure of the phase error.

This leads us to consider an all-digital  $\Delta$ - $\Sigma$  modulator, shown in Fig. 3(b), which performs a very similar function. The block diagram of the digital  $\Delta$ - $\Sigma$  modulator differs from the accumulator in several ways.

1) The accumulator gives its carry output result instantaneously, but is controlled by the clock to perform an operation once every cycle, whereas the  $\Delta$ - $\Sigma$  modulator requires at least one unit delay ( $D$ ) around the loop.

2) In the case of the accumulator of Fig. 2, the two values limiting the range of the input signal are defined by the accumulator size, i.e., between 0 and  $2^k$ . In the case of the digital  $\Delta$ - $\Sigma$  modulator of Fig. 3(b), the input signal range is limited to  $\pm M$ .

3) The accumulator produces a stream of 1's and 0's whereas the  $\Delta$ - $\Sigma$  modulator is traditionally interpreted to produce a stream of +1's and -1's consistent with the  $\pm M$  input range. This means that the  $\Delta$ - $\Sigma$  modulator is centered around 0 whereas the accumulator is centered around  $2^k - 1$ .

Despite these differences, the single integration and the quantization implied in the carry output of the accumulator

suggest that the dynamics of the two circuits should be substantially similar. With a single-bit output, the quantization noise is unavoidably large. However, both circuits use a noise-shaping action to push the resulting quantization noise away from dc and away from all multiples of the clock frequency. Consequently, we use the term  $\Delta$ - $\Sigma$  modulator to signify either an analog OSAD or an equivalent digital modulator which provides an input to the dual-modulus divider in Fig. 2.

The general technique will now be explained followed by two examples with experimental results. The novelty of the new technique to be described here lies in the use of a class of  $\Delta$ - $\Sigma$  modulators that are more complicated than the first-order  $\Delta$ - $\Sigma$  modulator identified in Fig. 3. The higher order  $\Delta$ - $\Sigma$  modulators to be used have more desirable characteristics embodied in a different spectral content of the bit stream than occurs in the pulse swallowing or the Wheatley random jittering case.

### III. HIGHER ORDER $\Delta$ - $\Sigma$ MODULATION FOR FRACTIONAL- $N$ DIVISION

#### A. The Concept

Our view of the accumulator in Fig. 2 as a  $\Delta$ - $\Sigma$  modulator allows one to apply knowledge of higher order OSAD's to frequency synthesis. Each integrator stage of an OSAD introduces a zero at the origin, thus noise shaping the quantization noise in the frequency domain. For the first-order  $\Delta$ - $\Sigma$  modulation implied in the pulse swallowing circuit of Fig. 2, the integration applied when converting from frequency to phase removes the zero from the noise-shaping function. The first-order  $\Delta$ - $\Sigma$  modulation also fails to randomize the quantization error [7], [8] and consequently spurious frequency components become a problem. However, a second or higher order of integration can be used to reduce the practical impact of this periodicity as demonstrated by numerous  $\Delta$ - $\Sigma$  modulator structures used as OSAD's, for example [9], [10]. This paper investigates the hypothesis that spurious output frequencies in fractional- $N$  frequency synthesis can similarly be reduced by such higher order noise-shaping techniques.

The new approach has the following features:

1. Two or more integrations of the error introduced by a quantizing nonlinearity are used to produce randomized or pseudorandomized behavior in the output bit stream.
2. The error resulting from the quantization nonlinearity is filtered by the  $\Delta$ - $\Sigma$  modulator to remove frequency components near dc and near all multiples of  $f_d$ , the  $\Delta$ - $\Sigma$  modulator clock.

The nonlinearity does not necessarily have to result from use of the accumulator overflow event. It could, for example, also result from the sign bit of two's complement number or some other multiple-bit (less coarse) quantization of the value  $R$  stored in one of the accumulators. That is, suitable  $\Delta$ - $\Sigma$  modulator structures are not limited to only those that produce a single-bit quantized output. Thus, the dual-modulus divider of Fig. 2 is a special case and, in general, multimodulus dividers are possible.

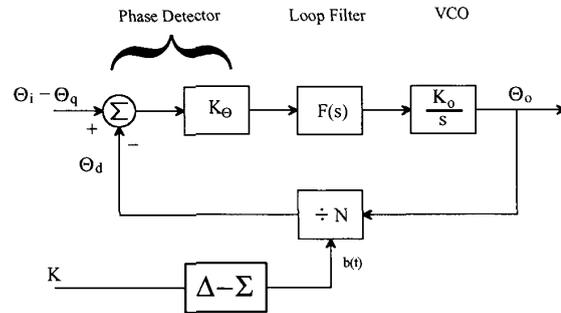


Fig. 4. The PLL of Fig. 1 in terms of phase showing the phase noise introduced by the  $\Delta$ - $\Sigma$  modulated dual-modulus divider.

#### B. Analytical Expressions for the Effect of Noise Shaping

In this section, a model for the phase noise in the output of the dual-modulus divider,  $f_d$ , is developed. A discussion of the effects of quantization noise on the overall output,  $f_o$ , follows. The goal is to model the dual-modulus divider as an ideal  $\div N$  with an additive phase noise,  $\Phi_q$ , at its output. This will allow presenting the PLL of Fig. 1 at the level of phase, including  $\Phi_q$ , as shown in Fig. 4. Our first step is to evaluate the phase noise in  $f_d$  assuming an ideal VCO at a fixed frequency.

The instantaneous frequency of  $f_d$ ,  $f_d(t)$ , is determined by the VCO frequency,  $f_o$ , and the instantaneous division rate. The instantaneous division rate in the case of the  $\Delta$ - $\Sigma$  modulated dual-modulus divider is given by  $n + b(t)$ , where  $b(t)$  is the bit stream alternating between 0 and 1; thus

$$f_d(t) = \frac{f_o}{n + b(t)}. \quad (2)$$

The bit stream can then be broken up into the desired dc value,  $K/M$ , and an additive quantization noise [6], [9]. In the time domain this quantization noise is labeled  $q(t)$ , giving

$$f_d = \frac{f_o}{n + \frac{K}{M} + q(t)}. \quad (3)$$

Since the nominal frequency is  $f_d = f_o/(n + K/M) = f_o/N$ , the normalized instantaneous frequency departure,  $y(t)$ , [10] is then given by

$$y(t) = \frac{1}{1 + \frac{q(t)}{N}} - 1. \quad (4)$$

By making use of the approximation,  $1/(1 + \epsilon) \cong 1 - \epsilon$  for small  $\epsilon$ , we can write

$$y(t) \cong -\frac{q(t)}{N}. \quad (5)$$

If the rms spectral density of the quantization noise,  $q(t)$ , is labeled  $Q(f)$ , then the power spectral density of the normalized frequency deviations will be given by

$$S_y(f) = \frac{|Q(f)|^2}{N^2}. \quad (6)$$



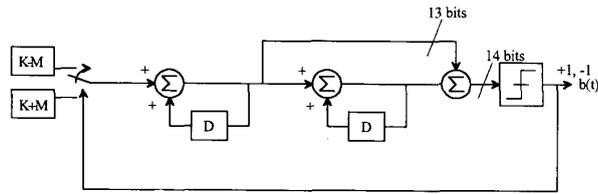


Fig. 6. Schematic diagram of a second-order  $\Delta-\Sigma$  modulator implementation.

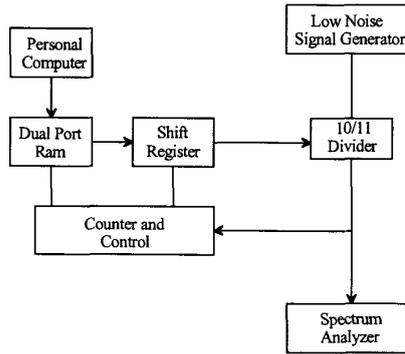


Fig. 7. Test circuit for the  $\Delta-\Sigma$  modulated dual-modulus divider.

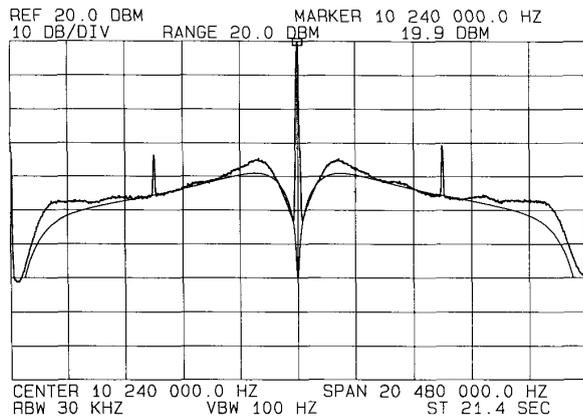


Fig. 8. Spectrum analyzer measurement of  $f_d$  (wide span) measured results compared to theoretical results. Vertical axis: 10 dB/div; horizontal axis: 500 kHz/div.

introduce a spur within the loop bandwidth and is considered to be a worst-case example.

The power spectral density of  $f_d$  for the second-order all-digital  $\Delta-\Sigma$  modulator implementation is shown in Fig. 8. The notchy region of the spectrum around the  $f_d$  frequency of 10.24 MHz shows that the noise shaping of the  $\Delta-\Sigma$  modulator works as intended. The full depth of the notch is not visible because of the resolution bandwidth of the spectrum analyzer. The calculated PSD using (7) and (10) is also shown using the spectrum analyzer resolution bandwidth of 30 kHz. The comparison indicates a close correspondence between predicted and measured results with the exception of the spur at half the clock frequency.

### B. A Third-Order All-Digital Digital $\Delta-\Sigma$ Modulator

A third-order structure is shown in Fig. 9. The linearized transfer function for this modulator is

$$H(f) = \frac{(1 - z^{-1})^3}{(1 - z^{-1})^3 + (0.25 + (1 - z^{-1}) + 2(1 - z^{-1})^2)} \quad (11)$$

The theoretical and measured power spectral density of  $f_d$  for the third-order all-digital implementation is shown in Fig. 10. It is also very close to the approximate analytical expression for the quantization noise.

This higher order implementation requires about 140 cells for the same channel spacing and reference frequency as the second-order modulator considered in Section IV-A. This is only a 40% increase in digital complexity.

The use of a higher order  $\Delta-\Sigma$  modulator reduces the theoretically expected quantization noise close to the carrier. The price to be paid for this is that there is more noise further away from the carrier. Moreover, the quantization noise rises at 20 dB per decade with the second-order  $\Delta-\Sigma$  modulator and 40 dB per decade with the third order  $\Delta-\Sigma$  modulator. Consequently, a classical PLL with only 40 dB per decade of attenuation outside the loop bandwidth results in a white-noise floor with the third-order  $\Delta-\Sigma$  modulator.

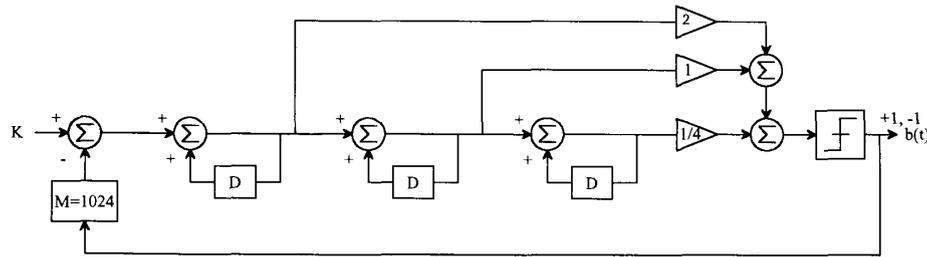
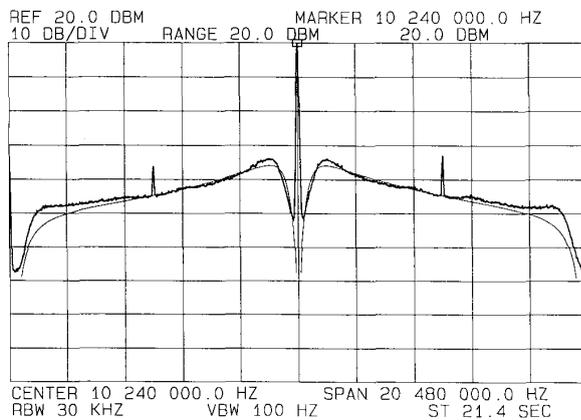
## V. CLOSED-LOOP EXPERIMENTAL RESULTS

A closed-loop prototype has been prepared and used to evaluate the technique. The prototype uses a relatively low-quality VCO based on a varactor tuned tank circuit, an ECL 40/41 divider, an ECL phase detector, and a loop filter, all implemented with discrete components on a printed circuit board. The reference frequency is approximately 10 MHz, giving an output tuning range centered at 405 MHz.

To test the technique in a closed-loop prototype, a third-order all-digital  $\Delta-\Sigma$  modulator as shown in Fig. 9 is simulated for  $2^{20}$  cycles, with the resulting bit stream stored in RAM. This bit stream is then clocked out of the RAM in real time by the divided down VCO clock. The input resolution of the simulated  $\Delta-\Sigma$  modulator is chosen as one part in 2048, giving a channel spacing of approximately 5 kHz. Consequently 405.005 MHz, one channel spacing above the center frequency, is chosen as a test frequency.

With a loop bandwidth of 30 kHz, the loop performance is primarily limited by the phase noise of the VCO, as would be expected in a monolithic PLL. The phase noise of the synthesizer is indicated in Fig. 11, where the lower (dotted) trace is the measured single sideband power spectrum of the loop (offset from the synthesized frequency) with a fixed divide by 40 and the upper (solid) trace is the measured spectrum with the  $\Delta-\Sigma$  modulation included. The  $\Delta-\Sigma$  quantization noise is attenuated above 30 kHz by the PLL and an extra pole introduced at 200 kHz at the VCO input, while it is negligible below 30 kHz due to the  $\Delta-\Sigma$  noise shaping.

Also shown in Fig. 11 at higher frequency offsets are some discrete spurious frequency components in the phase noise

Fig. 9. Block diagram of a third-order  $\Delta$ - $\Sigma$  modulator.Fig. 10. Spectrum analyzer measurement of  $f_d$  (wide span) measured results compared to theoretical results. Vertical axis: 10 dB/div; horizontal axis: 200 kHz/div.

spectrum. These are primarily due to: 1) feedthrough, in the experimental apparatus, of the reference frequency and its harmonics at 10 MHz and multiples away from the synthesized frequency; and 2) residual spurs not completely randomized by the  $\Delta$ - $\Sigma$  modulator such as the 5-MHz spur shown in Fig. 10. These spurs are relatively low and sufficiently far from the synthesized frequency that they need have no adverse effect in a local oscillator application for a radio receiver. However, they could be reduced further by improved circuit design in the case of 1) and higher order modulation in the case of 2). The improvement of  $\Delta$ - $\Sigma$  modulator architectures is a matter for further study and research.

## VI. CONCLUSIONS

The use of single-loop indirect digital synthesis to synthesize closely spaced frequencies near the limit of a given technology requires the use of precision analog components or the acceptance of some compromise in the  $\div N$  function using established approaches. In the pulse swallowing approach spurious frequencies arise, while Wheatley random jittering produces increased random phase noise. A new technique for monolithic implementation that avoids these difficulties has been proposed.

To develop the new technique, the pulse swallowing method has been shown to be similar to a first-order  $\Delta$ - $\Sigma$  modulated dual-modulus divider. By drawing on knowledge of OSAD's,

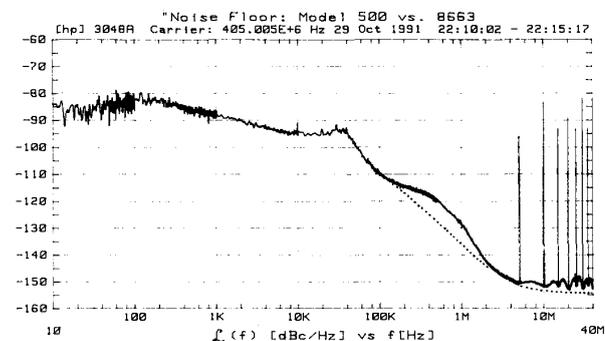


Fig. 11. Single sideband phase noise of the synthesizer. Vertical axis: dBc/Hz for noise, dBc for spurs (10 dB per division); horizontal axis: offset from the carrier (Hz).

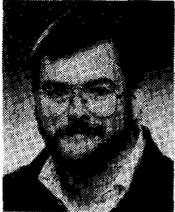
we show that higher order  $\Delta$ - $\Sigma$  modulation can be used to provide bit streams with a better spectral content for fractional- $N$  division. This is confirmed by experimental results showing that higher order modulation can whiten and then noise shape the jitter introduced by the dual-modulus divider. It is also shown that an all-digital  $\Delta$ - $\Sigma$  modulation can be performed without introducing substantial phase noise close to the carrier in both the open- and closed-loop context.

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Jointly with his co-researchers, Dr. Kwasniewski is a recipient of the 1991 Telecommunications Research Institute of Ontario Feedback Award and 1992 Canadian Standard Design Association Integrated Circuit Design Award for work on multiprocessor rapid IC prototyping and innovative CMOS dual-modulus divider design, respectively.