A Fully Integrated CMOS DCS-1800 Frequency Synthesizer

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***Abstract*—A prototype frequency synthesizer for the DCS-1800 system has been integrated in a standard 0.4-μm CMOS process without any external components. A completely monolithic design has been made feasible by using an optimized hollow-coil inductor low-phase-noise voltage-controlled oscillator (VCO). The frequency divider is an eight-modulus phase-switching prescaler that achieves the same speed as asynchronous dividers. The die area was minimized by using a dual-path active loop filter. An indirect linearization technique was implemented for the VCO gain. The resulting architecture is a fourth-order, type-2 charge-pump phase-locked loop. The measured settling time is 300 μs, and the phase noise is up to -123 dBc/Hz at 600 kHz and -138 dBc/Hz at 3-MHz offset.**

***Index Terms*— Analog integrated circuits, CMOS RF, frequency synthesizer, integrated inductors, phase-locked loop, phase noise.**

I. Introduction

IN WIRELESS transceivers, there is a clear trend toward full integration of the radio-frequency (RF) front end on a single die for reasons of low cost and power [1]–[4]. While most current designs use bipolar technologies, the design of CMOS RF building blocks is a very important research topic at the moment, as is demonstrated by many publications in that area [5]–[12]. The use of a submicrometer CMOS process for these circuits prepares to incorporate the digital baseband processing circuitry on the same chip in future wireless systems.

A major concern for full integration is the local oscillator (LO) frequency synthesizer. It contains high-frequency building blocks, such as the voltage-controlled oscillator (VCO) and the prescaler, as well as low-frequency filters and other circuitry. Both pose big design challenges and mostly require external components. Although some of the presented transceivers incorporate the VCO active circuitry on the die, they all need an external inductance–capacitance (LC) tank to achieve the required phase-noise specification. And the large time constants required for the loop filter generally lead to large and thus external capacitors. The prototype design presented here tries to give a solution to these problems.

In Section II, the global options taken in the phase-locked-loop (PLL) architecture are discussed. Section III discusses the several building blocks of the PLL. The two high-frequency blocks, the VCO and the frequency divider, are of course crucial in the feasibility of integration in a standard CMOS process. For the low-speed building blocks, the loop filter discussed in Section III-D especially is of great importance, as this will determine the transfer of circuit noise to the output phase noise. The measurement results are given in Section IV, and some conclusions are drawn in Section V.

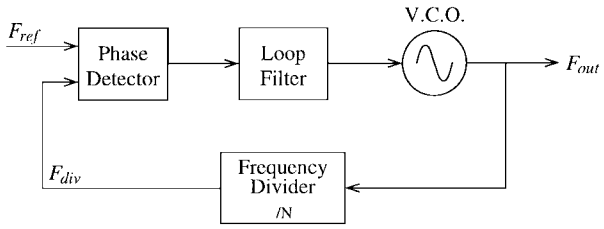

Fig. 1. PLL frequency synthesizer.

II. PLL Architecture

The frequency synthesizer is of course implemented by means of a PLL, the general block diagram of which is shown in Fig. 1. The feedback action in the loop causes the two input signals of the phase detector to lock, thereby creating a VCO output frequency $(F_{\rm out})$, which is a multiple of the reference frequency $(F_{\rm ref})$.

The value of the synthesized frequency is determined by the division factor of the frequency divider. The prescaler division factors (i.e., $64 - 71$) have been chosen in order to use this prescaler as the only block in the PLL frequency divider. Starting from a 26.6-MHz reference, the possible output frequencies range from 1702.4 to 1888.6 MHz, which neatly covers the required frequency band from 1.71 to 1.88 GHz. Of course, addition of the fractional-N division technique is necessary to achieve a 200-kHz frequency resolution [13], [14].

The VCO was designed to have a tuning range as large as possible to cover the full frequency band of the DCS-1800 system without the need for switching in or out discrete capacitors. This coarse extra tuning that can be added to the normal fine tuning of a VCO increases the frequency range but also adds some problems to the design. First, the digital logic system that controls the switching must be carefully integrated in the design of the full-loop dynamics in order to guarantee correct locking and stability over the complete range. Furthermore, it is not straightforward to add these switched capacitors to the oscillator's LC tank without deteriorating the overall quality factor. The switches must be implemented as MOS transistors, which always have some series resistance in their on state, as well as parasitic

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junction capacitance to the substrate from their source and drain regions. So the circuit design as well as the layout will have an important influence on the resulting quality factor.

A drawback of this "single-step" VCO tuning is the fact that the VCO sensitivity must be very large, which will have its consequences in the various transfer functions of charge pump and loop filter noise to the output. This will be investigated in Section III-D. Second, the fact that the junction capacitance used for VCO tuning cannot always be biased far from the forward region for the lower frequency range will increase the nonlinearities in the VCO. As a result, upconverted low-frequency $1/f$ noise will have a larger contribution to the VCO phase noise [15]. This is a problem that has not been solved yet.

III. PLL Building Blocks

A. Voltage-Controlled Oscillator

The performance of planar inductors has improved recently due to efficient analysis of the parasitics with finite-element simulation techniques [11], [12]. These studies have resulted in some general guidelines for designing high-quality spiral inductors on silicon substrates.

1) *Limit the width of the metal conductors:* This is due to a more important increase in the high-frequency resistance because of the skin effect.
2) *Use minimum spacing in between the conductors:* This will maximize the inductance value, and the fringing capacitance is generally negligible.
3) *Do not fill the inductor up to the center:* The innermost tracks contribute only a small amount of inductance, but due to eddy currents generated by the magnetic field of the outer turns, their high-frequency resistance increases enormously. It is best if they are simply omitted. This leads to the *hollow coil* shape.
4) *Limit the area occupied by the coil:* This way, the magnetic field penetrates less deeply into the substrate, and the associated substrate losses will be smaller. This guideline is only valid for conductive substrates, as the substrate currents in lowly doped wafers are already small.

As the process available for this design uses nonepi wafers, the substrate resistivity is high enough to indeed neglect the last guideline. This generally leads to larger values of L for the optimal coil. This is not always an advantage, as large inductance values lead to a smaller capacitance value and hence less tuning range, if an important part of the capacitance is already accounted for by the coil and transistor parasitics. Using two coils in series to form a balanced inductor will result in this constraint. The optimum VCO design must include only one coil in the inductor.

Therefore, a new coil shape was developed, as shown in Fig. 2. Instead of drawing a normal spiral track and then making the connection to the inner turn in a different metallization level, the metal track now moves inside every half turn, until the center is reached, and then moves outside again every half turn. Both the Metal1 and Metal2 routing levels are used, except for the cross sections, which use of course only one metal level for each direction. The number of cross sections is equal for both shapes, so this new shape has no effect on the dc series resistance. This coil is completely symmetrical and can thus be used as a differential floating inductor. Using the finite-element optimization procedure described in [11], the coil parameters given in Table I are obtained. In spite of the fact that only two metal layers are available, a quality factor as high as 8.6 is reached.

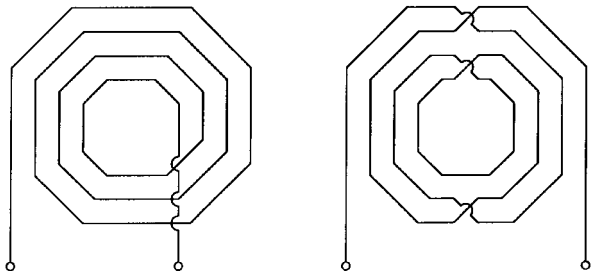

Fig. 2. Planar inductor coil shape: (a) standard octagonal and (b) symmetrical.

TABLE I
Optimized Coil Parameters

Radius	r	120	$[\mu m]$
Width	w	15	$[\mu m]$
Spacing	sp	1	$[\mu m]$
No. of Turns	n	3	[-]
Frequency	F	1.8	$[GHz]$
Inductance	L	2.8	$[nH]$
Total Resistance	R_{eff}	3.7	$[\Omega]$
Quality Factor	Q	8.6	[-]

The oscillator circuit schematic is shown in Fig. 3. The negative resistance is formed by the double cross connection of an NMOS ($M1$–$M2$) and a PMOS ($M3$–$M4$) differential pair in positive feedback. In a 3-V system, the supply current can be used twice for amplification with this circuit. A drawback of this configuration is of course the larger parasitic capacitances of the PMOS transistors with respect to an NMOS-only implementation. This will result in a slightly smaller available tuning range as the fixed part of the tank capacitance has increased. The use of slower PMOS transistors in this oscillator configuration is no problem, as the gate–source capacitance is situated in parallel with the resonance tank. An advantage is that there is no need for a connection to the common-mode point of the inductor, which would be a problem for the new symmetrical coil shape. The frequency tuning is done with the standard available P+/N-well junction capacitors. The bias current is set at 3.7 mA, and the transistors are biased at $V_{GS} - V_T = 0.33$ V.

The measured free-running oscillation frequency is 1.99 GHz, which is only 0.5% off of the predicted value of 1.98 GHz. The resulting phase noise was measured with a spectrum

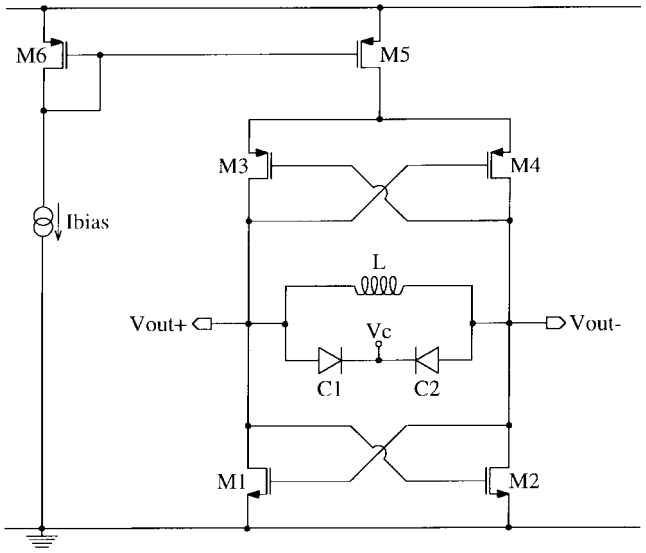

Fig. 3. Planar-LC oscillator circuit schematic.

analyzer to be −113 dBc/Hz at 200 kHz offset. Extrapolating this to 600 kHz results in −122.5 dBc/Hz. A 20% frequency range from 1.62 to 1.99 GHz can be covered [12].

B. Prescaler

With the phase-switching prescaler architecture of Fig. 4, multimodulus prescalers can be realized that do not suffer from any speed degradation with respect to prescalers with a fixed division ratio. This technique is based on the 90° phase relationship between the outputs of the master and the slave section of a master/slave divide-by-two toggle flip-flop [16]. Switching the phase-select output signal $F4$ from a certain phase of these four differential quadrature outputs to the one that lags the present signal inserts a 90° delay. This 90° at one-fourth of the input frequency is equivalent to a full period of the input signal. The modulus control block is designed to insert a number s of the phase switches per output period, thereby increasing the normal division modulus from 64 to 64 $+s$. The three bits of the control word *Mode* can set s to any value from zero to seven, so the resulting prescaler division moduli range from 64 to 71.

C. Phase Detector

The phase-frequency detector schematic is shown in Fig. 5. It is the commonly employed circuit that inserts pulses on the up and down outputs of a certain minimum width, even when the phase difference is zero. This eliminates the dead-zone problem of the PLL, i.e., changes in the phase detector gain when the loop is in lock [17], [18].

D. Loop Filter

The loop-filter charge-pump circuit is shown in Fig. 6. Both the up and the down current can be either connected to the output or drained to a dummy reference voltage by the four switches. To minimize clock feedthrough, all switches are implemented by an NMOS and a PMOS transistor, and every transistor has its own control signal, the relative timing of which is optimized to avoid glitches in the output. As will be shown in the following paragraphs, two pumps must be implemented, but the control signals are of course reused.

The loop-filter design is a big challenge, as it determines the PLL settling time and the output phase-noise characteristic and is responsible for the biggest contribution to the chip area because of the integrated capacitors. This filter will determine whether the DCS-1800 phase-noise specifications of −119 dBc/Hz at 600 kHz offset and −136 dBc/Hz at 3-MHz offset can be met.

The simplest configuration is a passive filter that uses two capacitors and a resistor, as shown in Fig. 7. The resulting PLL is then a type-2, third order.

The open loop gain equals

$$\begin{aligned} GH(s) &= \frac{I_{qp}\cdot K_{\text{vco}}}{2\pi\cdot N}\times\frac{1+s\cdot\tau_z}{s^2\cdot(C_z+C_p)\times[1+s\cdot\tau_p]}\\ \tau_z &= R_z\cdot C_z\\ \tau_p &= R_z\cdot\left(\frac{1}{C_z}+\frac{1}{C_p}\right)^{-1} \end{aligned} \tag{1}$$

with K_{vco} the VCO sensitivity, I_{qp} the charge-pump current, and N the frequency division modulus.

The cross-over frequency ω_c equals approximately

$$\omega_c \approx \frac{I_{qp}\cdot K_{\text{vco}}\cdot R_z}{2\pi\cdot N}\times\frac{C_z}{C_z+C_p}\approx\frac{I_{qp}\cdot K_{\text{vco}}\cdot R_z}{2\pi\cdot N}. \tag{2}$$

We will place the loop gain zero ω_z a factor α below ω_c and the third pole ω_p a factor β above ω_c to guarantee enough phase margin. These factors α and β are typically equal to four, which gives a phase margin of approximately 60°. The size of the passive elements can easily be calculated from the loop parameters

$$\begin{aligned} R_z &= \frac{2\pi\cdot N}{I_{qp}\cdot K_{\text{vco}}}\cdot\omega_c\\ C_z &= \frac{\alpha}{R_z\cdot\omega_c}=\frac{I_{qp}\cdot K_{\text{vco}}}{2\pi\cdot N}\cdot\frac{\alpha}{\omega_c^2}\\ C_p &= \frac{1}{\beta\cdot R_z\cdot\omega_c}=\frac{I_{qp}\cdot K_{\text{vco}}}{2\pi\cdot N}\cdot\frac{1}{\beta\cdot\omega_c^2}. \end{aligned} \tag{3}$$

This configuration might seem a good solution at first sight, but it cannot be used here for two reasons. First, the output voltage, which is the VCO input control voltage, must vary over a wide range to use the full tuning range of the VCO. Due to the finite output impedance of the current sources, the up and down current cannot be matched over this full range. This will result in a small offset at the input of the phase and frequency detector (PFD) and consequently cause spurs in the output spectrum. Increasing the output impedance by, e.g., placing cascode transistors in the charge pump is also not possible, as it will reduce drastically the output voltage range and hence also the frequency tuning range.

The second reason this configuration cannot be used here is the large contribution to the output phase noise of the thermal noise in the charge pump and the loop filter resistors. For offset

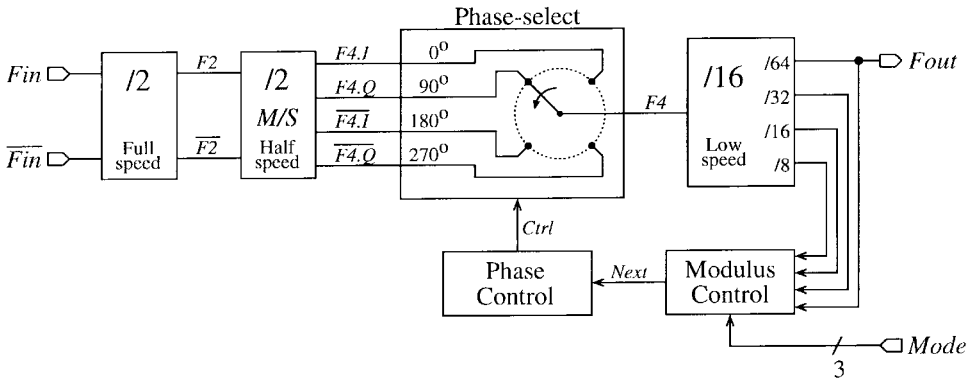

Fig. 4. Eight-modulus phase-switching prescaler.

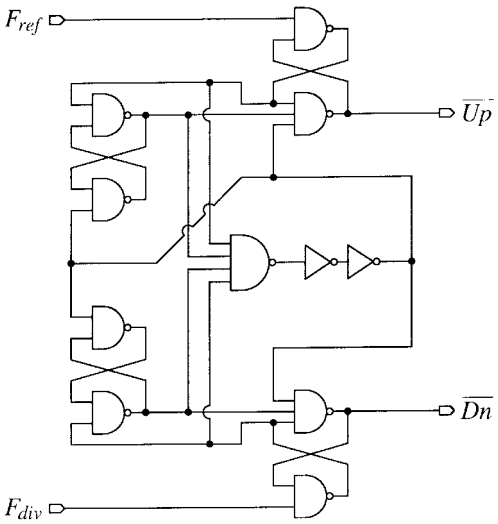

Fig. 5. Phase-frequency detector without dead zone.

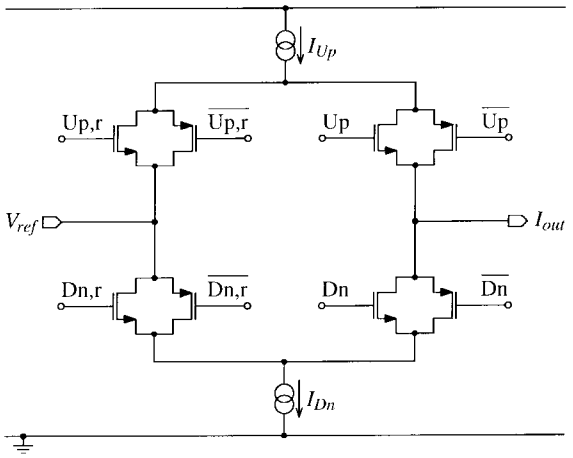

Fig. 6. Charge-pump core circuit.

frequencies larger than ω_c, these can be approximated by

$$\mathcal{L}_{QP}\{\Delta\omega\} = kT \cdot (4\pi \cdot N \cdot \beta)^2 \cdot \frac{2\alpha_{qp}}{I_{qp} \cdot (V_{GS} - V_T)_{qp}} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^4$$

$$\mathcal{L}_{Rz}\{\Delta\omega\} = kT \cdot (4\pi \cdot N \cdot \beta^2) \cdot \frac{K_{\text{vco}}}{I_{qp} \cdot \omega_c} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^4 \quad (4)$$

where $(V_{GS} - V_T)_{qp}$ is the overdrive voltage of the charge-pump current sources and α_{qp} is the fraction of time these current sources are active when the loop is in lock. For the charge-pump noise $\mathcal{L}_{QP}$, a very low loop bandwidth is needed to reduce the phase noise to a value well below the DCS-1800 specification. And for the filter resistor noise $\mathcal{L}_{Rz}$, a very low value for R_z is needed. Both equations hence lead to the use of extremely large capacitor values, which are not feasible for integration.

So a fourth pole must be inserted in the loop filter, as shown in Fig. 8. The extra pole is placed on top of ω_p by making $R_4 \cdot C_4 = \tau_p$. We keep one degree of freedom in doing this, i.e., if we make R_4 a factor γ smaller than R_z, we must increase C_4 by the same amount. To keep the phase margin high enough, β must be increased from four to six. Since the loop transfer function now falls off at 60 dB/decade for frequencies beyond ω_p, the noise of the charge pump and the loop filter resistor R_z will have a dependency on the offset frequency of $\Delta\omega^{-6}$. The following equations describe this behavior:

$$\mathcal{L}_{QP}\{\Delta\omega\} = kT \cdot (4\pi \cdot N \cdot \beta^2)^2 \cdot \frac{2\alpha_{qp}}{I_{qp} \cdot (V_{GS} - V_T)_{qp}} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^6 \quad (5)$$

$$\mathcal{L}_{Rz}\{\Delta\omega\} = kT \cdot (4\pi \cdot N \cdot \beta^4) \cdot \frac{K_{\text{vco}}}{I_{qp} \cdot \omega_c} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^6 \quad (6)$$

$$\mathcal{L}_A\{\Delta\omega\} = 2kT \cdot \frac{(\beta \cdot \omega_c \cdot K_{\text{vco}})^2}{G_{mA} \cdot \Delta\omega^4} \quad (7)$$

$$\mathcal{L}_{R4}\{\Delta\omega\} = kT \cdot (4\pi \cdot N \cdot \beta^2) \cdot \frac{K_{\text{vco}}}{\gamma \cdot I_{qp} \cdot \omega_c} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^4. \quad (8)$$

But also, this solution leads to a total capacitance that is too large to be integrated.

Therefore, a special filter topology is employed that splits up the loop filter in two paths, as was already done in [17]. The principle is explained in Fig. 9. The passive loop filter consisting of R_z, C_z, and C_p actually forms a pole at zero frequency, a zero at ω_z, and another pole at ω_p. It is the capacitor creating the zero that has the largest size and hence poses difficulties in integration. In this new technique, the same filter characteristic is achieved by combining two signals, which does not need an actual RC combination at the frequency of the zero.

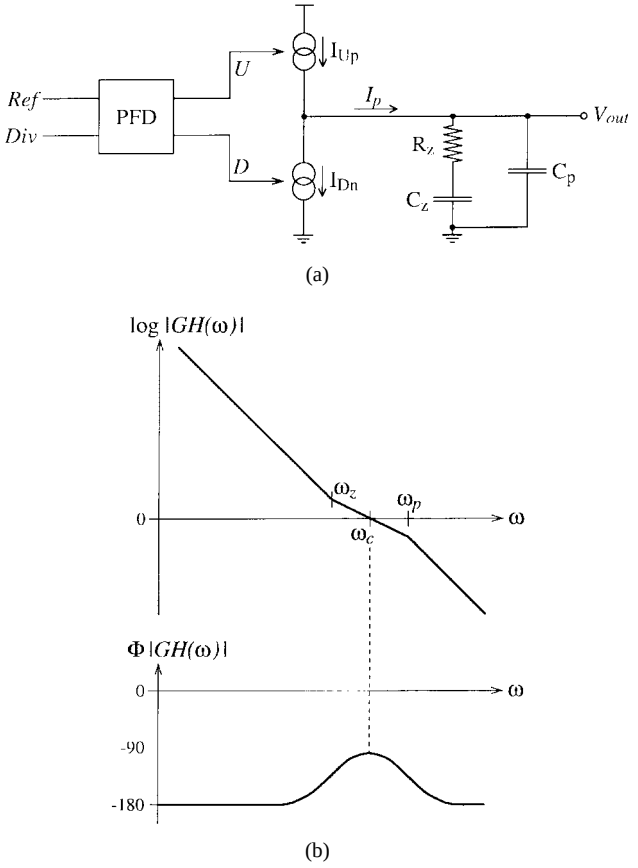

Fig. 7. (a) Third-order, type-2 charge-pump PLL passive filter. (b) Open loop gain Bode plot.

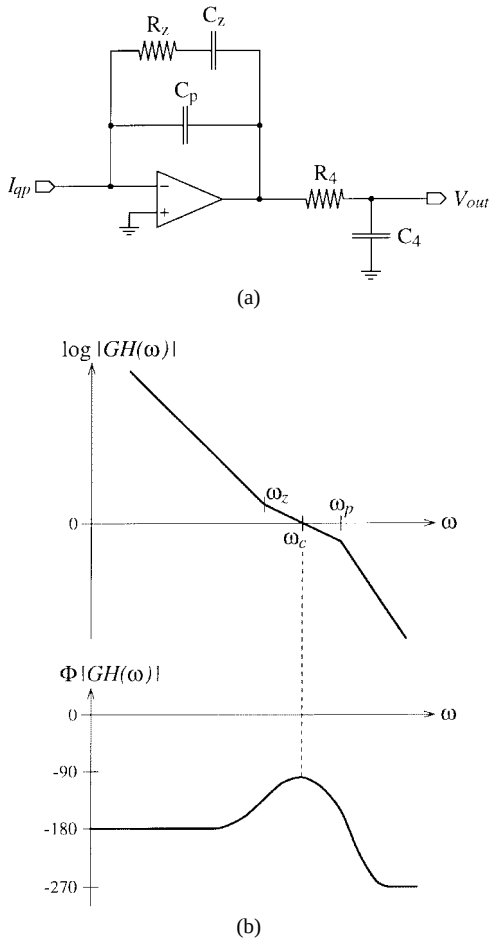

Fig. 8. (a) Active loop filter for a fourth order, type-2 charge-pump PLL. (b) Open loop gain Bode plot.

The goal is to add two signals, which we will call V_z and V_p. The first signal is an integrated version of the input current. So it has a pole at zero frequency

$$V_z = \frac{1}{sC_z} \cdot I_{\text{in}}. \tag{9}$$

The other signal path has a low-pass transfer function

$$V_p = \frac{R_p}{1 + sR_pC_p} \cdot I_{\text{in}}. \tag{10}$$

These two signals are now added to form the complete output signal, but the second one is amplified by a factor B. This results in

$$V_{\text{out}} = V_z + B \cdot V_p = \frac{1}{sC_z} \cdot \frac{1 + s\tau_z}{1 + s\tau_p} \cdot I_{\text{in}}$$

with

$$\begin{aligned} \tau_z &= R_p \cdot (C_p + BC_z) \approx BR_pC_z \\ \tau_p &= R_pC_p. \end{aligned} \tag{11}$$

So a large time constant (or a low frequency) is realized for the filter zero without the requirement for a large capacitor, as τ_z profits from the multiplication by the factor B. The implementation for this configuration is shown in Fig. 10. The circuit has two input currents, one to be integrated to V_z and one to be low-passed to V_p. The impact on the charge-pump design is minimal, as only the charge-pump core must

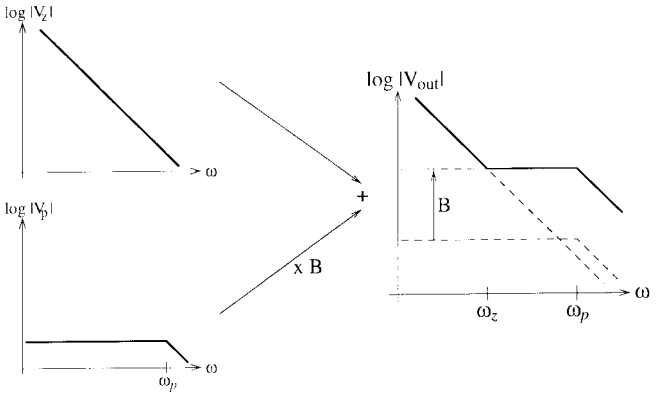

Fig. 9. Dual-path loop filter principle.

be implemented twice. The control signals can be reused for both parts. And multiplication of the second signal by a factor B is also very easy to do, as this is done in the current domain by using a pump current that is a factor B larger in the charge-pump core driving the signal V_p. Both input currents are represented here with a negative sign, which means that the position of the Up and the Dn terminals must be interchanged in the phase-frequency detector. The adder that sums the two signals is actually a subtracter the subtracts $-B \cdot V_p$ from V_z. Last, a fourth pole is added by the combination of R_4 and C_4.

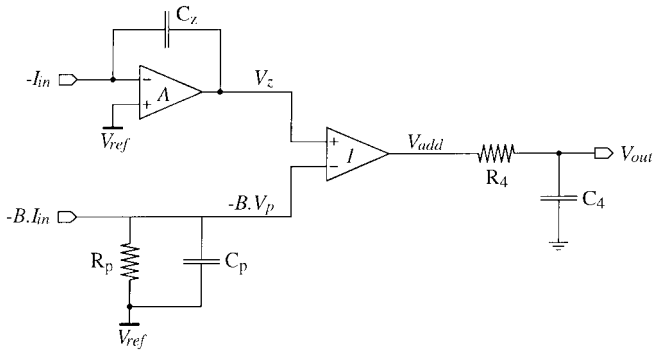

Fig. 10. Dual-path loop filter implementation.

Moreover, in the configuration of Fig. 10, the dc operating voltage of both current inputs is positioned at $V_{\rm ref}$. This is obvious in the active integrator, but it is also true for the low-pass path, as no current flows through R_p when the loop is in lock. So an active implementation for the R_p-C_p path is not necessary.

The resulting PLL open loop gain is equal to

$$GH(s) = \frac{I_{qp} \cdot K_{\rm vco}}{2\pi \cdot N} \times \frac{1 + s \cdot \tau_z}{s^2 \cdot C_z \times (1 + s \cdot \tau_p) \cdot (1 + s \cdot \tau_4)}. \tag{12}$$

The cross-over frequency is

$$\omega_c \approx \frac{I_{qp} \cdot K_{\rm vco}}{2\pi \cdot N} \times \frac{C_p + B.C_z}{C_z} \approx \frac{I_{qp} \cdot K_{\rm vco} \cdot B.R_p}{2\pi \cdot N} \tag{13}$$

provided that C_p can be neglected with respect to $B \cdot C_z$.

We will put the zero $\omega_z = 1/\tau_z$ a factor α below the loop bandwidth. Considering the two high-frequency poles $1/\tau_p$ and $1/\tau_4$, the best results for noise suppression outside the loop bandwidth versus phase margin are obtained if they coincide. We will place them a factor β above ω_c. So if the resistor R_4 is made a factor γ smaller than R_p, C_4 must be larger than C_p by the same amount. This gives the following equations for the passive element values:

$$\begin{aligned} R_p &= \frac{1}{B} \cdot \frac{2\pi \cdot N}{I_{qp} \cdot K_{\rm vco}} \cdot \omega_c \\ C_z &= \frac{\alpha}{B \cdot R_p \cdot \omega_c} = \frac{I_{qp} \cdot K_{\rm vco}}{2\pi \cdot N} \cdot \frac{\alpha}{\omega_c^2} \\ C_p &= \frac{1}{\beta \cdot R_p \cdot \omega_c} = \frac{I_{qp} \cdot K_{\rm vco}}{2\pi \cdot N} \cdot \frac{B}{\beta \cdot \omega_c^2} \\ R_4 &= \frac{R_p}{\gamma} \\ C_4 &= \gamma \cdot C_p. \end{aligned} \tag{14}$$

The several contributions to the out-of-band output phase noise can be approximated by

$$\mathcal{L}_{QP}\{\Delta\omega\} = kT \cdot (4\pi \cdot N \cdot \beta)^2 \cdot \frac{2\alpha_{qp}}{I_{qp} \cdot (V_{GS} - V_T)_{qp}} \cdot \left(\frac{1}{\alpha^2} + \frac{\beta^2}{B}\right) \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^6 \tag{15}$$

$$\mathcal{L}_{Rp}\{\Delta\omega\} = kT \cdot \frac{4\pi \cdot N \cdot \beta^4 \cdot K_{\rm vco}}{B \cdot I_{qp} \cdot \omega_c} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^6 \tag{16}$$

$$\mathcal{L}_{A}\{\Delta\omega\} = 2kT \cdot \frac{(\beta \cdot \omega_c \cdot K_{\rm vco})^2}{G_{mA} \cdot \Delta\omega^4} \tag{17}$$

$$\mathcal{L}_{D}\{\Delta\omega\} = 2kT \cdot \frac{(\beta \cdot \omega_c \cdot K_{\rm vco})^2}{G_{mD} \cdot \Delta\omega^4} \tag{18}$$

$$\mathcal{L}_{R4}\{\Delta\omega\} = kT \cdot \frac{4\pi \cdot N \cdot \beta^4 \cdot K_{\rm vco}}{B \cdot \gamma \cdot I_{qp} \cdot \omega_c} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^4 \tag{19}$$

where $\mathcal{L}_{QP}$ originates from the charge pump, $\mathcal{L}_{Rp}$ and $\mathcal{L}_{R4}$ from the filter resistors, $\mathcal{L}_A$ from the integrator amplifier, and $\mathcal{L}_D$ from the adder. G_{mA} and G_{mD} represent the equivalent input noise transconductance of the filter amplifier and adder, respectively. These equations illustrate the 60-dB per decade rolloff of the most important phase-noise contributions, i.e., the charge pump and the resistor R_p.

A behavioral linear model for the PLL implemented in SPICE, as shown in Fig. 11, was used to determine the loop parameters ω_c, I_{qp} and B. Voltages were used to represent the phase of the input and output signals. The loop filter can be implemented with ideal amplifiers or with real circuit schematics. Some biasing elements that are required to set all the correct operating points are not indicated in the figure. The appropriate noise sources can be introduced, and the resulting output phase noise is calculated with

$$\mathcal{L}\{\Delta\omega\} = \frac{S_{V_{\theta \rm out}}\{\Delta\omega\}}{2}. \tag{20}$$

Using this model, the loop parameters can be varied, and their effect on the PLL performance can be evaluated rapidly. We cannot change the relative position of the zero $1/\tau_z$ and the two poles at $1/\tau_p$ because the phase margin must be high enough to maintain a stable system. So we put $\alpha = 4$ and $\beta = 6$. The VCO gain $K_{\rm vco}$ equals at most $2\pi \cdot$ 400 MHz/V, and the division modulus N is 64. So the remaining loop parameters that are incorporated into the optimization are the loop bandwidth ω_c, the charge-pump current I_{qp}, the filter factor B, and the fourth pole parameter γ. Our goal is to achieve a low phase noise within two constraints. The first constraint is a low power consumption, which will be reflected in the restrictions on the values of G_{mA} and G_{mD}. The second constraint is the most important one and limits the occupied chip area. We must limit the sum of the capacitor sizes of C_z, C_p, and C_4 to a value realizable in an integrated circuit.

The final optimized loop parameters are listed in Table II. A pump current of 1 μA is used, and the loop bandwidth equals 45 kHz. This should be sufficiently large for the settling time. The total capacitance value is as large as 960 pF. This will be responsible for a large chip area, but it is the only way to achieve the required low phase noise. Even with these values, the spec is only achieved without any margin, i.e., any other phase noise introduced in the circuit will cause the phase noise to be higher than allowed in the DCS-1800 system. The situation is, however, much relaxed at lower VCO gains, which appear rapidly at slightly higher output frequencies. So the required specs will be achieved over most of the frequency range.

Fig. 12 shows the simulated open-loop gain, which has indeed a cross-over frequency of 45 kHz. The phase margin is 58°, a value that is high enough to avoid excessive ringing

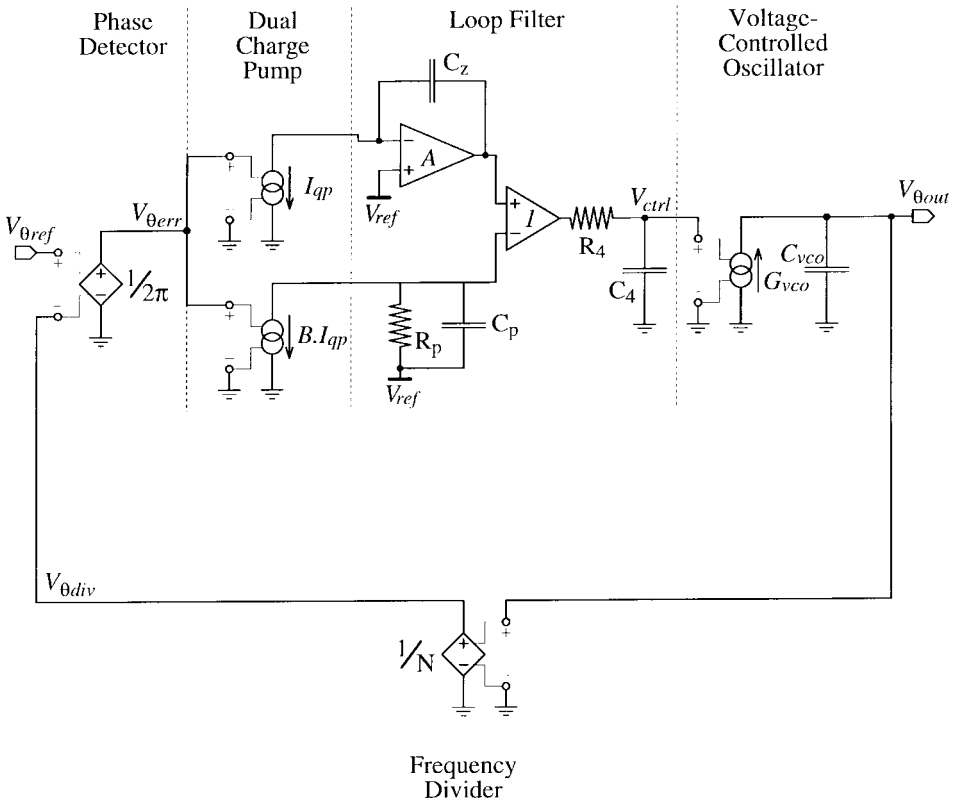

Fig. 11. Behavioral SPICE PLL model.

TABLE II
FINAL PLL PARAMETERS

Loop bandwidth	ω_c	45 kHz
Charge pump current	I_{qp}	1 μA
Zero frequency	α	4
Pole frequency	β	6
Filter current ratio	B	12
Fourth pole ratio	γ	3
Passive elements :	C_z	320 pF
	R_p	3.6 $k\Omega$
	C_p	160 pF
	R_4	1.2 $k\Omega$
	C_4	480 pF
Phase noise contributions at 600 kHz:		
Charge pump	$\mathcal{L}_{QP}$	-137 dBc/Hz
Resistor R_p	$\mathcal{L}_{Rp}$	-124 dBc/Hz
Integrater opamp	$\mathcal{L}_A$	-129 dBc/Hz
Filter adder	$\mathcal{L}_D$	-129 dBc/Hz
Resistor R_4	$\mathcal{L}_{R4}$	-121 dBc/Hz
Total	$\mathcal{L}\{600\ kHz\}$	-118.6 dBc/Hz

and slow settling. In the charge pump, an on-time fraction α_{qp} of 0.1 and a $V_{GS} - V_T$ of 0.3 V has been assumed.

Fig. 13 shows the several phase-noise contributions versus frequency for the designed loop parameters. The first graph shows the phase noise originating in the two charge pumps (N_QPZ for the integrating current path and N_QPP for the low-pass path). In the middle graph, the phase noise related to the thermal noise in the two resistors R_p (N_RP) and R_4 (N_R4) is shown. Last, the bottom graph lists the phase noise originating from the active elements used in the loop filter. N_EA represents the noise from the integrator amplifier and N_ED is due to the adder. We can clearly see the dependency on $\Delta\omega^{-4}$ or $\Delta\omega^{-6}$ in all graphs for high offset frequencies. The values at 600 kHz were already listed in the above table, and they agree very well with the theoretical formulas (15)–(19).

E. Linearization

Because the standard available P+/N-well junction capacitance has been used for the VCO tuning, its gain K_{vco} is highly nonlinear. As this changes the overall PLL loop gain, the feedback will become unstable if no countermeasures are taken. The insertion of a linearization block in between the loop filter and the VCO is not feasible for noise reasons. Indeed, noise inserted at this point is not suppressed at offset frequencies larger than the loop bandwidth. The power consumption needed to bring the linearization noise below the required level is too high.

Instead, it can be noted from (12) that the open loop gain is proportional to the product of the VCO gain and the charge-pump current. In the presented design, this current (I_{qp}) is adjusted to the proper value, dependent on the value of K_{vco}. A six-step piece-wise linear fitting of the VCO tuning characteristic is used in the linearization block of the PLL to switch on/off the required current sources in a

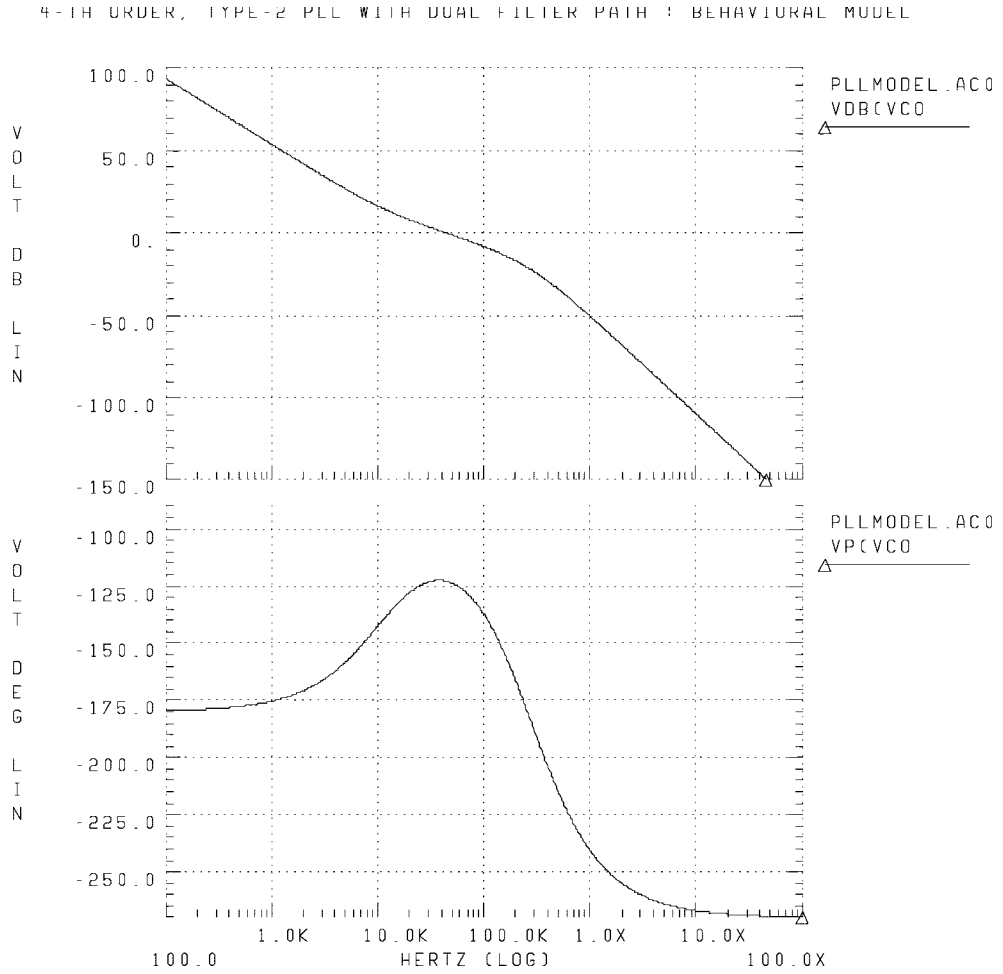

Fig. 12. Simulated PLL open-loop gain.

current mirror bank. The block diagram of the linearization circuitry is shown in Fig. 14.

The VCO control voltage is compared with five reference voltages. These reference levels are generated with the resistor string $R1 \cdots R5$ and the transistor Mr. The transistor Mr tracks the absolute value of the NMOS threshold voltage, and hence also tracks the VCO tuning curve, whose absolute position is partly determined by the NMOS amplifying transistors in the oscillator schematic. The five switch-control signals $S1 \cdots 5$ are used to add or remove current sources from the output current I_{qp}. Schmitt triggers are inserted to provide some hysteresis and avoid instabilities around the threshold voltages. The output current is fed to the charge pump to set the nominal current of I_{Up} and I_{Dn}. This approach has the advantage that almost no extra phase noise is introduced. Noise present in the linearization output is fed to the up as well as the down current source in the charge pump. In lock, both current sources are active for a short duration of time (given by the fraction α_{qp}) but they both contain the same amount of linearization noise, which cancels out since the two currents are subtracted.

IV. Measurement Results

All the circuits described above have been implemented in a single IC, shown in Fig. 15. The hollow coil used in the VCO can be clearly distinguished in the lower right-hand corner of the die. The prescaler is situated in the lower left-hand corner. The largest part of the IC is occupied by the three filter capacitors. They are realized using the poly/poly structure available in this process with a nominal capacitance value of 1.5 fF/μm^2. The active filter amplifiers are placed in between these capacitors. The phase-frequency detector and the charge pump are situated in the middle on the left-hand side of the die, and the linearization circuitry occupies the upper left-hand corner. The total die size is 1.7 $\times$ 1.9 μm^2. The reference frequency is 26.6 MHz, and the power-supply voltage is 3 V for all circuits. The power consumption of the chip is 51 mW, which is divided over the several building blocks as follows: PFD one, charge pump one, loop filter 18, VCO 11, prescaler 18, and linearization 2 mW.

An important aspect of the variation of the VCO gain with frequency is of course the different noise-transfer functions and hence different output phase noise. This is even deteriorated by the increase in $1/\omega^3$ noise in the VCO itself at low tuning voltages. Fig. 16 shows the output spectrum for two output frequencies, i.e., 1.71 and 1.88 GHz. The measurement was performed using a dedicated phase-noise measurement setup that is based on the delay-line method. Outside the loop bandwidth ($f >$ 45 kHz), we clearly see the dominant VCO noise. For the 1.71-GHz signal, it consists mainly of upconverted

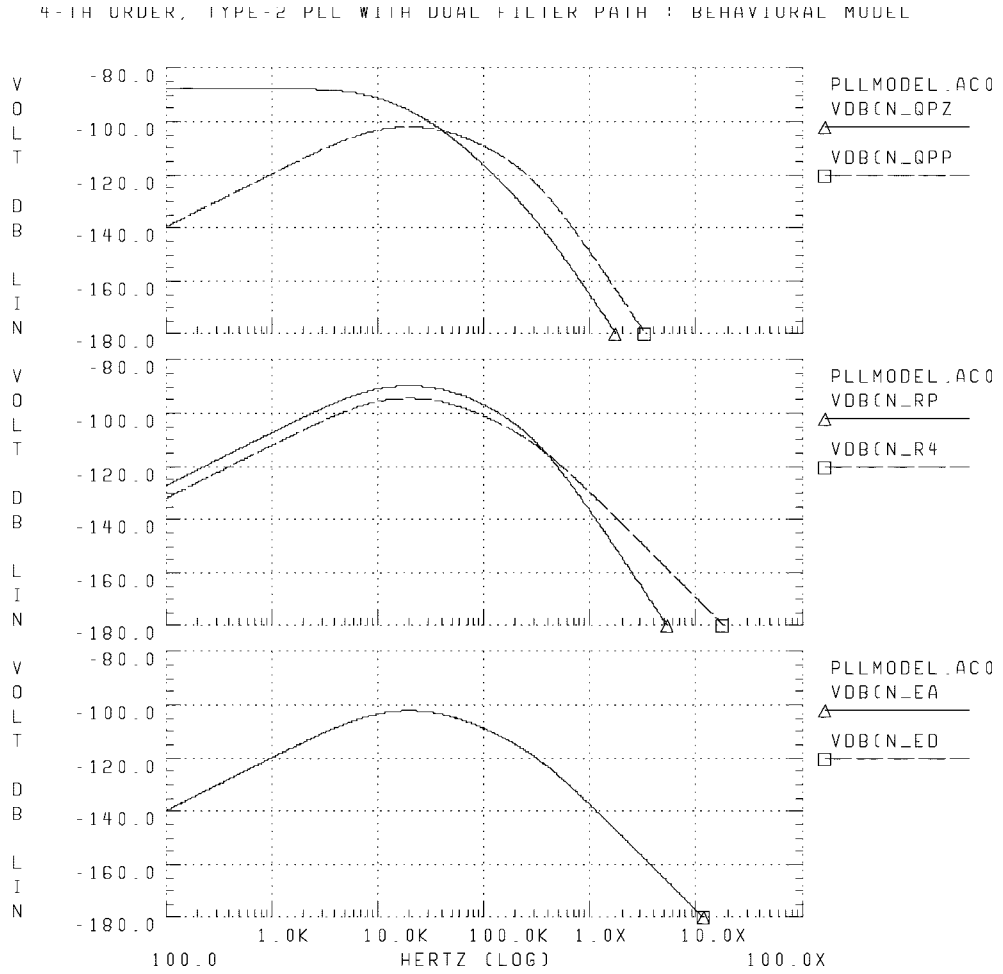

Fig. 13. Simulated PLL output phase noise.

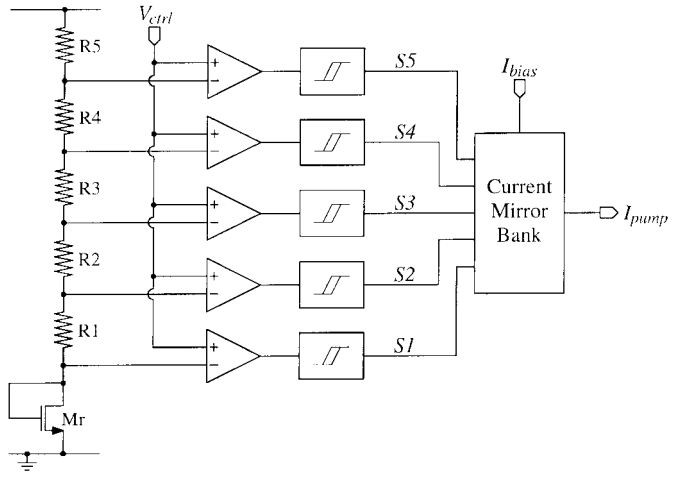

Fig. 14. Indirect linearization circuitry for the PLL.

$1/f$ noise, which results in a magnitude of -115 dBc/Hz at 600-kHz offset. Because of the smaller nonlinearities when operating at 1.88 GHz, the VCO spectrum is much cleaner and the PLL phase noise is correspondingly lower, down to -123 dBc/Hz at 600 kHz, which is sufficient according to the DCS-1800 specification. Further from the carrier, the measured phase noise at 3-MHz offset is -134 dBc/Hz and -138 dBc/Hz for the two output frequencies shown.

Inside the loop bandwidth, it is not the charge-pump noise that is dominant, as would be predicted by the simulations performed in Fig. 13. Unfortunately, missing data on the $1/f$ noise of the transistors in the active filter circuitry caused us to overlook the $1/f$ noise of the biasing circuitry for the amplifier and adder in the active filter. Therefore, the in-band phase noise is higher than expected but still remains below -75 dBc/Hz. Closer to the carrier, the phase noise increases again due to the reference-signal phase-noise feedthrough.

The second important thing that has been measured is the settling time after a change in the division factor N. Fig. 17 compares the simulated and measured waveforms of the VCO control voltage when changing the division modulus from 64 to 68 and back. Mixed-signal simulations predict a rise time of approximately 120 μs and a settling to a 100-Hz accuracy within 250 μs. The measurement is not accurate enough to determine the actual settling time to a voltage with μV accuracy, but based on the simulations and the small difference in rise time, we can conclude that the PLL has a settling time smaller than 300 μs.

V. Conclusions

In this paper, we have described a working prototype for a monolithic CMOS DCS-1800 frequency synthesizer. The integrated VCO uses an optimized hollow coil with a

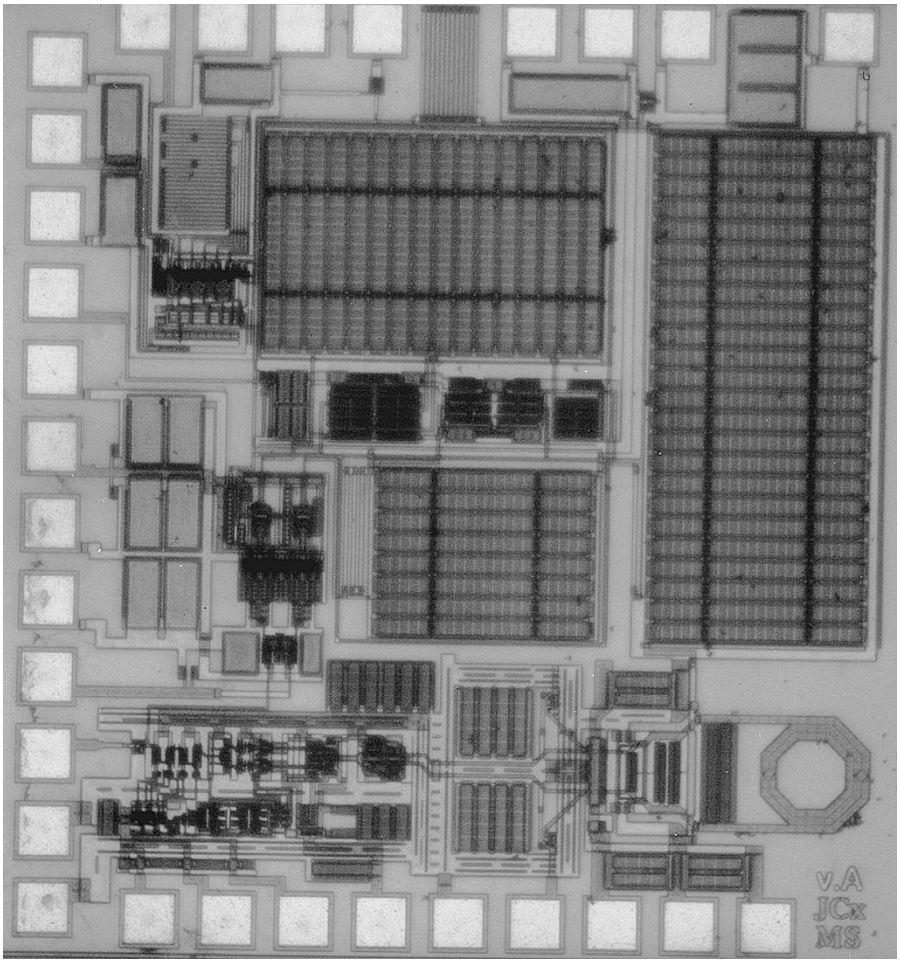

Fig. 15. IC microphotograph.

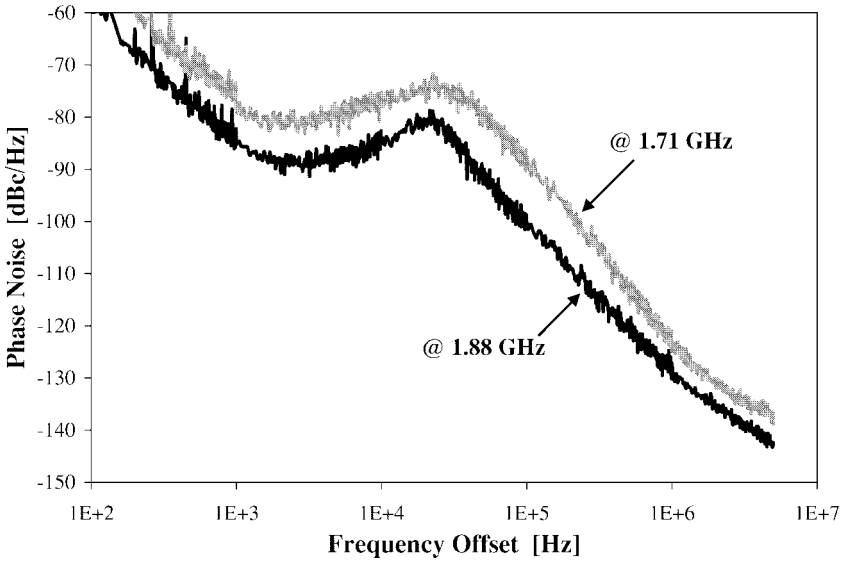

Fig. 16. Measured PLL output phase noise at two extreme output frequencies.

quality factor of 8.6 to achieve the required phase noise with minimal power consumption. The phase-switching prescaler architecture allows the implementation of multimodulus dividers without a speed penalty with respect to fixed prescalers.

Most design effort has been put in the loop filter and the linearization. The dual-path loop filter circuit uses two signal paths, one of which uses a scaled current, to create a small time constant without the need for very large capacitor values.

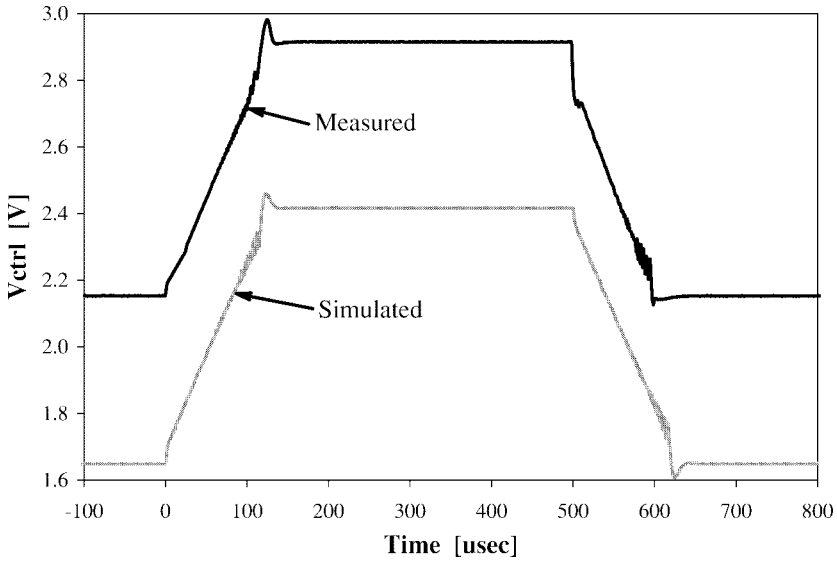

Fig. 17. Measured PLL settling.

A behavioral model of the PLL was implemented in SPICE to optimize the loop parameters for low noise and low area. An indirect linearization technique was used for the VCO that keeps the product of the charge-pump current and the VCO gain constant over the complete frequency range, which is also sufficient to create a constant open loop gain, and hence assures stability.

The PLL was realized on a 1.7×1.9 mm^2 die in a standard 0.4-μm CMOS process. Of course, it uses no external components and functions without tuning, trimming, or postprocessing steps. It consumes 51 mW from a single 3-V power supply. The loop bandwidth is 45 kHz, and a total capacitance of almost 1 nF is integrated.

The output phase noise complies with the DCS-1800 standard of -119 dBc/Hz at 600 kHz offset apart from two remaining problems, both of which are related to $1/f$ noise. The first one is the too-high ω^{-3} noise of the VCO for the lowest output frequencies, which is caused by the increased nonlinearities when the tuning junction capacitances are biased in almost-forward conditions. The second problem can easily be remedied because it originates from $1/f$ noise in the biasing circuitry of the active filter amplifiers. The measured settling time for a 100-MHz frequency step is below 300 μs, which is fast enough for the DCS-1800 standard.

To conclude, we can state that although this design does not fulfill the DCS-1800 specification over the complete frequency range, it has demonstrated the feasibility of a full CMOS PLL with no external components as the frequency synthesizer in a modern high-performant mobile communication system such as DCS-1800. As a suggestion for further improvement of the PLL, we think that coarse tuning of the VCO with a binary weighted bank of capacitors should be seriously considered. If one wants to be able to handle 3σ process variation of 20% in the junction capacitor values, this will anyway be necessary, as the full VCO tuning range must already be used for this.

Coarse digital tuning with a capacitor bank will have its disadvantages, such as careful design of the switches in the bank and the need for a well-conceived digital control system. But it will enable the operation of the VCO in the region with low gain K_{vco}, which will remove the $1/f$ noise problem in the VCO and facilitate the design of the other PLL building blocks, e.g., a simpler loop filter design. Due to the high VCO gain in this design, the noise transfer from the circuit blocks to the output phase noise has a rather high gain, which has resulted in a maximum value of only 45 kHz for the loop bandwidth and, more important, for a very large amount of integrated capacitance. Limiting K_{vco} will probably enable a small increase in the loop bandwidth, but not very much since the noise at 600-kHz offset must be reduced sufficiently by the low-pass function of the loop. But in the loop filter, the RC time constants required can be made using a larger (and more noisy) resistor and a smaller capacitance for the same amount of output phase noise. So the required chip area can probably be reduced by a large amount, and the DCS-1800 specifications can be achieved over the full frequency band.

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Michel S. J. Steyaert (S'85–A'89–SM'92), for a photograph and biography, see this issue, p. 1897.