Modeling of Pocket Implanted MOSFETs for Anomalous Analog Behavior

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Abstract

Pocket implant is widely used in deep-sub-micron CMOS technologies to combat short channel effects. It, however, brings anomalously large drain-induced threshold voltage shift and low output resistance to long channel devices. This creates a serious problem for high-performance analog circuits. In this paper, the first physical model of these effects are proposed and verified against data from a 0.18µm technology. This model is suitable for SPICE modeling.

Introduction

Pocket implant is widely used in deep sub-micron CMOS technologies to reduce V_T roll-off and punch-through [1]. This technique, however, produces large drain-induced V_T shift and low R_{out} in long channel devices [2], greatly affecting analog circuit design and performance. Physical compact model for these effects, however, is not available.

In this work, we report the first physical model of these effects suitable for compact MOSFET modeling. The proposed model is verified against both simulation and experimental data from a 0.18µm CMOS technology.

Drain-induced threshold voltage shift (DITS)

Fig. 1 illustrates the enhanced DITS effect in long channel devices with pocket implants compared with uniformly doped devices using 2-D simulation. Fig. 2 is an illustration of the structure used in the device simulation. DITS increases by 2 to 3 times for long channel devices. Fig. 3 shows the simulated φ_s vs. x for two V_{ds} biases for a pocket implanted device. Clearly, φ_s is independent of x in the center segment of the channel and the drain barrier peak decreases with increasing V_{ds} thus leading to DITS. Starting with the drift-diffusion equation, we derived a drain current expression by considering the source-end, center, and drain-end sections of the channel separately and applying a DIBL model [3] to the drain-side barrier only:

$$I_{ds} \approx \frac{qWD_nN_D\left(1-e^{-\beta V_{ds}}\right)}{\int_0^L e^{-\beta(\varphi_s-\varphi_{source})}dy} \cdot \frac{\varepsilon_{si}T_{ox}}{\beta\varepsilon_{ox}\left(V_{T0}-V_{FB}-2\varphi_B\right)} \approx AW\frac{1-e^{-\beta V_{ds}}}{C_1L+(1+e^{-C_2V_{ds}})} \quad (1)$$

where $\beta=q/kT$, φ_s is the surface potential, and C_1 and C_2 as

$$C_1 = e^{-\beta(\varphi_{s2}-\varphi_{\min 1})}\sqrt{\beta[qN_pX_{dep}-\varepsilon_{ox}(V_{T0}-V_{FB}-2\varphi_B)/T_{ox}]/\varepsilon_{si}X_{dep}\pi}, \quad (2)$$

$$C_2 = \beta\cdot(e^{-L_p/2l_p}+2e^{-L_p/l_p})$$

are model parameters. $l_p=\sqrt{\varepsilon_{si}T_{ox}X_{dep}/\varepsilon_{ox}}$. If V_T is defined to be the gate voltage at which $I_{ds}=I_{crit}=I_T\cdot W/L$, where I_T is the threshold current chosen experimentally. Then the threshold voltage shift can be derived as:

$$\Delta V_T = -S\cdot\log\left(\frac{I_{ds}}{I_{crit}}\right) = -S\cdot\log\left(\frac{(1-e^{-\beta V_{ds}})}{1+(1+e^{-C_2V_{ds}})/C_1L}\right) \quad (3)$$

where S is the sub-threshold swing and can be calculated or extracted [4].

Modeling the output resistance

Pocket implants also lower the output resistance, R_{out}. Figure 4 shows that at low V_{gs}, R_{out} can be 10 to 100 times smaller because of the pocket implant. Pocket implants affect output resistance in two ways. Firstly, DITS causes I_{ds} to increase with increasing V_{ds}. The early voltage due to this mechanism can be derived from (1):

$$V_{A,DITS} = I_{ds}\cdot\left(\frac{dI_{ds}}{dV_{ds}}\right)^{-1} = \frac{(C_1L+1)e^{C_2V_{ds}}+1}{C_2} \quad (4)$$

Since parameters C_1 and C_2 in (1) are used to model I_{ds} in subthreshold-threshold region, we introduce parameters C_{0c}, C_{1c}, and C_{2c} to accurately capture this effect in strong inversion region:

$$V_{A,DITS} = C_{0c}\cdot\frac{(C_{1c}L+1)e^{C_{2c}V_{ds}}+1}{C_{2c}} \quad (4a)$$

The second effect of the pocket implant on R_{out} is that the output resistance due to all mechanisms (CLM, DIBL, etc.) is reduced by a factor that varies with V_{gs} and L. Let us compare a pocket-implanted device with a MOSFET uniformly doped to the pocket concentration, N_p. In Figure 5, both devices are partitioned into two parts. The device on top has a length L_p, the length of the pocket. The lower part is the rest of the channel with length L-L_p. This partition is useful because in the saturation region, R_{out} is mainly determined by the effects in a small region close to the drain, and the rest of the channel, i.e. the lower device may be considered simply a source resistance. For the cascode circuit in Fig. 5(a), the output resistance in saturation is well known:

$$R_{out} = (g_{m1}r_{o2}+1)\cdot r_{o1} = (L/L_p)\cdot r_{o1} \quad (5)$$

where r_{o1} is the output resistance of the device on top. In a similar way, R_{out} of the pocket device, i.e. the circuit in Fig. 5(b) can be derived as:

$$R_{outp} = (g_{m1}r_{o2p}+1)\cdot r_{o1p} = \frac{L}{L_p}\left(1-\frac{L-L_p}{L}\left(1+\sqrt{\frac{L_p}{L}}\sqrt{\frac{(V_g-V_T)^2}{\delta V_T^{\,2}}-2\frac{V_g-V_T}{\delta V_T}+\frac{L_p}{L}}\right)^{-1}\right)\cdot r_{o1p} \quad (6)$$

where $\delta V_T = V_T(N_p)-V_T(N_{sub})$. Since M_1 and M_{1p} have the same doping and since Early voltage V_A is insensitive to V_{gs}, M_1 and M_{1p} should have the same V_A.

$$\frac{r_{o1}}{r_{o1p}} = \frac{V_A/I_{ds1}}{V_A/I_{ds1p}} = \frac{I_{ds1p}}{I_{ds1}} = \frac{(V_g-V_T-V_p^*)^2}{(V_g-V_T-V^*)^2} = \left(1+\left(1-\sqrt{L_p/L}\right)\cdot\frac{\delta V_T}{V_g-V_T}\right)^2 \quad (7)$$

7.5.1

Considering $\delta V_T \ll (V_g - V_T)$, using equations (5), (6) and (7) the output resistance of the pocket-implanted device can be rewritten as:

$$R_{outp} = F \cdot R_{out} \tag{8}$$

where R_{out} is the output resistance of the uniformly doped device, which can be modeled by conventional models such as BSIM3v3 [4]. F is a "degradation factor"

$$F = \left(1 + \sqrt{\frac{L}{L_p}} \frac{\delta V_T}{(V_s - V_T)}\right)^{-1} \cdot \left(1 + \left(1 - \sqrt{L_p / L}\right) \frac{\delta V_T}{V_g - V_T}\right)^{-2} \approx \left(1 + P_F \cdot \sqrt{L} / (V_g - V_T)\right) \tag{9}$$

where $P_F \equiv \delta V_T / \sqrt{L_p}$ should be considered a fitting parameter decided by the characteristics of pocket implant.

Results and Discussion

Eq. (3) can be added to a conventional V_T model as a new term. Fig.6 shows the agreement between the model and the measured V_T of a W/L=5μm/10μm device. Fig. 7 shows that the BSIM3 V_T model [3] does not model the V_{ds} dependence of V_T at long gate lengths. Fig. 8 shows that the new model significantly improves the fitting using parameters extracted from Fig. 6. The new threshold shift model can give rise to DITS at long channel lengths where the conventional DIBL theory predicts none. This can be explained by the fact that at $V_g \sim V_T$ and small I_{ds}, there is little voltage drop in most of the channel region. Therefore, even in a long channel device, nearly all the V_{ds} is available to reduce the drain-side barrier height as shown in Fig. 3 and the drain barrier height can significantly affect I_{ds}.

To verify the R_{out} model of (9), 2-D simulations and measurements are performed for identical devices with and without pocket implant. Fig. 9 shows that the "degradation factor" is indeed a constant, independent of V_{ds} in the saturation region which is in agreement with (9). Our derivation is general and does not depend on what mechanisms determine the R_{out}. From the model, at high V_{gs} and long L, if F is plotted versus $(V_{gs} - V_T)/\sqrt{L}$, all data should fall on a universal curve. This is verified in Fig. 10. F vs. V_{gs} for different L also agrees with the 2-D device simulation data in Fig. 11. In Fig. 12, this model of the degradation factor is compared with the ratio of output resistance measured on devices with and without pocket implants. The devices are otherwise identically fabricated using a 0.18 μm process. The agreement is excellent.

The proposed model not only provides the first physical analysis for the anomalous analog behaviors but is also suitable for use in compact modeling of analog devices. It was implemented into the BSIM3 model and model parameters were extracted for a 0.18μm technology. Fig. 13 shows that the output resistance fitting is excellent and the fitting in long channel, low V_{gs}-V_T region has been significantly improved.

Both the threshold voltage model and the output resistance model are reduced to the original model when $1/C_1$, C_{2c}, and δV_T approach zero. In that case, ΔV_T=0 in (3), $V_{A,DITS}=\infty$ in (4a), and F=1 in (9) respectively. Also from the expression, we can see that to minimize the degradation of the output resistance, pocket implant with lower peak concentration and wider lateral length is desired. These are also the conditions to minimize the long channel DITS effect. This agrees with the fact that output resistance degradation and long channel DITS are highly correlated [2]. Although the models are developed for pocket implanted devices, it can also improve the model accuracy of devices without pocket implant if it has reverse short channel effect (RSCE) due to defect-enhanced diffusion.

Acknowledgements

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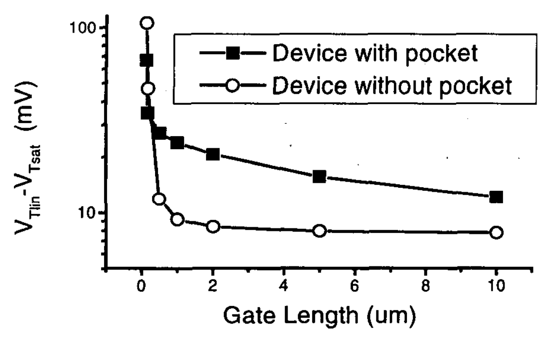

Fig. 1. Comparison of (V_{Tlin}-V_{Tsat}) vs. L between two devices with and without pocket implant by 2-D simulation. The threshold voltage shift is 2~3 times larger for the pocket implanted device at long gate lengths.

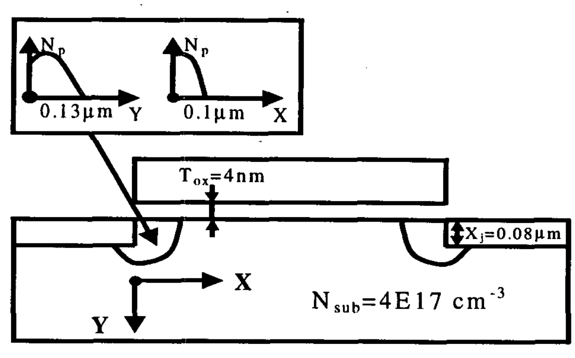

Fig. 2. Device structure used in 2-D device simulations. Pocket doping profile shown simulates that of a 0.18μm technology.

7.5.2

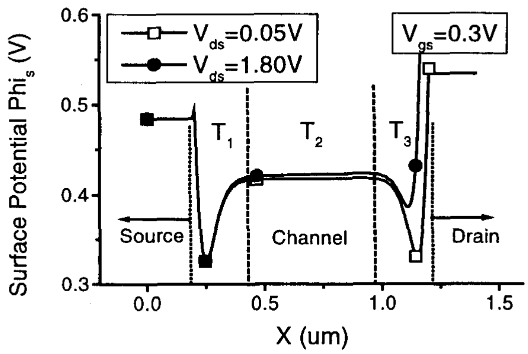

Fig. 3. Simulated channel surface potential. Only the drain barrier is significantly affected by V_{ds}. The integration in Eq. 1 is carried out in regions T_1, T_2, and T_3.

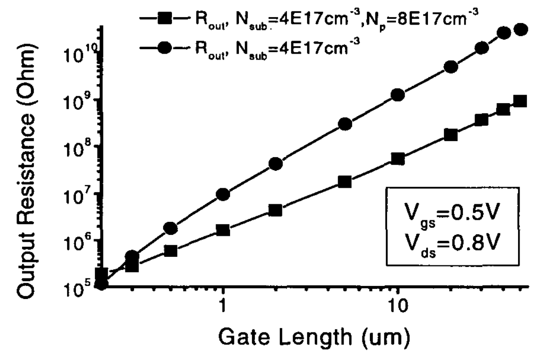

Fig. 4. Simulated R_{out} of the device with pocket implant is more than 10 times smaller at long channel length. One device has a pocket doping of N_p=8E17cm^{-3}, and pocket length L_p=0.08μm. The devices are otherwise identical.

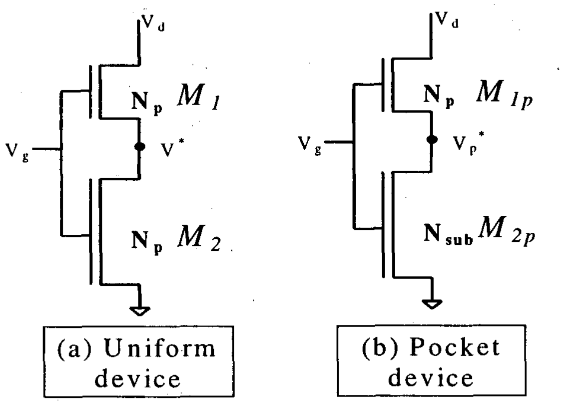

Fig. 5. Equivalent circuits used in the derivation of the output resistance model. A uniformly doped device is shown in (a) and a pocket implanted device in (b).

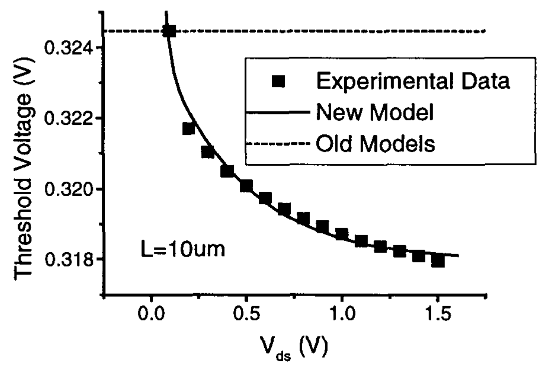

Fig. 6. The proposed model is in excellent agreement with measured V_T vs. V_{ds} of a 10μm MOSFET fabricated using a 0.18μm process with pocket implantation.

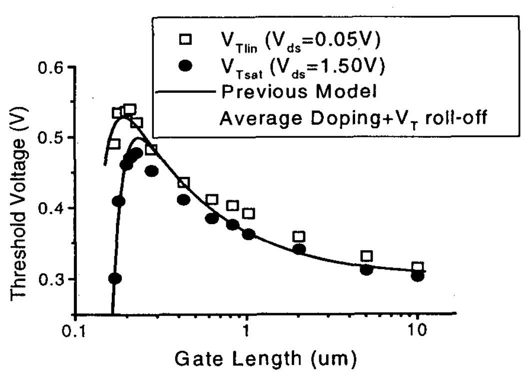

Fig. 7. Best-effort fitting of experimental data with the BSIM3 model. The model shows negligible DIBL effect (V_{ds} dependence) at long gate lengths.

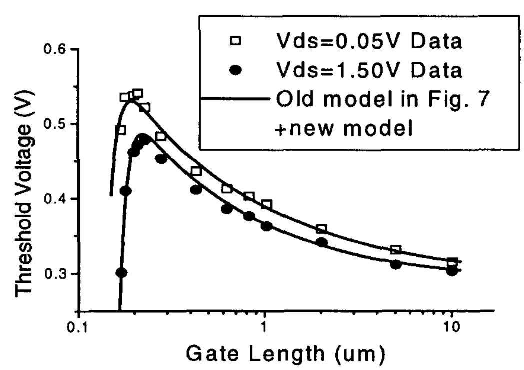

Fig. 8. Fitting of experimental data with the new model added to the BSIM model used in Fig. 7. The number of fitting parameters is the same as in Fig. 7 because parameters extracted in Fig. 6 are used in the new model.

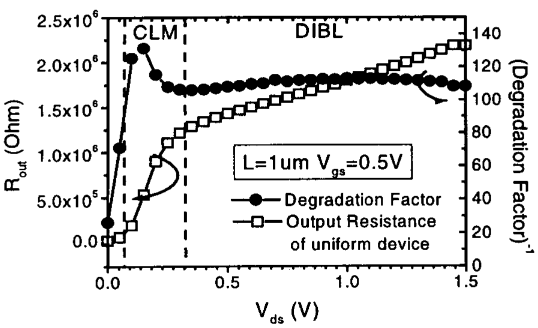

Fig. 9. Degradation Factor of output resistance from 2-D simulation is almost independent of V_{ds} as predicted by the proposed model in both channel length modulation (CLM) and drain-induced barrier lowering (DIBL) regions.

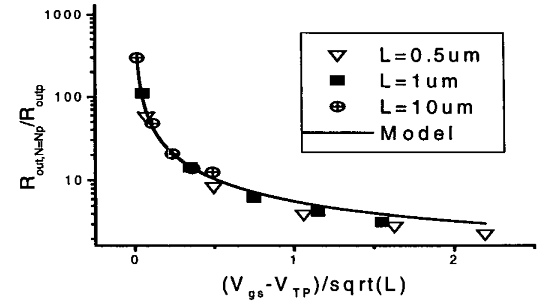

Fig. 10. Simulation verification of the predicted universal curve of the degradation factor (1/F plotted) vs. $(V_{gs}-V_{TP})/\sqrt{L}$.

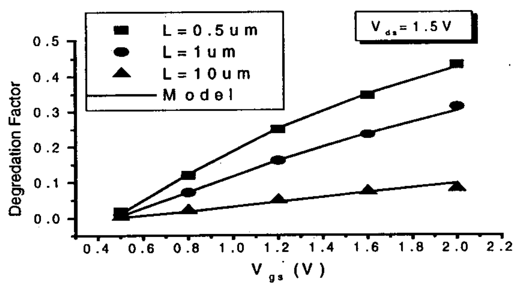

Fig. 11. Agreement of V_{gs} dependence of the degradation factor F between model and simulation for different gate lengths.

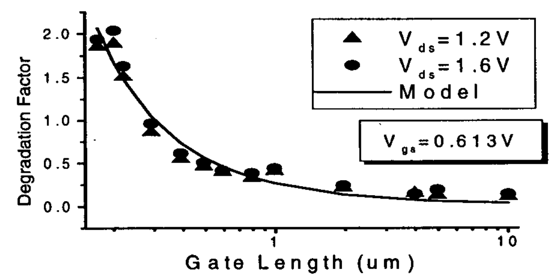

Fig. 12. Agreement of model and experimental data of a 0.18μm process with and without pocket implant. Note that the degradation factor is very different from Fig. 9,10,11 because the uniform device is doped to the substrate level.

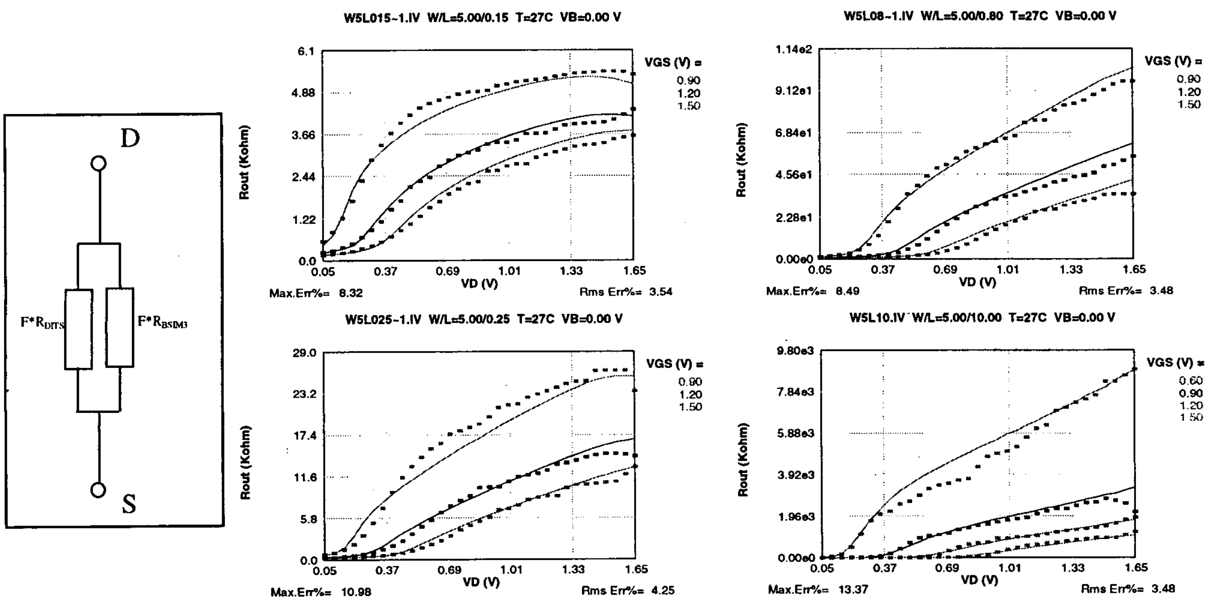

Fig. 13. On the left, the equivalent circuit of the implementation of proposed model. On the right is the fitting of measured R_{out} of 0.18μm technology using the model implemented. 12 devices with gate lengths from 0.15μm to 10μm are fitted using a single set of parameters without binning. The maximum error is 17.0% and the RMS error is 4.9%. A new V_{dsat} model and CLM R_{out} model were also implemented for the fitting.