TP 12.3 An Integrated 2.5GHz ΣΔ Frequency Synthesizer with 5μs Settling and 2Mb/s Closed Loop Modulation

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Three radio communication standards that share common performance requirements are gaining momentum. The 802.11 wireless LAN standard, the Bluetooth radio connectivity protocol, and the HomeRF SWAP home networking protocol all specify frequency hopping radios in the 2.4GHz band using FSK modulation in a 1MHz bandwidth. These standards require modest radio performance (compared to cellular systems), but demand small size and low cost. This paper describes a CMOS ΣΔ fractional-N (ΣΔFN) frequency synthesizer. In contrast to prior art [1,2], its 700kHz bandwidth type-1 phase-locked loop (PLL) enables sub-5μs frequency hops plus 2- and 4-level digital Gaussian frequency shift keying (GFSK) modulation at 1 or 2Mb/s.

Each feature described above enables substantial cost reduction of the complete radio solution. The order of magnitude reduction in frequency settling allows hopping in the short time between transmit and receive time slots. A single PLL can provide heterodyning of the receive channel to the radio intermediate frequency followed by direct FM at the transmit carrier frequency. Direct digital modulation eliminates I/Q DACs, mixers, and associated upconversion filters. The closed loop modulation is phase-accurate and resistant to VCO pulling, pushing, and gain variation. Thw synthesizer 50Hz frequency resolution facilitates digital correction of reference crystal accuracy and drift.

The ΣΔFN technique is illustrated by the synthesizer block diagram in Figure 12.3.1. The VCO frequency is divided by a dynamically changing modulus, the resulting phase error compared to a 48MHz reference, lowpass filtered, and applied back to the oscillator control input to complete the loop. The divider modulus is supplied by a 3rd-order, 3b oversampling ΣΔ modulator which interpolates the VCO frequency between integer multiples of the reference frequency. The ΣΔ process produces short-term phase errors, the main energy of which is noise-shaped to lie beyond the bandwidth of the loop filter and therefore removed before reaching the VCO. The 3rd-order lowpass response of the PLL cancels the FM noise produced by the 3rd-order ΣΔ divisor sequence, resulting in phase noise that rolls off at 20dB/decade.

The synthesizer is integrated on the same chip as the digital baseband logic of the radio which provides digital inputs for the carrier frequency (FC) and GFSK deviation from the carrier (FM). Only the (140MHz/V) VCO and passive elements of the loop filter reside off-chip.

In contrast to traditional PLLs which require near-zero phase error to minimize spur energy, a ΣΔPLL high reference frequency is easily filtered. Thus a fast-settling type-1 PLL architecture can be considered which, by definition, lacks an integrator in the loop filter to force zero phase error (Figure 12.3.2). Due to oversampling, a ΣΔFN PLL has a narrow bandwidth with respect to its phase-detector rate. Upon frequency hops, this leads to phase differences between the divider output and reference exceeding several cycles, surpassing the range of typical phase detectors. Consequently, a type-1 loop would fail to lock and a type-2 loop would exhibit severe cycle-slipping, destroying its settling time. This synthesizer surmounts this problem by employing an extended-range phase detector (ERPD) capable of continuously tracking multi-cycle phase errors [3].

The principle of ERPD operation is shown in Figure 12.3.3. A tristate phase-frequency detector (PFD), shown in the upper branch of the figure, tracks small phase errors. When its error surpasses 180°, the pump-up signal PU is sampled high by the negative edge of the reference clock, generating a count-up signal CU. This increments a digital register, causing a coarse-ranging DAC to add 180° of scaled current. Concurrently, the reference input to the PFD is inverted, subtracting 180° from its operation. The sum of the DAC current and charge-pump may thus track an arbitrarily mounting phase error while maintaining PFD operation within ±180°. The counting process ceases as the loop settles and only the PFD and charge-pump are active in the steady state. Hysteresis of DAC stepping eliminates the need for precise matching of DAC and charge-pump currents.

The ΣΔPLL large phase excursions demand attention to linearity in PFD logic and charge pump. Residual nonlinearities fold noise-shaped phase error energy back into the baseband. A tristate PFD of conventional architecture uses differential logic for symmetry and noise immunity. Its reset circuitry is crafted to suppress dead-zone gain variations as well as anomalies near 180° where the flip-flop clock inputs change level. The phase error between Fref and Fdiv is represented by the difference between PFD outputs PU and PD which drive the charge pump in Figure 12.3.4. The charge pump core consists of dual differential-pair current switches controlled by signals SU and SD. These signals are driven through multiplexors fed by buffered bias voltages arranged to provide minimal-swing saturating drive. The switch drivers produce overlapping-low signals to minimize tail-voltage transients. Simulations indicate that the circuits, with 1% matching of current sources, have sufficient linearity to reduce folded noise below the thermal noise levels of the current sources and loop filter.

The multi-modulus frequency divider shown in Figure 12.3.5 is composed of a divide-by-4/6 stage followed by three divide-by-2/3 stages [2]. It has a modulus range of 32 to 62 in increments of 2, and produces less than 4.6ps rms excess jitter in response to the ΣΔ sequence. Resistor-loaded differential logic at the front end of the divide-by-4/6 block achieves 2.5GHz operation in the 0.5μm process. The divide-by-4/6 operation uses phase shifting with glitch-free make-before-break switching, allowing robust operation over a much wider range of frequencies than the prior art [2,4]. To minimize delay variations, all transitions influencing the final output of the divider travel through the OUT_I path. The OUT_Q path is used only to achieve glitch-free switching between phases of 0 and 180°. The remaining divider blocks are implemented with full-swing, true single-phase clocked (TSPC) logic.

The synthesizer, integrated with a prototype HomeRF baseband transceiver ASIC in 0.5μm CMOS, is shown in Figure 12.3.8. The die is 4.30x4.53mm^2, of which ~3.5mm^2 is occupied by the ΣΔFN synthesizer. Phase noise, shown in Figure 12.3.6, is -100dBc/Hz in-band, rolling off at 20dB/decade past 700kHz offset. An inset demonstrates digital FSK carrier modulation. The settling time shown in Figure 12.3.7 is <5μs. Spurs from the baseband logic clock (24MHz) are -77dBc. Power consumption for the synthesizer, excluding the off-chip VCO, is 41mA at 3.3V.

References:

[1] Riley, T. A. and M. A. Copeland, "A simplified continuous phase modulator technique," IEEE Trans. Circuits Syst.-II, vol. 41, pp. 321-328, May 1994.
[2] Perrott, M. H., T. L. Tewksbury, and C. G. Sodini, "A 27mW CMOS fractional-N synthesizer/modulator using digital compensation for 2.5-Mb/s GFSK modulation," IEEE J. Solid-State Circuits, vol. 32, pp. 2048-2060, Dec. 1997.
[3] U.S. Patent 5,952,853, Agilent Technologies.
[4] Craninckx, J. and M. S. Steyaert, "A 1.75GHz/3V dual-modulus divide-by-128/129 prescaler in 0.7μm CMOS," IEEE J. Solid-State Circuits, vol. 31, pp. 890-897, July 1996.

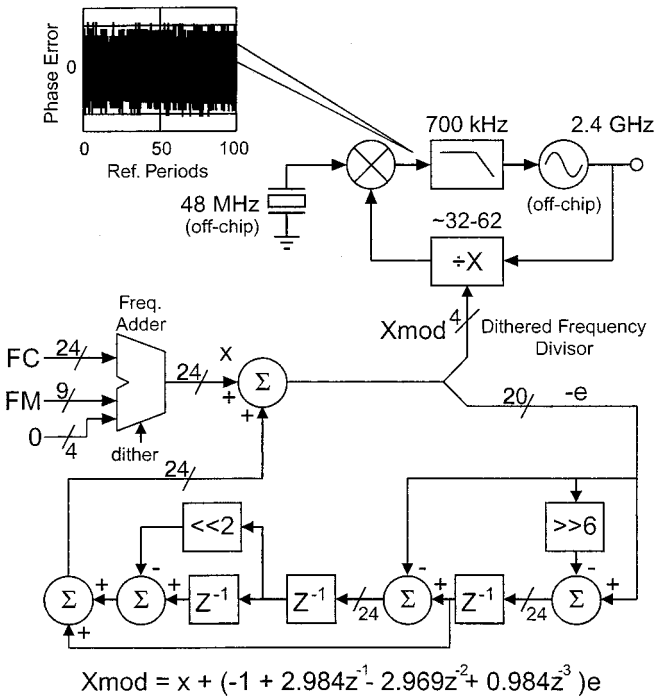

Figure 12.3.1: Block diagram of the wideband FN synthesizer PLL.

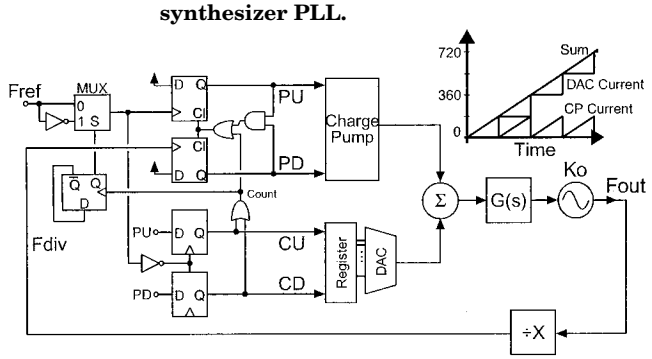

Figure 12.3.3: The extended-range phase detector concept.

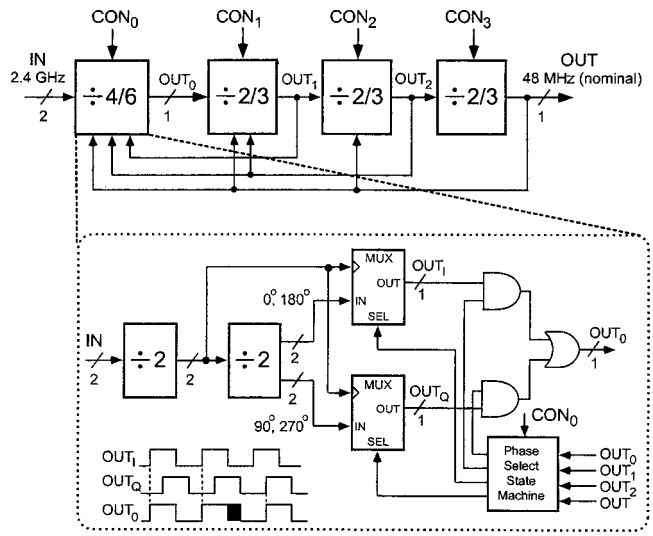

Figure 12.3.5: The high speed multi-modulus divider.

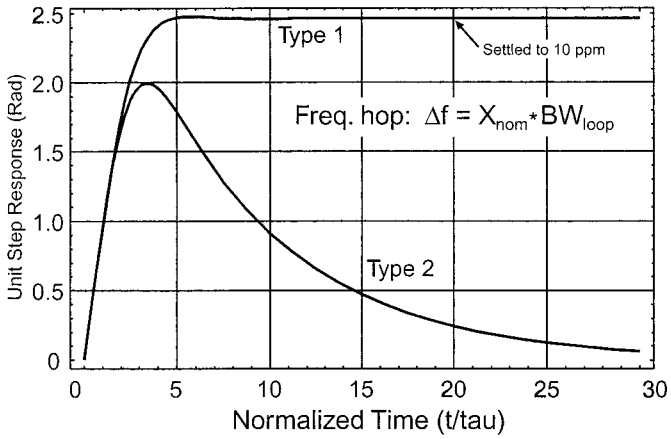

Figure 12.3.2: Ideal phase error transients of type-1 and type-2 PLLs.

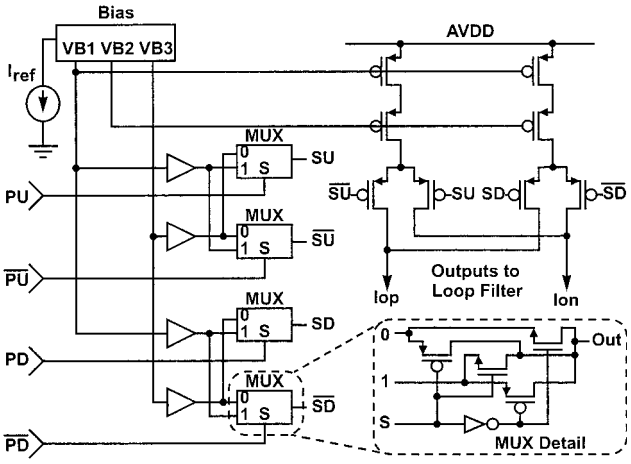

Figure 12.3.4: Charge pump schematic.

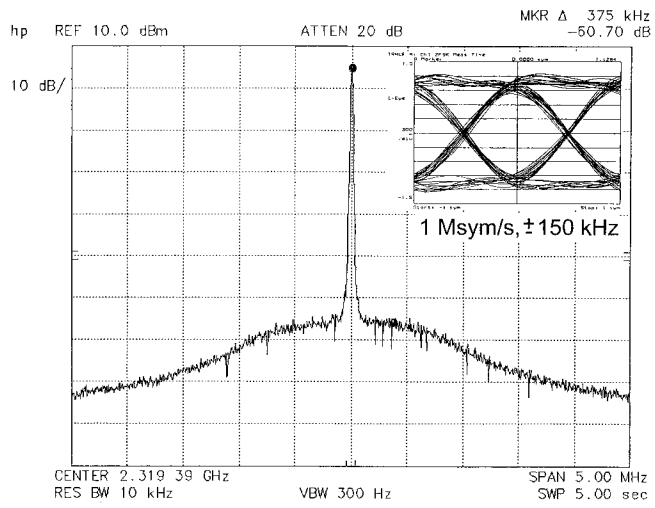

Figure 12.3.6: Unmodulated carrier spectrum (receive mode, 2319MHz) and modulated FSK eye diagram (transmit mode, 2430MHz).

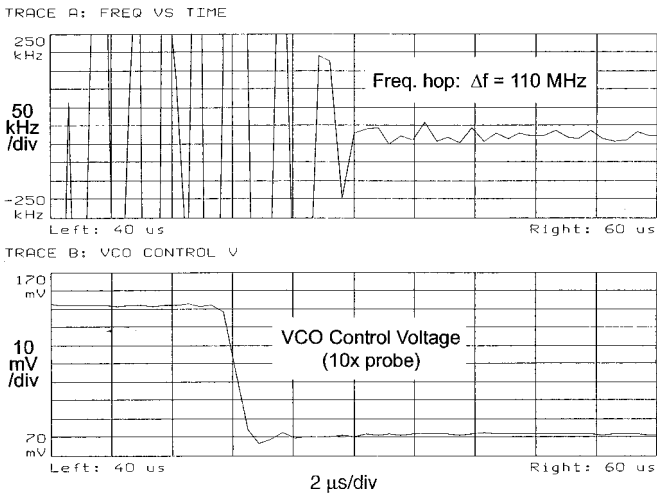

Figure 12.3.7: Frequency hop settling vs. time.

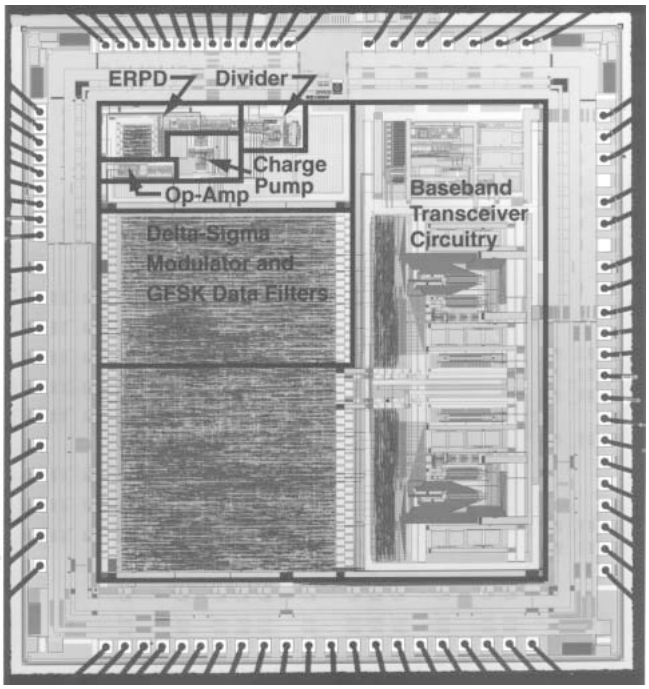

Figure 12.3.8: Prototype SWAP transceiver chip micrograph.