## 4.6 A Multiple-Crystal Interface PLL with VCO Realignment to Reduce Phase Noise

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This enhancement to a conventional phase-locked loop (PLL) periodically realigns a CMOS voltage-controlled oscillator (VCO) with the reference signal to reduce phase noise. The technique is generally applicable in situations where it is necessary to reduce VCO phase noise in very high frequency (VHF) PLLs. It is applied here to a 96MHz reference PLL for a next-generation version of the Bluetooth transceiver described in Reference [1] to facilitate operation from all of the popular crystal reference frequencies. The 96MHz signal is used to generate a 1MHz reference for the transceiver radio frequency (RF) PLL, and a 32MHz clock to drive the transceiver baseband circuitry and data converters. 10dB peak phase noise reduction and 8.3dB integrated phase noise reduction relative to the conventional PLL alone are demonstrated via measured results that closely match theoretical predictions.

The PLL design is challenging because of the requirements that it be implemented with only CMOS components for possible migration to a CMOS process, that it use a ring oscillator VCO to avoid external components, and that its phase noise between 1kHz and 50kHz from the carrier be below –100dBc/Hz (the loop bandwidth of the RF PLL is 50kHz). Unfortunately, CMOS ring oscillators are noisy. The measured VCO noise 100kHz from the carrier is –107dBc/Hz, so the loop bandwidth of a conventional PLL would have to be ~100kHz to sufficiently suppress the VCO noise with enough margin to allow for phase noise from the other PLL components. Such a large loop bandwidth ruled out the use of a conventional PLL. In a conventional PLL, the reference frequency is obtained by dividing each crystal frequency to the greatest common divisor of 96MHz, but to maintain stability over process and temperature extremes the PLL reference frequency must be approximately 20 times the loop bandwidth. Among the commonly used crystal references, this implies that the target phase noise cannot be met for 19.68 and 19.8MHz crystals in a conventional PLL.

The VCO realignment technique shown in Figure 4.6.1 avoids this problem. The idea is to use a buffered version of the PLL reference to correct the VCO once every reference period. As shown in Figure 4.6.2a, the noise introduced by a conventional ring oscillator "builds up" over time because the zero crossing error introduced by each inverter adds to all the previous zero crossing errors [2]. As shown in Figure 4.6.2b, the realignment technique shorts a buffered version of the clean reference signal to the VCO output at each point where a VCO edge ideally coincides with a reference signal edge. This causes the VCO edge to be "pulled" toward the correct position thereby suppressing the memory of past errors and reducing the phase noise.

A simplified circuit diagram of the realigned VCO is shown in Figure 4.6.3a. The VCO is a 7-stage ring oscillator in which 4 of the inverters are used to control the frequency and 3 introduce a fixed delay. This separation is made to minimize charge injection from the realignment switches into the sensitive VCO control node. Although not shown in the figure, the supply voltage on the fixed inverters is level shifted to 1.5V to approximately match the drain voltage of the VCO frequency control transistor. As illustrated in Figure 4.6.3b, the realignment process does not perfectly align the VCO and reference edges. Instead, circuit simulation and experimental measurements indicate that during each realignment the phase of the VCO is adjusted almost linearly by a factor of $\beta = 0.5$ times the difference between the actual and ideal VCO phases.

Without the realignment technique, the PLL phase noise, $\theta_{out}(s)$, is described by the well-known linearized model shown in Figure 4.6.4a, where $\theta_{ref}(s)$ is the phase noise of the reference source, $\theta_{vco}(s)$ is the phase noise of the VCO without realignment, $K_{dp}$ and $K_{vco}$ are the charge pump and VCO gains, respectively, and $H_{lp}(s)$ is the transfer function of the PLL loop filter [3]. With the realignment technique, assuming the realignment behavior described above occurs abruptly at each reference edge, an extension of the derivation in [3] indicates that the model contains two new blocks as shown in Figure 4.6.4b:

$$H_{ri}(j\omega)=1-\frac{\beta e^{j\omega T_{ref}/2}}{1+(\beta-1)e^{j\omega T_{ref}}}\cdot\frac{\sin(\omega T_{ref}/2)}{\omega T_{ref}/2}, \text{ and } H_{up}(j\omega)=\frac{M\beta e^{j\omega T_{ref}/2}}{1+(\beta-1)e^{j\omega T_{ref}}}\cdot\frac{\sin(\omega T_{ref}/2)}{\omega T_{ref}/2},$$

where $T_{ref}$ is the reference period. Figure 4.6.4c shows a comparison of the loop and VCO phase noise transfer functions for the PLL with realignment disabled ($\beta = 0$) and realignment enabled ($\beta = 0.5$). As is evident from the figure, the realigned PLL differs from the conventional PLL in that the VCO phase noise contribution is significantly reduced, the phase margin of the loop is increased, and the reference source phase noise contribution is slightly increased.

Measured data closely support these findings. Figure 4.6.5 shows measured and theoretical power spectral density (PSD) plots of the PLL phase noise with the realignment technique enabled and disabled for 19.68MHz crystal frequency and 25kHz loop bandwidth. Similar results are observed for the other crystal frequencies. The results indicate that the realignment technique reduces the peak in-band phase noise by 10dB, and reduces the phase noise integrated from 1 to 50kHz by 8.3dB. When the loop bandwidth is increased to a less conservative 50kHz, which is near the maximum value prior to instability, the integrated phase noise improvement changed from 8.3dB to 5.3dB. These results indicate that the realignment technique significantly reduces the PLL phase noise contributed by the VCO. However, mismatches between the two reference signal paths increase the power of the reference spur in the PLL output. The measured reference spur power was –34dBc with the technique enabled, and –78dBc with the technique disabled. While not of major concern for this project, the increased reference spur power may be a drawback in some applications. In anticipation of the possible future inclusion of an automatic path calibration loop, a variable delay element is inserted prior to the divider to allow for such calibration. With this feature enabled and manually calibrated, the measured spur power was –71dBc and static which suggests that an automatic calibration loop, if necessary, would be effective. Measured total power consumed by the PLL is 6.8mW with no observable difference when the realignment technique is disabled. The theoretical PSD plots are obtained by applying the phase noise models in Figure 4.6.4 a and b to measured PSD plots of the phase noise from the VCO and reference source in isolation. A good match between theory and measurement is evident. A performance summary and die micrograph are shown in Figure 4.6.6 and Figure 4.6.7, respectively.

*References:*

[1] Silicon Wave SiW1502 Bluetooth Radio Modem IC Data Sheet, Nov. 3, 2000.

[2] G. Chien, P. R. Gray, "A 900MHz Local Oscillator Using a DLL-Based Frequency Multiplier Technique for PCS Applications", ISSCC Digest Technical Papers, pp. 202-203, Feb., 2000.

[3] F. Gardner, "Charge-pump phase-lock loops", IEEE Trans. Comm., vol. COM-28, no. 11, pp. 1849-1858, Nov. 1980.

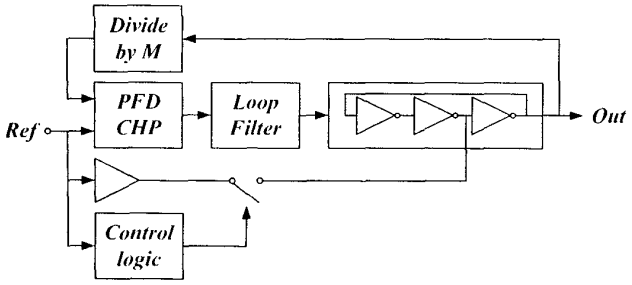



Figure 4.6.1: Top-level system block diagram.

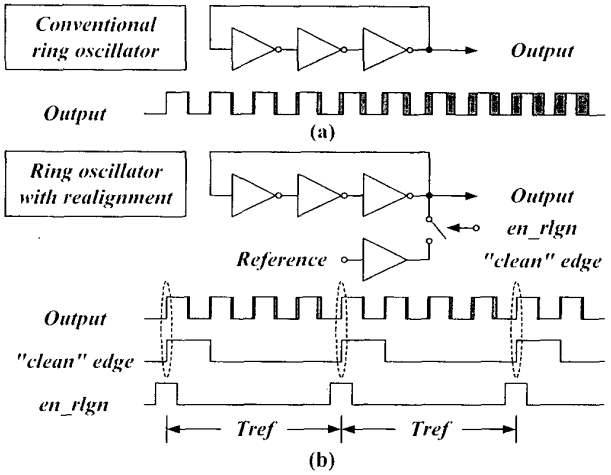
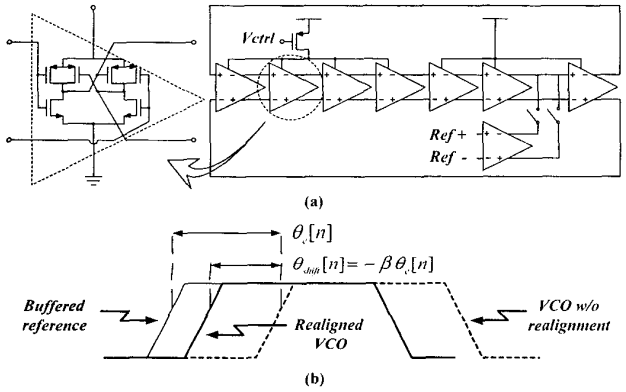
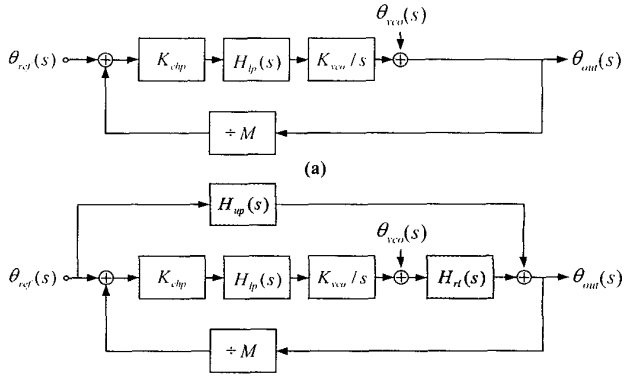
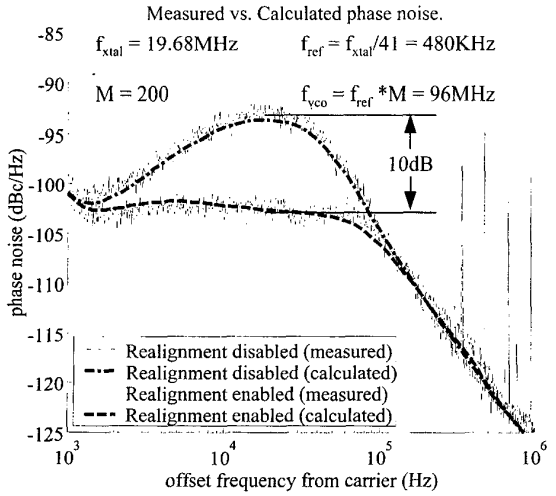



Figure 4.6.2: (a) Phase noise is accumulated in typical ring oscillators. (b) Periodically realigning the oscillator to a "clean" edge supresses the phase noise accumulation.




igure 4.6.3: (a) Simplified circuit diagram of the realigned ring oscillator. (b) hase realignment pulls the VCO edge toward its "correct" value.




jure 4.6.5: Measured and calculated phase noise PSD plots for the PLL with ılignment enabled and disabled. (PLL bandwidth = 25kHz).

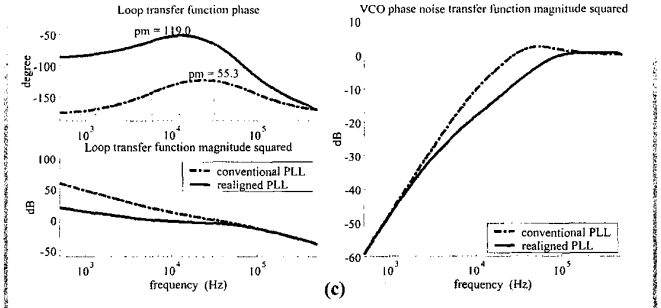



Figure 4.6.4: (a) Commonly-used phase noise model of a conventional interger-*N* PLL. (b) Modified version of the phase noise model describing the realigned PLL. (c) Plots of the loop and VCO phase noise transfer functions from the two models.

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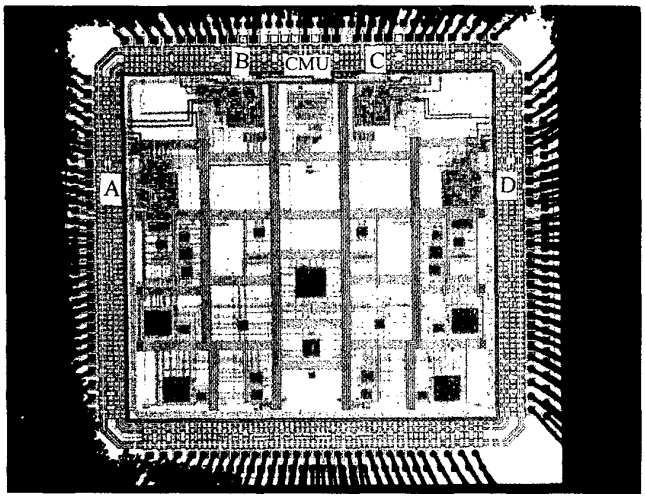


Figure 4.2.7: Die micrograph.

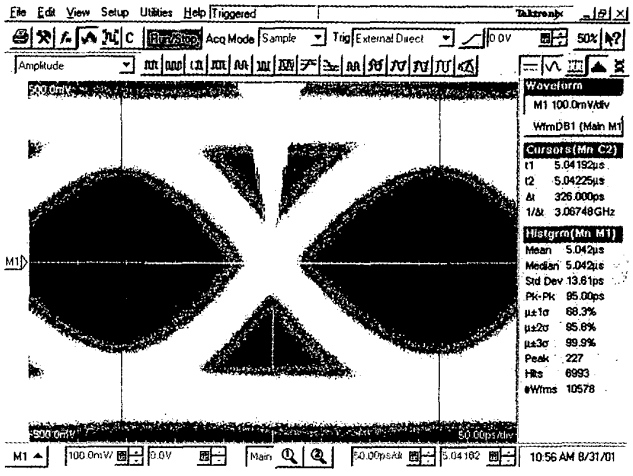


Figure 4.3.7: Eye diagram after crossing backplane at 3.1Gb/s.

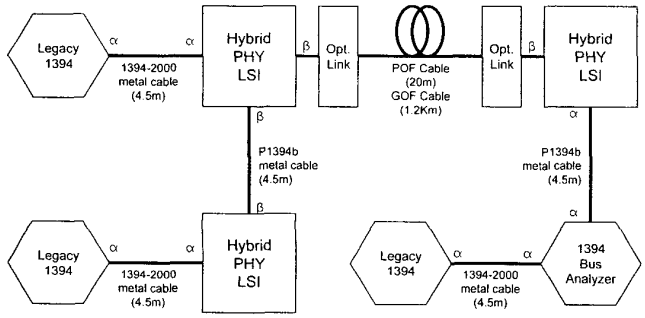


Figure 4.4.5: Block diagram of primary system evaluation.

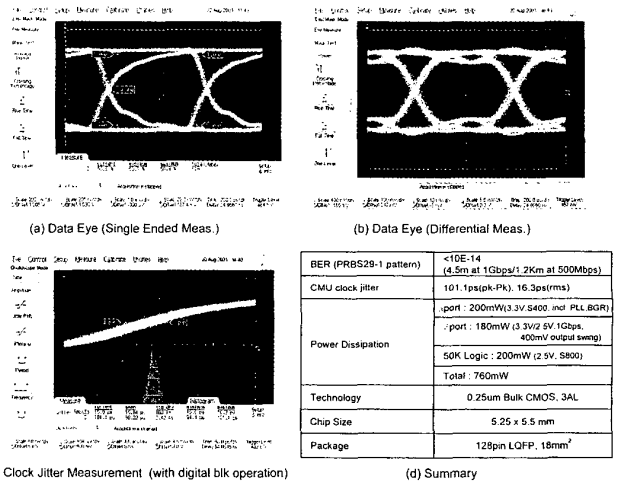


Figure 4.4.6: Measurement results.

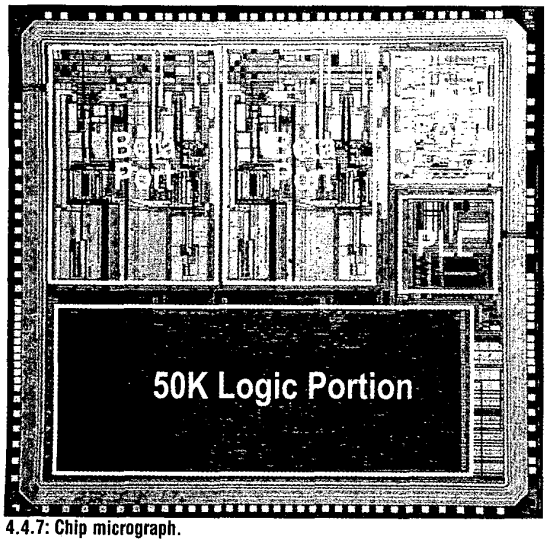


Figure 4.4.7: Chip micrograph.

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|---|---|
| Technology | 0.35µm BiCMOS SOI (with only CMOS components used) |
| Supply voltage | 2.7-3.3V (measurements at 3V) |
| Total power consumption | 6.8mW (no observable difference when realignment enabled) |
| Die size | 1.8mm² |
| Realigned PLL core area | 0.22mm². Conventional PLL: 73% Realignment circuitry: 27% |
| Spot noise at 20KHz offset (25kHz PLL bandwidth) | -92.5dBc/Hz (realignment disabled) -102.5dBc/Hz (realignment enabled) |
| Reduction of integrated noise power from 1kHz - 50kHz | 8.3dB w/ 25kHz PLL bandwidth 5.3dB w/ 50kHz PLL bandwidth |

Figure 4.6.6: Performance summary.