BSIM4 Modeling and Parameter Extraction

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CL TD SIM

Outline

- Evaluation of new BSIM4 Model Features

  - Modeling of Halo/Pocket Implanted MOSFETs

  - Gate-Induced Drain Leakage (GIDL) Modeling

  - Gate Direct Tunneling Current Modeling

- BSIM4 Parameter Extraction Strategy

- Modeling Challenges of Enhanced Physical Device Effects

- Modeling Approaches for Layout Specific Effects

- Outlook: Short-Term Future BSIM4 Version(s)

- Summary

Introduction and Motivation

Introduction of BSIM4 as the new standard compact model for our latest CMOS technologies, to improve our SPICE MOSFET models for circuit simulation.

⇨ Not modeled physical effects in previous BSIM3v3 versions, like halo implantation, gate tunneling current, GIDL, ...

I-V Model (New Features)

☑ Modeling of Halo/Pocket Implanted MOSFETs
  ⇨ Drain-Induced Threshold Voltage Shift (DITS) and
  ⇨ Output Resistance Degradation in Long Channel Devices
  ⇨ Body Bias Dependent Reverse Short Channel Effect (RSCE)
☑ Improved Vgsteff Function (Moderate Inversion Region)
☑ Universal/Predictive Mobility Model
☑ Gate-Induced Drain Leakage Current Model (GIDL)
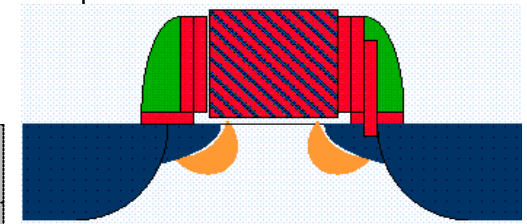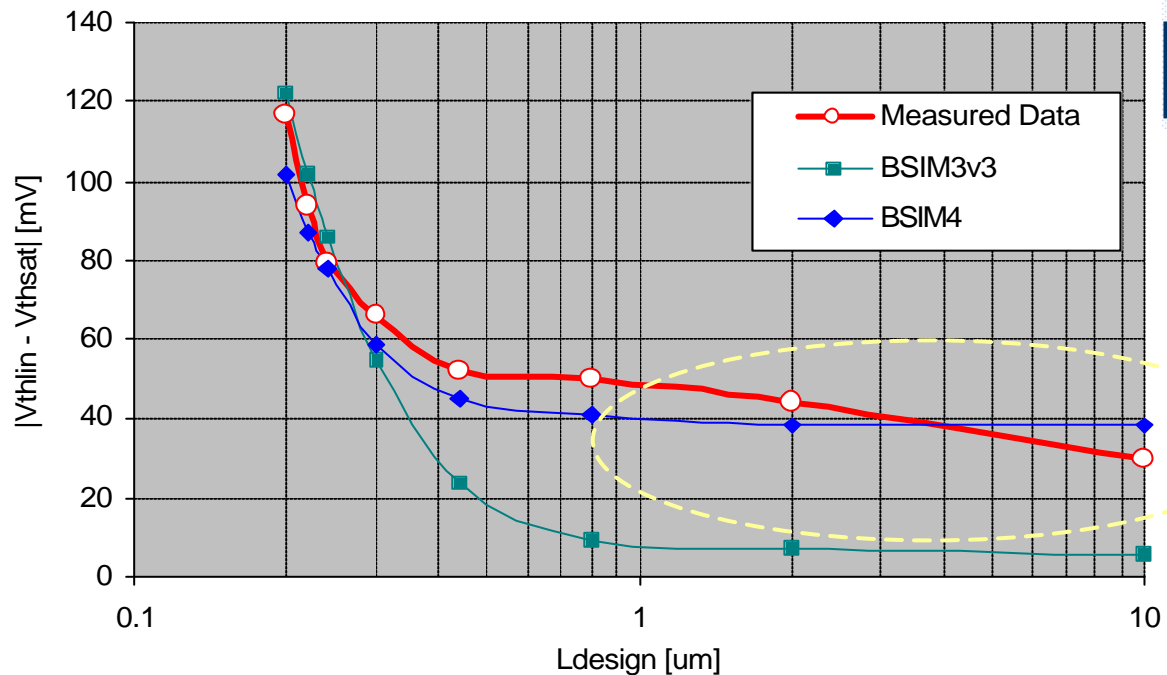☑ Gate Direct Tunneling Current Model

C-V Model

☑ Charge Thickness Capacitance Model (CTM)
  ⇨ Modeling Quantum-Mechanical Charge Layer Thickness and
  ⇨ Poly Gate Depletion Effect

RF / Noise

☐ Intrinsic-Input (Gate) Resistance and Substrate Resistance Network
☐ Non-Quasi-Static (NQS) Model
☐ Flicker Noise and (Holistic) Thermal Noise Model

Threshold Voltage for Halo/Pocket Technologies

**Long Channel DIBL Effect due to Halo Implantation**
PMOS Device

Chart legend:
- Measured Data (red, open circles)
- BSIM3v3 (teal, squares)
- BSIM4 (blue, diamonds)

Y-axis: $|Vth_{lin} - Vth_{sat}|$ [mV]
X-axis: Ldesign [um]

$\rightarrow \Delta Vth_{DITS\_longL} = Vth_{lin\_longL} - Vth_{sat\_longL}$

Halo implantation, used to combat short channel effects (to reduce Vth-roll-off and punch-through), can cause significant drain-induced threshold voltage shift (DITS) in long channel devices!

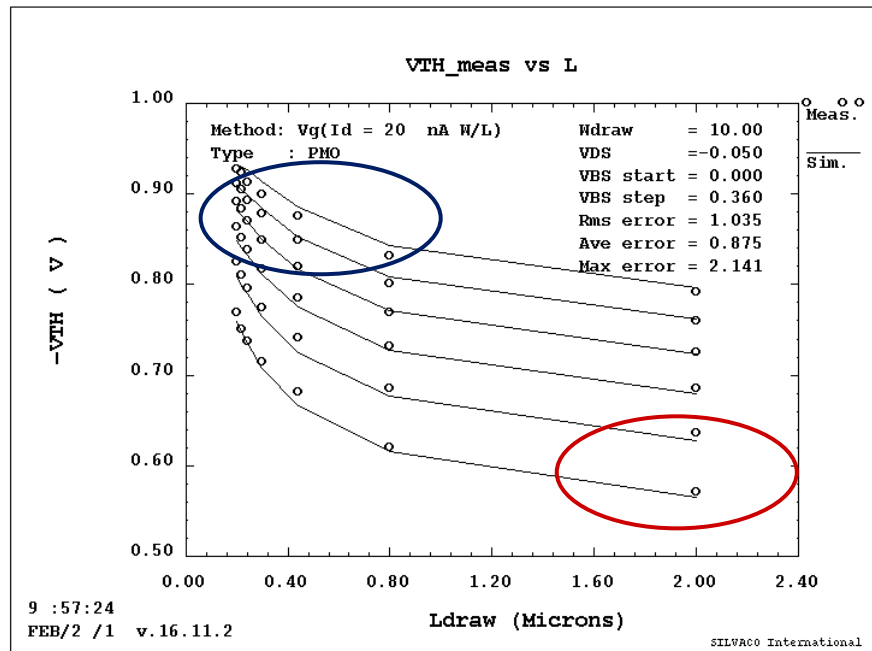# Example for Modeling of Halo/Pocket Implanted Devices (I): BSIM3v3 Threshold Voltage versus Channel Length
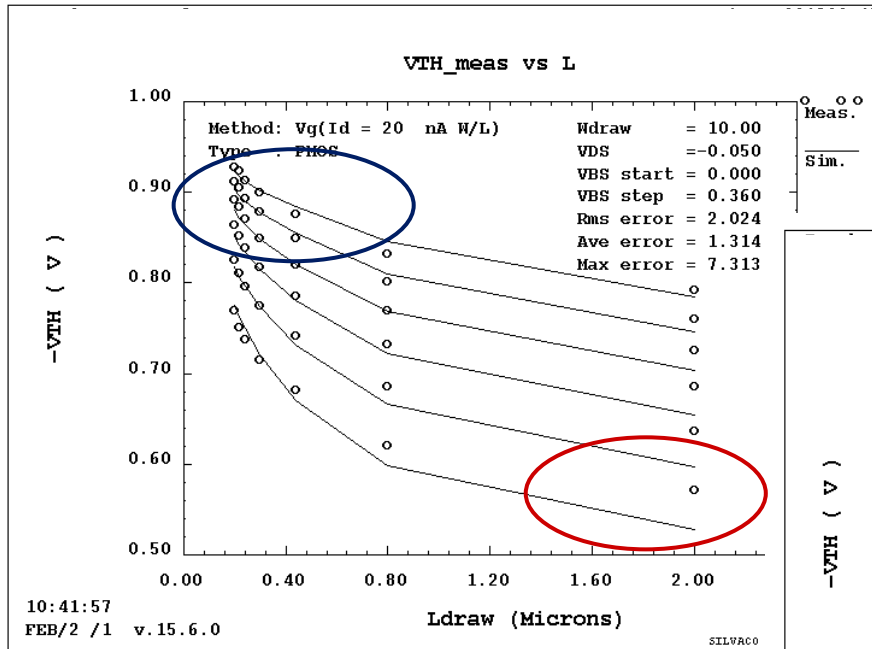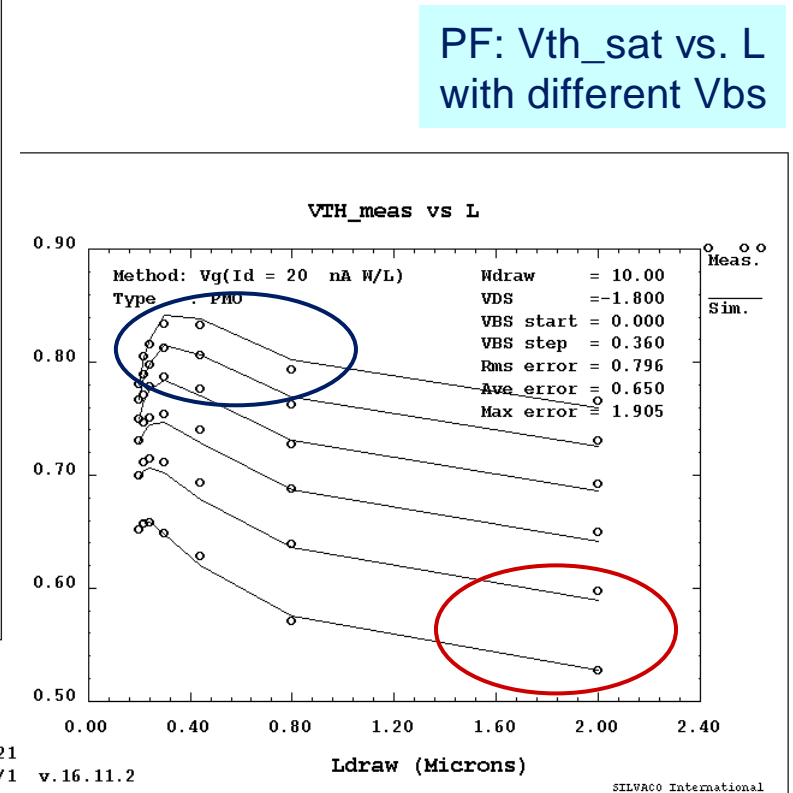
PF: Vth_sat vs. L
with different Vbs
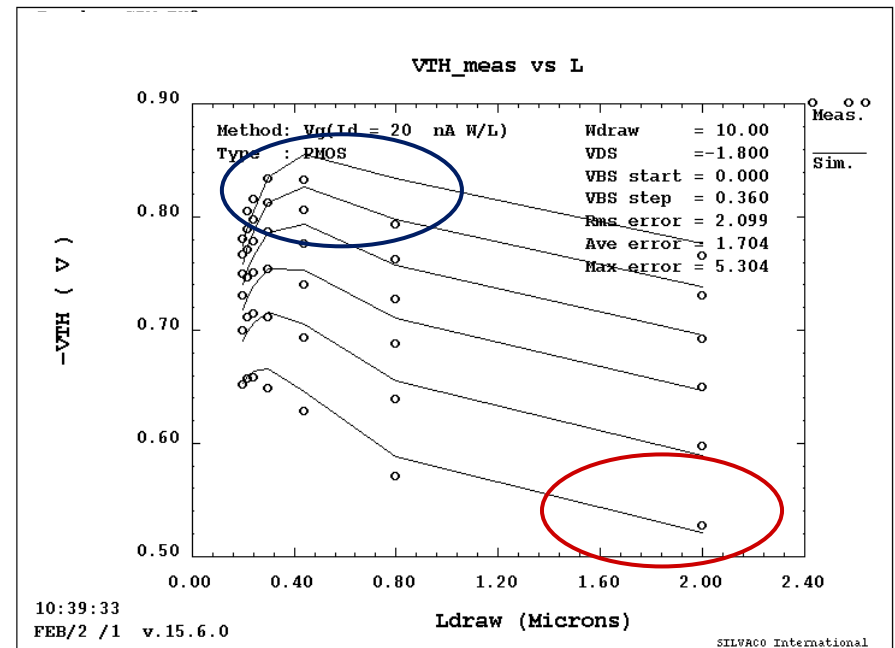
PF: Vth_lin vs. L
with different Vbs

Trade-off between threshold voltage accuracy in linear and saturation region due to long channel DIBL ($\Delta Vth_{DITS} \approx 45mV$).

Example for Modeling of Halo/Pocket Implanted Devices (II): BSIM4 Threshold Voltage versus Channel Length

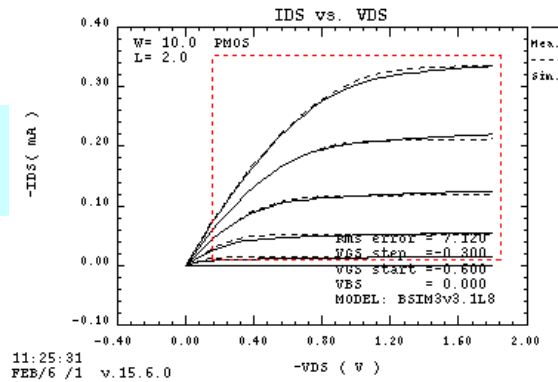PF: Vth_sat vs. L with different Vbs

PF: Vth_lin vs. L with different Vbs

DITS is implemented now!
Modeling accuracy significantly improved for threshold voltage as well as for saturation current length scaling.
Up to ΔVth_{DITS} of $\approx$ 60mV can be modeled with BSIM4.

Example for Modeling of Halo/Pocket Implanted Devices (III): BSIM3v3 Output Resistance Modeling

PF: Ids vs. Vds
@ Vbs = 0V

PF: Ids vs. Vds
@ Vbs = V_{DD}
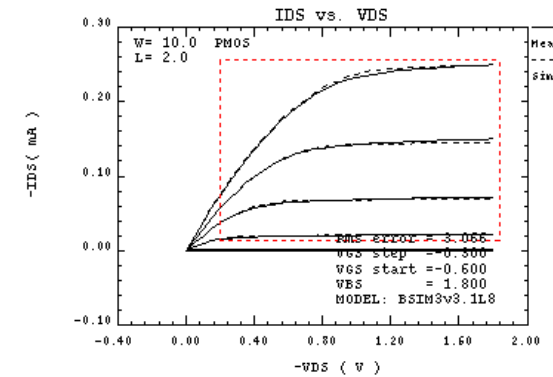
PF: gds
@ Vbs = 0V

PF: gds
@ Vbs = V_{DD}

Halo implants cause also low Rout (high gds) in long channel devices!
This output resistance degradation can <u>not</u> be modeled with BSIM3v3,
because drain-induced threshold voltage shift (DITS) isn´t considered.

Example for Modeling of Halo/Pocket Implanted Devices (IV): BSIM4 Output Resistance Modeling
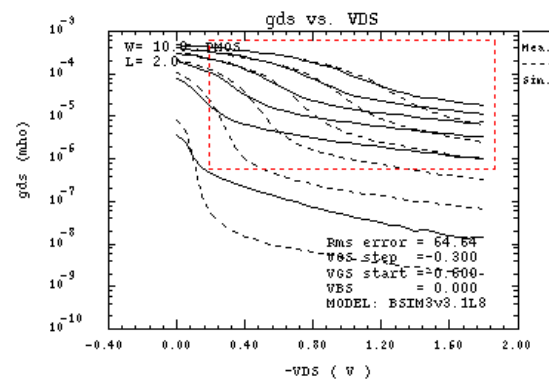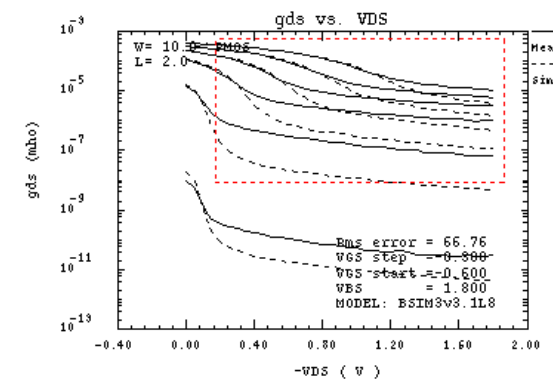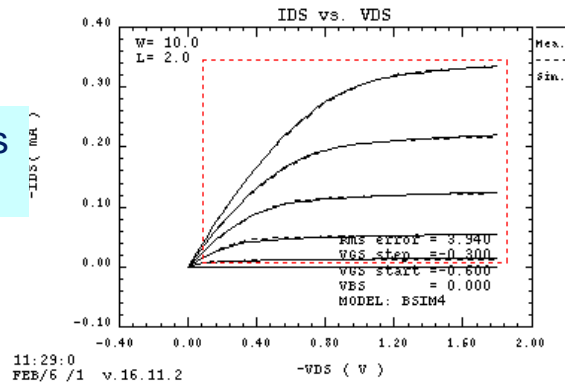
PF: Ids vs. Vds
@ Vbs = 0V

PF: Ids vs. Vds
@ Vbs = V_{DD}
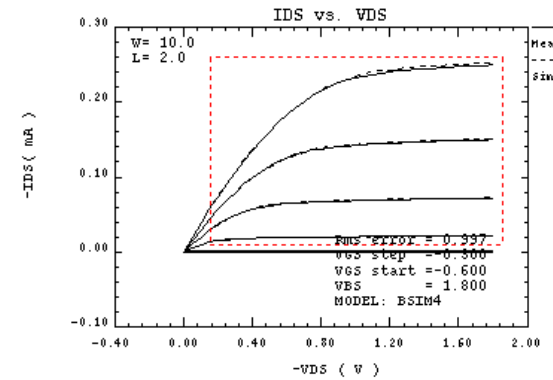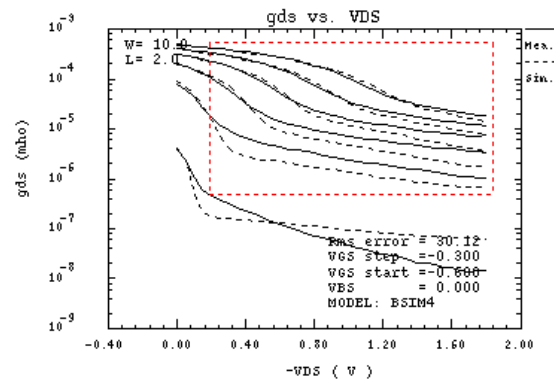
PF: gds
@ Vbs = 0V

PF: gds
@ Vbs = V_{DD}
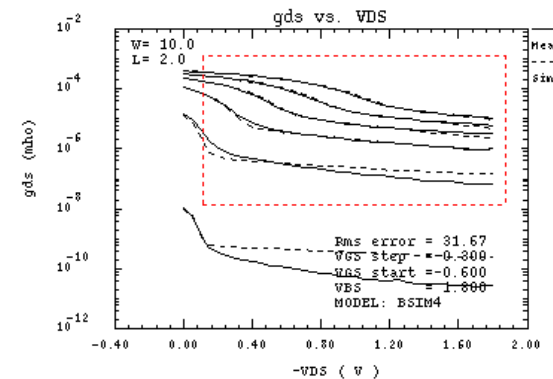
Output resistance accuracy significantly improved! But still a trade-off between modeling at V_{bs}= 0V and V_{bs}= V_{DD} necessary, since the DITS-output resistance model has no parameter for body bias effect.

PREG: Ids vs. Vds @ Vbs = 0V

PREG: Ids vs. Vds @ Vbs = V_{DD}
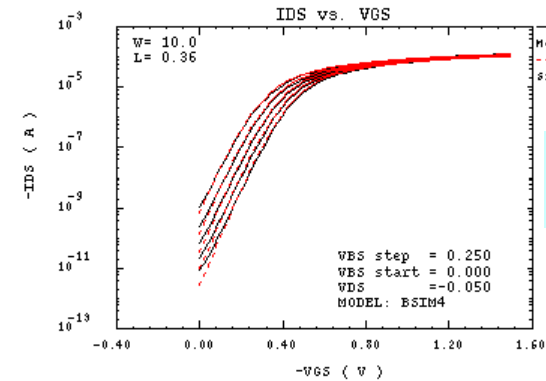
PREG: gds @ Vbs = 0V
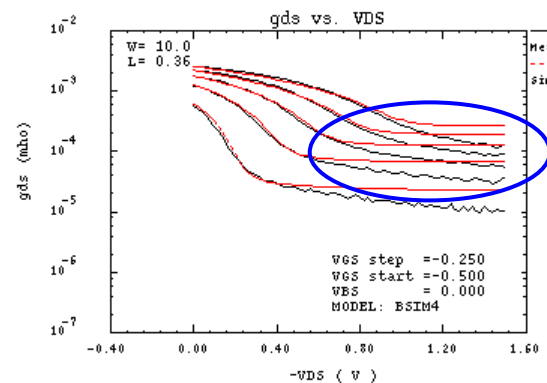
PREG: gds @ Vbs = V_{DD}
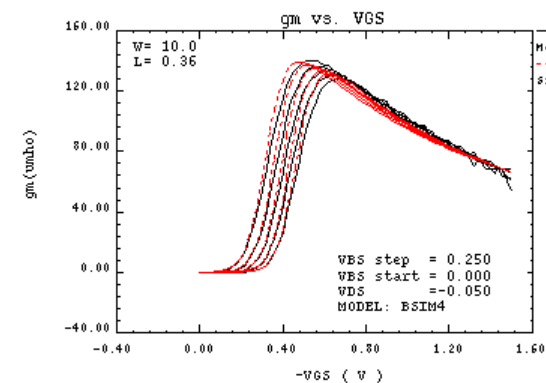
Early voltage can only be varied for intermediate channel lengths (e.g. 3·L_{nom}) with BSIM4! Such gds-deviations (inside above blue circles) have been adjusted using effect of DITS parameters on Rout. BSIM3v3 is only sensitive for early voltage variations at short channel gate lengths (i.e. gds-deviations of nominal devices can be modeled with BSIM3v3.x).

Device Off-Current Contributions
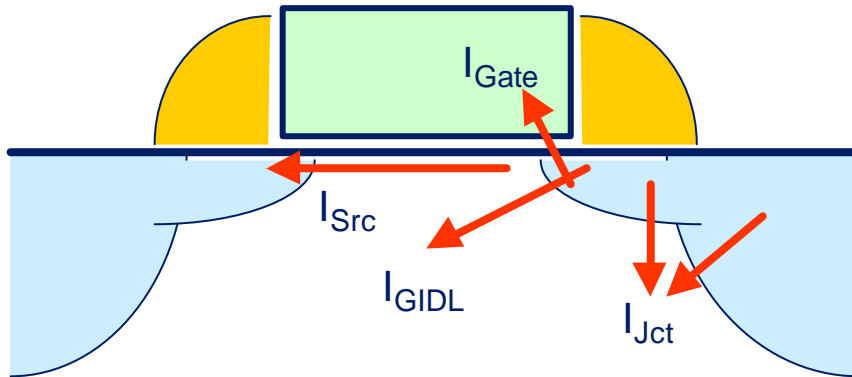
I_{Src} = Source current (T, S/D)

I_{Gate} = Gate leakage current, direct tunneling (Vdd, GOX)

I_{GIDL} = Gate Induced Drain Leakage (Vdd, GOX, S/D)

I_{Jct} = Junction leakage (Vdd, S/D, T)

I_{Gate}

I_{Src}

I_{GIDL}

I_{Jct}

130nm   100nm   65nm
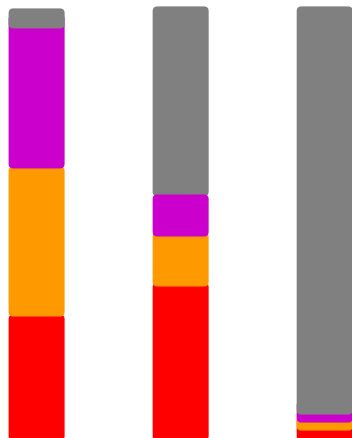
		BSIM3	BSIM4
🔴	Source current	✓	✓
⚫	Gate leakage current	-	✓
🟡	GIDL current	-	✓
🟣	Junction leakage	✓	✓

BSIM4 Gate-Induced Drain Leakage (GIDL) Current Model

NMOS Multi (constant wide channel width)
T=25°C, Vds=3V, W=322.5mm, L=0.4µm, TOX=8.6nm

Legend:
- ○ measured at Vbs=0V
- — simulated at Vbs=0V
- ○ measured at Vbs= -1V
- — simulated at Vbs= -1V
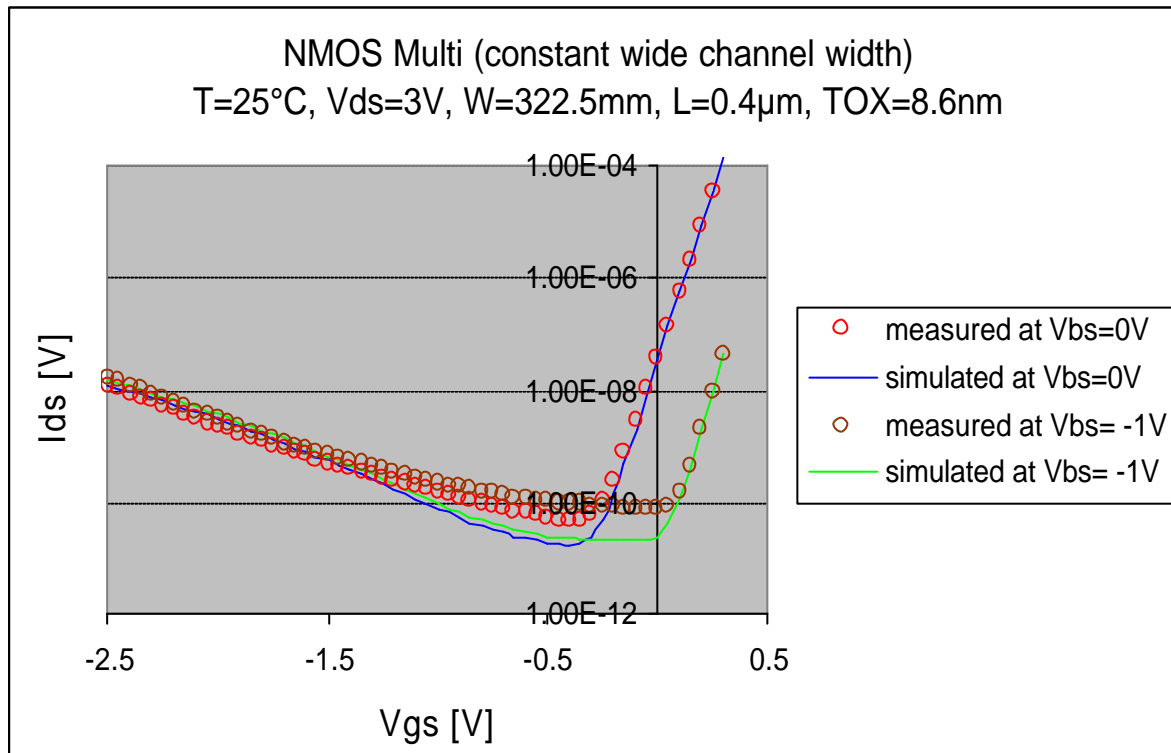
Transfer characteristic in deep subthreshold region (Vgs < 0V) at saturation:
log Ids vs. Vgs
@ Vds = 3V, Vbs = 0V & Vbs = -1V, T=25°C

Drain to gate voltage and body-bias dependence of I_{GIDL}

GIDL has a strong Vdg dependency and a weak body-bias effect (Vdb)! Due to a high field (large Vdg) across the oxide, a deep depletion region under the gate in the drain overlap region is created, which generates electrons and holes by band-to-band tunneling. The resulting drain to body current is called gate-induced drain leakage (GIDL) current.

Gate Leakage Current Modeling with BSIM4

Gate Direct Tunneling Current Simulation

NMOS (TOX_{EOT}=1.0nm) vs. NMOS (TOX_{EOT}=1.3nm) & NMOS (TOXphy=2.2nm)

- Vds=0.05V (TOX=2.2nm: BSIM4.2)
- Vds=1.5V (TOX=2.2nm: BSIM4.2)
- Vds=0.05V (TOX=1.3nm: BSIM4.2)
- Vds=1.2V (TOX=1.3nm: BSIM4.2)
- Vds=0.05V (TOX=1.0nm: BSIM4.2)
- Vds=1.2V (TOX=1.0nm: BSIM4.2)

Gate Direct Tunneling Current Simulation (TOX=1.3nm)

- NFET @ Vds=Vbs=0V
- PFET @ Vds=Vbs=0V
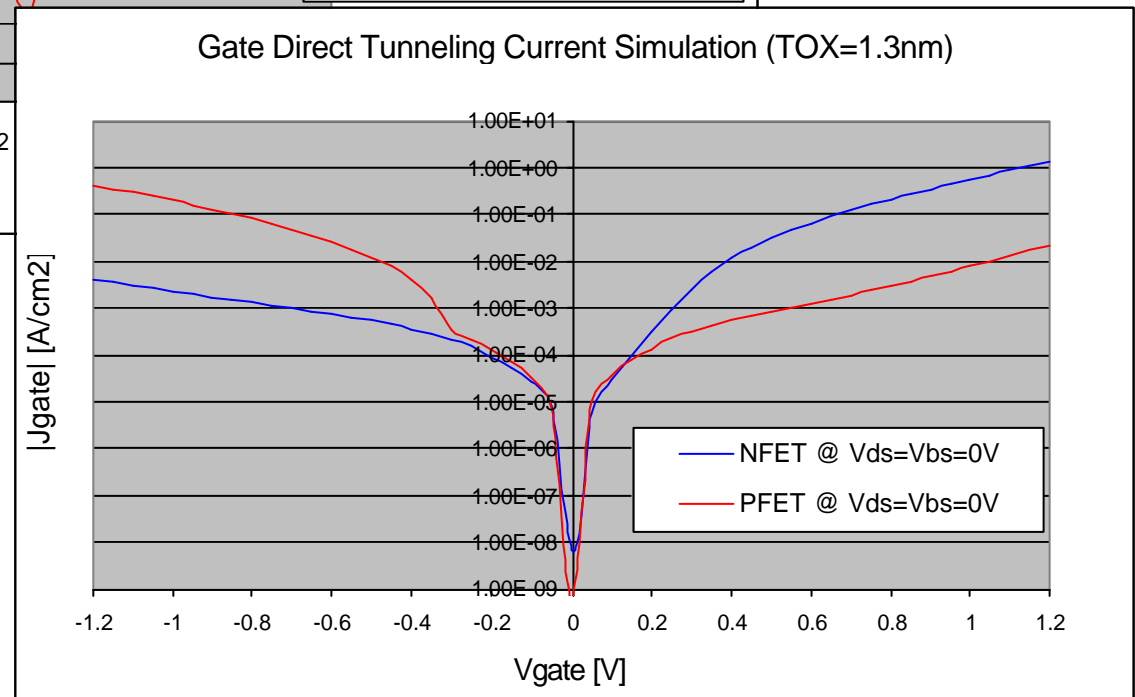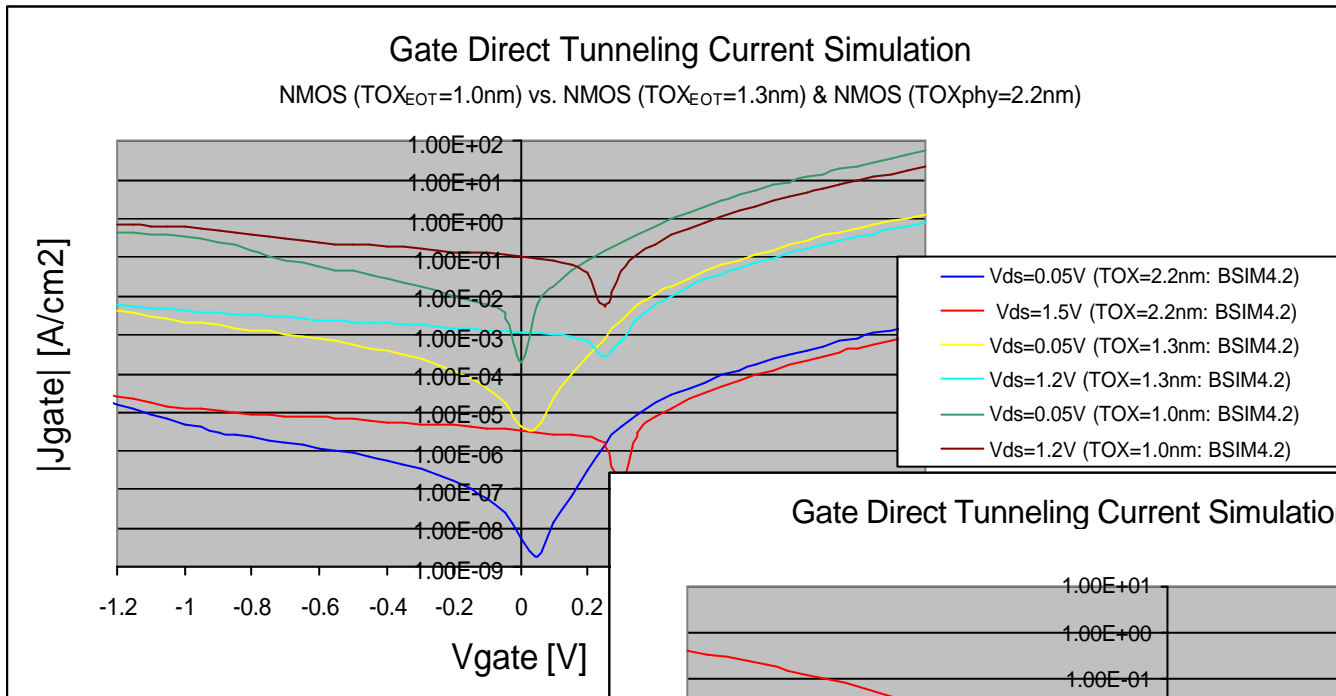
BSIM4 Parameter Extraction Strategy: Optimization Examples

BSIM4-Parameter	Selected Devices	Fitting Target
VTH0, K1, K2, DVTP0 (threshold voltage) **NFACTOR, VOFF, MINV** (subthreshold slope)	large L and W subthreshold characteristics in linear region at $|V_{DS}|$ typ. 0.05V	 log I_{DS} vs V_{GS}
TOXP, NGATE (quantum-mechanical charge layer thickness and poly gate depletion effect)	Multi/overlap or diffusion- bounded GOX structure intrinsic gate capacitances in strong inversion region	 C_{GG} vs V_G
AIGC, BIGC, CIGC, ... (gate-to-channel current) **AIGSD, BIGSD, CIGSD, ...** (gate-to-S/D-diffusion current)	large L and W gate current characteristics in strong inversion and subthreshold region	 log I_G vs V_{GS}
U0, UA, UB, UC (mobility) ⋮	large L and W transfer characteristics in linear region at $|V_{DS}|$ typ. 0.05V	 I_{DS} vs V_{GS}

- Physical device effects related to technology:

    - Halo implantation (lateral non-uniform doping)
    - ⇨ Drain-Induced Threshold Voltage Shift (DITS) in long channel devices
    - ⇨ Output resistance degradation in long channel devices
    - ⇨ Reverse Short Channel Effect (RSCE)
    - ⇨ (Trap-assisted) junction leakage tunneling current

    - (Ultra-)thin gate oxide thickness
    - ⇨ Poly gate depletion effect
    - ⇨ Gate direct tunneling current
    - ⇨ Quantum effects (finite charge layer thickness, V_{TH} shift, ...)

    - Proximity effects
    - ⇨ (Linear) proximity effects (isolated-nested effects)
    - ⇨ Non-linear proximity effects (lithography, OPC, ...)

    - Gate-Induced Drain Leakage (GIDL) current

    - Corner device (parasitic transistor due to shallow trench isolation)

Modeling Challenges: Enhancement of Physical Effects (II)

- Physical device effects related to technology and <u>layout</u>:

  - Webbing/dog-bone effect for narrow-short devices
    (depending on distance of source/drain connections to poly gate)
    ⇨ Effective channel width increased

  - Well proximity effect
    (depending on distance of device to well edges)
    ⇨ Local threshold voltage increased

  - STI-stress effect
    (depending on distance of shallow trench isolation to poly gate)
    ⇨ Mobility reduction for NMOS and mobility increase for PMOS
    ⇨ Threshold voltage increased for NMOS and PMOS
    ⇒ Drain current degradation for NMOS and enhancement for PMOS!

Example for Modeling of Technology and Layout dependent Effects (I): Webbing/Dog-bone Effect for Narrow-Short Devices

Diffusion

STI
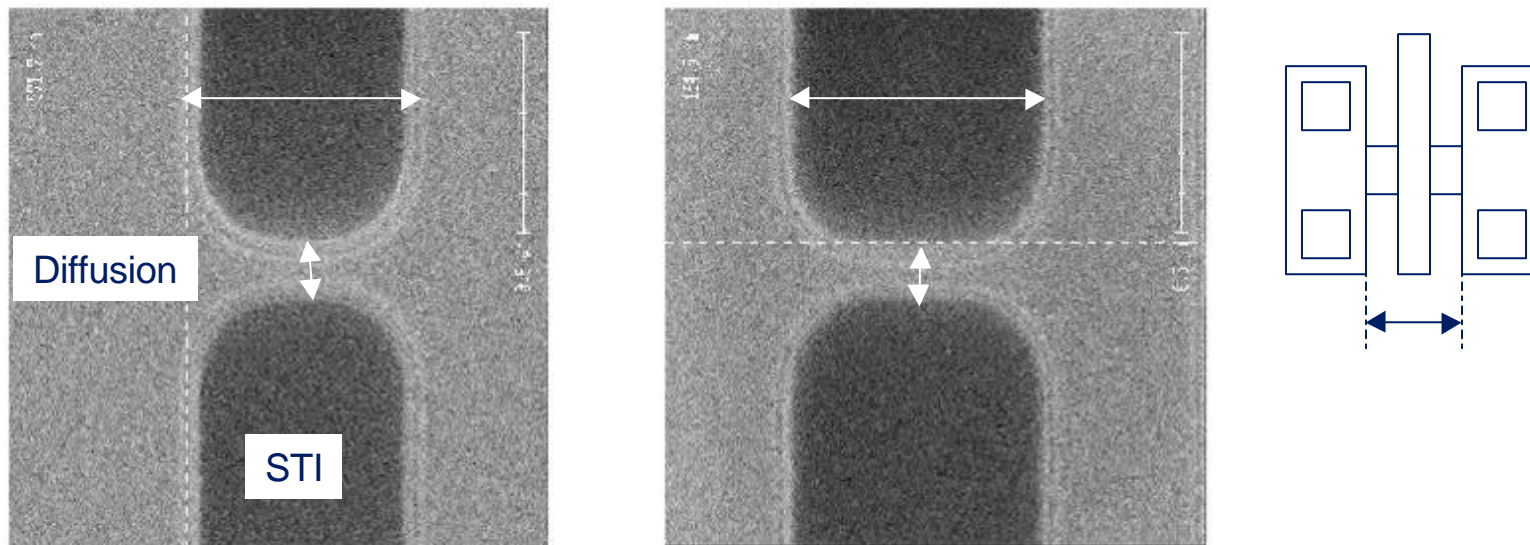
If the distance of active areas to poly gates shrinks then the effective channel widths will be increased due to webbing/dog-bone effect (corner rounding), especially for narrow-short devices.

Dedicated SPICE models have to be generated for SRAM devices, including specific narrow-short layout and isolated-nested effects.

High-energy well implant

Resist

NWell

STI

N⁺

N⁺

PWell

NWell

Distance NWell
Active Area

Effect dependent on:
- Device orientation
- Distance well edge to active area of device

The well implant causes lateral scattering of boron atoms out off the resist, which leads to threshold voltage increase for devices close to the well edge. Well proximity effect on NFET ΔVth $\approx$ +50mV and PFET ΔVth $\approx$ +20mV dependent on fab and process flow.

Parameterized SPICE well proximity macro models consist of subcircuits which use instance parameters considering distances of devices to well edges.

STI-Stress Effect

Influence of STI-Stress on NMOS Device

NMOS_W/L=10/0.12μm_Meas.
NMOS_W/L=10/0.12μm_Sim.

PC-STI

Mechanical stress due to shallow trench isolation (STI) causes drain current degradation (mobility reduction and threshold voltage increase) for devices with small PC-STI distances. The STI-stress effect is most sensitive on short channel devices and less sensitive for small or long channel devices, which differs from NFET (up to -15% in I_{ON} & ΔVth≈+40mV) to PFET (small impact).

Parameterized SPICE STI-stress macro models consist of subcircuits which use instance parameters considering the distances of the STI to poly gates.

Modeling Challenges: Increasing Compact Model Complexity

- BSIM4 (BSIM3v3) MOSFET model specific problems

    - Trade-off: "physicality" <−> accuracy
    ⇨ Use of (selected) non-physical binning parameters essential to maintain high accuracy levels (especially for narrow-short devices, width scaling)

    - Correlation between long and short channel parameters
    ⇨ BSIM4 model parameter extraction procedure becomes complicated

    - Not correctly and insufficient modeled physical effects
    ⇨ Channel length/doping dependent mobility model needed for halo/pocket technologies (conclusion: a new mobility model is required!)

Modeled physical effects:	BSIM3v3.x	BSIM4.x
halo implantation	−	✓
poly gate depletion	✓	✓
gate leakage current	−	✓
GIDL	−	✓
quantum effects	− (✓*)	✓
proximity effects	✓	✓
mechanical stress effect	−	✓**

# of parameters:
(for a single device without extra model binning parameters)

BSIM3v3.0: ~100

BSIM3v3.2: ~150

BSIM4.2:   ~200

BSIM4.3:   ~220

* in BSIM3v3.2 for CV-model (CTM) only   ** only at BSIM4.3

- **The next BSIM4.3 version contains:**

- Mechanical stress effect model due to STI

- Unified current-saturation model accounts for velocity overshoot as well as source injection thermal velocity limit

- Improved threshold voltage modeling for active well concepts

- New physical charge and capacitance model
  - ⇨ Improved symmetry (solves asymmetry) and reciprocity
  - ⇨ Fix for negative capacitance values
  - ⇨ Improves IV accuracy and predictivity

- Improved long channel threshold voltage roll-up modeling
- Provide hand-calculation friendly equations

Infineon technologies

Never stop thinking


```
Temp.  :25                    VTH_meas vs L
1.00                                                        o  o o
                                                              Meas.
    Method: Vg(Id = 20  nA W/L)        Wdraw      = 10.00
    Type    : PMO                      VDS        =-0.050    ____
0.90                                   VBS start  = 0.000    Sim.
                                       VBS step   = 0.360
0.80                                   Rms error  = 3.293
                                       Ave error  = 1.836
                                       Max error  = 12.83
0.70
0.60
0.50
0.40
    0.00   2.00   4.00   6.00   8.00  10.00  12.00
13:7 :59                    Ldraw (Microns)
FEB/2 /1  v.16.11.2                          SILVACO International
```

−VTH (V)

PF: Vth_lin vs. L with different Vbs

Long distance Vth-roll-up (RSCE) can not be modeled!
$\Delta Vth_{RSCE\_longL}=Vth_{2um}-Vth_{10um}\sim100mV$
This Vth shift, for longer channel lengths, caused by strong halo implantation and have been observed for buried channel devices.

RSCE modeling proposal: New parameter *LPEL* should be introduced to increase RSCE sensitivity for long channel devices, with a default value of 0.0m!

$$?Vth_{(RSCE)}=\sqrt{1+\frac{LPEB}{Leff}}\cdot K1\cdot(\sqrt{(f_S-V_{BS})}-\sqrt{f_S})+K1(\sqrt{1+\frac{LPEO}{Leff}-LPEL\cdot Leff}-1)\sqrt{f_S}$$

BSIM4 Summary

- I-V accuracy significantly improved for halo implanted devices

- Good results with gate direct tunneling current model obtained

- BSIM4 parameter extraction procedure more complicated (correlation between long and short channel parameters)

- # Model parameters ~ 220 (more than 60 new BSIM4 parameters)

- BSIM4 can be up to factor 2 slower than BSIM3v3 (if external source/drain series resistances will be used, i.e. 6 terminal device)

- Still known problems with symmetrical charge formulation (negative capacitance values related to bulk charge can arise)

- Poly gate depletion modeling only for surface-channel devices

- BSIM4 accounts for most currently know physical device effects

- For specific layout dependent effects (e.g. STI-Stress) own macro models have to be generated