A Wideband 2.4-GHz Delta-Sigma Fractional-N PLL With 1-Mb/s In-Loop Modulation

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***Abstract*—A phase noise cancellation technique and a charge pump linearization technique, both of which are insensitive to component errors, are presented and demonstrated as enabling components in a wideband CMOS delta-sigma fractional-N phase-locked loop (PLL). The PLL has a loop bandwidth of 460 kHz and is capable of 1-Mb/s in-loop FSK modulation at center frequencies of $2402 + k$ MHz for $k = 0, 1, 2, \ldots, 78$. For each frequency, measured results indicate that the peak spot phase noise reduction achieved by the phase noise cancellation technique is 16 dB or better, and the minimum suppression of fractional spurious tones achieved by the charge pump linearization technique is 8 dB or better. With both techniques enabled, the PLL achieves a worst-case phase noise of -121 dBc/Hz at 3-MHz offsets, and a worst-case in-band noise floor of -96 dBc/Hz. The PLL circuitry consumes 34.4 mA from 1.8–2.2-V supplies. The IC is realized in a 0.18-μm mixed-signal CMOS process, and has a die size of 2.72 mm $\times$ 2.47 mm.**

***Index Terms*—Bluetooth, delta-sigma, fractional-N, frequency synthesizer, in-loop modulation, phase-locked loop (PLL).**

I. Introduction

THIS PAPER presents a phase noise cancellation technique that relaxes the fundamental tradeoff between phase noise and bandwidth in conventional delta-sigma ($\Delta\Sigma$) fractional-N phase-locked loops (PLLs), and a charge pump linearization technique that improves the spurious performance of wideband fractional-N PLLs. Together, the techniques make it practical to significantly increase the bandwidth of $\Delta\Sigma$ fractional-N PLLs without degrading phase noise and spurious performance. They are demonstrated in a CMOS $\Delta\Sigma$ fractional-N PLL that can be configured as a Bluetooth-compliant wireless local-area network (LAN) transmitter and a local oscillator for a direct conversion Bluetooth-compliant receiver. The techniques enable the PLL to achieve the required phase noise and spurious performance specifications with a bandwidth of 460 kHz, which is sufficiently wide to allow in-loop modulation of the required 1-Mb/s transmit signal. Moreover, the wide bandwidth significantly reduces the susceptibility of the voltage-controlled oscillator (VCO) to pulling, and causes the PLL phase noise arising from $1/f$ noise and $1/f^3$ noise in the VCO to be largely attenuated [1], [2]. The phase noise cancellation technique avoids many of the problems faced by the other reported methods of in-loop modulation. Unlike narrow-bandwidth methods such as digital pre-emphasis of the modulation signal and two-point modulation, it is not sensitive to analog component errors and does not require calibration [3]–[6]. Unlike other wide-bandwidth methods, it is not sensitive to timing delay errors in multiphase fractional dividers and it does not require a Type-1 PLL and the associated phase detector complications [7]–[9]. The benefit of the charge pump linearization technique is that it does not require dynamic bias adjustment, so its bandwidth is not limited by an analog feedback circuit [10]. Although the two techniques complement each other in that they both enhance performance in wideband $\Delta\Sigma$ fractional-N PLLs, they are independent and each can be applied in the absence of the other.

A high-level block diagram of the implemented PLL is shown in Fig. 1. It differs from a conventional $\Delta\Sigma$ fractional-N PLL in that the dark gray blocks have been added to implement the phase noise cancellation technique, and the charge pump and phase-frequency detector (PFD) blocks have been modified from their conventional forms to implement the charge pump linearization technique. The details of the PLL are described throughout the remainder of the paper. Sections II and III describe the signal processing details of the phase noise cancellation technique and the charge pump linearization technique, respectively. Section IV presents circuit details, and Section V presents measurement results.

II. Phase Noise Cancellation Technique

A. Problems With Conventional Fractional-N PLLs

The core of a typical fractional-N PLL is shown in Fig. 2. It consists of a PFD, a charge pump, a loop filter, a VCO, and a frequency divider. The divider output, $v_{\rm div}(t)$, is a two level signal in which the nth and $(n+1)$th rising edges are separated by $N + y[n]$ periods of the VCO output, for $n = 1, 2, 3, \ldots$, where N is a constant integer, and $y[n]$ is a sequence of integers generated by digital logic not shown in the figure. As indicated in the figure for the case where the PLL is locked, if the nth rising edge of the reference signal, $v_{\rm ref}(t)$, occurs before that of $v_{\rm div}(t)$, the charge pump generates a current pulse of nominal amplitude ICP and a duration equal to the time difference between the two edges. Otherwise, the situation is similar except the polarity of the current pulse is reversed.

If $y[n]$ could be set to any desired value between -1 and 1, say, α, then the output frequency of the PLL would settle to $(N+\alpha)f_{\rm ref}$, so it would be possible to achieve any output frequency between $(N-1)f_{\rm ref}$ and $(N+1)f_{\rm ref}$. Unfortunately, $y[n]$ is restricted to integer values because the divider simply counts

Manuscript received January 17, 2003; revised September 24, 2003. This work was supported by the National Science Foundation under Grant CCR-0073552 and by the University of California Communications Research Program under Grant CORE00-10069.

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Digital Object Identifier 10.1109/JSSC.2003.820858

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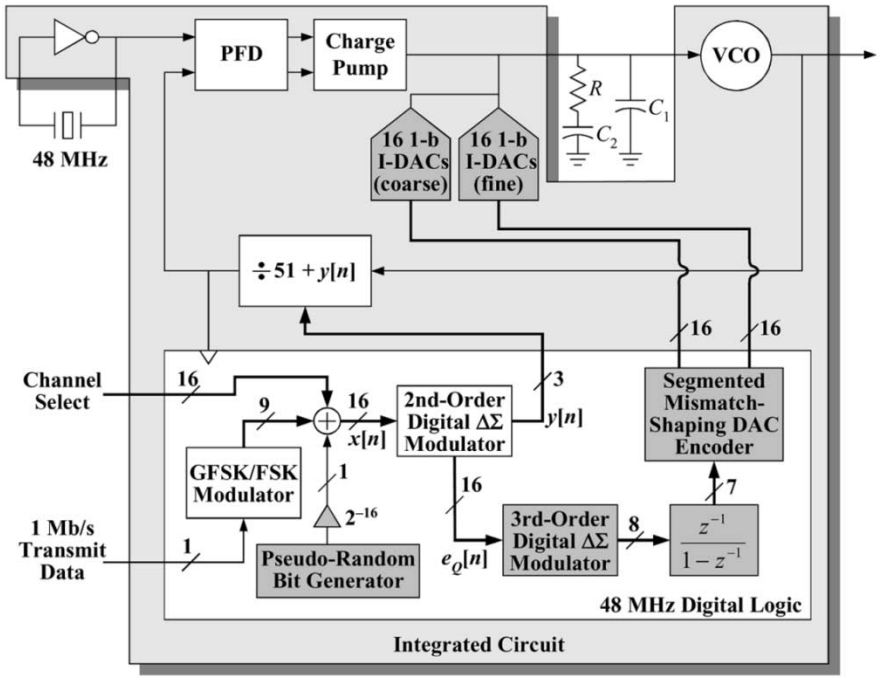

Fig. 1. High-level functional diagram of the implemented $\Delta\Sigma$ fractional-N PLL.

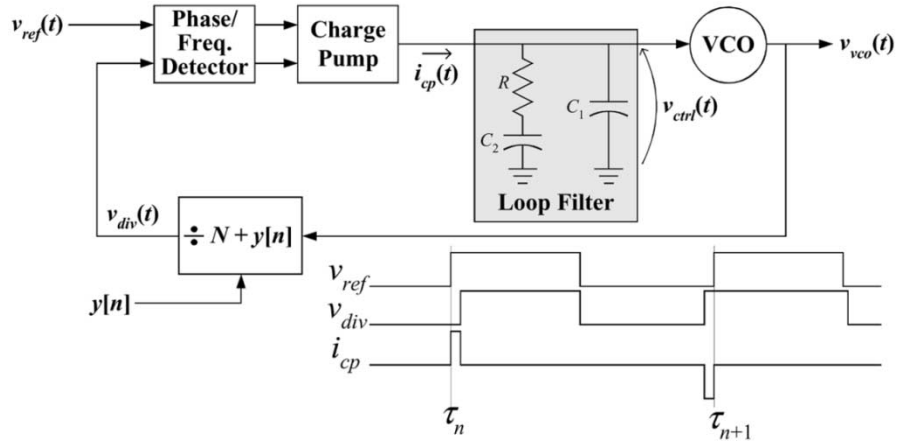

Fig. 2. Core of a typical fractional-N PLL.

rising VCO edges. However, $y[n]$ can be a sequence of integer values that *average* to α. Such a sequence can be written as $y[n] = \alpha + e_Q[n]$, where $e_Q[n]$ is zero-mean quantization noise caused by using integer values in place of the ideal fractional value. In this case, the PLL output frequency settles to $(N + \alpha)f_{\text{ref}}$ as desired, although a price is paid in terms of added phase noise.

As shown in [11], in terms of the effect it has on the PLL phase noise, the quantization noise can be modeled as a sequence of additive charge samples, $Q_Q[n]$, that get injected into the loop filter once every reference period. Neglecting a constant offset associated with the initial conditions of the loop filter, it can be shown that $Q_Q[n]$ is well modeled as

$$Q_Q[n] = T_{\text{VCO}} I_{\text{CP}} \sum_{k=n_0}^{n-1} e_Q[k] \tag{1}$$

where T_{VCO} is the period of the VCO output, and $n_0 < n$ is an arbitrary initial time index. The PLL acts on this sequence as a low-pass filter in the process of converting it to output phase noise. Therefore, spectral components of $e_Q[n]$ outside the bandwidth of the PLL are suppressed, but those inside the bandwidth of the PLL are amplified through the discrete-time integration in (1) and can add significantly to the overall phase noise of the PLL.

In early fractional-N PLLs, the problem of suppressing the PLL phase noise that would otherwise result from $e_Q[n]$ has been addressed using a DAC cancellation path to suppress $Q_Q[n]$ [12], [13]. Because $y[n]$ is generated digitally, $-Q_Q[n]$ can be calculated by digital circuitry, converted by a DAC to an analog current, and added to the output of the charge pump. If the DAC has sufficient precision and the correct gain, the added signal nearly cancels the component of the charge

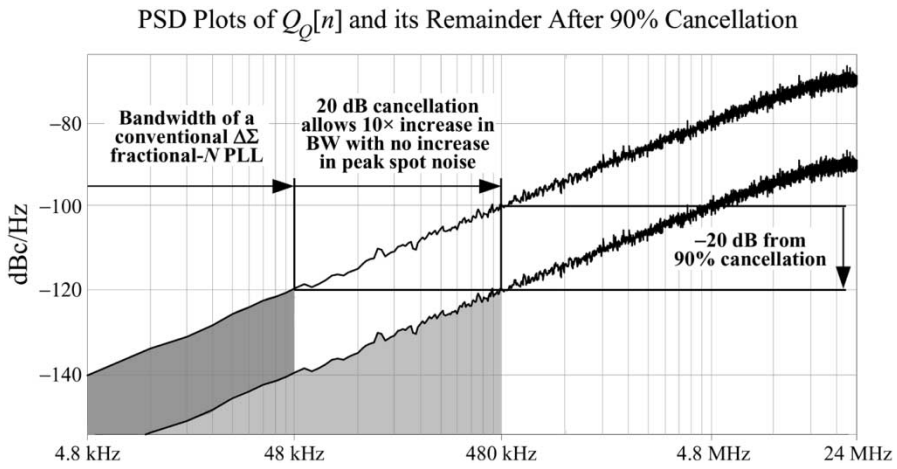

Fig. 3. Illustration of how the cancellation process increases the useable PLL bandwidth.

pump output corresponding to $Q_Q[n]$. In most fractional-N PLLs of this type, $y[n]$ is generated using one or two digital error-accumulator structures designed to ensure that the sum of $e_Q[n]$ in (1) is bounded. The resulting $Q_Q[n]$ sequence tends to have a large dynamic range, a high spurious tone content, and significant spectral power within the PLL bandwidth. Therefore, excellent cancellation accuracy is required; if $Q_Q[n]$ is only partially cancelled because of gain errors, distortion, or insufficient dynamic range in the DAC cancellation path, the remaining portion of $Q_Q[n]$ contains in-band noise and spurious tones which can contribute significant phase noise [14], [15]. Consequently, the approach has been used mainly in high-cost applications such as test and measurement equipment wherein component trimming and calibration are practical.

A more recent technique that circumvents the DAC precision and gain matching problems uses a digital $\Delta\Sigma$ modulator with at least second-order quantization noise shaping to generate $y[n]$ such that $Q_Q[n]$ has at least one zero at dc with most of its power concentrated at high frequencies, outside the passband of the PLL [16]–[18]. Provided the bandwidth of the PLL is sufficiently narrow, most of the quantization noise is suppressed by the PLL so a DAC cancellation path is not necessary. Such PLLs have come to be known as $\Delta\Sigma$ fractional-N PLLs, and have become widely used in consumer-oriented communication devices over the last decade. Nevertheless, the need to suppress out-of-band quantization noise imposes a fundamental bandwidth versus phase noise tradeoff in $\Delta\Sigma$ fractional-N PLLs that causes problems in many applications.

One such problem is VCO pulling. For example, when a narrowband PLL is used to provide the RF local oscillator for a direct conversion transmitter, even a small amount of parasitic coupling of the transmitted signal to the VCO circuitry tends to corrupt or *pull* the VCO output which, in turn, causes the upconverted transmit signal to be distorted. However, if the bandwidth of the PLL is at least comparable to the modulation bandwidth, the PLL is much less susceptible to this problem because the feedback within the PLL tends to fight the corrupting effects of the modulated transmit signal.

Another problem with narrowband fractional-N PLLs is that they often preclude in-loop VCO modulation for direct synthesis of frequency modulated transmit signals. In principle, such signals can be generated directly by a $\Delta\Sigma$ fractional-N PLL, thereby eliminating the need for conventional upconversion stages and much of the attendant analog circuitry. Specifically, if α in the discussion above is replaced by $\alpha + x_m[n]$, where $x_m[n]$ is a zero-mean modulation sequence, the resulting PLL output has a center frequency of $(N + \alpha)f_{\rm ref}$ but is frequency modulated by a low-pass filtered version of $x_m[n]f_{\rm ref}$. The PLL must have a sufficiently narrow bandwidth to suppress the phase noise, yet must have a sufficiently wide bandwidth to accommodate the VCO modulation. In many applications, such as the Bluetooth transmitter application used as a demonstration vehicle in this work, it is not possible to simultaneously satisfy both of these requirements using conventional techniques.

B. Phase Noise Cancellation Technique Overview

As shown in Fig. 1, the phase noise cancellation technique combines the two fractional-N PLL approaches described above. A second-order digital $\Delta\Sigma$ modulator generates $y[n]$ as in a conventional $\Delta\Sigma$ fractional-N PLL, and a DAC cancellation path attenuates $Q_Q[n]$. As explained below, the combination of the two approaches, in conjunction with quantization noise-shaping, mismatch noise-shaping, and 1-bit dither, greatly reduces the respective limitations suffered by each approach in isolation.

Fig. 3 illustrates that combining the two approaches makes it possible to widen the PLL bandwidth relative to that of a conventional $\Delta\Sigma$ fractional-N PLL without increasing the peak spot phase noise. The top curve in the figure represents a power spectral density (PSD) plot of $Q_Q[n]$ scaled by the dc value of the PLL phase transfer function between $Q_Q[n]$ and the PLL output, so its units are dBc/Hz referred to the PLL output. The bottom curve represents the PSD, also in units of dBc/Hz referred to the PLL output, of the portion of $Q_Q[n]$ that remains after cancellation where the DAC cancellation path has a 10% gain error but is otherwise ideal. Suppose, as an example, that the peak spot phase noise resulting from quantization noise is to be limited to -120 dBc/Hz. Without the DAC cancellation path, i.e., in the case of a conventional $\Delta\Sigma$ fractional-N PLL, it can be seen from the top curve in the figure that the bandwidth of the PLL would have to be limited to 48 kHz. In contrast, it

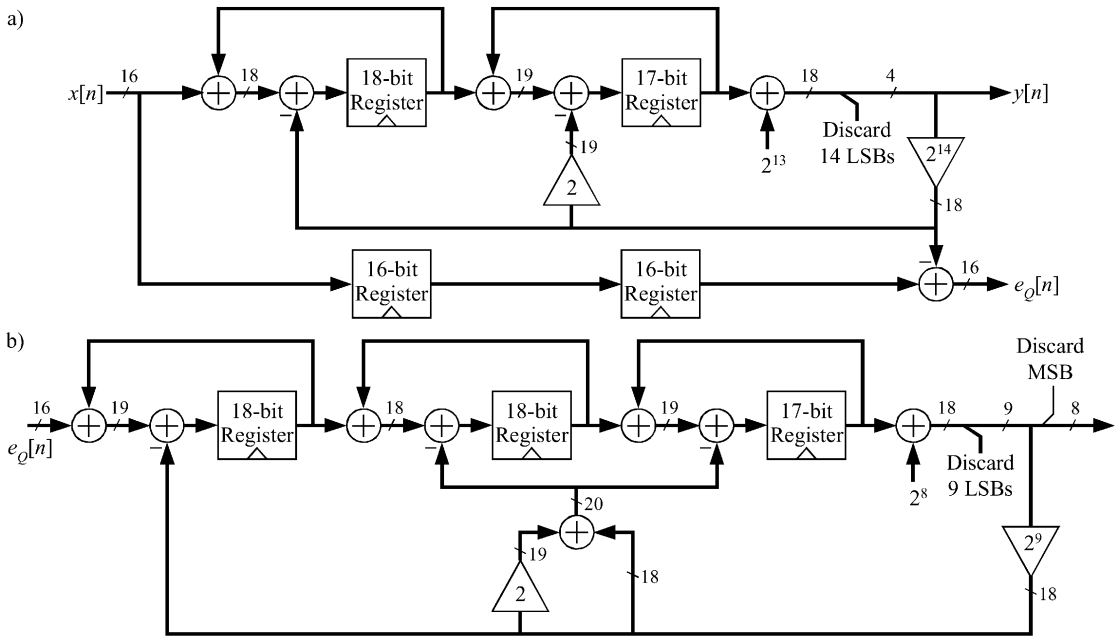

Fig. 4. (a) Details of the second-order $\Delta\Sigma$ modulator. (b) Details of the third-order $\Delta\Sigma$ modulator.

can be seen from the bottom curve in the figure that with the DAC cancellation path the bandwidth of the PLL can be set to 480 kHz. Thus, even with a 10% gain error in the DAC cancellation path, the bandwidth of the PLL can be increased by a factor of 10 without increasing the peak spot phase noise of the PLL.

While combining the two fractional-N PLL approaches relaxes both the bandwidth versus phase noise tradeoff and the required gain accuracy in the DAC cancellation path relative to the two approaches, respectively, in isolation, it does not reduce the dynamic range and linearity requirements of the DAC cancellation path. Furthermore, $Q_Q[n]$ must be nearly free of spurious tones, or else high gain-accuracy would again be required in the DAC cancellation path to properly cancel the spurious tones. While some architectures that combine the two fractional-N PLL approaches have been reported [19]–[22], none satisfactorily address all of these problems, thereby limiting the phase noise cancellation accuracy and limiting applicability to either low-bandwidth or low-performance fractional-N PLLs. These problems are addressed in the implemented PLL by several means. As described in detail below, delta-sigma requantization and a segmented mismatch-shaping current pulse DAC are used to obtain high DAC cancellation path dynamic range and linearity, and 1-bit dithering is used to eliminate spurious tones.

C. Phase Noise Cancellation Technique Signal Processing Details

As shown in Fig. 1, the architecture consists of a 48-MHz crystal reference source, the PLL core described above, a 48-MHz digital section, a bank of 16 coarse 1-bit current pulse DACs, and a bank of 16 fine 1-bit current pulse DACs. The 48-MHz digital section consists of digital logic in which all registers are clocked on the rising edges of the divider output. It generates $y[n]$ and 32 1-bit sequences that control the two banks of 1-bit current pulse DACs. During each reference period, each 1-bit current pulse DAC generates a positive or negative pulse of current depending upon whether its input bit is high or low. Each pulse has a duration of four VCO periods. The nominal magnitudes of the current pulses are $I_{\rm CP}/16$ and $I_{\rm CP}/128$ for the coarse and fine 1-bit current pulse DACs, respectively.

The input to the second-order $\Delta\Sigma$ modulator, $x[n]$, is a 16-bit two's complement number in the range -1 to 1 of the form $x[n] = \alpha + x_m[n] + d[n]$, where $\alpha = (k - 46)/48$ selects the desired Bluetooth channel frequency for $k = 0, 1, \ldots, 78$, $x_m[n]$ is optional FSK or GFSK modulation, and $d[n]$ is a 1-bit pseudorandom dither sequence. The dither sequence is generated by an on-chip length-22 linear feedback shift register and is scaled such that it represents the least significant bit (LSB) of $x[n]$. The details of the second-order $\Delta\Sigma$ modulator are shown in Fig. 4(a). It has unity gain and a quantization step size of unity, so its output has the form $y[n] = x[n-2] + e_Q[n]$, and takes on values in the range: -2, -1, 0, 1, 2.

In most conventional PLLs with DAC cancellation paths, either dither is not used or the $\Delta\Sigma$ modulator has only two output levels [19]–[22]. In either case, $e_Q[n]$ can have significant spurious tones. In the current work, as proven in [23] and [24], the 1-bit dither sequence, $d[n]$, completely eliminates spurious tones in $e_Q[n]$, so $e_Q[n]$ has the same PSD as white noise passed through a discrete-time filter with two zeros at dc. The discrete-time integration in (1) cancels one of the zeros, so $Q_Q[n]$ has the first-order shaped PSD represented by the top curve in Fig. 3. Although the dither behaves as white noise, its magnitude is sufficiently small that its contribution to the PLL phase noise is negligible in the band of interest.

Ideally, the DAC cancellation path would digitally integrate $e_Q[n]$ to obtain $Q_Q[n]$ as in (1), and, for each n, inject a current pulse into the loop filter with a width equal to that of the corresponding current pulse from the charge pump and an amplitude chosen such that the total charge carried by the pulse is precisely

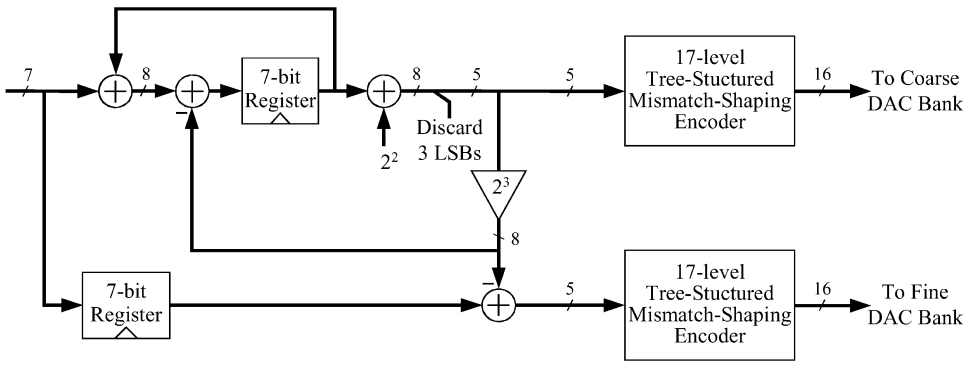

Fig. 5. Details of the mismatch-shaping digital encoder.

$Q_Q[n]$. Unfortunately, this is difficult to accomplish in practice because the precise width of the charge pump pulse is not known *a priori*, and the pulse can be very narrow. Instead, a fixed-width current pulse can be used. In this case, $Q_Q[n]$ is not cancelled immediately as it is added, so the cancellation process introduces a voltage transient each period at the VCO input. Most of the power associated with the voltage transient is outside of the PLL bandwidth, so its contribution to the PLL phase noise tends to be small. In most conventional PLLs with DAC cancellation paths, the pulsewidth is equal to the reference period [19], [20]. However, in the current work the pulsewidth is set to four VCO periods to better match the charge pump pulsewidth, thereby reducing the transient at the VCO and decreasing the resulting PLL phase noise contribution.

If $Q_Q[n]$ were calculated directly using $e_Q[n]$ in (1), a 15-bit current DAC with a step size of $0.5 \cdot I_{\rm CP} \cdot 2^{-15}$, e.g., 19.5 nA for the implemented PLL, would be required to generate the necessary current pulses. Such a DAC would be very difficult to implement. In most conventional PLLs with DAC cancellation paths, $e_Q[n]$ is simply truncated to make the implementation of the DAC feasible [19]. Unfortunately, truncation causes a portion of the power of $e_Q[n]$ to fold in-band and introduces spurious tones which adversely affects the phase noise cancellation. In the current work, as indicated in Fig. 1, $e_Q[n]$ is requantized from 16 bits to 8 bits by a third-order digital $\Delta\Sigma$ modulator, the details of which are shown in Fig. 4(b), and the result is digitally integrated and converted to current pulses. The output of the integrator is a 7-bit sequence proportional to $Q_Q[n-1]+e_{\rm rq}[n]$, where $e_{\rm rq}[n]$ is second-order shaped requantization noise resulting from digitally integrating the requantization noise from the third-order digital $\Delta\Sigma$ modulator. Because of its second-order high-pass shape and small magnitude, $e_{\rm rq}[n]$ does not result in a significant increase in the PLL phase noise. Thus, requantization reduces the problem of designing a 15-bit DAC with a minimum step size of 19.5 nA to that of designing a 7-bit DAC with a minimum step size of 10 μA. The DAC is implemented by the two banks of 1-bit current pulse DACs. During the nth reference period, the input bits to the 1-bit DACs are chosen such that

$$v[n] = \left[8 \cdot \sum_{k=1}^{16} \left(v_{c_k}[n] - \frac{1}{2} \right) + \sum_{k=1}^{16} \left(v_{f_k}[n] - \frac{1}{2} \right) \right] \Delta_v \tag{2}$$

where $v[n]$ is the output of the digital integrator, $v_{c_k}[n]$ and $v_{f_k}[n]$ are 0 or 1 input values to the kth 1-bit DACs in the coarse and fine DAC banks, respectively, and Δ_v is the LSB weight of $v[n]$.

For most values of $v[n]$, there are several combinations of $v_{c_k}[n]$ and $v_{f_k}[n]$ that satisfy (2). For example, when $v[n] = -63\Delta_v$, any one of the 16 1-bit DAC inputs in each DAC bank can be set to 1 with the rest set to 0. To the extent that the 1-bit DACs in each DAC bank are perfectly matched and the ratio between coarse and fine 1-bit DACs is exactly 8, it does not matter which of the possible input selections is made. In conventional segmented DACs, good matching is assumed, so for each value of $v[n]$ only one of the combinations of $v_{c_k}[n]$ and $v_{f_k}[n]$ that satisfy (2) is ever used. Unfortunately, if the conventional approach had been used in this work, even mismatches of less than 1% among the unit current sources that make up the 1-bit DACs would give rise to harmonic distortion severe enough to prevent the PLL from meeting the target specifications, and reducing the mismatches to much less than 1% in present CMOS technology can be difficult. To circumvent this problem, a segmented mismatch-shaping DAC encoder is used prior to the banks of 1-bit DACs [25]–[27].

During the nth reference period, the encoder selects one of the combinations of $v_{c_k}[n]$ and $v_{f_k}[n]$ that satisfy (2) as a function of $v[n]$ such that the error from mismatches introduced by the DAC, referred to as mismatch noise, has first-order high-pass spectral shaping with no spurious tones. Consequently, much of the mismatch-noise power is outside the PLL bandwidth. For the implemented PLL, simulations indicate that the target specifications can be met provided the matching of the unit current sources has a standard deviation of no more than 5% which is not difficult to achieve in practice. As shown in Fig. 5, the encoder consists of a first-order digital $\Delta\Sigma$ modulator and two 17-level tree-structured mismatch-shaping encoders of the type presented in [28]. The $\Delta\Sigma$ modulator quantizes $v[n]$ to a 17-level sequence which drives the 17-level mismatch-shaping encoder associated with the coarse DAC bank. The quantization noise from the $\Delta\Sigma$ modulator drives the 17-level mismatch-shaping encoder associated with the fine DAC bank.

Fig. 6 shows simulated output phase noise PSD plots corresponding to quantization noise and mismatch-noise for the implemented PLL with various DAC cancellation path gain error levels. The results were generated by an event-driven simulator that accurately models both the discrete-time and

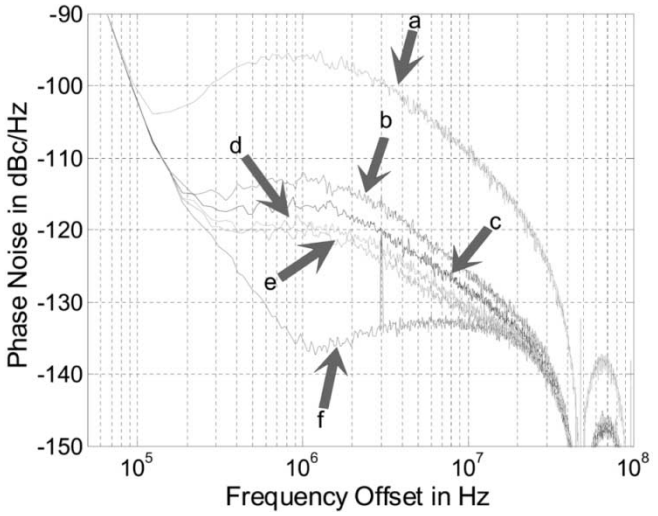

Fig. 6. Simulated output phase noise PSD plots of the implemented PLL. (a) Without the phase noise cancellation technique. (b)–(e) With the phase noise cancellation technique, 5% unit current source errors in the 1-bit DACs, and 12%, 8%, 4%, and 0% gain mismatches, respectively. (f) With ideal phase noise cancellation.

continuous-time portions of the system. The unit current source values in the 1-bit current pulse DACs were chosen with random errors such that they have a 5% standard deviation from their nominal value. As indicated in the figure, even with a 8% DAC cancellation path gain error and the relatively poor current source matching (curve "c" in the figure), the phase noise cancellation technique reduces the peak spot phase noise by 20 dB, and the spot phase noise at a 3-MHz offset from the carrier is below the -120-dBc/Hz value required by the Bluetooth specification.

While the phase noise cancellation technique described above makes it feasible to widen the PLL bandwidth without increasing the spot phase noise resulting from quantization noise, it should be noted that widening the PLL bandwidth may cause other noise sources to become dominant. Specifically, the noise from the reference oscillator, charge pump, PFD, and frequency divider must also be sufficiently low for the application. In a wide-bandwidth $\Delta\Sigma$ fractional-N PLL, this can be a nontrivial task owing to the reduced attenuation from the loop filter.

III. Charge Pump Linearization Technique

A. The Problem

A conventional charge pump and the associated timing diagram are shown in Fig. 7. The rising edges of the PFD outputs, U and D, are triggered by those of $v_{\rm ref}(t)$ and $v_{\rm div}(t)$, respectively. The falling edges of U and D both occur after a delay of T_D following the later of the rising edges of $v_{\rm ref}(t)$ and $v_{\rm div}(t)$. The delay ensures that each current source in the charge pump is turned on for a minimum duration of T_D every reference period to solve the charge pump dead-zone problem [29]. The positive and negative current sources in the charge pump are on when U and D, respectively, are high and are off otherwise.

Ideally, $I_{\rm CP+}$ and $I_{\rm CP-}$ are equal, but in practice they can differ significantly because the current sources have finite

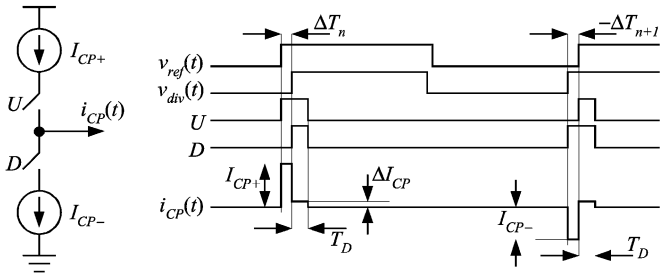

Fig. 7. Conventional charge pump and the associated timing diagram.

output impedances and the voltages they drop differ from each other as a function of the VCO control voltage. Component mismatches resulting from fabrication inaccuracies tend to add to the difference between $I_{\rm CP+}$ and $I_{\rm CP-}$, although usually to a much lesser extent. In general, the current source values can be written as

$$I_{\rm CP+} = I_{\rm CP} + \frac{\Delta I_{\rm CP}}{2} \quad \text{and} \quad I_{\rm CP-} = I_{\rm CP} - \frac{\Delta I_{\rm CP}}{2} \tag{3}$$

where $I_{\rm CP}$ and $\Delta I_{\rm CP}$ are the average of and difference between $I_{\rm CP+}$ and $I_{\rm CP-}$, respectively.

It follows from the timing diagram in Fig. 7 that the charge carried by $i_{\rm CP}(t)$ during the nth reference period is

$$Q_{\rm CP}[n] = \Delta T_n I_{\rm CP} + T_D \Delta I_{\rm CP} + |\Delta T_n| \frac{\Delta I_{\rm CP}}{2} \tag{4}$$

where ΔT_n is the time difference between the nth rising edges of $v_{\rm div}(t)$ and $v_{\rm ref}(t)$. The first term in (4) is the desired component. The second two terms represent error resulting from imperfect matching of $I_{\rm CP+}$ and $I_{\rm CP-}$. The first of these error terms is just a constant, so it has no effect on the PLL phase noise aside from introducing a small constant offset. Unfortunately, the second of the error terms is nonlinear with respect to ΔT_n.

The nonlinearity induces spurious tones at multiples of $\alpha f_{\rm ref}$ in the PLL phase noise. While this effect has been reported previously [30], a theoretical proof of the generation of spurious tones, particularly when dither is used as shown in Fig. 1, is not yet available. In qualitative terms, the nonlinearity causes spurious tones because of the dependence of ΔT_n on the running sum of $(y[n] - \alpha)$. As shown in [11]

$$\Delta T_n = T_{\rm VCO} \sum_{k=n_0}^{n-1} (y[k] - \alpha) + T_{\rm VCO} \frac{\phi(t_n)}{2\pi}$$

where $\phi(t_n)$ is the excess phase of the VCO approximately at the time of the nth divider output rising edge. Behavioral simulations of the absolute value nonlinearity shown in (4) both in the context of the fractional-N PLL and acting just on the running sum of $(y[n] - \alpha)$ have confirmed the generation of spurious tones. The problem becomes increasingly severe as the bandwidth of the PLL is increased, because spurious tones that are well out of band and, thus, highly attenuated in a narrowband PLL are less out of band, and, thus, less attenuated in a wideband PLL. A conventional solution is to use analog feedback to equalize $I_{\rm CP+}$ and $I_{\rm CP-}$ [10]. However, in a wideband PLL, the charge pump output voltage variations tend to be very abrupt, which makes the design of an effective analog compensation circuit difficult.

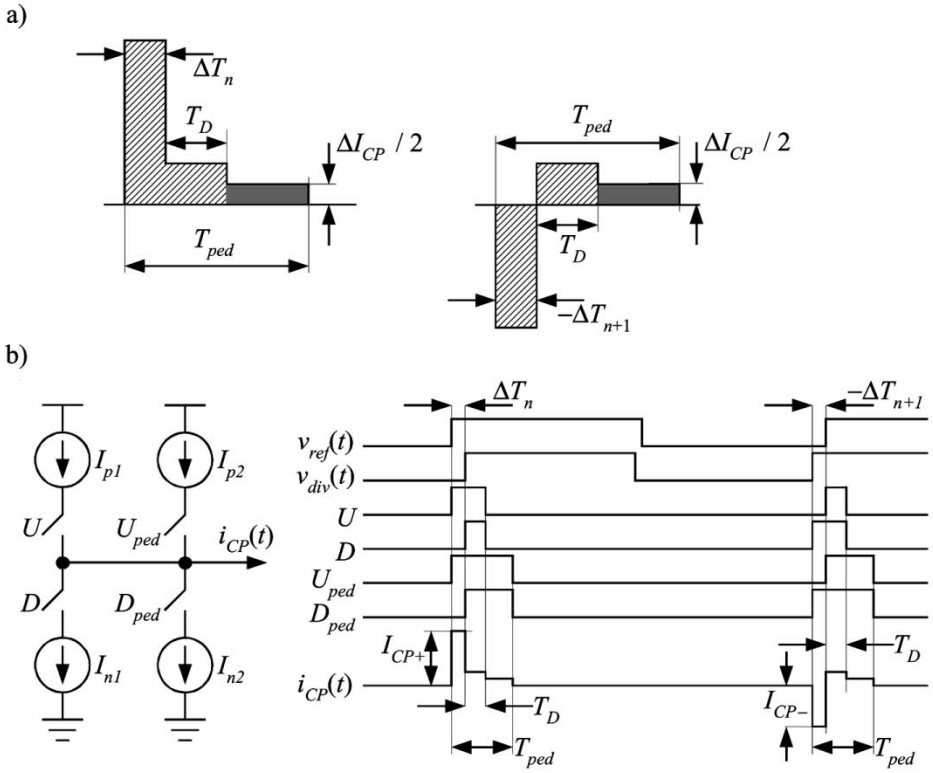

Fig. 8. (a) Representations of positive and negative charge pump output current pulses using the charge pump linearization technique. The hatched portion of each pulse is the same as generated by the conventional charge pump shown in Fig. 7, and the shaded portion is additional current introduced by the charge pump linearization technique. (b) The modified charge pump and the associated timing diagram.

B. Proposed Technique

The idea behind the charge pump linearization technique is illustrated in Fig. 8(a), which shows two representative charge pump pulses. The hatched portions of the pulses are identical to the current pulses generated by the conventional charge pump shown in Fig. 7. The shaded portions of the pulses represent additional current introduced by the charge pump linearization technique. As indicated in the figure, the total charge carried by the shaded portion of each pulse is

$$(T_{\rm ped} - T_D - |\Delta T_n|)\frac{\Delta I_{\rm CP}}{2}$$

where $T_{\rm ped}$ is a constant referred to as the pedestal time. Thus, the charge carried by the extra current introduced by the charge pump linearization technique cancels the nonlinear term in (4).

Implementation of the technique involves modifications to both the PFD and the charge pump. The modified PFD generates U and D signals as in the conventional case, but also generates two new signals, $U_{\rm ped}$ and $D_{\rm ped}$. As shown in Fig. 8(b), each reference period the rising edges of $U_{\rm ped}$ and $D_{\rm ped}$ are aligned with those of U and D, respectively, but their falling edges both occur after a delay of $T_{\rm ped}$ following the earlier of the rising edges of $v_{\rm ref}(t)$ and $v_{\rm div}(t)$. The charge pump is modified in that the $I_{\rm CP+}$ and $I_{\rm CP-}$ current sources are each split into two nominally identical half-sized current sources

$$I_{p1} = \frac{I_{\rm CP+} + \Delta I_p}{2}, \quad I_{p2} = \frac{I_{\rm CP+} - \Delta I_p}{2}$$
$$I_{n1} = \frac{I_{\rm CP-} + \Delta I_n}{2}, \quad I_{n2} = \frac{I_{\rm CP-} - \Delta I_n}{2} \qquad (5)$$

where ΔI_p and ΔI_n are differences arising from component mismatches between the values of the two positive and the two negative current source halves, respectively. The I_{p1} and I_{p2} current sources are switched by U and $U_{\rm ped}$, and the I_{n1} and I_{n2} current sources are switched by D and $D_{\rm ped}$. The duration, $T_{\rm ped}$, is designed to be longer than the maximum value of $|\Delta T_n| + T_D$ when the PLL is locked. This maximum value is three VCO periods plus T_D for the implemented PLL, so $T_{\rm ped}$ can be made sufficiently small that its effect on the noise introduced by the charge pump is negligible.

It follows from the timing diagram shown in Fig. 8(b) that if ΔI_p and ΔI_n were both zero, the charge pump pulses would be as depicted in Fig. 8(a). In this case, nonlinearity is avoided even when $\Delta I_{\rm CP}$ is not zero. Unfortunately, ΔI_p and ΔI_n generally are not zero in practice because of fabrication mismatches between nominally identical components in each of the two current source halves. It follows from (3), (5), and the timing diagram shown in Fig. 8(b), that such mismatches give rise to an additive nonlinear term in $Q_{\rm CP}[n]$ of the form

$$\frac{1}{2}(\Delta I_p - \Delta I_n)|\Delta T_n|. \qquad (6)$$

Therefore, as in the conventional charge pump, current source mismatches give rise to a nonlinear term in $Q_{\rm CP}[n]$ proportional to $|\Delta T_n|$. However, in contrast to the conventional case, the nonlinear term is a result of mismatches between like current sources with identical voltages across their respective transistors. Therefore, the nonlinearity introduced by the proposed technique is much less than that introduced by a conventional charge pump and PFD. Although it was not necessary in this

TABLE I
SIMULATED PHASE NOISE CONTRIBUTIONS OF THE VARIOUS CIRCUIT BLOCKS AND THE RELEVANT PLL PARAMETERS

Fractional-*N* phase locked loop parameters	
Reference frequency	48 MHz
Loop bandwidth	460 kHz
Zero location	92 kHz
Pole location	2.3 MHz
Charge pump current	1.28 mA
Minimum PFD pulse duration, T_D	0.5 ns – 1 ns
Pedestal duration, T_{ped}	3 ns – 6 ns
Simulated worst case phase contributions at 3 MHz offset:	
Voltage controlled oscillator and buffers	-127 dBc/Hz
Modified phase frequency detector	-132 dBc/Hz
Charge pump and DACs	-134 dBc/Hz
Crystal reference oscillator	-134 dBc/Hz
1.8 Volt – 2.7 Volt converters	-139 dBc/Hz
Loop filter resistor	-147 dBc/Hz
Multi-modulus frequency divider	-153 dBc/Hz

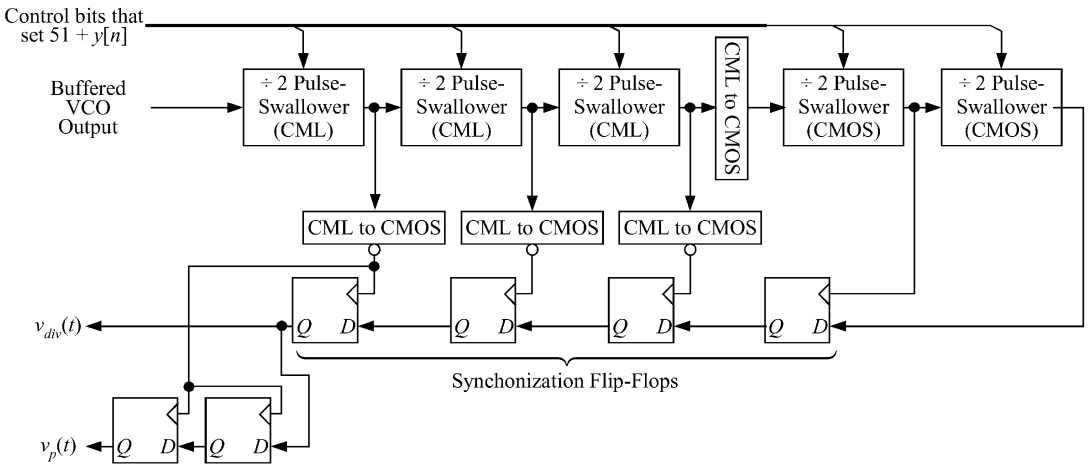

Fig. 9. Frequency divider circuit.

project, the nonlinearity can be further suppressed by randomly interchanging the signals U and $U_{\rm ped}$ and D and $D_{\rm ped}$ using a pseudorandom bit sequence.

IV. CIRCUIT ISSUES

A. Overview

The circuit is implemented in the TSMC 0.18-μm one-poly six-metal mixed-signal CMOS process with the thin top-metal option, and installed in a 5-mm TQFP 32-pin package. All pads include electrostatic discharge (ESD) protection circuitry. The PFD, charge pump, DAC banks, and VCO are designed for a 2.7-V supply. The remaining components are designed for a 1.8-V supply. All the blocks shown in Fig. 1 except the crystal and the loop filter capacitors and resistor are implemented on-chip. A VCO output buffer, a VCO divider buffer, a 1.8–2.7-V logic converter block, and a three-wire digital interface are also included on the chip. Separate deep n-wells under the digital logic and critical analog circuitry and separate supply domains help prevent digital interference from disturbing analog circuit behavior. A summary of the designed loop parameters and simulated phase noise contributions of the various circuits are shown in Table I.

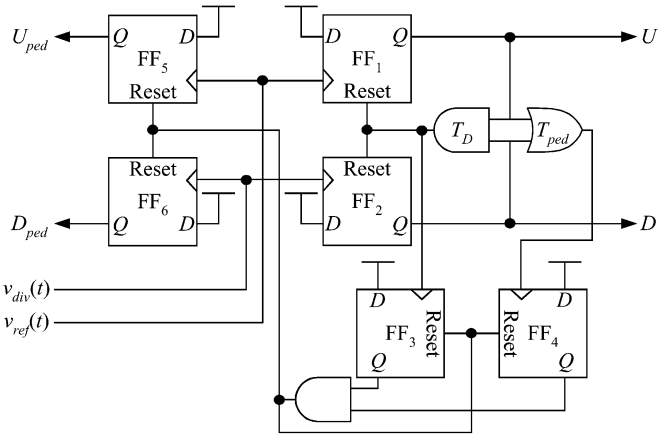

Fig. 10. Modified PFD circuit.

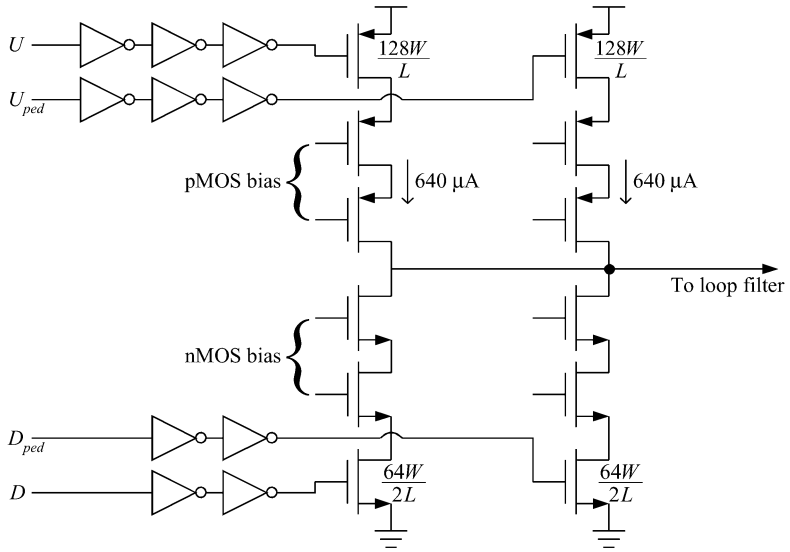

Fig. 11. Modified charge pump circuit.

B. Frequency Divider

As shown in Fig. 9, the core of the divider consists of five divide-by-two pulse-swallowing blocks [31]. The three highest frequency pulse-swallowing blocks consist of current-mode logic (CML), and the other two blocks consist of static CMOS logic. The four synchronization flip-flops ensure that the rising edges of $v_{\rm div}(t)$ are aligned to the appropriate rising edges of the first pulse-swallowing block. Two additional flip-flops are used to derive a DAC pulse termination signal that goes high four VCO periods after each rising edge of $v_{\rm div}(t)$.

The reason for synchronizing the rising edges of $v_{\rm div}(t)$ to edges of the first pulse-swallowing block is to reduce modulus-dependent delay mismatches, i.e., systematic timing errors in $v_{\rm div}(t)$ that depend upon $y[n]$. Such errors have an effect similar to charge pump nonlinearity in that they induce spurious tones in the PLL phase noise at multiples of $\alpha f_{\rm ref}$. Simulations of the implemented PLL indicate that modulus-dependent delay mismatches must be restricted to less than 1% of the VCO period, i.e., to less than 4 ps, to suppress the spurious tones to less than -60 dBc. This is achieved by the synchronization flip-flops which successively align the edges of the signal from the last pulse-swallowing block to those of the previous pulse-swallowing blocks. In principle, only the final flip-flop is necessary, but the other three are included to avoid race conditions.

C. PFD, Charge Pump, and 1-Bit Current Pulse DACs

The PFD is shown in Fig. 10. Flip-flops 1 and 2 and the associated AND gate generate the U and D signals as in a conventional PFD, and the remaining circuitry generates the $U_{\rm ped}$ and $D_{\rm ped}$ signals. The circuit is configured such that the rising edges of $U_{\rm ped}$ coincide with those of U, and the rising edges of $D_{\rm ped}$ coincide with those of D. The AND gate and OR gate driven by U and D have built-in delays of T_D and $T_{\rm ped}$, respectively. Therefore, during the nth reference period, flip-flops 1 and 2 are reset after a delay of $\Delta T_n + T_D$ following the earlier of the times at which U and D go high, whereas flip-flops 5 and 6 are reset after a delay of the maximum of $\Delta T_n + T_D$ and $T_{\rm ped}$ following the earlier of the times at which U and D go high.

As described in the previous section, $T_{\rm ped}$ is chosen to be longer than the maximum value of $\Delta T_n + T_D$ expected to occur when the PLL is locked, in which case the PFD output signals are as illustrated in Fig. 8. When the PLL is in the process of acquiring lock, $\Delta T_n + T_D$ is usually longer than $T_{\rm ped}$. In this case U coincides with $U_{\rm ped}$ and D coincides with $D_{\rm ped}$, so the current from the charge pump is the same as in the conventional case. Therefore, the charge pump linearization technique does not affect the behavior of the PLL during acquisition.

As shown in Fig. 11, and explained in the previous section, the charge pump consists of two halves, one controlled by U and D, and the other controlled by $U_{\rm ped}$ and $D_{\rm ped}$. Each half consists of positive and negative 640 μA cascode current sources with triode MOS switches near the supply rails [32]. The pMOS transistors that make up the switches and cascode current sources have twice the width and half the length of the corresponding nMOS transistors so as to approximately match the loading on the PFD output lines and the switching speeds of the positive and negative current sources. The chains of inverters are scaled to have a common propagation delay so the inverted copies of U and $U_{\rm ped}$ presented to the pMOS switches are properly aligned with the noninverted copies of D and $D_{\rm ped}$ presented to the nMOS switches [29].

Fig. 12 shows a simplified circuit diagram of the kth coarse 1-bit current pulse DAC and the pulse generator shared by all the 1-bit current pulse DACs. The switched current sources in the coarse and fine 1-bit current pulse DACs are, respectively, 40- and 5-μA scaled-down versions of the those in the charge pump. The pulse generator contains a copy of the conventional portion of the PFD described above and four chains of scaled inverters similar to those that drive the charge pump switches. The PFD is driven by the two divider output signals, so each reference period its top output goes high for a duration of four VCO periods plus T_D, and its bottom output goes high for a duration of only T_D. Inverted and noninverted copies of these signals are presented to each 1-bit current pulse DAC to drive

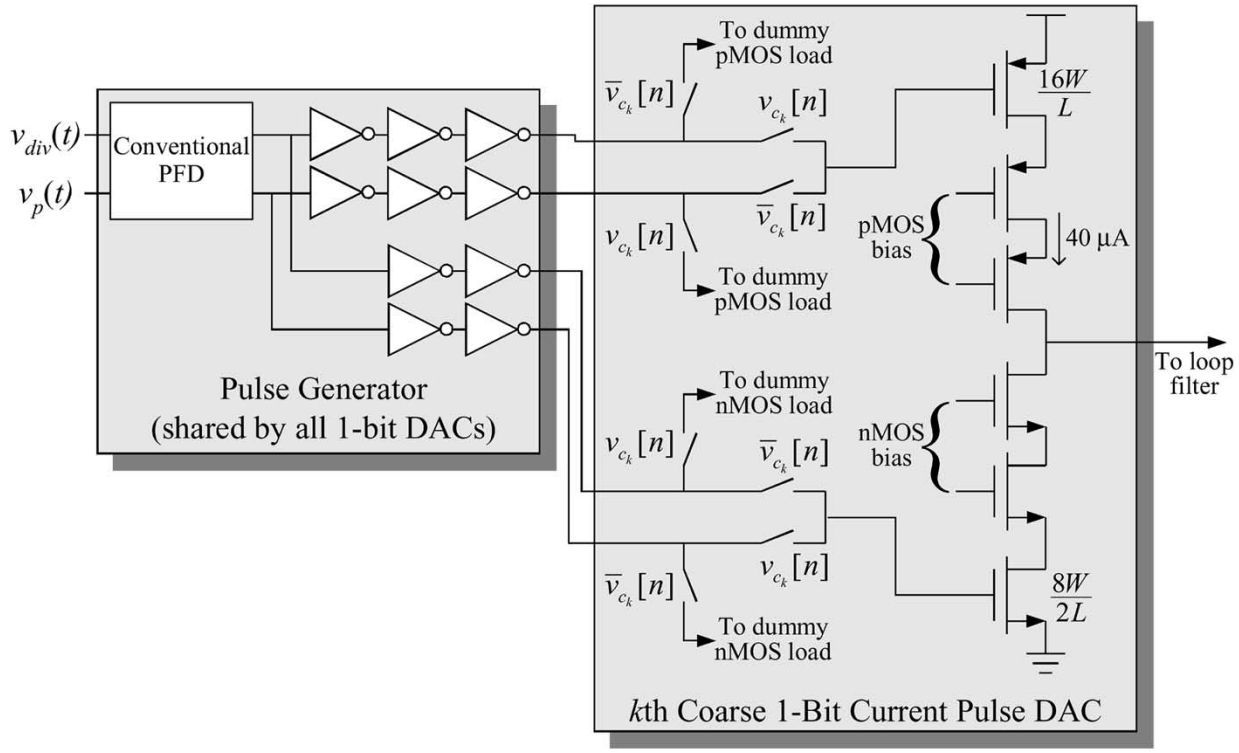

Fig. 12. DAC pulse generator and the kth coarse 1-bit current pulse DAC circuits.

the pMOS and nMOS switches, respectively. In each case, the 1-bit DAC input causes one of these signals to be presented to the MOS switch and the other to be presented to a dummy MOS switch. The purpose of the dummy MOS switches is to maintain data-invariant loads on the pulse generator output lines.

D. VCO

The on-chip VCO is a negative-g_m CMOS *LC* oscillator designed to have a center frequency of 2.448 GHz. It incorporates a differential inductor implemented as a square spiral of metal layers 5 and 6 sandwiched together. A MOS varactor provides 200-MHz/V tuning over a 1-V range. The differential VCO outputs are ac-coupled to two resistively loaded differential source-coupled buffers: one to drive the divider and one to drive 50-Ω loads off the chip. A configuration option allows for the use of an off-chip VCO in place of the on-chip VCO; the on-chip VCO can be disabled and a direct connection is provided from a pin to the input of the divider buffer.

E. Loop Filter

The loop filter components are as follows: $R = 641\ \Omega$, $C_1 = 100$ pF, and $C_2 = 2.4$ nF, of which R, C_2, and 60 pF of C_1 are off-chip. The remaining 40 pF of C_1 is on-chip to help reduce the voltage variations caused by fast charge pump current switching through the inductive bond wires. Given that the divider modulus is approximately 51, the VCO gain is 200 MHz/V, and the nominal charge pump current magnitude is $2 \times 640\ \mu$A, these component values give rise to a PLL bandwidth of approximately 460 kHz. In addition, another pole is placed at about 10 MHz (not shown in Fig. 1) to provide extra out-of-band attenuation, and to reduce the reference spur to negligible levels.

F. 48-MHz Digital Logic

The 48-MHz digital logic was implemented using a standard cell library available to the authors in which the transistors have a minimum gate length of 0.25 μm. While a more compact and lower power design would have been possible with a standard cell library optimized for the 0.18-μm process, the project schedule did not permit such optimization.

V. Measurement Results

Three copies of the IC were tested on separate circuit boards. The performance of each part was verified for all 79 Bluetooth channels with the phase noise cancellation and charge pump linearization techniques individually and simultaneously enabled and disabled with and without FSK modulation. On each Bluetooth channel and each part, the phase noise cancellation technique was found to reduce the spot phase noise by 16 dB or better, and the charge pump linearization technique was found to reduce the spurious tone floor by 8 dB or better. With both techniques enabled, each part was found to achieve a worst-case phase noise of -121 dBc/Hz at 3-MHz offsets, a worst-case spurious tone level of -54 dBc, and a worst-case in-band noise floor of -96 dBc/Hz. The measured results are summarized in Table II, and a die photograph is shown in Fig. 13.

Figs. 14 and 15 show representative PSD plots measured with the PLL set to the 2.431-GHz Bluetooth channel and the phase noise cancellation and charge pump linearization techniques both enabled and both disabled. Fig. 14 shows

TABLE II
PERFORMANCE SUMMARY

Design Details:			
Technology	TSMC 0.18μm 1P6M CMOS		
Package	5 × 5 mm^2, 32 pin TQFP		
Die Area	2.72 × 2.47 mm^2 (includes pads and ESD protection)		
Frequency Range	2402 + k MHz, k = 0, 1, 2, …, 78		
Crystal Reference	48 MHz		
Loop Bandwidth	460 kHz		
Measured Current Consumption, V_{DD}, and Area by Block:			
VCO	3.0 mA @ 1.9 V	0.4 mm^2	67 mW
PFD, CP & DAC	10.3 mA @ 1.9 V	0.04 mm^2	
Divider	6.7 mA @ 1.8 V	0.4 mm^2	
Digital Logic	8.8 mA @ 2.2 V	0.68 mm^2	
Internal VCO Buffer	5.6 mA @ 1.8 V	0.013 mm^2	
Crystal Oscillator Buffer	4.1 mA @ 2.2 V	0.04 mm^2	21 mW
External VCO Buffer	6.9 mA @ 1.8 V	0.015 mm^2	
Measured Worst Case Performance With Both Techniques *Enabled*:	On-chip VCO:	Off-chip VCO:	
Phase Noise @ 50 kHz	–96 dBc/Hz	–96 dBc/Hz	
Phase Noise @ 3 MHz	–121 dBc/Hz	–127 dBc/Hz	
Largest Fractional Spur @ < 2 MHz	–54 dBc @ 1 MHz	–45 dBc @ 1 MHz	
Largest Fractional Spur @ ≥ 2 MHz	–56 dBc @ 2 MHz	–58 dBc @ 2 MHz	
Largest Fractional Spur @ ≥ 3 MHz	–57 dBc @ 3 MHz	–62 dBc @ 3 MHz	
Reference Spur	–65 dBc	–66 dBc	
Measured Worst Case Performance With Both Techniques *Disabled*:	On-chip VCO:	Off-chip VCO:	
Phase Noise @ 50 kHz	–96 dBc/Hz	–96 dBc/Hz	
Phase Noise @ 3 MHz	–107 dBc/Hz	-107 dBc/Hz	
Largest Fractional Spur @ < 2 MHz	–40 dBc @ 1 MHz	–35 dBc @ 1 MHz	
Largest Fractional Spur @ ≥ 2 MHz	–44 dBc @ 2 MHz	–46 dBc @ 2 MHz	
Largest Fractional Spur @ ≥ 3 MHz	–49 dBc @ 3 MHz	–52 dBc @ 3 MHz	
Measured Performance With Both Techniques *Disabled*:	On-chip VCO:	Off-chip VCO:	
Effect of charge pump linearization technique on phase noise	None observed	None observed	
Effect of ΔΣ noise cancellation technique on fractional spur level	None observed	2-9 dB spur reduction	

PSD plots of the PLL output signal and phase noise with the PLL operating without modulation. Fig. 15 shows PSD plots of the PLL output signal for the PLL operating with 1-Mb/s FSK modulation. In both cases, the phase noise improvement resulting from the techniques is evident. Similar results are seen for each part on every Bluetooth channel.

Fig. 16 shows an eye pattern from the PLL with 1-Mb/s FSK transmit modulation and both techniques enabled measured by downconverting the PLL output signal to an intermediate frequency through a spectrum analyzer and frequency demodulating the result using a vector analyzer. The minimum frequency deviation is approximately 120 kHz and the zero-crossing error is less than 1/8 of the symbol period as required by the application. Again, almost identical results were observed for each part on every Bluetooth channel.

The spurious tone reduction achieved by the charge pump linearization technique is most easily observed when the PLL is tuned to Bluetooth channels that are close to integer multiples of the 48-MHz reference frequency. In such cases α is small, so the spurious tones in the PLL phase noise resulting from nonlinearity, which occur at multiples of αf_{ref}, are not highly attenuated by the low-pass transfer function of the PLL. Fig. 17 shows PSD plots of the PLL output signal with and without the charge pump linearization technique enabled for such a case, i.e., for the VCO tuned to 2.453 GHz so that $\alpha f_{\text{ref}} = 5$ MHz. The overlaid plots are intentionally displaced in frequency to make the spurious tone reduction visible.

As mentioned in the previous section, the VCO and charge pump were designed to operate from a 2.7-V supply with a VCO center frequency of 2.448 GHz, but the measured VCO center frequency turned out to be 2.25 GHz. To force the VCO into the Bluetooth frequency range the VCO and charge pump, which share the same power supply lines, had to be run from a 1.9-V supply during testing. It is likely that this increased the phase noise by at least 3 dB and increased distortion because several critical transistors were forced into their triode regions. Nevertheless, as described above and summarized in Table II, the IC performed well.

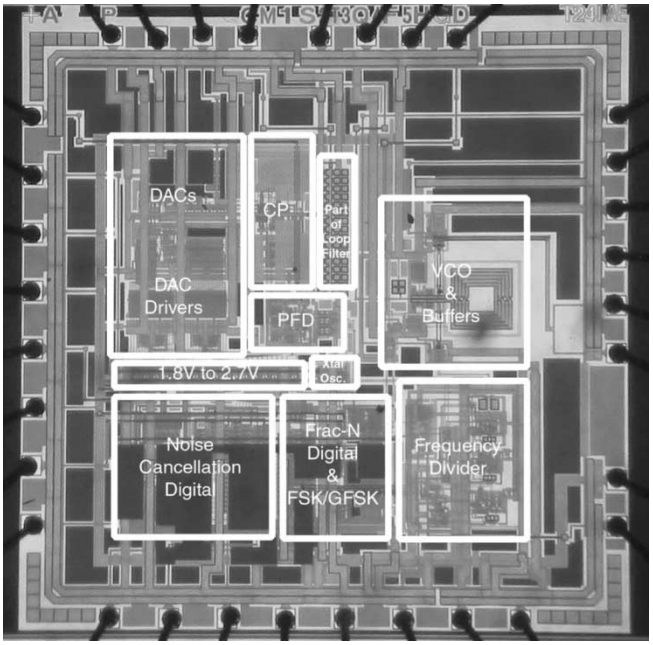

Fig. 13. Die photograph.

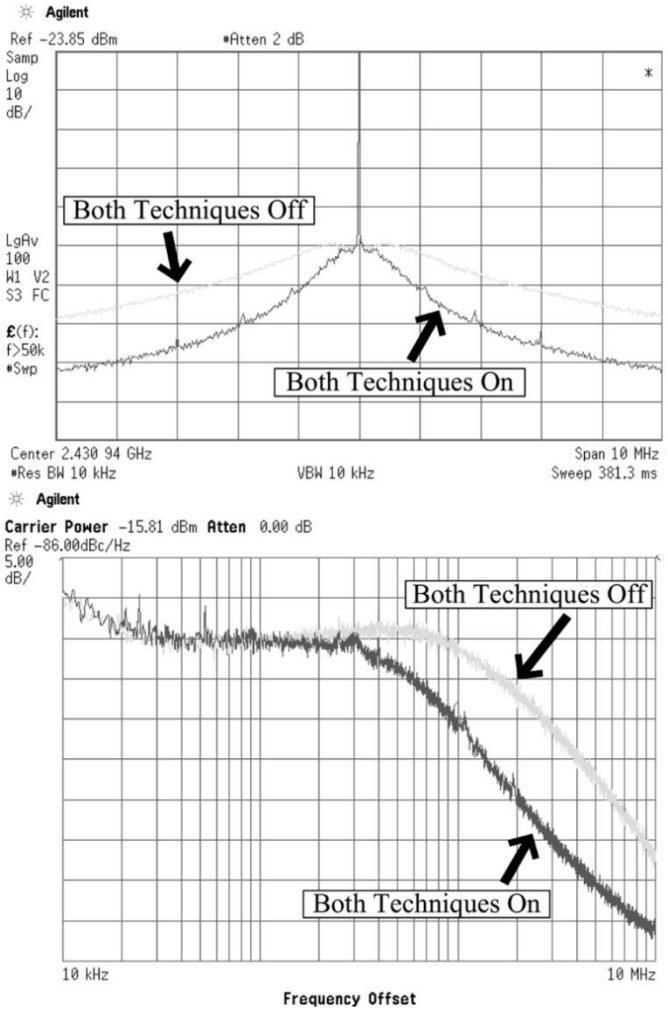

Fig. 14. Measured PSD plots of the output signal and phase noise of the PLL tuned to 2.431 GHz without modulation.

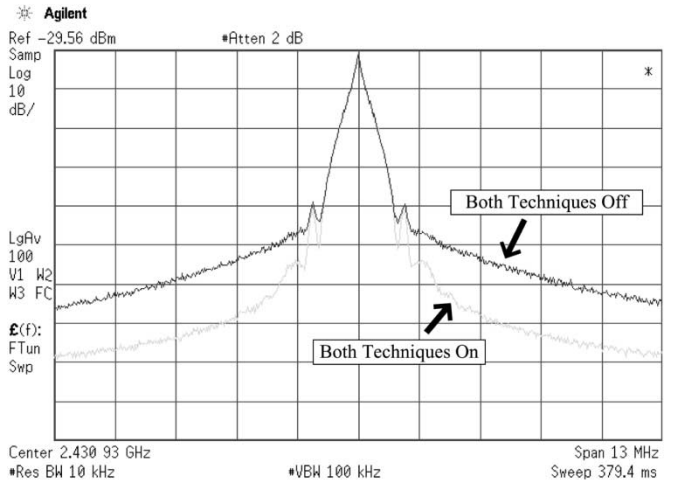

Fig. 15. Measured PSD plot of the output signal of the PLL tuned to 2.431 GHz with 1 Mb/s FSK modulation.

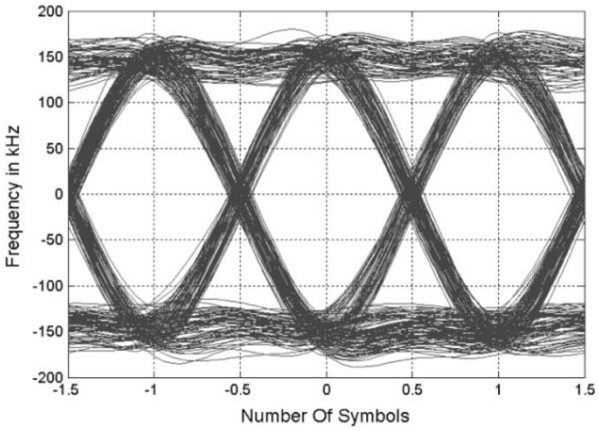

Fig. 16. Measured eye pattern corresponding to the output signal shown in Fig. 15.

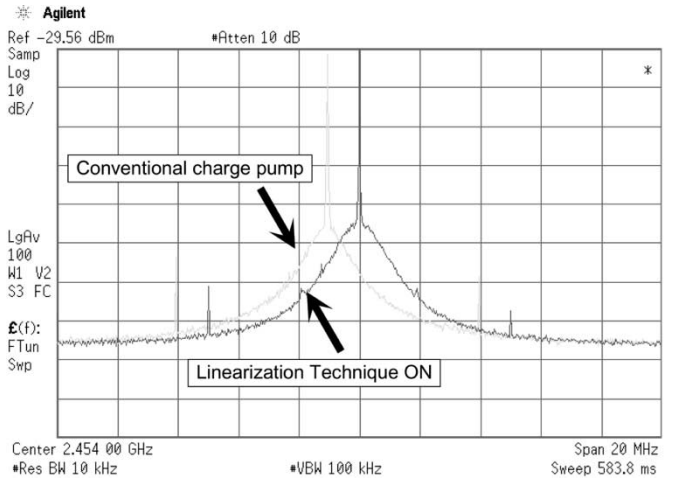

Fig. 17. Measured PSD plots of the PLL tuned to 2.453 GHz with the charge pump linearization technique enabled and disabled.

Each of the tested parts met the Bluetooth phase noise and eye pattern specifications on all channels. They also met the Bluetooth spurious tone specifications except for a small number of channels on which the spurious tones were at most 3 dB above the specification. The slightly elevated spurious tone level is a

result of having to run the VCO and charge pump from a 1.9-V supply instead of the 2.7-V supply for which it was designed. In support of this assertion, the PLL configured with an off-chip VCO and the charge pump operating from a 2.7-V supply was found to meet all required specifications on all channels (see Table II).

The circuitry was designed conservatively to help ensure first-silicon success and clearly demonstrate the phase noise cancellation and charge pump linearization techniques. In particular, as tabulated in Table I, large noise margins were used in designing the circuits to ensure that the phase noise below 5 MHz would be dominated by residual $\Delta\Sigma$ quantization noise and spurious tones resulting from nonlinearities. Consequently, the measured in-band phase noise is much lower than required to meet the Bluetooth specifications. While this design strategy has served the purpose of demonstrating the phase noise cancellation and charge pump linearization techniques, the current consumption of the PLL could be reduced significantly by optimizing the analog circuitry so that its in-band noise contribution is closer to the Bluetooth specification.

VI. Conclusion

A phase noise cancellation technique and a charge pump linearization technique have been proposed and demonstrated as enabling components in a wideband CMOS $\Delta\Sigma$ fractional-N PLL configured as a Bluetooth wireless LAN transmitter. The phase noise cancellation technique relaxes the fundamental tradeoff between phase noise and bandwidth in conventional $\Delta\Sigma$ fractional-N PLLs and does not require tight component matching or calibration. Theoretical and experimental results have been presented that indicate the technique enables a tenfold increase in PLL bandwidth without an increase in spot phase noise. The charge pump linearization technique provides a simple means of improving the spurious performance of wideband fractional-N PLLs that avoids the bandwidth limitations of previously presented techniques involving analog feedback circuits.

Acknowledgment

The authors are grateful to E. Fogleman, K. Seendripu, E. Siragusa, Andrea Spandonis, A. Swaminathan, K. Wang, J. Welz, and S. Ye for their assistance and advice regarding this project.

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