A 700-kHz Bandwidth $\Sigma\Delta$ Fractional Synthesizer With Spurs Compensation and Linearization Techniques for WCDMA Applications

Enrico Temporiti, Guido Albasini, Ivan Bietti, Rinaldo Castello, *Fellow, IEEE*, and Matteo Colombo

***Abstract*—A $\Sigma\Delta$ fractional-N frequency synthesizer targeting WCDMA receiver specifications is presented. Through spurs compensation and linearization techniques, the PLL bandwidth is significantly extended with only a slight increase in the integrated phase noise. In a 0.18-μm standard digital CMOS technology a fully integrated prototype with 2.1-GHz output frequency and 35 Hz resolution has an area of 3.4 mm^2 PADs included, and it consumes 28 mW. With a 3-dB closed-loop bandwidth of 700 kHz, the settling time is only 7 μs. The integrated phase noise plus spurs is -45 dBc for the first WCDMA channel (1 kHz to 1.94 MHz) and -65 dBc for the second channel (2.5 to 6.34 MHz) with a worst case in-band (unfiltered) fractional spur of -60 dBc. Given the extremely large bandwidth, the synthesizer could be used also for TX direct modulation over a broad band. The choice of such a large bandwidth, however, still limits the spur performance. A slightly smaller bandwidth would fulfill WCDMA requirements. This has been shown in a second prototype, using the same architecture but employing an external loop filter and VCO for greater flexibility and ease of testing.**

***Index Terms*—Charge pump, CMOS RF integrated circuits, fractional-N, frequency synthesizer, phase frequency detector, phase-locked loop, phase noise, quantization noise, sigma-delta modulation, spurs compensation.**

I. Introduction

THE fast growing market of wireless communications has driven many efforts toward the development of high-performance low-cost CMOS wireless systems. This is especially true with respect to the implementation of a highly integrated RF frequency synthesizer. In this context, fractional synthesis is a suitable solution to overcome the limitation of classical integer phase-locked loops (PLLs), i.e., the tradeoff between bandwidth and frequency resolution, even if suffering of spurs problem [1], [2]. This paper describes spurs generation mechanisms in a fractional synthesizer and proposes methodologies to strongly reduce their energy without sacrificing the PLL bandwidth. These studies have been proved with the implementation of two $\Sigma\Delta$ fractional synthesizers, targeting 3G standard specifications.

The paper is organized as following: in Section II a brief description of the working principles of PLL frequency synthesizers, and particularly of fractional ones, is presented; Section III describes a methodology for simulating the spurs shaping at the output of a $\Sigma\Delta$ PLL, whereas the circuit implementation of the two realized synthesizers are illustrated in Section IV. Sections V and VI report the proposed solutions to reduce the energy of the quantization spurs and of the fractional one, respectively. The main measurement results are reported in Section VII, and some conclusions are eventually drawn in Section VIII.

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II. PLL Frequency Synthesizer

Integer PLL synthesizers generate an output signal whose frequency is a multiple of that of a reference signal Fref, typically generated by a crystal oscillator (XO). This is done thanks to a negative feedback loop where the error signal is obtained by a phase comparison between Fref and the by-N divided PLL output. This comparison is achieved via a phase frequency detector (PFD), usually employing a charge pump (CP). Its output is filtered by the loop filter (LF) and drives the control node of the voltage-controlled oscillator (VCO) (Fig. 1).

When the PLL is either powered on or programmed for a different output channel, the circuit reaches a steady state, with its output frequency equal to $\mathrm{Fout} = N \cdot \mathrm{Fref}$, after a transient called *locking time.*

An integer synthesizer is characterized by some intrinsic limitations. The main one is that the output frequency resolution is forced to be equal to a multiple of Fref. In this case, if a fine output frequency resolution is needed (e.g., for RF channel selection or XO drift compensation), a correspondingly low Fref has to be chosen. This forces the loop bandwidth to be very narrow, since it must be much lower than Fref for loop stability reasons. A factor 10 is usually taken between Fref and the PLL bandwidth; in which case it is possible to consider the PLL as a linear continuous time system, discarding the discrete-time nature of the phase detection. If a transfer function in the discrete time domain is calculated, this factor can be reduced, but not arbitrarily. Van Paemel [3] claims that a factor 3 can be reached. In any case, due to a fundamental limitation of a sampled feedback system, the signal bandwidth has to be at least two times lower than the sample frequency.

The immediate consequence of the loop bandwidth reduction is an increase of the PLL locking time and of the channel switching time. Moreover, a low reference frequency requires a high feedback division ratio to synthesize the desired output frequency, thus causing a strong enhancement of the output in-band

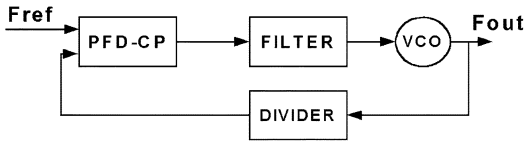

Fig. 1. Diagram of a classical integer PLL.

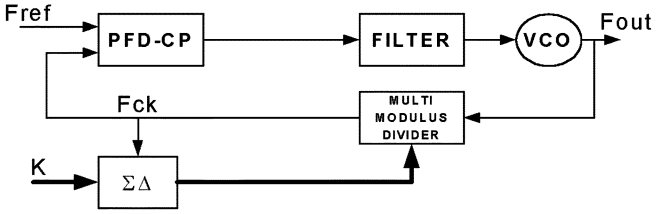

Fig. 2. Diagram of a fractional synthesizer.

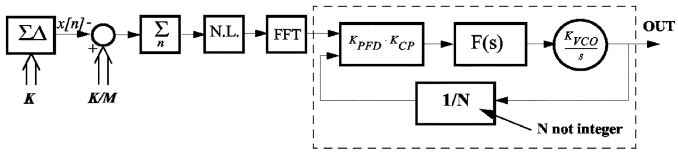

Fig. 3. Mixed time-frequency domain model.

phase noise (which mainly arises from the multiplication by N of the reference, the PFD-CP and the divider noise).

Fractional synthesizers can avoid these limitations, thus achieving fast locking, agile channel switching, potentially arbitrary output frequency resolution, and more freedom in the reference frequency choice. This is accomplished thanks to their noninteger frequency division capability, obtained by varying the feedback division ratio between different integers, using a multi modulus divider. The division ratio is dynamically programmed by a control pattern, whose average value corresponds to the fractional division factor. As an example, in the simple case of a dual modulus divider capable to divide by N and $N+1$, a division ratio of $N+(1/100)$ can be obtained dividing once by $N+1$ and 99 times by N. More generally, the resulting output average frequency is $\mathrm{Fout} = (N + K/M) \cdot \mathrm{Fref}$, where K is the number corresponding to the selected channel frequency and M is the fractionality depth, i.e., the total number of selectable channels.

The algorithms used to generate the division control pattern are generally characterized by an intrinsic periodicity. This causes the generation of spurious signals around the carrier, herein called *quantization spurs*. In fact, after each change in the division ratio, the phase coherence between the divider output and the reference is lost, and consequently the PFD-CP injects current pulses into the loop filter. A low-pass filtered version of these pulses appears on the VCO control node, and is eventually up-converted by the VCO itself. Unlike in an integer synthesizer, in a fractional one a classical lock condition, characterized by permanent phase coherence between input and output signal, is never reached. Only a dynamic lock can be achieved, characterized by the PFD-CP injecting current pulses according to the periodical divider control pattern. It would be desirable to move most of the quantization spurs energy at frequencies far away from the carrier, where it can be filtered out by the loop transfer function. This shaping is intrinsically accomplished driving the fractional divider with a ΣΔ modulator (see Fig. 2). This generates the expected average division ratio, while shaping the quantization noise (and thus the synthesizer quantization spurs) in a high-pass fashion [4].

In an actual realization, two main problems arise: first, to sufficiently filter out the quantization spurs, the loop bandwidth cannot be too wide, thus partially losing the fractional architecture main advantage. Second, the linearity required for the critical ΣΔ PLL building blocks, i.e., those placed between the multi-modulus divider and the loop filter (mainly the PFD-CP), must be much higher than in an integer synthesizer. In fact, any nonlinearity seen by the ΣΔ modulated signal folds part of the high-frequency spurs energy close to the carrier. Both these limitations have been addressed: the first problem via a compensation scheme, the second via linearization techniques, as it will be explained below.

III. Fractional Synthesizer Simulations

In the design of fractional synthesizers, extensive simulations are needed to predict quantization spurs amplitude and frequency distribution for a large number of selectable output frequencies and for different modulator architectures. To this aim the availability of a computationally efficient approach is necessary because traditional device level transient analysis is unacceptably time consuming, due to the long periodicity of the divider control pattern, i.e., of the ΣΔ output (up to $2 \cdot 10^6$ clock cycles in the case of a third-order ΣΔ with 20-bit accumulators, as in our project). Even the use of an high-level time domain model (e.g., VerilogA/VHDL) does not solve this problem.

For this reason, an approach similar to the one proposed by Perrott *et al.* [5], based on the mixed time-frequency domain model shown in Fig. 3, has been introduced. In this model, the ΣΔ output sequence $\mathrm{x[n]}$ no longer modulates the feedback division factor, but it is taken out of the loop, processed as shown in the figure and fed into a linear frequency domain model of the PLL (dashed box in Fig. 3). With this approach, PFD-CP nonlinearity can be easily taken into account by the nonlinear block (N.L.), while compensation algorithms (as the one described in Section V) can be modeled with minor modifications.

It is worth noting that in the real case, the ΣΔ clock is slightly modulated, being derived from the PLL output signal (the amount of the residual modulation depends on the loop bandwidth). This is not the case in this simplified model. The error associated with this approximation is however negligible. This has been verified through simulations over a restricted number of channels computing the difference between the true model and the proposed one. As an example, in Fig. 4, a comparison between a closed-loop high-level time domain simulation and an open-loop one based on the mixed time-frequency domain model is shown for a given channel. Each symbol in the figure represents the power level of the spur at the corresponding x-axis frequency offset from the carrier.

IV. Chip Implementation

Two test chips have been integrated, in 0.18-μm digital CMOS technology, to test the performance of large-bandwidth

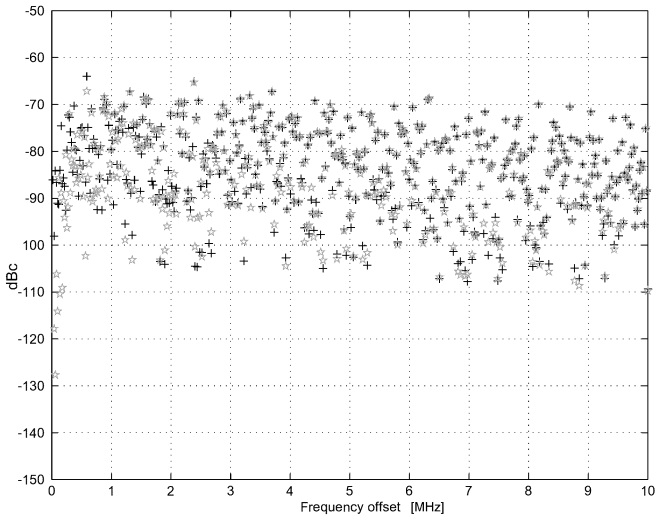

Fig. 4. Simulated output spurs after closed loop VerilogA simulation (+) and after mixed time-frequency domain simulation ($\star$).

fractional synthesizers implementing quantization spurs compensation and linearization techniques. The building blocks and design solutions adopted in both prototypes are first described, then some specific details for each version are given.

The 35-MHz reference clock enters the chip through a differential stage, whose immunity to common mode noise is higher than a classical single ended one. This reduces cross coupling between the high-frequency output and the reference input, which is very important in fractional synthesizers. In fact, since the two frequencies are not multiples of each other, any coupling causes an increase of the *fractional spur*, which is located at an offset frequency equal to $\mathrm{Fref} \cdot K/M$. This particular tone is one of the many quantization spurs but it can be strongly enhanced over its nominal amplitude due to parasitic and nonlinear effects (as described in Section VI), one of these being the coupling phenomenon mentioned above.

The output frequency resolution has been pushed below 35 Hz, since in many mobile applications this allows compensation of the crystal frequency drift, avoiding the need for an expensive voltage-controlled crystal oscillator (VCXO). For a 35-MHz Fref, a 20-bit fractionality ($M = 2^{20}$) resulted. After extensive simulations, a MASH 1-1-1 $\Sigma\Delta$ modulator [6] has been chosen because of its superior performance for the targeted specifications. The entire digital part has been integrated on-chip and placed into a triple-well isolating structure in order to reduce cross-talk with the analog part of the PLL.

Since this $\Sigma\Delta$ modulator has a 3-bit output, the divider is based on a *swallow counter architecture* [7] to allow multi modulus division using a dual modulus prescaler, capable to divide by 3 or 4. It is built up using three current mode logic (CML) flip-flops that can be connected as a bubble divider (division by 3) or as a classical divider by 4 (using only 2 of them), as shown in Fig. 5. The logic to select the division according to the $\Sigma\Delta$ control word is done using standard CMOS logic because of the lower speed (about 700 MHz). The divider total power consumption is 7.2 mW.

The PFD makes use of the classical topology based on two flip-flops, reset by the logic AND of their outputs. Proper delay

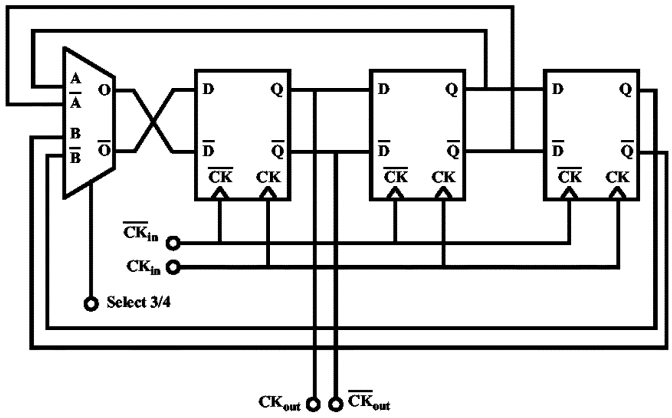

Fig. 5. Block diagram of the 3–4 prescaler.

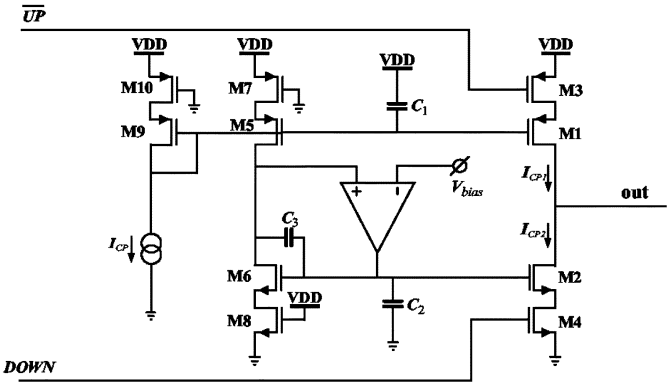

Fig. 6. Circuit diagram of the charge pump.

has been added in the feedback path to avoid the *dead zone* effect [7].

The CP circuit is represented in Fig. 6. The current flowing through M5 and M6 is obtained mirroring the Icp reference current. Making M3 equal to M7 and M4 equal to M8, this current is mirrored to the output when the UP or DOWN signals are active, producing the positive and the negative CP pulses respectively. Therefore the symmetry between the up and down pulses depends only on the matching (in terms of both device characteristics and biasing conditions) between M1 (M2) and M5 (M6). To ensure this condition, two techniques are adopted: first, relatively large transistor sizes are used. Second, the drain voltage of M1 (M2) is forced to be the same as M5 (M6) by the negative feedback, implemented with M6 and the operational amplifier, whose inverting input Vbias follows the CP output voltage. For stability reasons, Vbias has been derived low-pass filtering the CP output voltage itself.

The need for such a good matching is a key point in a fractional synthesizer not only to minimize the *reference spur* level (i.e., the one located at an offset frequency equal to Fref) as in a classical integer one, but also to improve the linearity of the PFD-CP characteristic (*injected current* versus *phase error*). The latter effect determines the amount of high-frequency quantization spurs energy folded at low frequencies, and in particular the level of the fractional spur, as it will be explained in Section VI.

The first chip is a fully integrated fractional PLL that requires an area of 1.9×1.8 mm^2 (PADs included) and whose

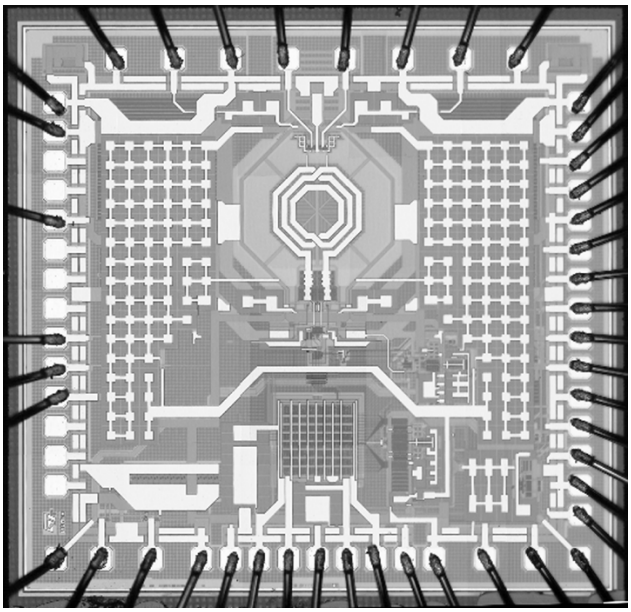

Fig. 7. Die photograph.

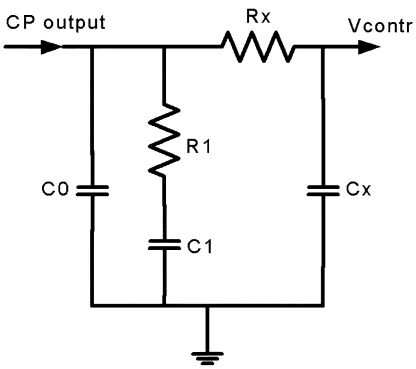

Fig. 8. Third-order passive loop filter.

microphotograph is shown in Fig. 7. The reference oscillator is the only external component required to realize the complete synthesizer. A 700-kHz 3-dB closed-loop bandwidth has been chosen for very fast locking time and to potentially allow TX direct modulation for several standards [6]. An on-chip third-order LF has been integrated. The order of the loop filter affects both the reference spur level, as in a classical integer PLL, and the attenuation of the high-frequency quantization spurs. Particularly, to adequately filter them out, the high-frequency slope of the closed-loop transfer function must be equal or higher than the ΣΔ order. In fact, a first-order filtering effect on the spectrum of the ΣΔ quantization noise is implicit in the frequency to phase conversion performed by the fractional divider [8]. Unfortunately, the LF order cannot be arbitrarily high for stability reasons. A passive filter (Fig. 8) has been chosen to improve phase noise (PN), compared to an active one. The LF is connected between the frequency control node and ground, to which the VCO common mode voltage is referred, to improve the power supply rejection ratio (PSRR).

The VCO has been implemented with an *LC* tank structure and an NMOS cross coupled differential pair that compensates the tank losses and sustains a stable oscillation (see Fig. 9). A

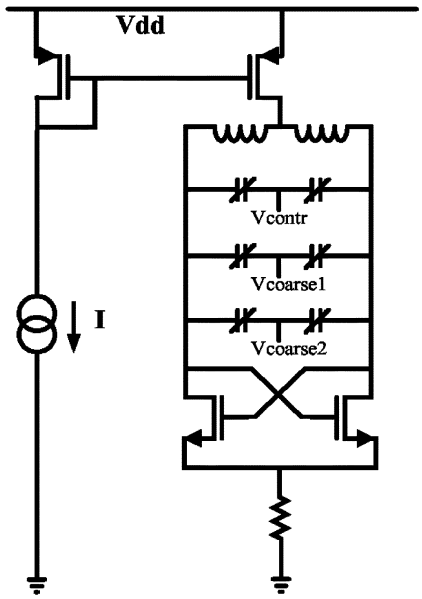

Fig. 9. Circuit diagram of the VCO.

quality factor of 7 has been measured for the tank, limited by the integrated spiral inductor. The VCO achieves −123-dBc/Hz phase noise at 1-MHz offset drawing 7 mA with 1.8-V supply. These values have been measured for the free-running VCO using a proper measurement setup. Regarding the frequency control, an array of NMOS varactors placed within an NWELL has been used [9]. The varactors are partly digitally selected (switching them between two low-gain states) and partly driven by the loop control voltage. The digital control is programmed to achieve a coarse centering of the oscillation frequency. This split is useful to reduce the VCO gain associated with the analog control voltage Vcontr, therefore lowering the sensitivity to on-chip noise.

A second version of the PLL has been realized with an external loop filter and VCO, in order to improve flexibility. In fact, this allows to optimize the PLL bandwidth, which can result in a better quantization spurs performance compared to that achieved by the first one, if needed. To show the effectiveness of the compensation technique, the external VCO has been chosen with a good PN at low-frequency offsets (−135 dBc/Hz at 1-MHz offset, 12 dB better than that of the integrated one). Unfortunately, this commercial component has a noise floor at high-frequency offsets worse than the integrated one (−138 dBc/Hz versus less than −150 dBc/Hz).

The chosen 3-dB closed-loop bandwidth for this second PLL is 200 kHz, which still results in a fast locking time. The use of an external VCO gives also the possibility to directly measure the importance of various sources in fractional spur generation, which are not directly measurable in the fully integrated PLL.

V. Quantization Spurs Compensation

The quantization phase error at the input of the PFD-CP is not random, but deterministic, and related to the divider control pattern as described in Section II. Its periodicity depends on the modulator type, the fractionality depth and the selected frequency. Therefore, this phase error is predictable and it is

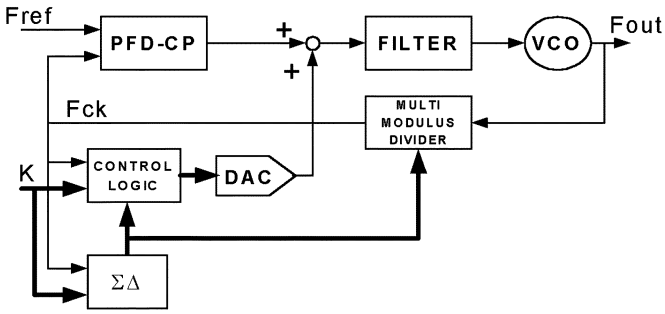

Fig. 10. Quantization spurs compensation technique.

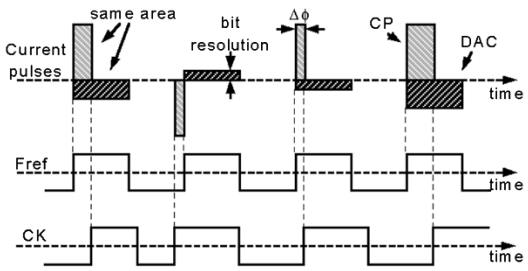

Fig. 11. DAC versus CP pulses.

possible to compensate its effect on the VCO control node by injecting the proper set of current pulses at the output of the PFD-CP. Ideally, this completely cancels the output pulses of the PFD-CP due to the periodic error at its inputs. Thus the fractional architecture properly works and synthesizes the wanted frequency, whereas no spurs are generated.

The correction sequence, which is related to the phase error $\Delta\phi$ at the input of the PFD, can be numerically evaluated by a control logic, according to the following equation:

$$\Delta\phi[n] = \Delta\phi[n-1] + 2\pi\left(\frac{K - M\,x[n]}{MN + K}\right).$$

The correction value is applied to a current DAC, as shown in Fig. 10. To help intuition, notice that for the simple case of a first-order single-bit $\Sigma\Delta$ modulator (i.e., an accumulator), the phase error $\Delta\phi$ corresponds to the accumulator content. The compensation DAC injects current pulses synchronously with the reference clock, as shown in Fig. 11. The DAC current pulse value changes according to the DAC input word, whereas its width is constant (equal to $\mathrm{Tref}/4$ in our case). On the contrary, the CP current pulse value is constant (300 μA in our case), and its width varies according to PFD output. Because of these different pulse shapes, this compensation technique is not exact and its effectiveness decreases at high-frequency offsets.

In addition to this, several possible non idealities in the DAC can impair the effectiveness of this cancellation technique, resulting in an actual degradation of the in-band spurious signal. To avoid these possible problems, the following features have been adopted.

A. Shaping of the DAC Quantization Error

The output of the compensation logic has a resolution that is related to the number of bits in the sigma-delta modulator; using a 20-bit MASH 1-1-1, a 22-bit DAC should be required. Such an ideal approach is hardly feasible and not power efficient, so a reduction of the DAC resolution is needed. This can be done using truncation [e.g., only the five most significant bits (MSBs) of the control logic output are applied to a 5-bit DAC]. Unfortunately, since any nonlinear effect folds down the $\Sigma\Delta$ high-frequency energy close to the carrier, the DAC quantization error arising from truncation in the compensation algorithm has a nonlinear effect that causes a strong increase of spurs at low-frequency offsets. This has been verified by simulations. To solve this problem, the truncation error can be processed through a proper digital algorithm, and its spectral content spread over the $\mathrm{Fref}/2$ bandwidth. In particular, the solution proposed in this paper consists in the use of a second-order $\Sigma\Delta$ modulator to shape the error, pushing it to higher frequencies, according to the scheme in Fig. 12. In this way, not only the MSBs but also a processed (by the second-order $\Sigma\Delta$) version of the least significant bits (LSBs) are used to feed the input of the compensation DAC. The input word for the compensation DAC is obtained summing the one-bit output of this auxiliary $\Sigma\Delta$ to the five MSBs. This results in a $-16 \div +16$ DAC range.

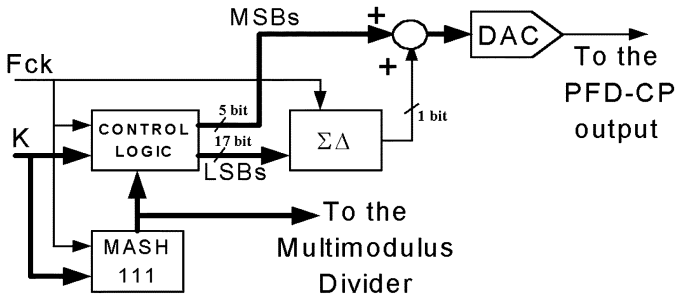

Fig. 12. Reduction of the quantization error of the DAC.

B. Improvement of the DAC Linearity

The DAC nonlinearity has an effect similar to that of the quantization error, i.e., it folds down, close to the carrier, the $\Sigma\Delta$ high-frequency energy. The implemented solution to reduce the differential DAC nonlinearity consists in the use of a thermometric architecture, based on 32 unit elements, instead of a 5 bit binary-weighted one. Furthermore, to reduce also the integral nonlinearity, a barrel shifter scrambling algorithm is used [10]. The result is that the spurs energy due to the DAC nonlinearity is whitened over the $\mathrm{Fref}/2$ bandwidth and so mostly canceled by the loop filter.

C. High-Pass Filtering of the Compensation Signal

As a result of the solutions proposed at points A and B, the quantization spurs enhancement close to the carrier is mostly avoided. However, an increase of low-frequency spurs level arises from any residual non idealities in the DAC cancellation technique. To reduce this effect, an high-pass filtering of the compensation current has been implemented. This is not affecting the compensation where it is beneficial and avoids any penalty in the low-frequency range where no correction is needed, since the $\Sigma\Delta$ quantization spurs are negligible if compared to in-band PN.

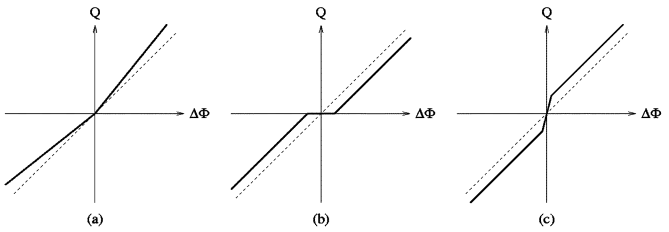

Fig. 13. PFD-CP nonlinear I/O characteristics (solid lines) versus ideal ones (dashed lines): (a) P-N mismatch; (b) dead zone; (c) residual gain enhancement.

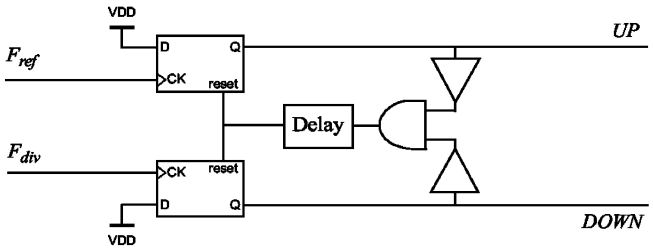

Fig. 14. Circuit diagram of the improved phase frequency detector.

VI. Fractional Spur Reduction

Any nonlinearity in the PLL building blocks, mainly in the PFD-CP I/O characteristic, increases in-band spurs and particularly the fractional one, located at an offset frequency equal to $\mathrm{Fref} \cdot K/M$, as already mentioned. A typical PFD-CP nonlinearity [Fig. 13(a)] is caused by the mismatch between the P-source and the N-source used as current generators in the CP, as described in Section IV. More generally, other nonlinearities can be identified in the injected charge Q versus input phase error $\Delta\Phi$ characteristic, especially for small $\Delta\Phi$ values [Fig. 13(b) and (c)].

After a careful investigation, the PFD has been identified as the main contributor to the residual nonlinearity at small $\Delta\Phi$ values even after dead zone suppression and P-N mismatch correction. The corresponding simulated shape of the charge versus phase error characteristic for the PFD-CP is shown in Fig. 13(c). The situation can be further improved by equalizing the impedance loading the UP and DOWN output lines of the PFD. This has been done through the introduction of two buffers at the inputs of the feedback AND gate (Fig. 14). From simulations, a reduction in the residual gain enhancement of the PFD at small $\Delta\Phi$ values from 8% to less than 1% has been obtained. Even in this case, however, the portion of the PFD-CP I/O characteristic corresponding to small $\Delta\Phi$ values is still the most nonlinear one. Therefore, to completely avoid the effects of this nonlinearity, the PFD-CP has been forced to work in a more linear part of its characteristic. The most simple way to do so is to inject a dc current into the loop filter; this however has the drawback of emphasizing the reference spur. A better solution (used here) consists in the injection of periodic current pulses into the loop filter. Each current pulse must be long enough to force operation outside the nonlinear portion of the PFD-CP characteristic, and must be injected synchronous with the comparison edges at the PFD inputs. An efficient way to generate these pulses uses the VCO edges, since they constitute

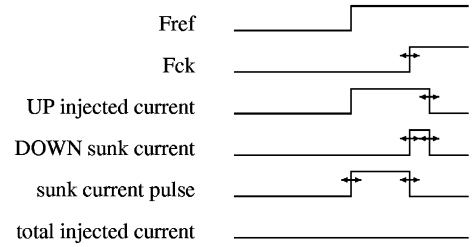

Fig. 15. Timing diagram in lock condition with pulse injection.

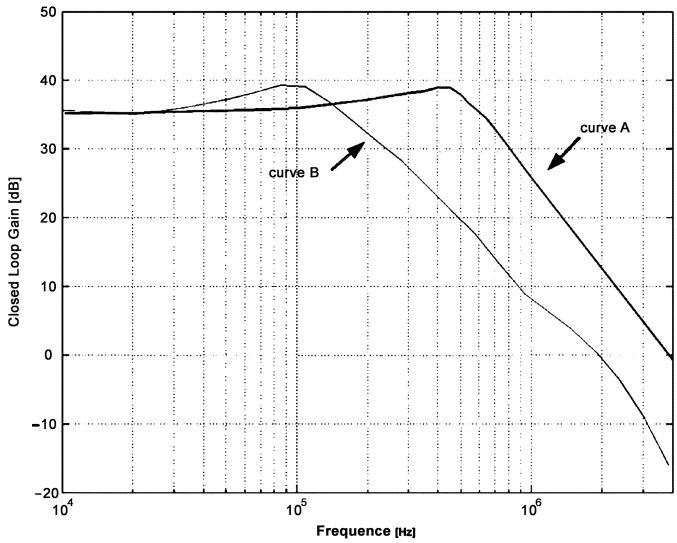

Fig. 16. Measured PLL closed-loop gain for the fully integrated synthesizer (curve A) and for the version with external LF and VCO (curve B).

the most precise high-frequency time base available in the PLL. Fig. 15 shows the timing diagram of the most significant signals in the PFD-CP in lock condition. The (sunk) pulse used to move the PFD away from its nonlinear region is synchronous with Fck and its length is equal to a programmable number of VCO cycles. Compared to the injection of a dc current, this technique has the advantage of leaving unchanged the level of the *reference spur*. In fact, the total injected current is zero not only when averaged over one period, but also instantaneously.

These two linearization techniques (i.e., buffering the PFD outputs and injecting the synchronous current pulses) can be enabled or disabled, in order to test their effectiveness.

VII. Measurements Results

A 700-kHz 3-dB closed-loop bandwidth has been measured for the fully integrated PLL (Fig. 16 curve A). This results in a locking time of ~ 7 μs [Fig. 17(a)], making the synthesizer suitable for application in transceivers requiring fast frequency hopping or allowing single PLL vertical hand over between different standards.

Fig. 18 shows the measured PN plus spurs performance of the 700-kHz bandwidth synthesizer. Curve A shows the measured PLL PN, corresponding to the selection of channel $0/2^{20}$, i.e., when the $\Sigma\Delta$ is OFF and the PLL is equivalent to an integer one. At frequencies where the PN is dominated by the VCO, an excellent spectral purity is achieved (e.g.,

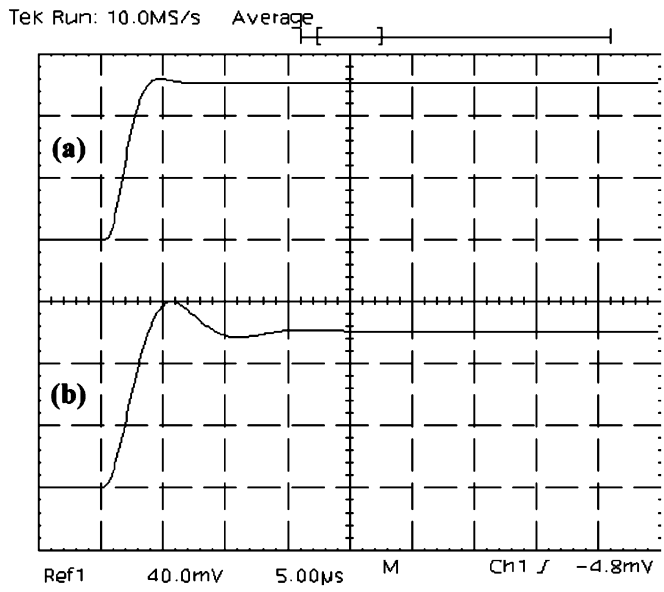

Fig. 17. Locking time plot for (a) the fully integrated synthesizer and (b) the version with external LF and VCO.

−129 dBc/Hz at 2 MHz), showing that the PN of the fully integrated synthesizer (excluding the effect of the $\Sigma\Delta$ fractional divider) can meet the WCDMA specifications. Curve B shows the measured PN plus spurs, resulting from the selection of channel $1/2^{20}$, when the $\Sigma\Delta$ is working and the compensation algorithm is OFF. Curve C is the measured PN plus spurs in the same conditions as B, but with the compensation algorithm enabled. A strong reduction of spurs at high-frequency offsets is achieved, with a limited degradation for those close to the carrier. The residual difference between curves C and A is due to the quantization error of the compensating DAC, that is pushed at high frequencies and only partly filtered by the 700-kHz loop bandwidth. This difference can be strongly reduced if the loop bandwidth is lowered, as done in the chip with the external LF and VCO. Its measured 3-dB closed-loop bandwidth is "only" 200 kHz (Fig. 16, curve B), but it still achieves a locking time lower than 20 μs [Fig. 17(b)]. The same set of measurements that has been performed on the first PLL is reported in Fig. 19 for the second one. A PN plus spurs level lower than −130 dBc/Hz at 1-MHz offset is achieved, with a residual difference between curves C and A lower than 3 dB at all frequency offsets. All these measurements are in good agreement with simulations.

When channel $1/2^{20}$ is selected, the resulting quantization spurs are 17.5 Hz apart and the fractional tone is 35 Hz away from the carrier (too close to be detected in the measurement). For channels characterized by a fractional frequency lower than the loop bandwidth, so that no filtering action is occurring, but far enough from the carrier (e.g., channel $257/2^{20}$), a sharp tone can be identified at the fractional frequency (8.5 kHz for the channel $257/2^{20}$). In both chips, this tone is about −40 dBc when the linearization techniques of the PFD-CP described in Section VI are disabled (Fig. 20, curve A). In this condition a gain enhancement of about 8% in the charge versus phase error characteristic of the PFD-CP for small $\Delta\Phi$ (<250 ps) has been

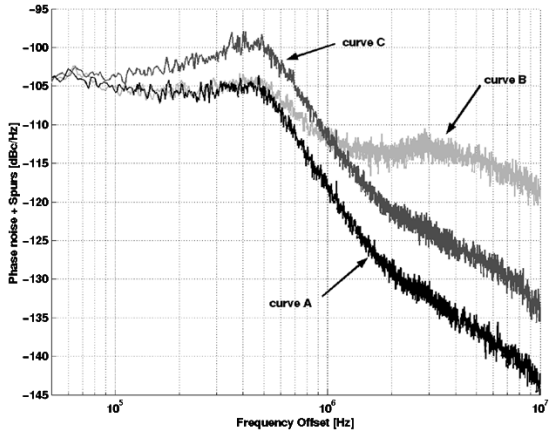

Fig. 18. Phase noise performance of the 700-kHz bandwidth synthesizer.

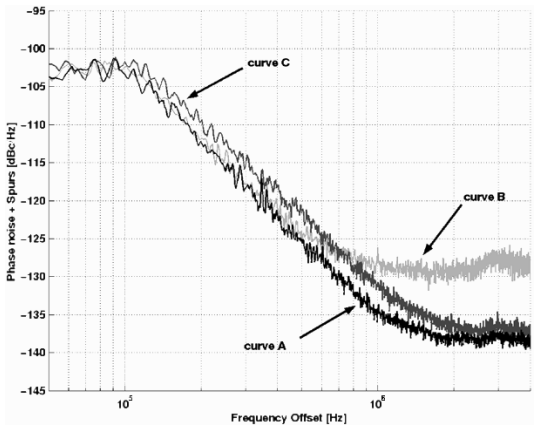

Fig. 19. Phase noise performance of the 200-kHz bandwidth synthesizer.

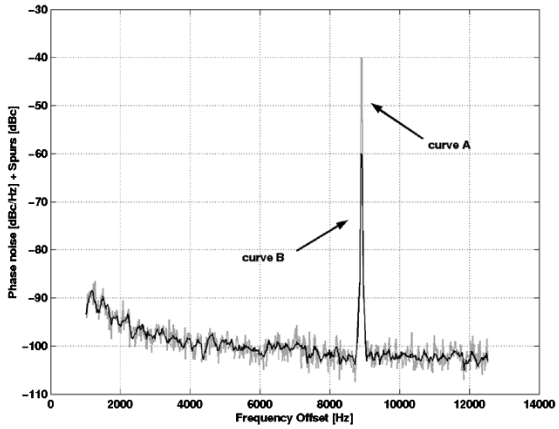

Fig. 20. Worst case in-band fractional spur level for the 700-kHz bandwidth synthesizer with linearization techniques disabled (curve A) and enabled (curve B).

measured. Including this effect in the simulations, an almost perfect agreement with measurements is observed. On the contrary, with both proposed linearization techniques enabled, the fully integrated PLL shows a worst case in-band measured fractional spur of −60 dBc (Fig. 20, curve B), whereas the chip with external loop filter and VCO achieves only −55 dBc. These values prove that the main cause for the fractional spur is no more the

TABLE I
MEASUREMENT RESULTS SUMMARY

	Fully integrated synthesizer	Synthesizer with external VCO and LF
Power consumption	28mW	15mW+VCO
Area in 0.18 μm CMOS (1)	1.9x1.8 mm^2	1.1x1.1 mm^2
Reference frequency	35MHz	35MHz
Output frequency resolution	35Hz	35Hz
3dB closed loop bandwidth	700kHz	200kHz
Locking time	~ 7μs	< 20μs
Worst case in-band fractional spur	-60dBc	-55dBc
Integrated PN plus spurs		
1kHz - 1.94 MHz	-45dBc	-50dBc
2.5MHz - 6.34 MHz	-65dBc	-71dBc
In-band PLL noise floor	-104dBc/Hz	-103dBc/Hz
PLL (VCO) noise floor at high frequency offsets	< -150dBc/Hz (2)	-138dBc/Hz

(1) including PADs and ESD protections
(2) measurement limited by instrument noise floor

linearity of the PLL building blocks but on-chip cross-talk for the fully integrated PLL, and on-board coupling for the version with external VCO. Since −60 dBc is a very good value, it can be stated that on-chip cross-talk is well under control. Fractional spur level is rarely reported in literature, especially the in-band one, although it is a critical parameter. Pamarti *et al.* [11] report similar measurements, but slightly out of band.

Comparing the achieved results with the specifications associated with a WCDMA receiver, the 700-kHz bandwidth synthesizer still has an excessive level of PN plus spurs, at least in the adjacent channel band. In fact, it achieves −45 dBc integrated PN plus spurs in the band from 1 kHz to 1.94 MHz and −65 dBc in the band from 2.5 to 6.34 MHz, versus the target specification of −40 dBc and −70 dBc, respectively. In principle, this performance can be improved implementing a slightly different shaping algorithm for the DAC quantization error and designing an integrated VCO with better PN. On the other hand, the 200-kHz bandwidth synthesizer fulfills the requirements in both specified bands. In fact, in this case, in the band from 1 kHz to 1.94 MHz the integrated PN plus spurs is −50 dBc, whereas in the band from 2.5 to 6.34 MHz it is −71 dBc.

The overall performance of the synthesizers is summarized in Table I.

VIII. CONCLUSION

A fully integrated fractional synthesizer characterized by a large loop bandwidth and a fine output frequency resolution has been presented. The test chip proves that the tradeoff between loop bandwidth and quantization spurs level, limiting the classical ΣΔ fractional PLL performance, can be partially broken using an adequate compensation scheme. A strong reduction of the fractional spur level has also been achieved, thanks to PFD-CP linearization techniques and controlling on-chip cross-talk. This is particularly useful for those channels where this spur falls inside the loop bandwidth and therefore cannot be attenuated by the loop filter. Though significantly improved by the above mentioned solutions, the resulting amount of PN plus spurs measured in the presented chip is still too high to allow its use in a real WCDMA application. However, a slight reduction of the bandwidth is enough to meet the required specifications. To further demonstrate this point, a second lower bandwidth PLL prototype, with external LF and VCO, has been realized and it fulfills the specifications also in the second band, where they are very tough.

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