29.3 Low-Power g_m-boosted LNA and VCO Circuits in 0.18µm CMOS

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As multi-channel transceivers emerge, there is a growing demand for CMOS RF front-end circuits that give state-of-the-art performance, consume less power, and exhibit robustness against PVT variations. Previously, the inductively degenerated commonsource LNA (CSLNA) and the cross-coupled LC VCO topologies were dominant. We propose the passively-coupled common-gate LNA (CGLNA) and Colpitts VCO configurations as alternatives. A CGLNA, a differential Colpitts VCO, and a quadrature VCO (QVCO) are presented that employ g_m -boosting with low current consumption.

A conventional CGLNA (Fig. 29.3.1a) has superior input matching, linearity, stability and robustness to PVT variations [1], but the inductively degenerated CSLNA achieves a lower noise figure (NF) at low operating frequencies. The input matching requirement of $g_{\rm m}R_{\rm s}=1$ for CGLNA bounds its noise factor at $F = 1+\gamma/\alpha$ where $\alpha = g_m/g_{d0}$. Clearly, α should be increased to decrease F. This seems infeasible because α is constrained at the device level. However, passive coupling techniques proposed herein allow the effective g_m to be increased without increasing g_{d0} . Figure 29.3.1b depicts the g_m -boosted scheme where an inverting gain from source to gate decouples g_m from g_{d0} . The effective transconductance at the input is increased to $(1+A)g_m$ and F is reduced to $1+\gamma/(1+A)\alpha$.

Noise issues prohibit active realizations of the inverting gain A. One possible passive implementation employs capacitor crosscoupling using inversions available in a differential topology [2]. However, a differential configuration consumes 2X more current and silicon area than a single-ended version, and the gate capacitance makes A < 1.

To minimize current consumption and realize $A \ge 1$, an on-chip transformer is used to achieve anti-phase operation between the source and gate terminals of M_1 (Fig. 29.3.1c). $A = kn = k \sqrt{L_s/L_p}$ is determined by the turns ratio n and the coupling factor k of transformer T_1 . The small-signal input admittance at the source is $Y_{in} \approx 1/sL_p + (1+kn)g_m + (1+2kn+n^2)sC_{gs}$. Assuming ideal magnetic coupling (k=1) and n=1:1, $Y_{in} \approx 1/sL_p + 2g_m + 4sC_{gs}$. Thus, the use of transformer coupling effectively doubles the transconductance and enables a 2X reduction in power consumption. In addition, Fis reduced to $1+\gamma/2\alpha$ under the new input matching condition $2g_m R_s = 1.$

LNA and VCO circuits share many similarities. For example, a Colpitts oscillator can be viewed as a common-gate amplifier in a positive feedback configuration. Its phase noise is superior to a cross-coupled VCO [3] because the noise current from active devices is injected into the *LC* tank when the tank voltage is minimum and the impulse sensitivity is low. However, poor start-up characteristics, high power consumption, lower tuning range and lack of differential operation have impeded its adoption. The design presented in [3] addresses these shortcomings through the use of a current-switching technique. We use the common-gate g_m -boosting techniques to overcome these drawbacks.

In order to realize a differential Colpitts oscillator with enhanced transconductance, the gate of one branch is connected to a node with an opposite voltage swing to that of the source. As depicted in Fig. 29.3.2a, the two branches can be capacitive cross-coupled. The resultant increase in transconductance eases the start-up requirement with lower power consumption than other techniques. The in-phase relationship between the source and drain voltages (via capacitive feedback with C_1 and C_2) also suggests an

alternative approach - to connect the gate to the drain of the other branch, resulting in the self-biased Colpitts configuration (Figure 29.3.2b). This topology has an effective transconductance of $-(2C_1C_2+C_2^2)g_m/(C_1+C_2)^2$, which is $(2+C_2/C_1)$ times higher than that of the standard Colpitts VCO. Furthermore, because the gate and source terminals are driven with anti-phase signals, faster commutation with better noise suppression from the differential pair is achieved.

In a standard cross-coupled VCO, the second harmonic present at the common-source node is modulated by the flicker noise from the differential pair and down-converted to the fundamental frequency, thus increasing the close-in phase noise [4]. This phenomenon does not arise in the proposed differential Colpitts topologies because there is no common-source node present, which leads to a superior close-in phase noise performance.

Finally, applying series coupling [4] to the VCO of Fig. 29.3.2b leads to the Colpitts QVCO of Fig. 29.3.2c. Optimization of the QVCO involves sizing both the switching and coupling transistors to achieve efficient current switching with minimal phase noise. On-chip transformers are used to avoid long interconnect lines and to obtain higher Q (≈ 10) than with the inductors (Q ≈ 8) used in the VCO. Active tail current sources are used rather than resistors in the VCO/QVCO for better robustness at the expense of higher flicker noise.

A prototype chip is fabricated in a standard 6-metal 0.18µm CMOS RF process. For the $g_{\rm m}$ -boosted CGLNA, a transformer turns ratio of 1:1 is chosen for demonstration purposes. Further reduction in NF is possible with A>1 using a larger turns ratio. The measured S-parameters (Fig. 29.3.3) show S₂₁ of 9.4dB peaking at 5.8GHz. The LNA draws only 1.9mA from 1.8V owing to the g_m -boosting technique. Measured IIP3 is 7.6dBm and NF at maximum gain is 2.5dB (Fig. 29.3.4). The proposed LNA has an excellent FOM compared to competing designs (Fig. 29.3.6). It is noted that some common-source designs achieve better noise performance at higher power consumption and with off-chip components.

The Colpitts differential VCO (Fig. 29.3.2b) operates at a center frequency of 1.79GHz with a tuning range of 22% while the Colpitts QVCO (Fig. 29.3.2c) operates from 1.83GHz to 2.24GHz for a 20% tuning range. Figure 29.3.5 shows measured phase noise plots of the VCO/QVCO. The VCO has a phase noise of -97dBc/Hz at 50kHz offset and -128dBc/Hz at 1MHz offset. It draws 3.6mA from a 2.0V supply. The QVCO draws only 4.3mA from 2.0V to attain a close-in phase noise of -104dBc/Hz at 50kHz offset. Its phase noise at 1MHz offset is -127dBc/Hz. Figure 29.3.6 compares its FOM to existing designs. The chip micrograph is shown in Fig. 29.3.7.

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