3.2 A 6.4Gb/s CMOS SerDes Core with Feedforward and Decision-Feedback Equalization

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Increasing clock rates of processing cores with continuing advances in silicon technology drives the need to push inter-chip I/O to ever higher data rates. As industry-standard data rates pass 3Gb/s and approach the 6+Gb/s to 11+Gb/s [1] realm, degradations from channel effects such as bandwidth loss, reflections, and crosstalk can distort the signal to such an extent that reliable data recovery requires equalizer-based I/O core designs [2]. In this paper, the architecture and design of key components of a CMOS 4.9 to 6.4Gb/s 2-level SerDes I/O core which employs a 4-tap feed-forward equalizer (FFE) in the transmit section and a 5-tap decision-feedback equalizer (DFE) in the receive section, is described. A single PLL macro drives up to 4 TX/RX pairs and generates the reference 4.9 to 6.4GHz clock for the system. The design is realized in 0.13μm CMOS technology using Cu/Al interconnects.

A diagram of the transmitter is shown in Fig. 3.2.1. To minimize diffusion capacitance load at the driver output, the FFE tap weights are sized to maximum weights of 0.25, 1.0, 0.5, and 0.25 for the pre-cursor through final tap settings. If a desired FFE setting cannot be contained within the fixed tap weight range, the main cursor tap can be backed off from full-scale to accommodate the FFE setting. The tap weights can be either programmed to fixed values or optionally adapted on power-up using an up-channel link protocol. An automatic level control algorithm scales the transmit drive level so the peak-to-peak output voltage maintains a fixed programmed setting as tap values change. The driver swings up to $1200mV_{ppd}$ into a 100Ω differential load. A typical 6.4Gb/s transmission demonstrates a total jitter (TJ) of $34ps_{pp}$ for BER <1E-12.

The receiver features a variable-gain amplifier (VGA), DFE, and phase-rotator-based CDR loop as shown in Fig. 3.2.2. The VGA enables linear (<1dB compression) operation on up to $1200mV_{ppd}$ input signals. To improve linearity of the VGA for high input levels, the received signal is split into full-amplitude and half-amplitude paths by using a resistive divider in the 50Ω termination network as shown in Fig. 3.2.2. Each path drives a separate switched-gain amplifier as shown in Fig. 3.2.3. Gain is adjusted by setting the degeneration resistance of each amplifier to one of the 8 values using thermometer-coded switched-R networks, resulting in 16 VGA steps with a targeted gain range from 0.5 to 3. For large input levels, the bias current to the full-amplitude path amplifier is biased off, while for small signals both amplifiers are biased on. To enable gain adjustment without corrupting data, the full-amplitude path VGA bias is switched on and off with a slow time constant.

The VGA drives a second-stage peaking amplifier that is used to provide additional gain and add a programmable amount of high-frequency peaking. A simplified diagram of the peaking amplifier is shown in Fig. 3.2.4. The peaking level is adjusted by controlling the tail current to two amplifiers, one with a fixed 6dB peak and one with no peaking. No bias to the 6dB peaking amp and full bias to the second amplifier produces no peaking, while full bias on the 6dB peaking amp and no bias on the second amplifier gives maximum peaking. Both the peaking amount (0 to 6dB) and pole position, which sets the frequency location of the peak, can be varied in 16 steps.

A conceptual diagram of the DFE system is shown in Fig. 3.2.2. The DFE sums a compensation value to the received signal as a function of prior received data bits and associated tap weights. DFE correction is added to the signal by pulling weighted currents down on either the ± leg of a differential amplifier output using current switches as shown in Fig. 3.2.5. The tail current magnitudes in the current switches set the desired tap weight. Pass-gates are used to XOR the data value with the tap weight sign. The tap weights are generated using a sign-error driven adaptation algorithm. Capacitive degeneration in the summer circuit is used to add high-frequency peaking to extend the bandwidth of the summers while minimizing power draw. The cascaded VGA, peaking amplifier, and DFE summation sections achieve a gain of 3 with 3dB bandwidth of 3.2GHz and 1-dB compression point of 300mV with a minimum supply voltage of 1V.

The PLL core generates the 4.9 to 6.4GHz system clock. The PLL employs an LC-tank [3] based VCO design with 16 overlapping coarse-tune bands to lower VCO tuning sensitivity and minimize jitter while covering the 4.9 to 6.4GHz band. Measurements have demonstrated clock jitter in the range of 0.4ps to 1ps rms over an integration bandwidth of 6MHz to 3.2GHz. The receiver divides the full-rate clock from the PLL by 2 to produce half rate I/Q outputs as shown in Fig. 3.2.2. The I/Q signals drive two 4-quadrant phase rotators that produce data and edge latch clocks with phase controllable from 0 to 360 degrees. For simplicity, only one edge/data latch is illustrated in Fig. 3.2.2, although it is understood that the ½-rate design requires data and edge latches for both true and complementary phases of the rotator outputs. A digital CDR algorithm with tracking bandwidth of 6MHz continually updates the rotator phase shifts at a rate of approximately 800MS/s to maintain the desired data sampling point in the presence of frequency offset or time jitter on the received data.

The described system demonstrates error-free operation at 6.25Gb/s on a lossy transmission-line channel with an attenuation of 32dB at 3.125GHz using FFE/DFE. A legacy backplane channel with 25dB loss at 3.125GHz runs error free with receiver DFE-only equalization. Eye diagrams at the receiver sample latch for each of these conditions are shown in Fig. 3.2.6. This level of performance predicts reliable operation at 6.4Gb/s data rate over a wide range of challenging application channels in the high-speed I/O industry. A die micrograph of a 4-port TX/RX core with PLL slice is shown in Fig. 3.2.7.

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[2] J. Jaussi et al., "An 8Gb/s Source-Synchronous I/O Link with Adaptive Receiver Equalization, Offset Cancellation and Clock Deskew," *ISSCC Dig. Tech. Papers,* pp. 246-247, Feb., 2004.
[3] H. Ainspan et al., "A Comparison of MOS Varactors in Fully Integrated CMOS LC VCO's at 5 and 7GHz," *ESSCIRC*, pp. 448-451, Sept., 2000.

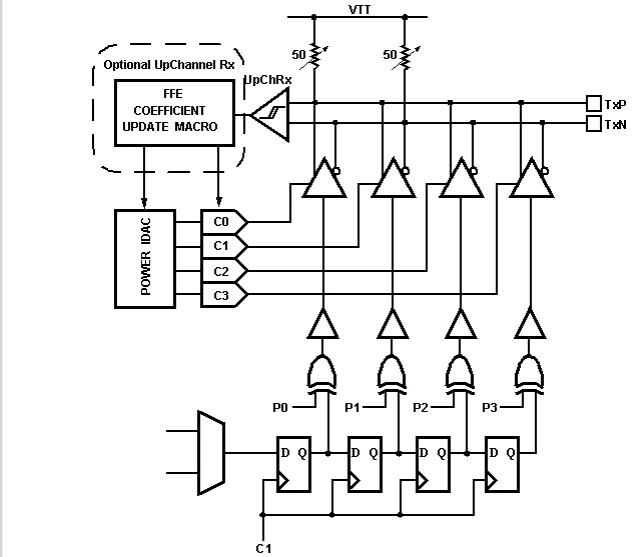

Figure 3.2.1: Transmitter with 4-tap FFE.

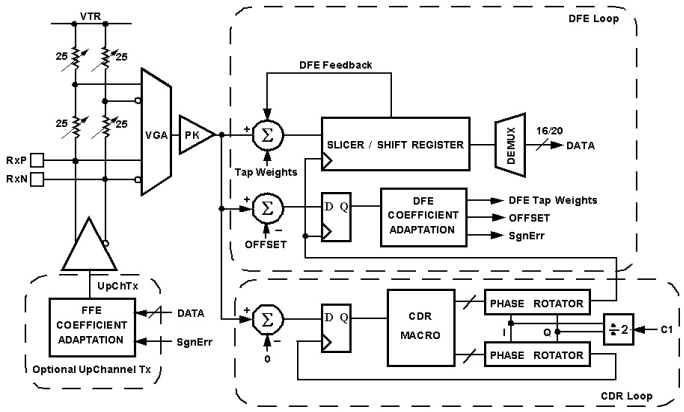

Figure 3.2.2: Receiver with 2-path VGA and 5-tap DFE.

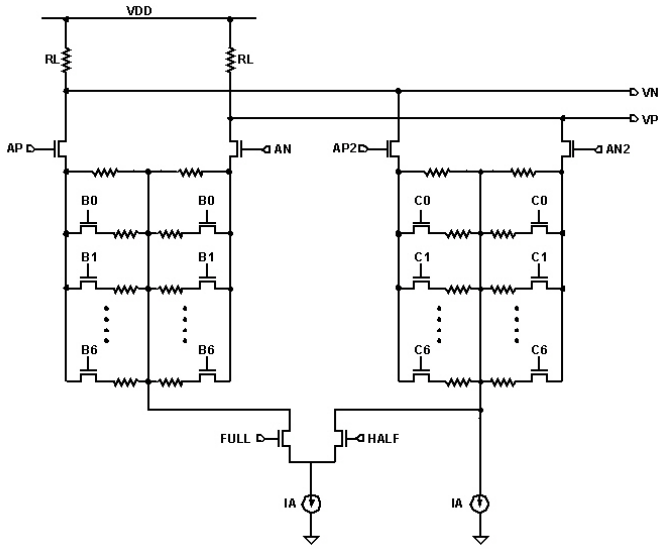

Figure 3.2.3: Circuit diagram of 2-path VGA.

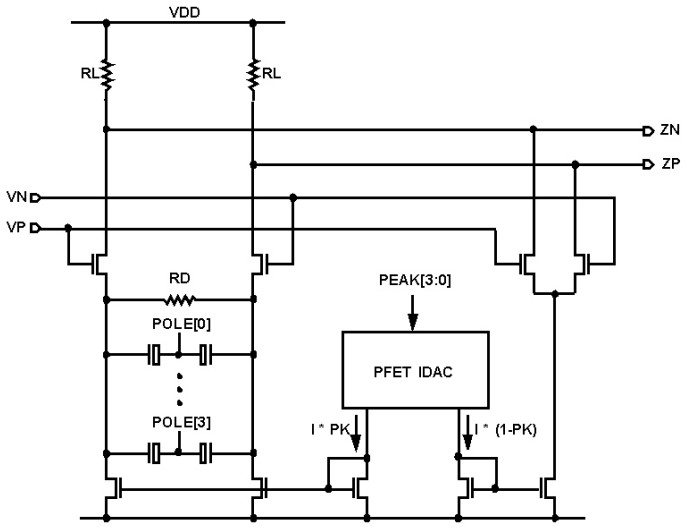

Figure 3.2.4: Circuit diagram of peaking amp.

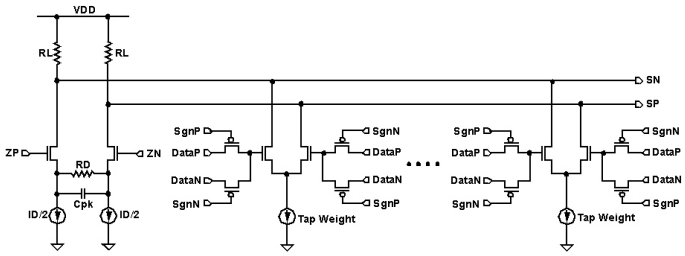

Figure 3.2.5: Circuit diagram of multiple-tap DFE summer.

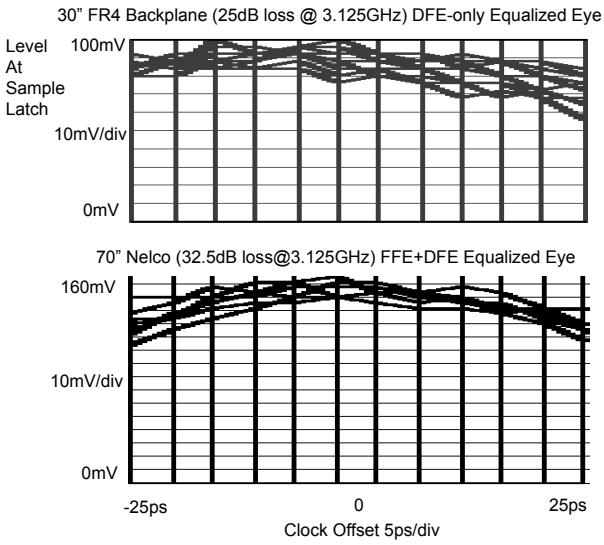

Figure 3.2.6: Receiver equalized signal at 6.25Gb/s.

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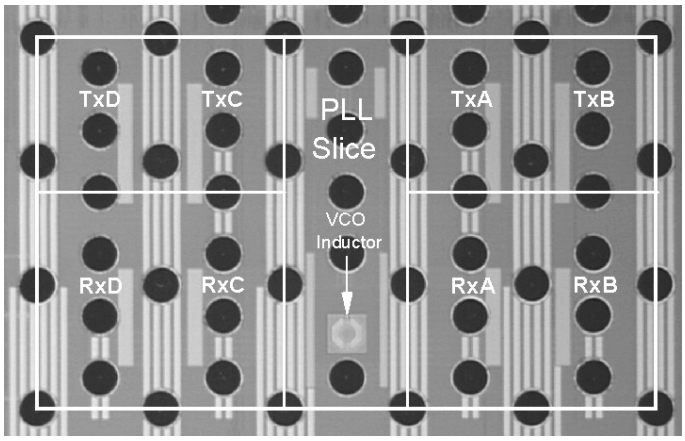

Figure 3.2.7: Die micrograph of 4-port TX/RX core.

