G_m-Boosted Common-Gate LNA and Differential Colpitts VCO/QVCO in 0.18-μm CMOS

Xiaoyong Li, *Member, IEEE*, Sudip Shekhar, *Student Member, IEEE*, and David J. Allstot, *Fellow, IEEE*

***Abstract*—The demand for radio frequency (RF) integrated circuits with reduced power consumption is growing owing to the trend toward system-on-a-chip (SoC) implementations in deep-sub-micron CMOS technologies. The concomitant need for high performance imposes additional challenges for circuit designers. In this paper, a g_m-boosted common-gate low-noise amplifier (CGLNA), differential Colpitts voltage-controlled oscillators (VCO), and a quadrature Colpitts voltage-controlled oscillator (QVCO) are presented as alternatives to the conventional common-source LNA and cross-coupled VCO/QVCO topologies. Specifically, a g_m-boosted common-gate LNA loosens the link between noise factor (i.e., *noise match*) and input matching (i.e., *power match*); consequently, both noise factor and bias current are simultaneously reduced. A transformer-coupled CGLNA is described. Suggested by the functional and topological similarities between amplifiers and oscillators, differential Colpitts VCO and QVCO circuits are presented that relax the start-up requirements and improve both close-in and far-out phase noise compared to conventional Colpitts configurations. Experimental results from a 0.18-μm CMOS process validate the g_m-boosting design principle.**

***Index Terms*—Colpitts VCO, low-noise amplifier, noise figure, phase noise, quadrature VCO, radio frequency integrated circuits, transformer, voltage-controlled oscillator.**

I. Introduction

EXPLOSIVE growth in wireless communication during the last decade has created a burgeoning demand for low cost system-on-chip transceivers. Concurrently, the exponential scaling of CMOS has fueled a drive toward more digital signal processing functionality integrated with radio frequency (RF) front-end and mixed-signal baseband circuitry. A key goal is the realization of state-of-the-art RF front-end circuits that consume lower power per function for emerging portable applications dictated by stringent wireless standards [1]. Another challenge is the design of RF front-end circuits such as the low-noise amplifier (LNA) and voltage-controlled oscillator (VCO) (used in the direct conversion receiver front-end of Fig. 1) that have low noise properties and are robust to process, voltage, and temperature (PVT) variations. This paper addresses the goal of designing for simultaneous low noise and low power in RF LNA and VCO circuits. The design principles, validated in 0.18-μm CMOS prototypes, are also applicable to RF circuit designs that employ other technologies.

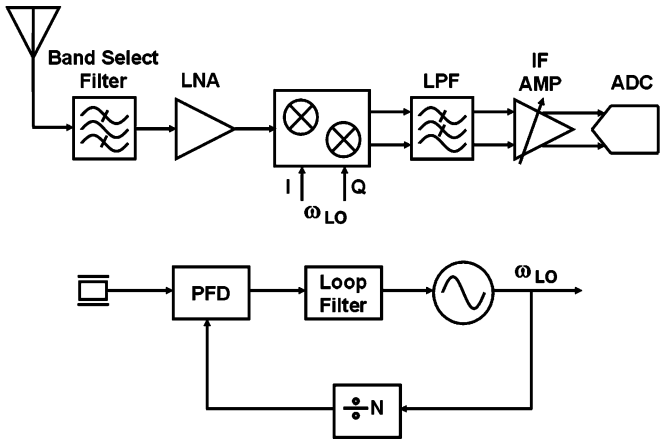


Fig. 1. A typical direct conversion receiver front end (top) and a simple integer-*N* frequency synthesizer loop (bottom).

Section II compares the conventional common-source and common-gate topologies. To retain the advantages of the common-gate configuration and overcome its deficiencies, a g_m-boosting scheme applied to a common-gate LNA (CGLNA) breaks the traditional link between input matching and noise figure, and leads to a simultaneous reduction in noise and power dissipation. Section III details differential Colpitts VCO and quadrature VCO (QVCO) circuits that ease the well-known start-up difficulties of the conventional Colpitts topology. The faster switching associated with the differential configuration improves the phase noise characteristics. In Section IV, experimental results from 0.18-μm CMOS prototypes are presented.

II. G_m-Boosted Common-Gate Low Noise Amplifier

A. Principle of Operation

Designing an RF low-noise amplifier for wireless applications involves several challenges [2]. The LNA must provide sufficient gain to boost the weak RF input signal received from the antenna. To ensure proper operation of the off-chip band-select filter that interfaces the antenna to the LNA, it should exhibit resistive input impedance (typically 50 Ω) over the frequency band of interest; errors in the terminating impedance may result in substantial performance degradations. It should also add minimum noise in the RF signal path while synthesizing the input impedance; this precludes simple-minded approaches such as shunting a 50 Ω resistor to ground at the input. LNA design is

Manuscript received April 26, 2005; revised July 15, 2005. This work was supported by the National Science Foundation under Contracts CCR-0086032 and CCR-0120255, and by the Semiconductor Research Corporation under Contracts 2001-HJ-926 and 2003-TJ-1093.

X. Li was with the Department of Electrical Engineering, University of Washington, Seattle, WA 98195 USA. He is now with Qualcomm Incorporated, San Diego, CA 92121 USA (e-mail: xyli@qualcomm.com).

S. Shekhar and D. J. Allstot are with the Department of Electrical Engineering, University of Washington, Seattle, WA 98195 USA (e-mail: allstot@ee.washington.edu).

Digital Object Identifier 10.1109/JSSC.2005.857426

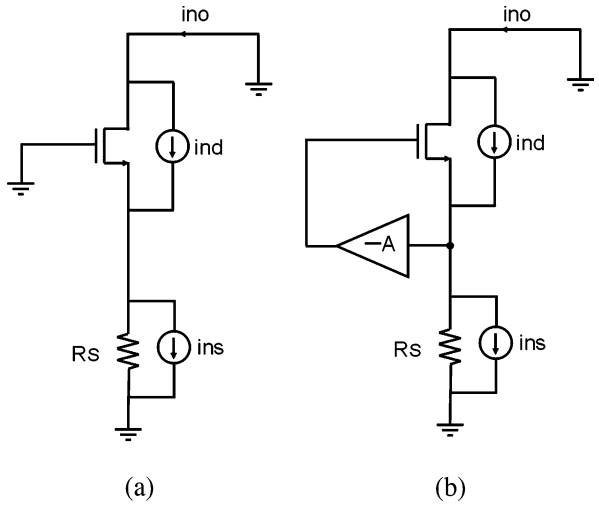


Fig. 2. (a) Conventional, and (b) g_m-boosted common-gate LNA topologies.

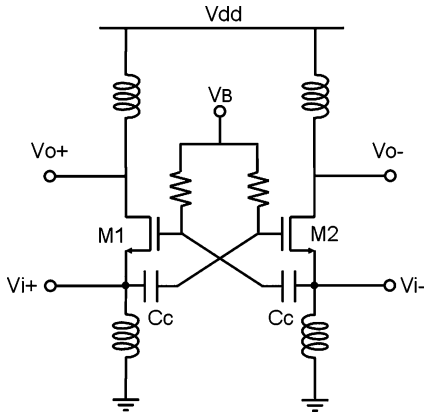


Fig. 3. Capacitor cross-coupled common-gate LNA configuration.

further complicated by tradeoffs among linearity, stability, reverse isolation, robustness to PVT variations, power consumption, etc.

The inductor-degenerated common-source LNA (CSLNA) is a popular choice for narrow-band applications as it provides both high gain and relatively low noise [3]. However, the induced gate noise of the input transistor may be significant because it is enhanced by the quality factor (Q) of the series resonant input matching circuit [3]. The minimum degeneration inductance (L_S) is limited in single-ended implementations as the MOSFET cutoff frequency $f_{\rm T}$ increases due to parasitic bond wire inductance to ground. A fully differential topology eases this limitation at a cost of twice the silicon area and power consumption. In general, low noise is achieved using high power consumption and/or high-Q off-chip inductors.

The common-gate LNA topology is attractive because the resistive input impedance match is realized as $1/g_m$ of the input transistor. Compared to the common-source LNA, the common-gate configuration features superior broadband input match, linearity, stability and robustness to PVT variations [4]. However, its noise factor is limited in accordance with the $1/g_m$ input match. To appreciate this point, consider a basic common-gate LNA [Fig. 2(a)]. The dominant noise sources are the noise current, $i_{\rm ns}$, of the source resistance and the drain current noise, $i_{\rm nd}$, of the MOSFET; induced gate noise is usually negligible in a CGLNA circuit. Small-signal analysis reveals the noise factor F:

$$F = 1 + \frac{\overline{i_{nd}^2}\cdot\left(\dfrac{1}{1+g_mR_S}\right)^2}{\overline{i_{nS}^2}\cdot\left(\dfrac{g_mR_S}{1+g_mR_S}\right)^2} = 1 + \frac{\overline{i_{nd}^2}}{\overline{i_{nS}^2}}\left(\frac{1}{g_mR_S}\right)^2 \quad (1)$$

With $\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f$, $\overline{i_{nS}^2} = 4kTR_S^{-1}\Delta f$ and $\alpha = g_m/g_{d0}$, (1) reduces to

$$\begin{aligned} F &= 1 + \frac{4kT\gamma g_{d0}\Delta f}{4kTR_S^{-1}\Delta f}\left(\frac{1}{g_mR_S}\right)^2 \\ &= 1 + \frac{\gamma g_{d0}}{g_m^2R_S} = 1 + \left.\frac{\gamma}{\alpha}\right|_{g_mR_S=1} \end{aligned} \quad (2)$$

where α and γ are empirical process- and bias-dependent parameters.

The analysis above reinforces the notion of a tight link between input matching and noise factor in a conventional CGLNA; i.e., constrained by the input matching condition, $g_mR_S = 1$, g_m cannot be increased arbitrarily to reduce the noise factor. However, the possibility of improved noise performance arises if a decoupling mechanism is introduced between the input matching and noise figure characteristics. From another viewpoint, α in (2) should be effectively increased to decrease F. This seems infeasible as $\alpha = g_m/g_{d0}$ is constrained at the device level. As shown below, however, the goal is met by increasing the effective g_m while keeping g_{d0} unchanged.

When an inverting gain, A, is inserted between gate and source terminals as shown in Fig. 2(b), the effective g_m is boosted to $(1+A)g_m$, and as a consequence, the noise factor F is reduced to [5], [6]

$$\begin{aligned} F &= 1 + \frac{4kT\gamma g_{d0}\Delta f}{4kTR_S^{-1}\Delta f}\left(\frac{1}{(1+A)g_mR_S}\right)^2 \\ &= 1 + \frac{\gamma g_{d0}}{(1+A)^2g_m^2R_S} \\ &= 1 + \left.\frac{\gamma}{\alpha(1+A)}\right|_{(1+A)g_mR_S=1}. \end{aligned} \quad (3)$$

Note that the new structure provides the same resistive input impedance using less bias current in accordance with $(1+A)g_mR_S = 1$. In the g_m-boosted common-gate configuration, smaller bias current means less channel noise from the input transistor (or g_{d0}) and a correspondingly smaller noise contribution.

There are several possible ways to implement the inverting gain, A, but noise issues discourage active realizations and make passive implementations more attractive. The capacitor cross-coupling technique of Fig. 3, where the inversion is naturally available in the differential configuration [7], is a special case of the general scheme depicted in Fig. 2(b). It has two drawbacks: it consumes twice the bias current and silicon area as its single-ended counterpart, and A is always less than one due to the capacitor divider between C_{gs} and coupling capacitance $C_{\rm C}$.

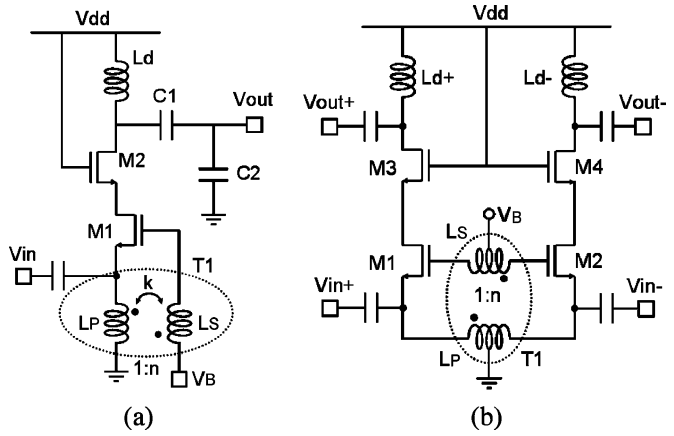


Fig. 4. Transformer-coupled g_m-boosted common-gate LNA topologies: (a) single-ended, and (b) fully differential.

B. Transformer-Coupled g_m-Boosted CGLNA

The desire to realize an inverting gain, A, greater than one motivates the transformer-coupled g_m-boosted CGLNA single-ended [Fig. 4(a)] and fully differential [Fig. 4(b)] circuits. Transformer T_1 [Fig. 4(a)] consists of primary and secondary inductors, L_P and L_S, respectively. Magnetic coupling between L_P and L_S provides anti-phase operation between the gate and source terminals, effectively enhancing the transconductance at the source of M_1. V_B produces an AC ground for L_S and a proper DC bias for M_1. Cascode transistor M_2 is added to improve reverse isolation between the input and output ports at the cost of additional noise. Load inductor L_D, along with C_1 and C_2 form a tapped-capacitor impedance matching network at the output.

The input impedance of the transformer-coupled CGLNA is found using the small-signal model of Fig. 5 wherein the transformer model of [8] is adopted and the MOSFET body effect is neglected. Applying KCL at node S with mutual inductance, M, between the primary and secondary windings yields

$$i_x + g_m v_{gs} - i_S = \frac{M i_S}{L_P} + \frac{v_x}{sL_P} \tag{4}$$

$$i_S = \frac{v_g}{sL_S} + \frac{M i_P}{L_S} \tag{5}$$

$$v_{gs} = -\frac{i_S}{sC_{gs}} \tag{6}$$

$$i_P = \frac{M i_S}{L_P} + \frac{v_x}{sL_P} \tag{7}$$

$$v_g = v_x + v_{gs}. \tag{8}$$

Solving (4)–(8) with coupling coefficient $k = M/\sqrt{L_P L_S}$ and turns ratio $n = \sqrt{L_S/L_P}$ gives the input admittance

$$\begin{aligned} Y_{\text{in}} &= \frac{i_x}{v_x} \\ &= \frac{1}{sL_P} \cdot \frac{1 + \frac{k}{n} g_m s L_S + \left(1 + \frac{k}{n}\right) s^2 L_S C_{gs}}{1 + (1-k^2) s^2 L_S C_{gs}} + \frac{1}{sL_S} \\ &\quad \cdot \frac{g_m s L_S + (1+nk) s^2 L_S C_{gs}}{1 + (1-k^2) s^2 L_S C_{gs}}. \end{aligned} \tag{9}$$

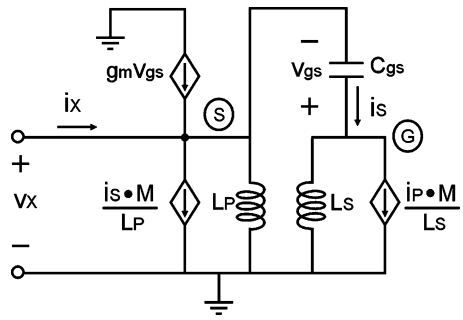


Fig. 5. Small-signal model for transformer-coupled g_m-boosted CGLNA analysis.

For modern IC technology, the coupling coefficient is typically in the range of 0.6–0.9. Hence, $|(1-k^2)\, s^2 L_S C_{gs}| \ll 1$, and (9) reduces to

$$\begin{aligned} Y_{\text{in}} \approx \frac{1}{sL_P} + \frac{k}{n} g_m \cdot \frac{L_S}{L_P} + \left(1 + \frac{k}{n}\right) sC_{gs} \\ \cdot \frac{L_S}{L_P} + g_m + (1+nk) sC_{gs}. \end{aligned} \tag{10}$$

With $n^2 = L_S/L_P$, (10) becomes

$$Y_{\text{in}} \approx \frac{1}{sL_P} + (1+nk) g_m + (1 + 2nk + n^2) sC_{gs}. \tag{11}$$

Thus, the inverting gain factor, $A = kn = k\sqrt{L_S/L_P}$, is determined by the turns ratio and the coupling factor; i.e., the transformer-coupled configuration provides an additional degree of freedom in setting the value of A. It is seen from (11) that transformer coupling increases the effective transconductance by $(1+nk)$. Equation (11) has a clear physical meaning: the input impedance of the g_m-boosted CGLNA can be viewed as a parallel-resonant RLC circuit, in contrast to the series-resonant circuit characteristic of CSLNA, where

$$L = L_P \tag{12}$$

$$C'_{gs} = (1 + 2nk + n^2) C_{gs} \tag{13}$$

$$G_m = (1+nk) g_m. \tag{14}$$

In the case of ideal magnetic coupling with $k = 1$ and $n = 1:1$, the input admittance is

$$Y_{\text{in}} \approx \frac{1}{sL_P} + 2g_m + 4sC_{gs}. \tag{15}$$

Owing to g_m boosting, the CGLNA noise factor is reduced to $F \approx 1 + \gamma/\alpha(1+nk)$, neglecting induced gate noise, under the input matching condition $(1+nk) g_m R_S = 1$. This suggests that increases in A reduce F to an arbitrarily low value, which is not correct. When induced gate noise is considered, F is (as discussed in the Appendix)

$$F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1+nk} + \frac{\delta\alpha}{5} \cdot \left(\frac{\omega}{\omega_T}\right)^2 \cdot \frac{(1 + 2nk + n^2)^2}{(1+nk)^3}. \tag{16}$$

Equation (16) suggests that k should be maximized to minimize F. Simplification of (16) assuming an ideal coupling coefficient of $k = 1$ gives

$$F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1+n} + \frac{\delta\alpha}{5} \cdot \left(\frac{\omega}{\omega_T}\right)^2 \cdot (1+n). \tag{17}$$

The effect of g_m boosting by transformer coupling on F is clearly seen from (17); i.e., channel noise is reduced by $(1+n)$ while induced gate noise is increased by the same factor. Thus, the optimum turns ratio occurs where the contributions of channel noise and gate noise are equal. Setting $\partial F/\partial n = 0$ results in

$$n_{opt} = \left(\frac{\omega_T}{\omega}\right) \cdot \sqrt{\frac{5\gamma}{\delta\alpha^2}} - 1. \tag{18}$$

The corresponding optimum noise factor F is

$$F_{opt} \approx 1 + 2\sqrt{\frac{\delta\gamma}{5}} \cdot \left(\frac{\omega}{\omega_T}\right). \tag{19}$$

Note that the optimum noise factor in (19) assumes a power-matched condition, which is therefore higher than the minimum noise factor, $F_{\min}$, obtained for the noise-matched case. Nonetheless, excellent noise performance is achieved from the g_m-boosted CGLNA. The conventional CGLNA is a special case of the g_m-boosted CGLNA with $n = 0$. Hence, from (16) or (17), its F value is

$$F = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5} \cdot \left(\frac{\omega}{\omega_T}\right)^2. \tag{20}$$

In practice, nonidealities associated with an on-chip transformer limit improvement with increased n. Recall that the secondary inductance of the transformer scales quadratically with n. Hence, both the parasitic resistance and capacitance of the secondary scale similarly. Losses associated with these parasitic elements at the gate of the transistor manifest as increased noise at the output. A large value of n is also not feasible because of the corresponding restrictions on the self-resonant frequency. Finally, practical considerations limit A between 2 and 3 to achieve the optimal noise factor.

III. Differential Colpitts VCO and Quadrature VCO Circuits

A. Differential Colpitts VCOs

Amplifier and oscillator circuits share many similarities in that an oscillator can be viewed as an amplifier configured in positive feedback fashion. More specifically, a cross-coupled oscillator [Fig. 6(a)] is essentially a two-stage common-source amplifier and a Colpitts oscillator [Fig. 6(b)] is basically a one-stage common-gate amplifier. The cross-coupled VCO in CMOS has attracted considerable interest due to its easy start-up and good phase noise characteristics [9]–[13]. On the other hand, the Colpitts configuration features superior phase noise because noise current from the active devices is injected into the LC tank during minima of the tank voltage when the impulse sensitivity is low [14], [15]. Unfortunately, the conventional Colpitts VCO suffers from poor start-up characteristics; i.e., higher power consumption is needed to ensure reliable start-up in the presence of standard PVT variations. The capacitor feedback network also reduces its tuning range. Finally, the lack of differential outputs needed to suppress common-mode coupling such as that from substrate, etc., has impeded its adoption in CMOS.

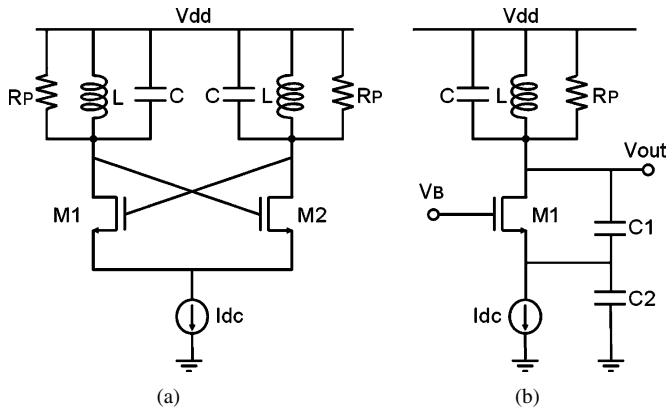


Fig. 6. (a) Cross-coupled and (b) Colpitts VCOs.

The synthesis of a differential Colpitts oscillator using a current-switching technique was described in [16]. Based on the similarities between amplifiers and oscillators, alternative approaches to overcome the difficult start-up shortcoming are presented herein. Section II showed that simply connecting the gate terminal in a conventional common-gate configuration to a DC bias voltage is inefficient and this certainly applies to the conventional Colpitts oscillator of Fig. 7(a). As described above, coupling the signal from the source to gate terminal enhances the effective transconductance, and improves the start-up behavior of the Colpitts oscillator. The first step in synthesizing a circuit with improved start-up performance is to float the gate node [Fig. 7(b)]. The next step is to apply the appropriate signal to the gate. Note that such an inverted signal does not exist in the single-ended version of Fig. 7(b).

Bearing in mind that a differential Colpitts oscillator is to be synthesized with enhanced effective transconductance, the intermediate differential version of Fig. 7(c) follows in which the required inversion is readily available. Next, the gate nodes are connected to the source nodes of the opposite sides as in the g_m-boosted CGLNA. This leads to the conceptual differential Colpitts VCO in Fig. 7(d). Finally, DC bias circuitry including blocking capacitors and bias resistors is added leading to the capacitor cross-coupled Colpitts VCO in Fig. 7(e).

The in-phase relationship between the source and drain voltages via the capacitive feedback suggests an alternative topology: the gates and drains of M_1 and M_2 can be directly cross-coupled, resulting in the differential Colpitts configuration shown in Fig. 8. Compared to the circuit of Fig. 7(e), the differential Colpitts VCO is self-biased and requires no blocking capacitors and bias resistors.

The small-signal admittance looking into the drain of M_1 or M_2 of the differential Colpitts VCO in Fig. 8 is

$$Y_{\text{in}} = \frac{s^2 C_1 C_2 - g_m s C_2}{g_m + s(C_1 + C_2)}. \tag{21}$$

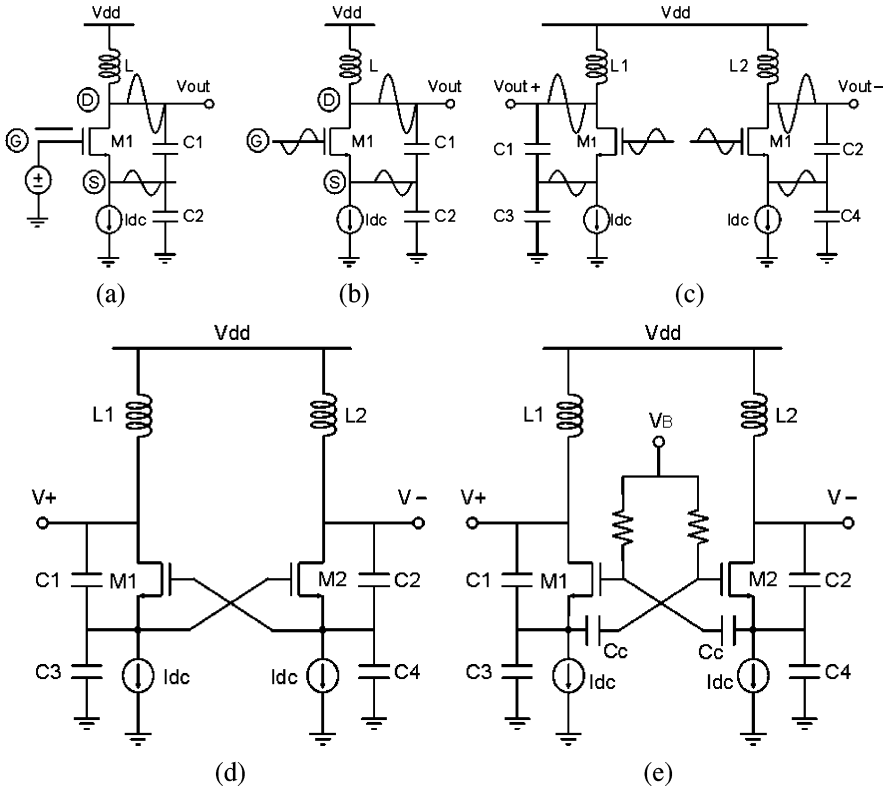


Fig. 7. Evolution of the differential Colpitts oscillator: (a) conventional, (b) with floating gate terminal, (c) differential with floating gate terminals, (d) capacitor cross-coupled, and (e) capacitor cross-coupled with DC bias and blocking circuitry.

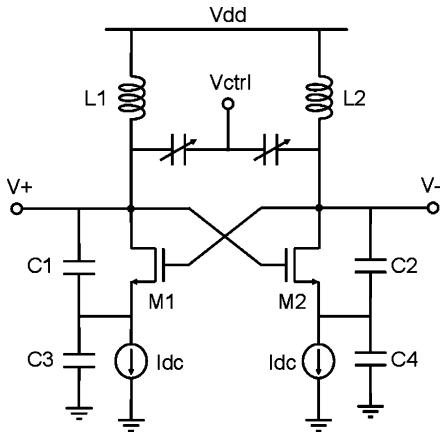


Fig. 8. Differential Colpitts VCO circuit no. 1 (VCO1).

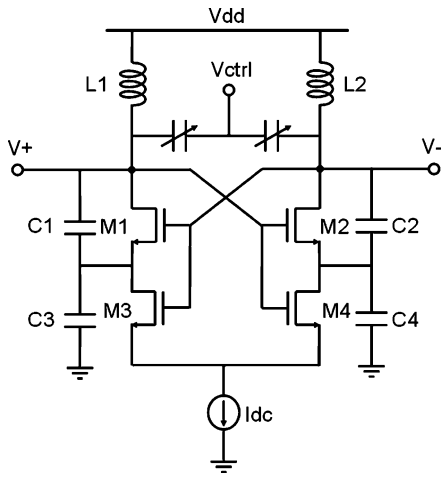


Fig. 9. Differential Colpitts VCO no. 2 (VCO2).

The real and imaginary parts are

$$\mathrm{Re}[Y_{\mathrm{in}}] = -\frac{g_m\omega^2 C_2[2C_1 + C_2]}{g_m^2 + \omega^2(C_1 + C_2)^2} \tag{22}$$

$$\mathrm{Im}[Y_{\mathrm{in}}] = j\frac{\omega^3 C_1 C_2[C_1 + C_2] - g_m^2\omega C_2}{g_m^2 + \omega^2(C_1 + C_2)^2}. \tag{23}$$

Recall that the negative small-signal conductance in the conventional Colpitts oscillator is

$$\mathrm{Re}[Y_{\mathrm{in}}] = -\frac{g_m\omega^2 C_1 C_2}{g_m^2 + \omega^2(C_1 + C_2)^2}. \tag{24}$$

Comparing (22) and (24), it is seen that the negative conductance generated in the new differential Colpitts VCO is increased by $(2 + \mathrm{C_2/C_1})$ compared to that of the conventional Colpitts VCO. Hence, the power consumption needed to ensure reliable start-up is reduced. Note that this factor can be recast as $1 + A$ where $A = 1 + C_2/C_1$ is the g_m-boosting factor.

Another benefit of the differential Colpitts VCO is faster switching of M_1 and M_2, which is needed to suppress noise contributions from the active devices during the zero-crossings of the tank voltage to improve the phase noise characteristics.

The two current sources in Fig. 8 can be combined using M_3 and M_4 as shown in Fig. 9. This arrangement is similar to the current switching technique described in [16]. The main difference is that the gates of M_3 and M_4 in Fig. 9 are connected

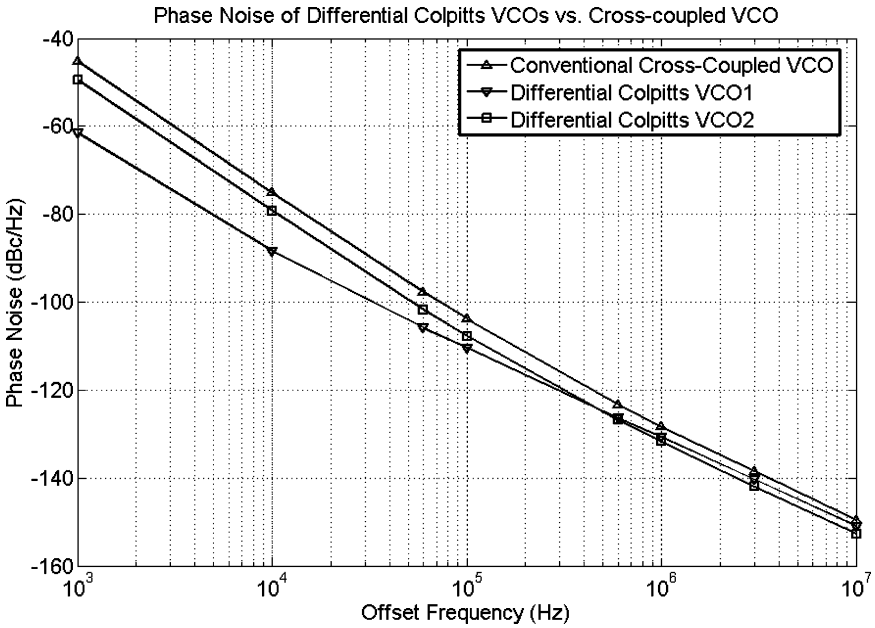


Fig. 10. Simulated phase noise comparison between conventional cross-coupled VCO [Fig. 6(a)] and differential Colpitts VCO circuits VCO1 (Fig. 8) and VCO2 (Fig. 9).

directly to the VCO outputs to relax the voltage headroom requirements.

The conventional cross-coupled VCO, the differential Colpitts VCO in Fig. 8 (VCO1), and the differential Colpitts VCO in Fig. 9 (VCO2) are designed and simulated using Cadence SPECTRE. The three oscillators are designed to operate at the same frequency (1.66 GHz) with the same total bias current. Each VCO uses the same inductance values and the MOSFETs are sized for minimum phase noise. The simulated phase noise characteristics are compared in Fig. 10. The differential Colpitts VCO1 has superior close-in phase noise and the differential Colpitts VCO2 has the best far-out phase noise.

B. Colpitts Quadrature VCO

Quadrature down-conversion is often required in direct conversion, image reject and wide-band IF receiver architectures. There are several ways to achieve quadrature operation. It can be achieved using $2\times$ frequency division from a VCO operating at twice the desired LO frequency. The drawbacks of this approach are that the VCO operates at a higher frequency and the additional frequency divider circuitry consumes more power. Quadrature LO signals are also synthesized by applying differential signals from a VCO to an *RC* polyphase filter. Signal attenuation in the passive *RC* filter usually necessitates the use of buffers with higher power consumption. A third way to generate quadrature signals is through the use of a quadrature VCO, which is essentially a pair of oscillators coupled so that it outputs quadrature signals directly [17]–[20]. The key point is that the unidirectional coupling between the two oscillators should always be in an inverse sense.

Next, a novel QVCO based on the differential Colpitts VCO2 with its superior phase noise performance is synthesized. Recall that achieving quadrature operation from two identical oscillators requires coupling between them; in the differential Colpitts VCO2 of Fig. 9, M_3 and M_4 are used as the coupling devices. More specifically, as depicted in Fig. 11, the gates of M_3 and M_4 in the I-phase VCO are connected to the outputs of Q-phase VCO and those of M_7 and M_8 are connected to the outputs of I-phase oscillator in an inverse fashion. Positioning the coupling transistors below the switching transistors is referred as series coupling in [18]. Series coupling has the advantage that the phase error deviation from the ideal quadrature relationship is relatively insensitive to the circuit imbalances. Optimization of the QVCO involves sizing both the switching and coupling transistors to achieve fast current switching with minimal phase noise.

IV. Experimental Results

The transformer-coupled CGLNA [Fig. 4(a)], differential Colpitts VCO1 (Fig. 8), and QVCO (Fig. 11) were fabricated in a 0.18-μm RF CMOS process. The circuits were tested on a wafer-probe station with high-frequency probing capability.

To verify the g_m-boosting design principle, the turns ratio in the specific implementation of Fig. 4(a) was designed to be $n = 1{:}1$ due to its ease of implementation and modeling. As described earlier, $A > 1$ is also possible using a larger turns ratio. For example, if the turns ratio is $n = 1{:}2$, $A = 2$ is achieved which with $k = 1$ results in a lower noise figure. The transformer was designed to resonate with the capacitance at the source of M_1. A transformer circuit model was extracted using ASITIC. Minimum spacing was adopted to maximize the coupling coefficient k. A coupling factor of 0.74 for T_1 is predicted by ASITIC; the measured value is 0.69. Fortunately, the required modeling accuracy is relaxed owing to the relatively wide-band input matching characteristics of the CGLNA.

The S-parameters measured using an Agilent E8364A Programmable Network Analyzer are plotted in Fig. 12. S_{21} is 9.4 dB with its peak at 5.8 GHz, S_{22} is -14.8 dB, and S_{12} is -30.3 dB. As shown, S_{11} is less than -10 dB from 4 to 7 GHz,

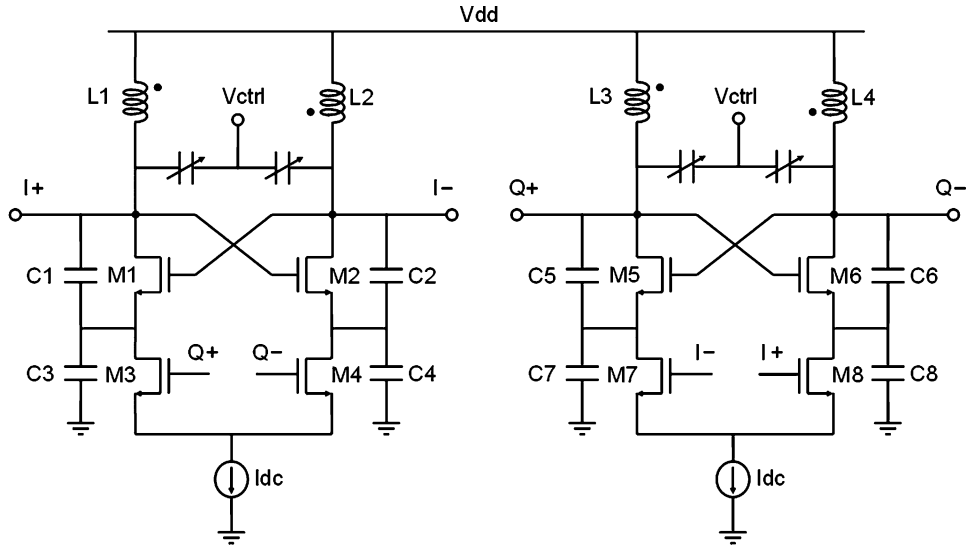
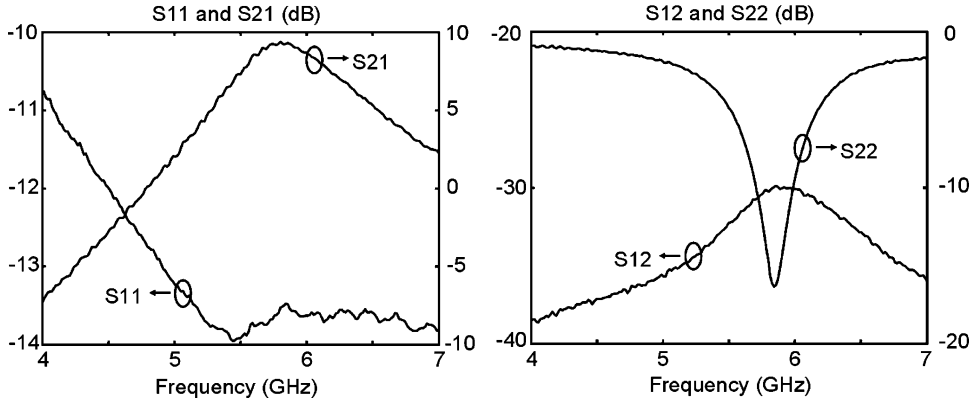
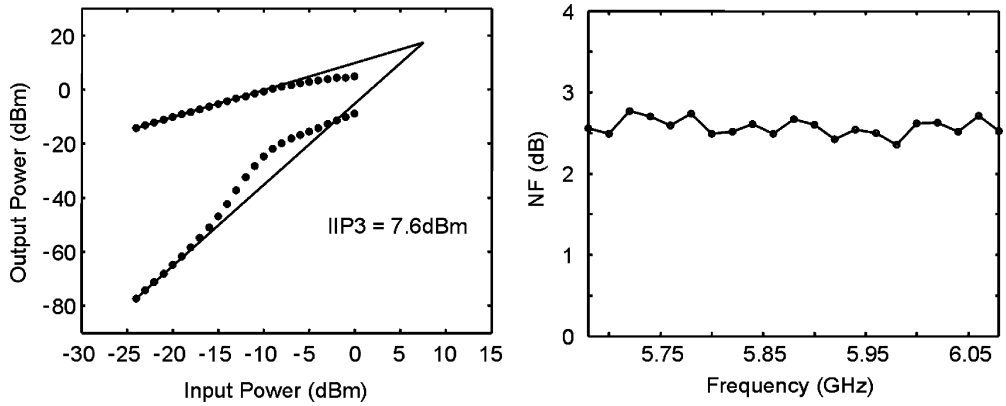


Fig. 11. Colpitts QVCO.



(a) (b)

Fig. 12. Measured S-parameters of the transformer-coupled CGLNA of Fig. 4(a): (a) S_{11} and S_{21}, and (b) S_{12} and S_{22}.



(a) (b)

Fig. 13. Measured (a) IIP3 and (b) noise figure of the transformer-coupled CGLNA of Fig. 4(a).

which validates the broadband input matching of the common-gate topology and also suggests the possibility of applying the proposed topology in ultra-wide-band (UWB) receivers.

The third-order input intercept point (IIP3) was measured using a two-tone test. Two Agilent E8254A Programmable Signal Generators created the two tones at $f_1 = 5.8$ GHz and $f_2 = 5.805$ GHz. They are subsequently combined using a hybrid coupler and applied to the input of the LNA. The LNA output is fed into an Agilent E4446A Spectrum Analyzer to perform spectral analysis. The input power $P_{\rm IN}$ is swept from -24 dBm to 0 dBm with steps of 1 dB. Fig. 13(a) plots output power against input power for both the fundamental and the third-order intermodulation components, giving an IIP3 of 7.6 dBm.

The noise figure (NF) measured using an Agilent N8975A Noise Figure Analyzer is plotted in Fig. 13(b). Table I sum-

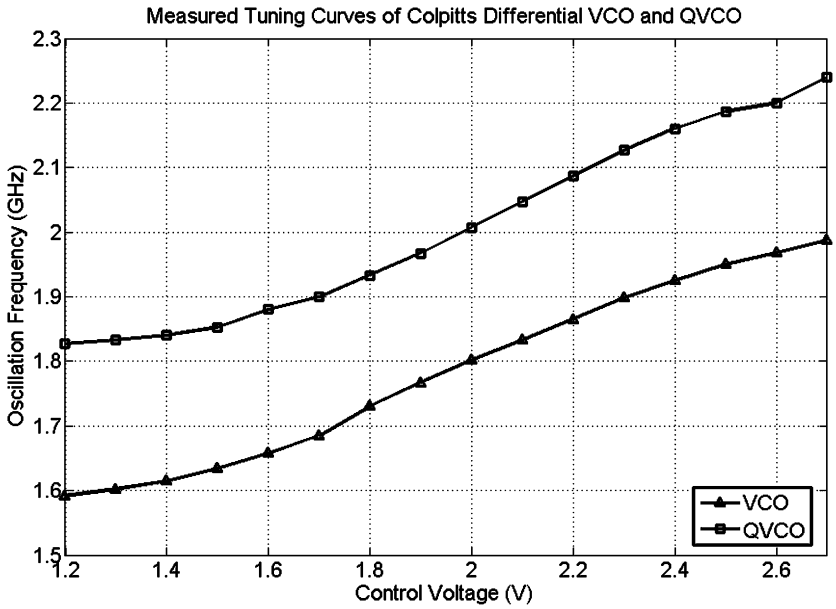


Fig. 14. Measured tuning curves: (▲) differential Colpitts VCO and (■) Colpitts QVCO.

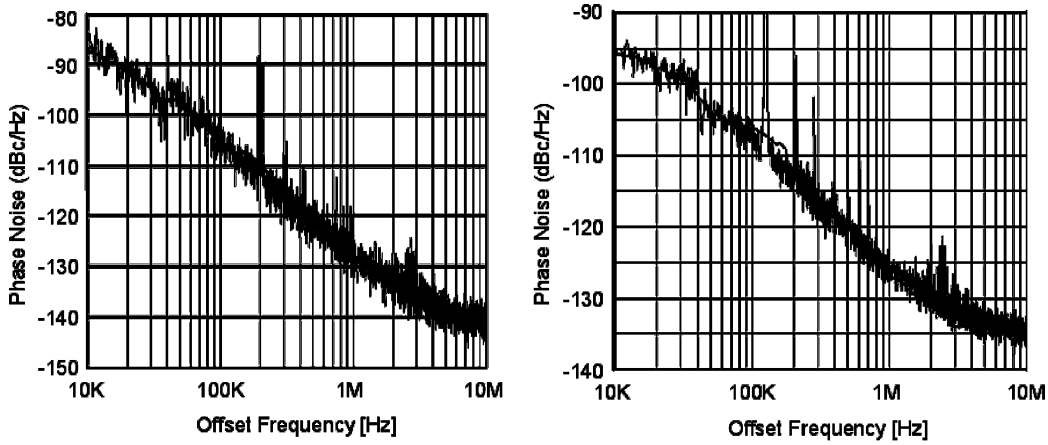


Fig. 15. Measured phase noise: (a) differential Colpitts VCO and (b) Colpitts QVCO.

TABLE I
MEASURED PERFORMANCE SUMMARY OF TRANSFORMER-COUPLED CGLNA

V_{DD}	1.8V	
DC Current	1.9mA	
Operating Frequency	5.8GHz	
S-parameters	S_{11}	-13.5dB
	S_{21}	+9.4dB
	S_{12}	-30.3dB
	S_{22}	-14.8dB
Noise Figure	2.5dB	
IIP3	7.6dBm	
Die Area	910μm × 670μm	

marizes the overall performance of the transformer-coupled CGLNA.

The differential Colpitts VCO1 (Fig. 8) and QVCO (Fig. 11) were fabricated in the same process. To deliver sufficient power to the 50 Ω input of the spectrum analyzer, an open-drain differential pair buffer driven by the sources of M_1 and M_2 is used. This prevents the buffer from directly loading the LC tank circuit. The tuning range is also maintained using the buffer stage. Simulations show that even with a relatively low power supply voltage of 1.8 V, the voltage swings at the sources of M_1 and M_2 are sufficient to fully switch the buffer stage to steer the tail current to the 50 Ω output load. Care was taken in the layout to maintain symmetry to minimize flicker noise up-conversion. Sizing of the switching transistors involves a compromise between tuning range and phase noise; several design and optimization iterations were required to achieve the optimal tradeoff.

In implementing the Colpitts QVCO, two on-chip transformers were used to obtain a higher Q (≈10) than for the inductors (Q ≈ 8) used in the VCO, at the cost of some loss from longer inter-connect lines.

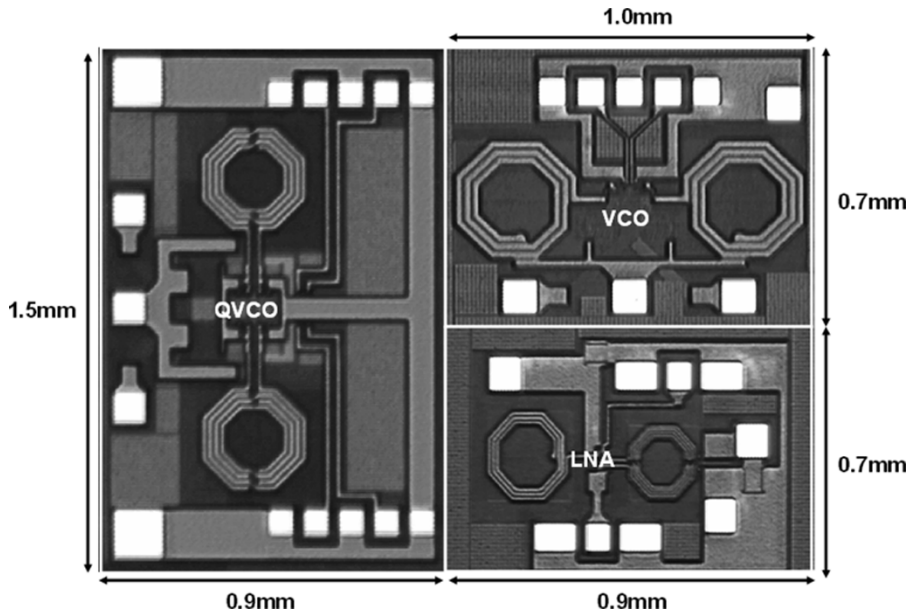


Fig. 16. Chip microphotograph in a 0.18-μm CMOS process.

TABLE II
MEASURED PERFORMANCE SUMMARY OF DIFFERENTIAL COLPITTS VCO AND QVCO

	VCO	QVCO
V_{DD}	2.0V	2.0V
DC Current	3.6mA	4.3mA
Frequency	1.59GHz ~ 1.98GHz	1.83GHz ~ 2.24GHz
Tuning Range	22%	20%
Phase noise	-97 dBc/Hz @ 50KHz	-104 dBc/Hz @ 50KHz
	-128 dBc/Hz @ 1MHz	-127 dBc/Hz @ 1MHz
Die Area	970μm × 710μm	1450μm × 940μm

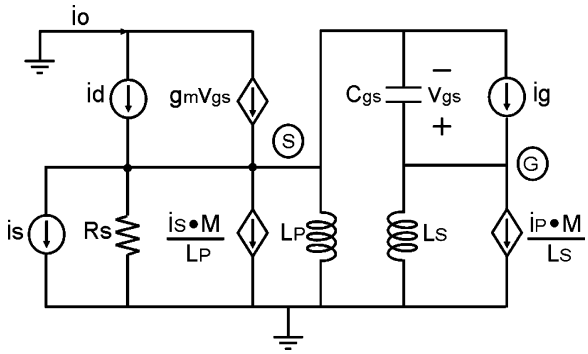


Fig. 17. Small-signal model used to calculate the noise factor of the transformer-coupled g_m-boosted CGLNA [Fig. 4(a)].

The differential Colpitts VCO operates at a center frequency of 1.79 GHz with a tuning range of 22%, and the Colpitts QVCO oscillates from 1.83 to 2.24 GHz with a 20% tuning range as shown in Fig. 14. Fig. 15 shows measured phase noise characteristics of the Colpitts VCO and QVCO circuits. The VCO exhibits a phase noise of −97 dBc/Hz at 50 kHz and −128 dBc/Hz at 1 MHz offset, and consumes 3.6 mA of current from a 2.0-V power supply. The QVCO draws only 4.3 mA from 2.0 V to attain a close-in phase noise of −104 dBc/Hz at 50 kHz offset. Its phase noise at 1 MHz offset is −127 dBc/Hz. Table II summarizes the measured performances of the Colpitts VCO and QVCO circuits. A chip microphotograph is shown in Fig. 16.

V. CONCLUSION

A g_m-boosted common-gate topology is introduced that exhibits a lower noise figure and consumes less power than a conventional CGLNA while retaining the robust input matching feature of the common-gate topology. Rather than connecting the gate terminal to an AC ground, coupling between the source and gate terminals is used to enhance the effective transconductance and lower the noise figure. A single-ended fully integrated transformer-coupled CGLNA is presented as a specific implementation for the general g_m-boosted common-gate scheme.

Differential Colpitts VCOs and a quadrature Colpitts VCO are also described. The differential operation provides faster commutation with more efficient suppression of phase noise. The enhancement of the effective transconductance leads to easier start-up and reduces the DC power needed to guarantee oscillation. Finally, prototype circuits in a 0.18-μm RF CMOS process validate the g_m-boosting design principles.

APPENDIX

The small-signal model of Fig. 17 is used to perform the small-signal noise analysis. The first step is to calculate the transfer functions of the different noise sources; applying KCL at node S gives (A-1)–(A-3), shown at the top of the next page.

For simplicity, apply the approximation $|(1 - k^2)\, s^2 L_S C_{gs}| \ll 1$. At the resonance frequency determined from $1/(j\omega L_P) + (1 + 2nk + n^2) j\omega C_{gs} = 0$, (A-1)–(A-3) simplify to

$$i_{o,S} = \frac{(1+nk)g_m}{(1+nk)g_m + (1/R_S)} \cdot i_{nS} \qquad \text{(A-4)}$$

$$i_{o,S} = \frac{(1+nk)g_m}{(1+nk)g_m + sC_{gs}(1+2nk+n^2) + \dfrac{1}{sL_P} + \dfrac{1}{R_S} + \dfrac{(1-k^2)s^2C_{gs}L_S}{R_S}} \cdot i_{nS} \tag{A-1}$$

$$i_{o,d} = \frac{sC_{gs}(1+2nk+n^2) + \dfrac{1}{sL_P} + \dfrac{1}{R_S} + \dfrac{(1-k^2)s^2C_{gs}L_S}{R_S}}{(1+nk)g_m + sC_{gs}(1+2nk+n^2) + \dfrac{1}{sL_P} + \dfrac{1}{R_S} + \dfrac{(1-k^2)s^2C_{gs}L_S}{R_S}} \cdot i_{nd} \tag{A-2}$$

$$i_{o,g} = \frac{g_m(1+2nk+n^2) + g_m\dfrac{(1-k^2)sL_S}{R_S}}{(1+nk)g_m + sC_{gs}(1+2nk+n^2) + \dfrac{1}{sL_P} + \dfrac{1}{R_S} + \dfrac{(1-k^2)s^2C_{gs}L_S}{R_S}} \cdot i_{ng} \tag{A-3}$$

$$i_{o,d} = \frac{1/R_S}{(1+nk)g_m + (1/R_S)} \cdot i_{nd} \tag{A-5}$$

$$i_{o,g} = \frac{g_m(1+2nk+n^2)}{(1+nk)g_m + (1/R_S)} \cdot i_{ng}. \tag{A-6}$$

From (A-4)–(A-6), the noise factor F is

$$\begin{aligned} F &= 1 + \frac{\overline{i_{o,d}^2} + \overline{i_{o,g}^2}}{\overline{i_{o,S}^2}} \\ &= 1 + \frac{1}{\left((1+nk)g_mR_S\right)^2}\gamma g_{d0}R_S \\ &\quad + \frac{(1+2nk+n^2)^2}{(1+nk)^2}\delta g_gR_S \\ &= 1 + \frac{\gamma}{\alpha}\cdot\frac{1}{1+nk} + \frac{\delta\alpha}{5}\cdot\left(\frac{\omega}{\omega_T}\right)^2 \\ &\quad \cdot \left.\frac{(1+2nk+n^2)^2}{(1+nk)^3}\right|_{(1+nk)g_mR_S=1} \end{aligned}$$

as shown earlier in (16).

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Xiaoyong Li (S'00–M'04) was born in Baoji, China, in 1975. He received the B.S. and M.S. degrees from Peking University, Beijing, China, all in computer science and technology, in 1997 and 2000, respectively. He received the Ph.D. degree in electrical engineering from the University of Washington, Seattle, in 2004.

Since August 2004, he has been with Qualcomm Incorporated, San Diego, CA, engaging in the design and development of CMOS integrated circuits for cellular applications. His research interests include the design of RF, analog and mixed-signal integrated circuits.

Dr. Li received the Motorola Scholarship in 1996, the Academic Excellent Scholarship in 1997, the P&G Scholarship in 1998 and the Kodak Scholarship in 1999, all at Peking University, Beijing, China. He was awarded the Excellent Graduate Student of Peking University in 1998 and 2000. He was the recipient of the 2002 Analog Devices Outstanding Student Designer Award and the corecipient of the first-place winners of Phase I of the 2003 SRC SiGe BiCMOS Design Contest.

Sudip Shekhar (S'00) received the B.Tech. degree (Hons.) in electrical and electronics communication engineering from the Indian Institute of Technology, Kharagpur, in 2003. He received the M.S. degree in electrical engineering from the University of Washington, Seattle, in 2005, where he is currently working toward the Ph.D. degree.

From April to September, 2005, he was an intern with Intel Corporation, Hillsboro, OR, where we worked on the modeling of serial links and design of clock and data recovery circuits. His current research interests include RF transceivers, wide-band amplifiers, and mixed-signal circuits for high-speed I/O interfaces.

David J. Allstot (S'72–M'72–SM'83–F'92) received the B.S., M.S., and Ph.D. degrees from the University of Portland, Oregon State University, and the University of California, Berkeley, respectively.

He has held several industrial and academic positions and has been the Boeing-Egtvedt Chair Professor of Engineering at the University of Washington since 1999; he is currently Chair of the Department of Electrical Engineering. He has advised about 80 M.S. and Ph.D. graduates and published more than 225 papers.

Dr. Allstot is the recipient of several outstanding teaching and advising awards His awards include the IEEE W.R.G. Baker Prize Paper Award in 1978, the IEEE Circuits and Systems Society Darlington Best Paper Award in 1995, the IEEE International Solid-State Circuits Conference Beatrice Winner Award in 1998, the IEEE Circuits and Systems Society Golden Jubilee Medal in 1999, the Technical Achievement Award of the IEEE Circuits and Systems Society in 2004, and the Aristotle Award of the Semiconductor Research Corporation in 2005. His professional service includes Associate Editor, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING from 1990 to 1993; Editor, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING from 1993 to 1995; Technical Program Committee, IEEE Custom IC Conference from 1990 to 1993; Board of Governors, IEEE Circuits and Systems Society from 1992 to 1995; Technical Program Committee, IEEE International Solid-State Circuits Conference from 1994 to 2004; Executive Committee Member and Short Course Chair, IEEE International Solid-State Circuits Conference from 1996 to 2000; Distinguished Lecturer, IEEE Circuits and Systems Society from 2000 to 2001; and Co-General Chair, IEEE International Symposium Circuits and Systems in 2002. He is a Member of Eta Kappa Nu and Sigma Xi.