26.5 A 1.8GHz Spur-Cancelled Fractional-N Frequency Synthesizer with LMS-Based DAC Gain Calibration

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Modern wireless LAN and digital TV standards use higher order phase modulations like 64 or 256-QAM, and require very low phase-noise frequency synthesizers. In fractional-N synthesizers, frequency divider averages many integer cycles over time to get a fractional divider ratio. A simple accumulator with overflow can control a fractional N/N+1 divider to interpolate any fractional values. However, such a simple fractional divider creates fractional spurs that affect the phase-noise performance. One solution is that the ratio error is modulated using ΔΣ technique, and the high-frequency shaped noise can be filtered later with PLL loop filter. For this, the loop bandwidth should be made narrow, which in turn reduces the PLL loop gain that is badly needed to suppress VCO phase noise. To avoid this trade-off, spur-cancellation schemes have been proposed so that the accumulated ratio error can be subtracted using a DAC in real time [1, 2, 3, 4, 5]. Their effectiveness depends on the PFD/CP linearity and DAC and charge-pump (CP) gain matching. The PFD/CP nonlinearity results from the PFD dead zone and CP up/down current mismatch, but is reduced when operating it in class-A mode avoiding the zero-crossing point [2]. However, the critical DAC and CP gain mismatch problem has not been addressed to date. In this work, a sign-sign LMS feedback concept is used to correlate the actual accumulated ratio error at the loop-filter output with its sign polarity, and the DAC gain is adaptively trimmed with the polarity of the gain mismatch error.

The proposed system with a spur-cancellation DAC is shown in Fig. 26.5.1. Two functional blocks added to a ΔΣ fractional-N synthesizer are spur-cancellation DAC with its randomization logic and LMS spur-correlation block. This LMS spur-correlation block decides whether to increase or decrease the DAC gain for calibration. An 8b DAC is used so that the DAC resolution does not affect the performance of the PLL. The DAC output is further shaped using a 3rd-order ΔΣ modulator to minimize the effect of any periodic DAC quantization noise. The 5 MSBs of the DAC are thermometer coded to achieve monotonicity while the 3 LSBs are binary-coded. If there is a mismatch in the charges pumped by the DAC and CP as shown in Fig. 26.5.2, a residual low-frequency voltage will be left on the loop filter, which modulates the VCO and hence generates fractional spurs. The spur-cancellation concept with CP linearization is shown with timing in Fig. 26.5.3. Since the total integrated ΔΣ phase error is smaller than $\pm 2T_{VCO}$, an amplitude-modulated DAC pulse of fixed width equal to $4T_{VCO}$ is used to inject cancellation current. For CP linearity, an additional fixed charge is injected into the loop filter by switching the nominal charge-pump current for the duration of $4T_{VCO}$.

The key to the proposed spur-cancellation scheme is how to detect the small residual ratio error accumulated in the loop-filter voltage, and then how to correlate it with its sign sequence without disturbing the loop-filter voltage. The loop filter voltage is first sensed with a source-follower buffer to prevent kick-back. The buffered loop-filter voltage is then correlated with the sign sequence of the same accumulated error. The correlated energy is integrated for long so that un-correlated noise may not affect the decision. The correlation by 1b (multiply by ±1) is just a polarity flip, and the sign change is done in the input sampling stage of the 1b ΔΣ ADC as shown in Fig. 26.5.4. The bit stream from the ADC is accumulated for low-pass filtering. Depending on the sign of the accumulator output, an 8b control word is updated. The DAC gain is adjusted by trimming the DAC bias current. The requirement on the sign sequence is that it should have a zero mean so that any dc component can be chopped and averaged out. The residual dc component of the ΔΣ ADC itself can be calibrated easily in the digital domain. Once the DAC gain is matched with that of the CP, the fractional spur disappears, and the fractional-N synthesizer operation is almost equivalent to any integer synthesizer regardless of the order of the ΔΣ divider ratio modulator.

A 1.8GHz synthesizer prototype is designed using a 2nd-order ΔΣ modulator. A low-frequency reference clock of 14.3MHz is chosen to make it useful for systems with low-frequency crystals. The frequency resolution is about $14.3\text{MHz}/2^{20} \sim 14\text{Hz}$. The chip is fabricated in 0.18μm CMOS, occupies 2mm^2, and consumes 29mW at 1.8V. The breakdown of the current consumed in each block is 8, 2, 4, and 2mA, for VCO, CP/DAC, ΔΣ ADC, and digital logic, respectively. About 5mA (~31%) out of the total 16mA is consumed for spur cancellation. An inductor-loaded CMOS VCO with a tail current uses MOS varactors for tuning. The PLL loop bandwidth is set to 400kHz. The CP current is 900μA, and the nominal VCO gain is 40MHz/V. Figure 26.5.5 shows measured phase noises for the integer mode and the fractional mode before and after DAC gain correction. First, the in-band phase noise of the integer synthesizer to emulate is -101dBc/Hz, and the spot phase noise is -118dBc @1MHz offset. The integrated phase noise from 1kHz to 10MHz is 0.68°. As expected, in the fractional mode, the integrated phase noise is measured to be 6.37°. The high phase-noise results from the high-pass shaped divider ratio error of the ΔΣ modulator, and most fractional-N synthesizers keep loop bandwidth narrow to further attenuate the high-frequency noise. In this 400kHz wideband example, the loop filter cannot attenuate it enough, but the proposed method effectively removes the fractional spur noise. After DAC gain correction, the in-band phase noise and the total integrated noise are measured to be -98dBc/Hz and 0.82°, respectively, which approaches the phase-noise performance of the integer synthesizer within a close range of 3dB and 0.14°. The measured outputs before and after DAC gain correction demonstrate that the fractional spur is suppressed by 30dB as shown in Fig. 26.5.6, where the fractional spur at 14.3MHz/4 ~ 3.58MHz is well below the 70dB noise floor. The die micrograph is shown in Fig. 26.5.7.

Acknowledgements:
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References:
[1] G. Gillette, "Digiphase Synthesizer," *Proc. 23rd Annual Freq. Cont. Symp.*, pp. 201-210, 1969.
[2] I. Bietti, et al., "An UMTS ΔΣ Fractional Synthesizer with 200kHz Bandwidth and -128dBc/Hz @1MHz Using Spurs Compensation and Linearization Techniques," *Proc. IEEE CICC*, pp. 463-466, Sept., 2003.
[3] S. Meninger and M. Perrott, "A fractional-N Synthesizer Utilizing a Mismatch Compensated PFD/DAC Structure for Reduced Quantization-Induced Phase Noise," *IEEE Trans. Circuits and Systems: II*, vol. 50, no. 11, pp. 839-849, Nov., 2003.
[4] S. Pamarti and I. Galton, "Phase Noise Cancellation Design Tradeoffs in Delta-Sigma Fractional-N PLLs," *IEEE Trans. Circuits and Systems: II*, vol. 50, no. 11, pp. 829-838, Nov., 2003.
[5] W. Rhee and A. Ali, "An On-Chip Compensation Technique in Fractional-N Frequency Synthesis," *Proc. IEEE Int. Sym. Circuits and Systems*, pp. 363-366, May, 1999.

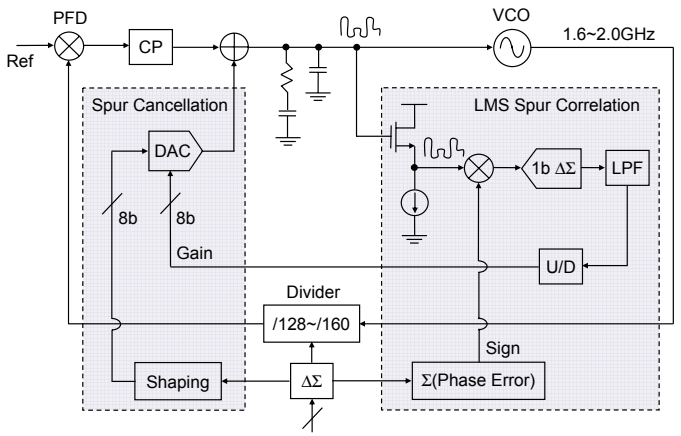


Figure 26.5.1: Fractional synthesizer system with gain-calibrated spur-cancellation DAC.

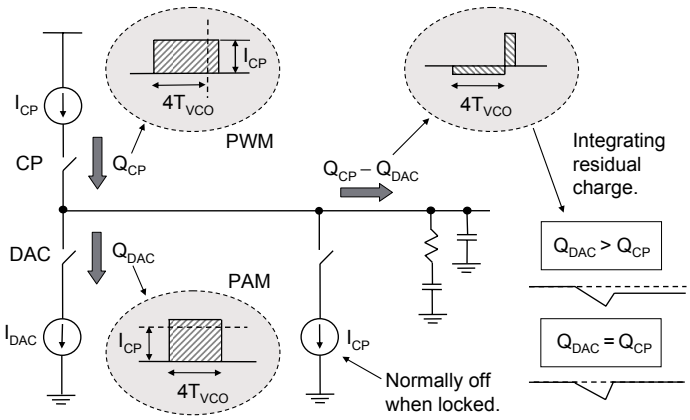
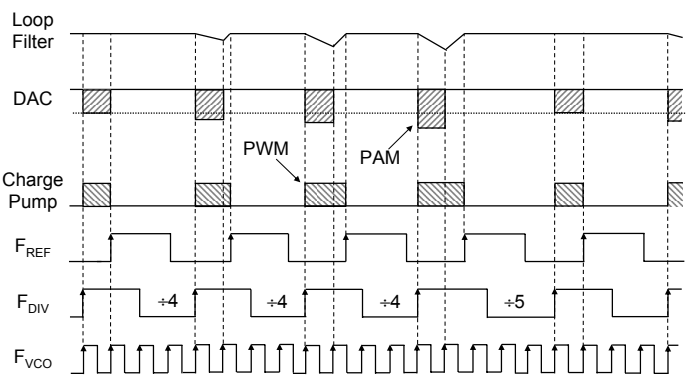


Figure 26.5.2: Linearized CP/DAC and integrated residual charge due to their mismatch.



Example: DAC pulse width is T_{VCO}, and fractional ratio is 4.25.

Figure 26.5.3: Timing for spur cancellation with DAC and CP linearization.

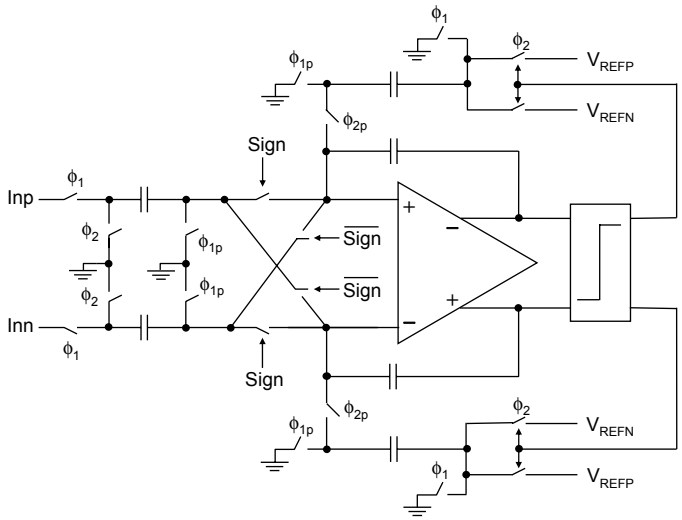


Figure 26.5.4: 1b ΔΣ ADC for spur correlation.

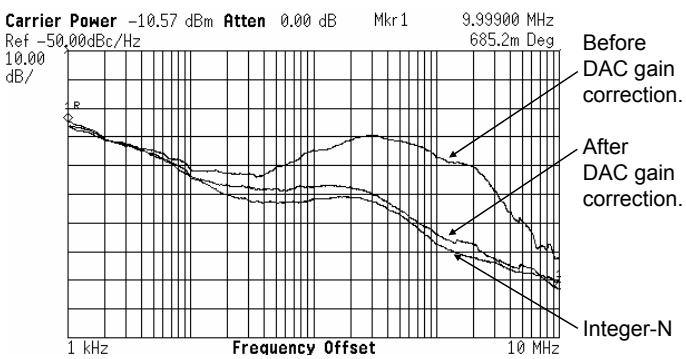


Figure 26.5.5: Phase-noise comparison: Integer, fractional-N before and after DAC gain correction.

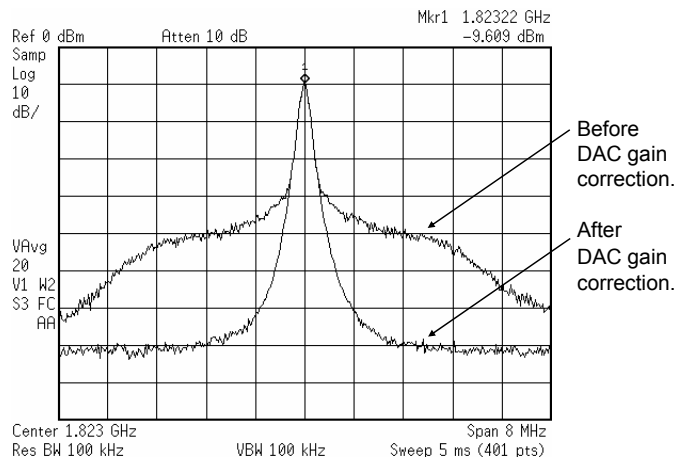


Figure 26.5.6: Fractional-N output spectrum before and after DAC gain correction.

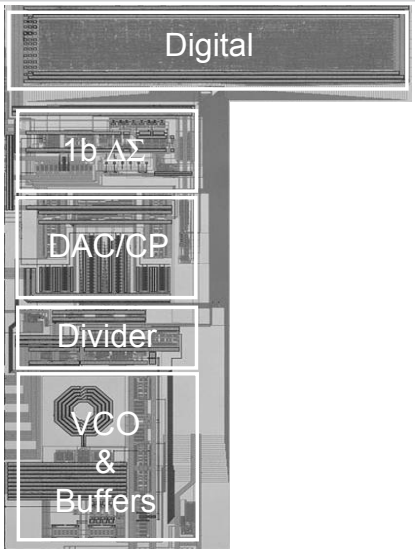
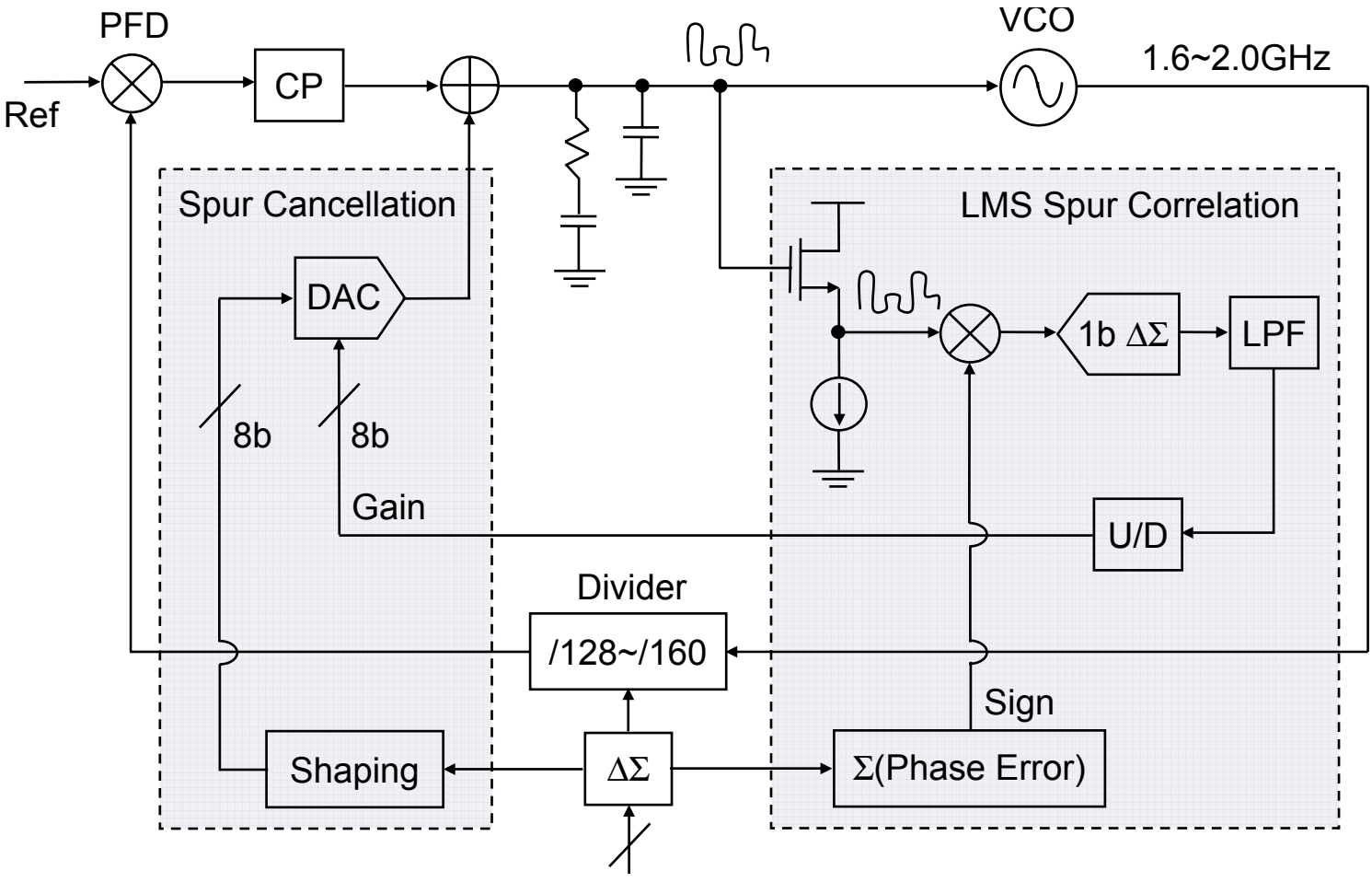


Figure 26.5.7: Chip micrograph.



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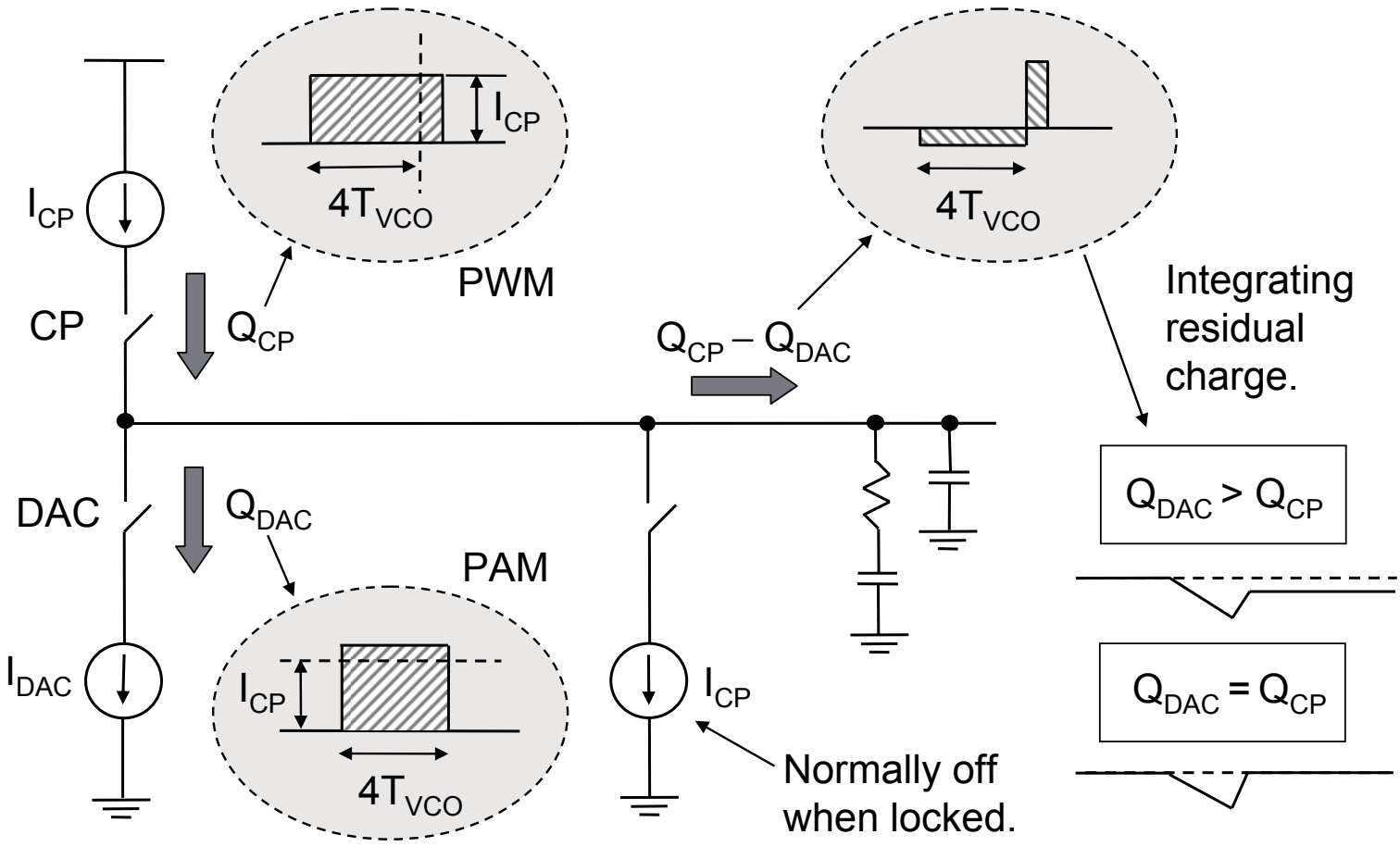

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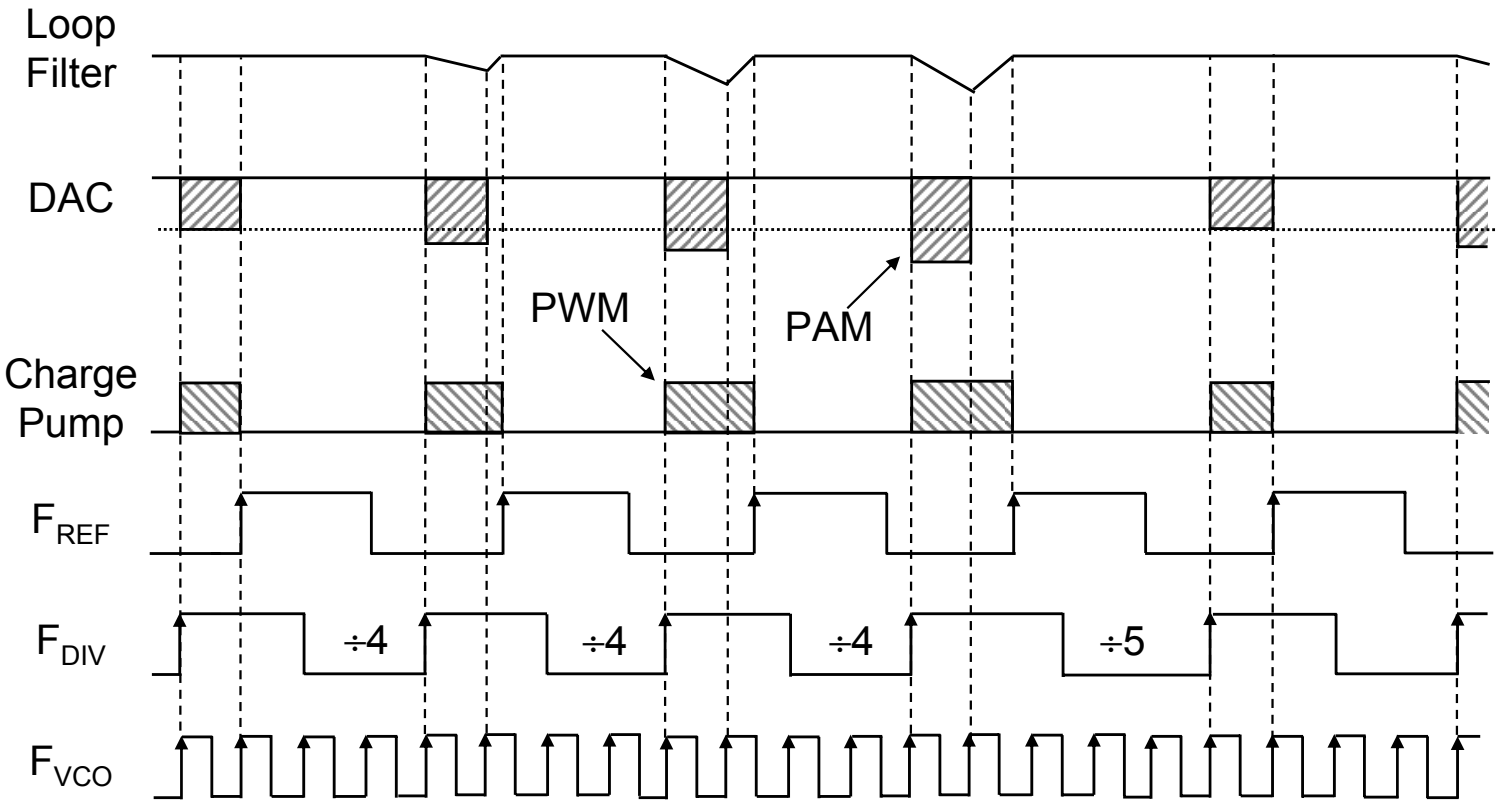

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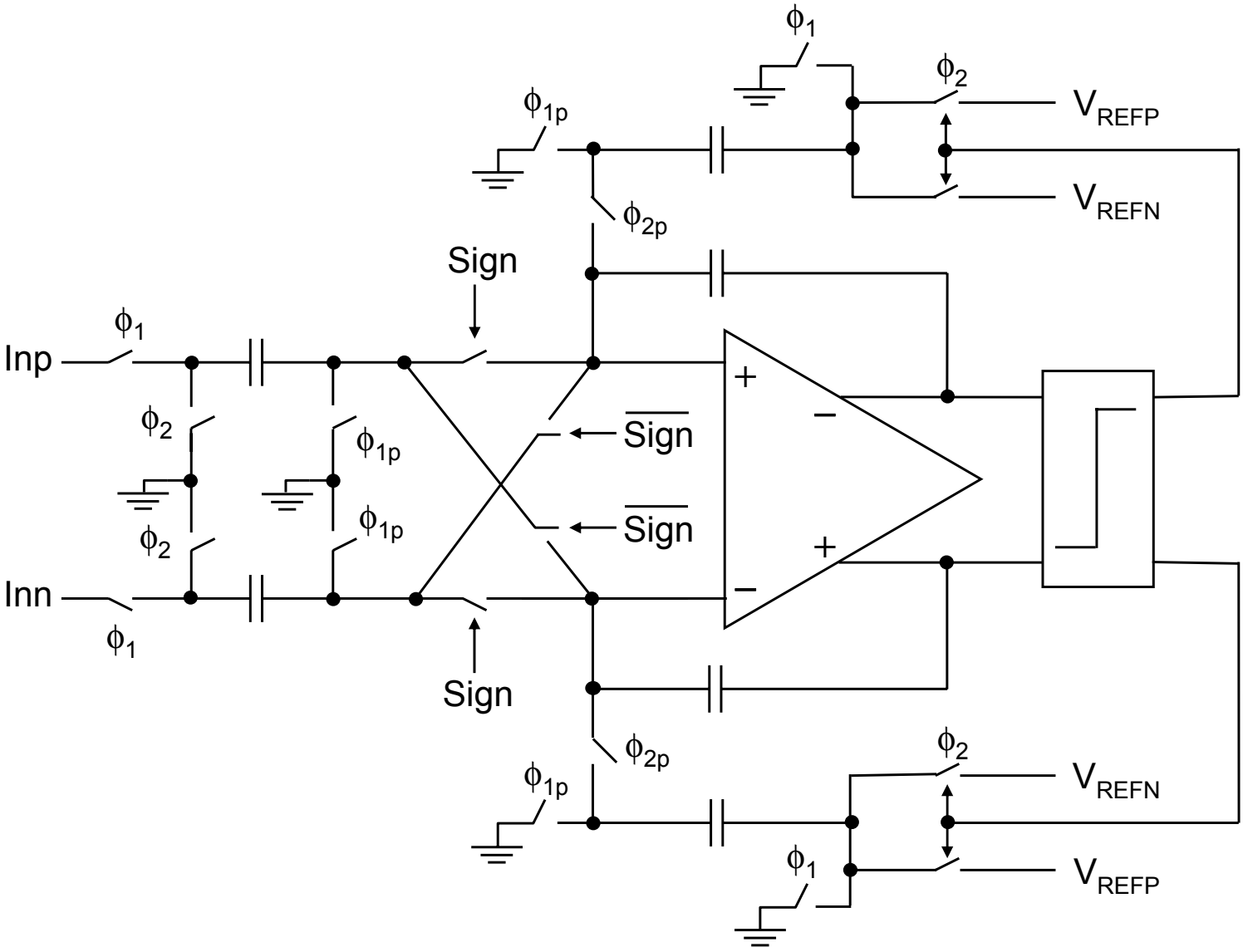

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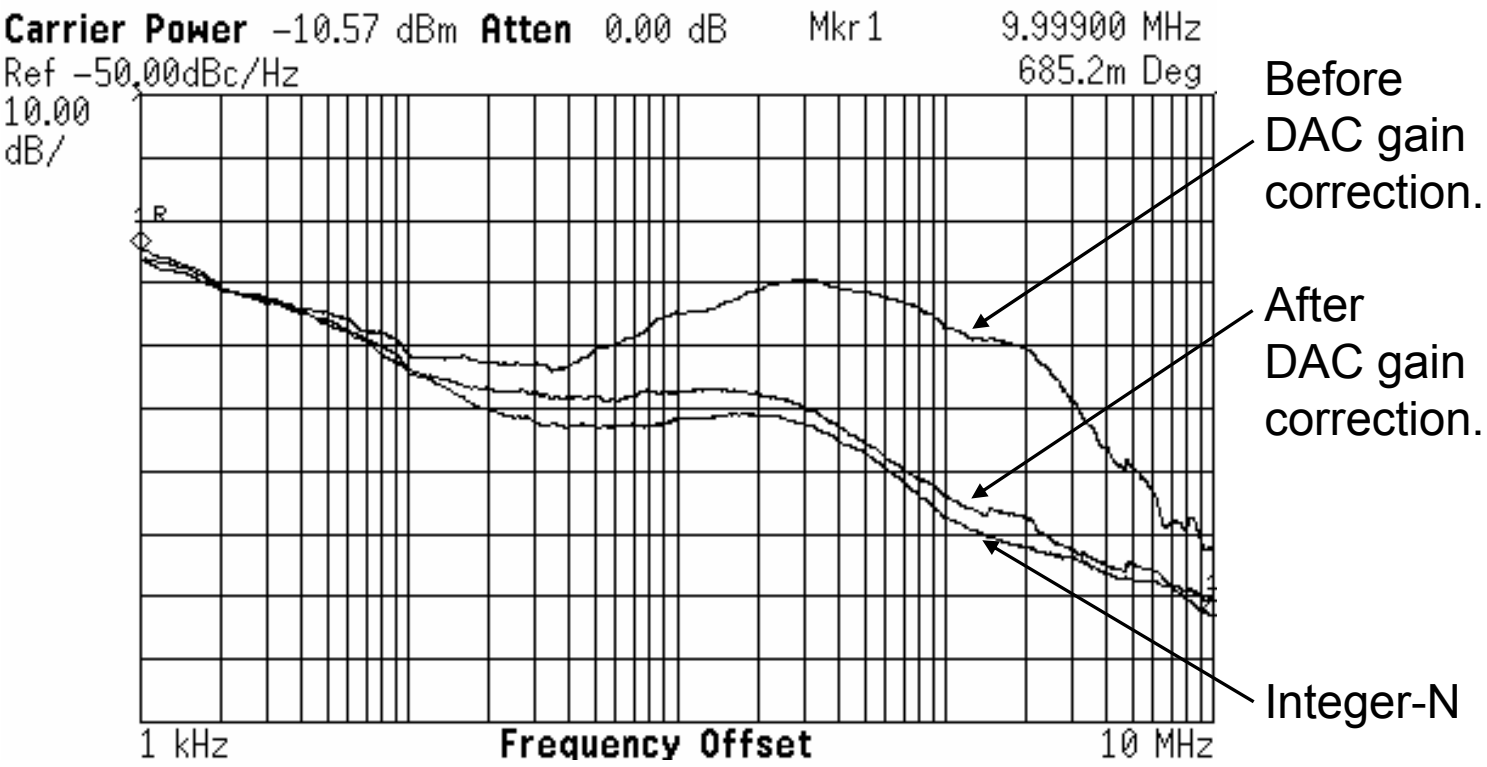

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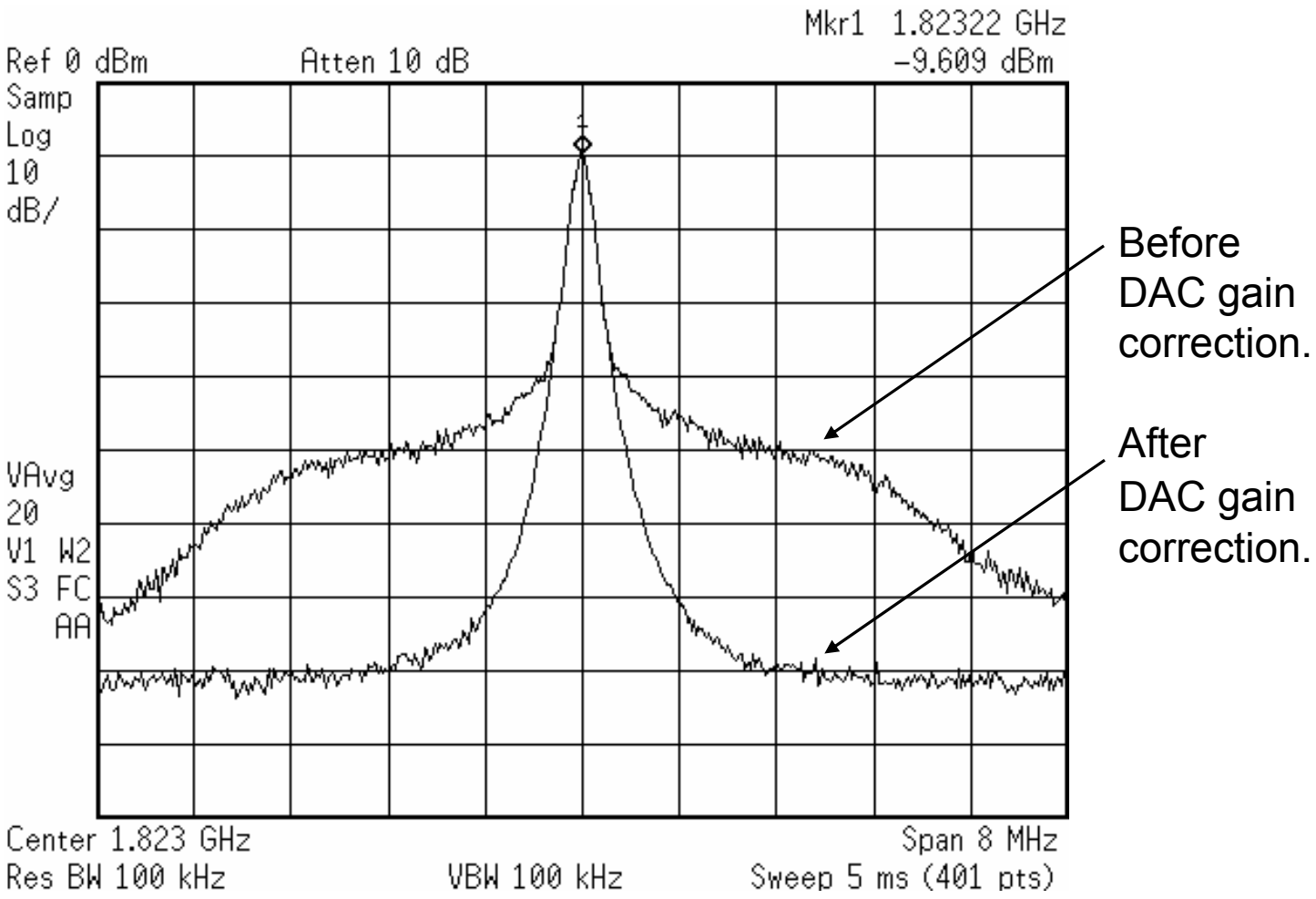

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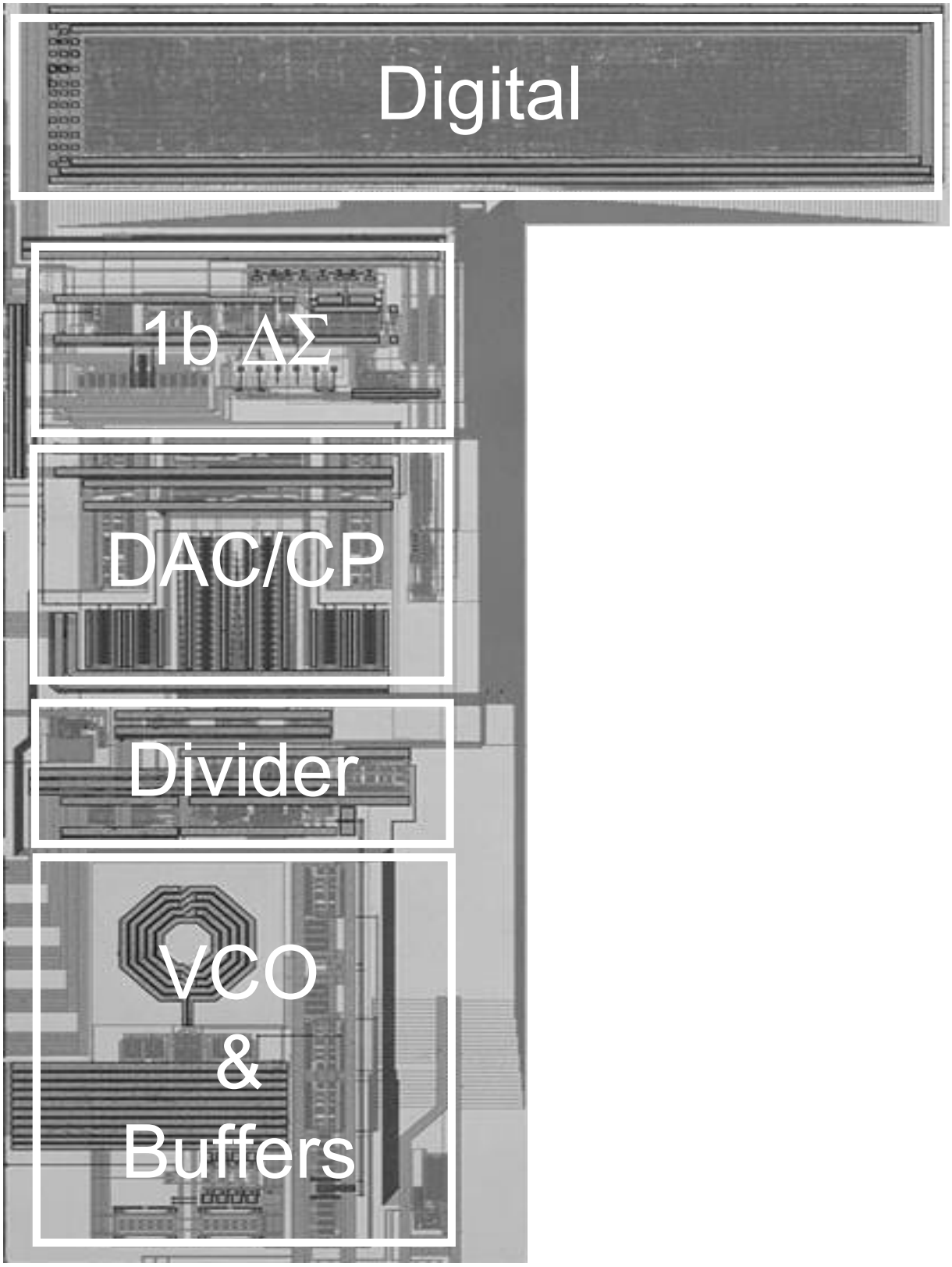

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