A Versatile 90-nm CMOS Charge-Pump PLL for SerDes Transmitter Clocking

Alvin L. S. Loke, *Senior Member, IEEE*, Robert K. Barnes, *Senior Member, IEEE*, Tin Tin Wee, *Senior Member, IEEE*, Michael M. Oshima, *Senior Member, IEEE*, Charles E. Moore, *Member, IEEE*, Ronald R. Kennedy, *Member, IEEE*, and Michael J. Gilsdorf, *Senior Member, IEEE*

***Abstract*—This paper presents a low-jitter charge-pump phase-locked loop (PLL) built in standard 90-nm CMOS for 1 to 10 Gb/s wireline SerDes transmitter clocking. The PLL employs a programmable dual-path loop filter with integral path and resistorless sample-reset proportional path that are independently controlled for flexible setting of closed-loop bandwidth and peaking. Frequency is synthesized by a digitally calibrated *LC*-VCO achieving 45% calibration tuning range with inversion-mode nMOS varactors and area-efficient helical inductors. Following calibration, 4.8% hold range compensates for VCO sensitivity to supply voltage and temperature drift. The PLL exhibits 0.81 ps rms jitter at 10 Gb/s. Critical for ASICs integrating noisy digital cores and multiple SerDes channels, design considerations to minimize jitter induced by supply noise are described. Deep-submicron CMOS effects on design are also examined to improve manufacturability and performance.**

***Index Terms*—CMOS integrated circuits, dual-path loop filter, frequency synthesizers, jitter, phase-locked loops, serial links, temperature sensitivity, voltage-controlled oscillators.**

I. Introduction

SERIAL data communication with binary non-return-to-zero (NRZ) signaling has become ubiquitous for Gb/s wireline links [1]. As transceiver equalization [2]–[4] and coding [5]–[7] techniques advance to overcome limitations in low-cost electrical channels, faster short-haul networking continues to postpone migration to costlier optical alternatives. The pervasive inertia of wireline Serializer-Deserializer (SerDes) I/O has spawned many protocols (examples in Table I) to standardize link requirements for various applications. To meet these increasingly demanding protocols cost-effectively, practical SerDes transceivers must frequently span multiple data rates to enable new link rates while supporting compatibility with legacy rates.

Manuscript received December 1, 2005; revised March 3, 2006.

A. L. S. Loke and T. T. Wee were with the Enterprise ASIC Laboratory of Avago Technologies, Fort Collins, CO 80525 USA, recently divested from Agilent Technologies. They are now with the Mile High Design Center of Advanced Micro Devices, Fort Collins, CO 80525 USA (e-mail: alvin.loke@ieee.org; tintin.wee@ieee.org).

R. K. Barnes, C. E. Moore, R. R. Kennedy, and M. J. Gilsdorf are with the Enterprise ASIC Laboratory of Avago Technologies, Fort Collins, CO 80525 USA (e-mail: bob_barnes@ieee.org; charles.moore@avagotech.com; ron.kennedy@avagotech.com; mike.gilsdorf@ieee.org).

M. M. Oshima was with the Enterprise ASIC Laboratory of Avago Technologies, San Jose, CA 95131 USA. He is now with PMC-Sierra, Santa Clara, CA 95054 USA (e-mail: oshima@ieee.org).

Digital Object Identifier 10.1109/JSSC.2006.875289

Transmitting data with low jitter is critical to ensure reliable data recovery by the receiver. In typical wireline channels such as FR-4 backplanes and UTP cables, channel attenuation, intersymbol interference from frequency dispersion, reflections from impedance discontinuities, and crosstalk from adjacent channels all contribute to serial data eye closure. At higher data rates, these effects increasingly impair the receiver's ability to sample incoming bits without error.

This paper presents a CMOS transmitter phase-locked loop (PLL) that provides versatile low-jitter clocking for the outgoing serial data. Closed-loop bandwidth and peaking are adjusted by programming a dual-path charge-pump loop filter. The transmitter clock is generated by an *LC*-based voltage-controlled oscillator (VCO) that spans 45% calibration tuning range. This, in conjunction with flexible feedback divider ratios of 10 to 100, enables support of multi-rate protocols including Ethernet and Fibre Channel. The PLL is integrated in fully embedded SerDes transceiver macros that target networking protocols with data rates ranging from 1.0625 to 10.3 Gb/s. It is fabricated in a standard 90-nm foundry bulk CMOS logic technology with 1.0-V core FETs, 1.8-/2.5-/3.3-V I/O FETs, and 8-metal copper/low-κ interconnects. Throughout the paper, we discuss design considerations to minimize jitter induced by supply voltage ($V_{\rm DD}$) noise as well as address technology effects and manufacturability concerns introduced by deep-submicron CMOS.

II. Dual-Path Charge-Pump PLL Architecture

A. Motivation for Dual-Path Loop Filter

A dual-path charge-pump PLL architecture with separate integral and proportional loop filter control is chosen over the conventional single-path charge-pump PLL [8]–[11]. As will be demonstrated, the dual-path loop filter offers simple control of closed-loop bandwidth and damping through dialing the gains of the two paths. This flexibility extends the PLL applicability across a wide spectrum of networking protocols for a given design effort.

In the foregoing comparison of the single- versus dual-path PLLs shown in Fig. 1(a) and (b), respectively, we assume that the capacitance (C) and VCO gains are not programmable. Without loss of generality, the phase detector is modeled as a unitless unity-gain phase subtractor.

In the single-path PLL, the loop filter charge pump generates current pulses to accumulate charge (hence voltage) across capacitor, C, for gradual frequency correction as well as develop voltage pulses across resistor, R, for instantaneous phase correction that stabilizes the feedback loop. Ignoring the role of C_2

TABLE I
WIRELINE LINK PROTOCOLS AND NETWORK APPLICATIONS

Protocol	Network Application	Link Rate (Gb/s)
XFI (10Gb/s Ethernet)	Ethernet, Storage	10.5188, 10.3125
10GBASE-KR	Ethernet	10.3125
CEI-6GLR	Ethernet – Backplane	6.25
XAUI (10Gb/s Ethernet)	Ethernet – Backplane	3.125 (× 4 lanes)
XFI (10Gb/s Ethernet)	Ethernet – Frontplane	3.125 (× 4 lanes)
10GBASE-CX4	Ethernet – Frontplane	3.125 (× 4 lanes)
1000BASE-X (SGMII)	Ethernet	1.25
Fibre Channel	Storage	8.5, 4.25, 2.125, 1.0625
Serial ATA (SATA)	Storage	6.0, 3.0, 1.5
Serial Attached SCSI (SAS)	Storage	6.0, 3.0, 1.5
10Gb/s Fibre Channel	Storage	3.1875 (× 4 lanes)
PCIe	Computer I/O	5.0, 2.5
InfiniBand	Computer I/O	2.5
SONET	Telecommunication	9.95328, 2.48832

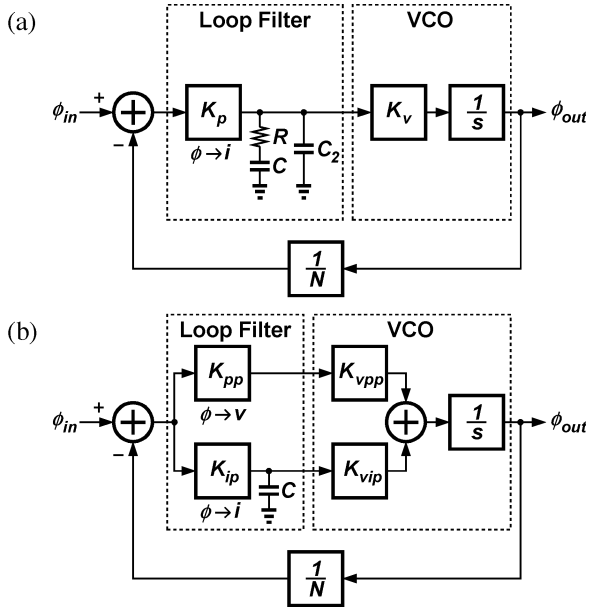


Fig. 1. Simplified charge-pump PLL model with (a) single-path loop filter and (b) dual-path loop filter.

to suppress reference spurs, the phase transfer function of the single-path charge-pump PLL can be simplified to

$$H_{sp}(s) = \frac{\Phi_{\text{out}}(s)}{\Phi_{\text{in}}(s)} = N \times \frac{1 + sRC}{1 + sRC + s^2\left(\dfrac{NC}{K_p K_v}\right)} \quad (1)$$

where K_p (A/rad) and K_v (rad/(s · V)) are, respectively, the phase-to-current ($\phi \rightarrow i$) charge pump gain and voltage-to-angular-frequency VCO gain of the single forward path.

The dual-path PLL performs frequency and phase corrections using independent charge pumps. Its simplified transfer function can be written as

$$\begin{aligned} H_{dp}(s) &= \frac{\Phi_{\text{out}}(s)}{\Phi_{\text{in}}(s)} \\ &= N \times \frac{1 + s\left(\dfrac{K_{pp}K_{vpp}}{K_{ip}K_{vip}/C}\right)}{1 + s\left(\dfrac{K_{pp}K_{vpp}}{K_{ip}K_{vip}/C}\right) + s^2\left(\dfrac{N}{K_{ip}K_{vip}/C}\right)} \end{aligned} \quad (2)$$

where K_{ip} (A/rad) and K_{vip} (rad/(s · V)) are, respectively, charge pump and VCO gain parameters for the integral path, analogously K_{pp} (V/rad) and K_{vpp} (rad/(s · V)) for the proportional path. Since the proportional path does not share the same charge pump as the integral path, the phase-to-voltage ($\phi \rightarrow v$) conversion affords, as later demonstrated, an area-efficient CMOS implementation without using a resistor.

Both (1) and (2) can be interpreted in relation to the classical second-order form

$$\begin{aligned} H(s) &= N \times \frac{1 + \dfrac{s}{z_1}}{1 + 2\zeta\left(\dfrac{s}{\omega_n}\right) + \left(\dfrac{s}{\omega_n}\right)^2} \\ &= N \times \frac{1 + \dfrac{s}{z_1}}{\left(1 + \dfrac{s}{p_1}\right)\left(1 + \dfrac{s}{p_2}\right)} \end{aligned} \quad (3)$$

where expressions for the familiar parameters ω_n (natural frequency), ζ (damping factor), and z_1 (closed-loop zero) are compared in Table II. The corresponding closed-loop poles are p_1 and p_2. For most SerDes transmitter clocking applications, the

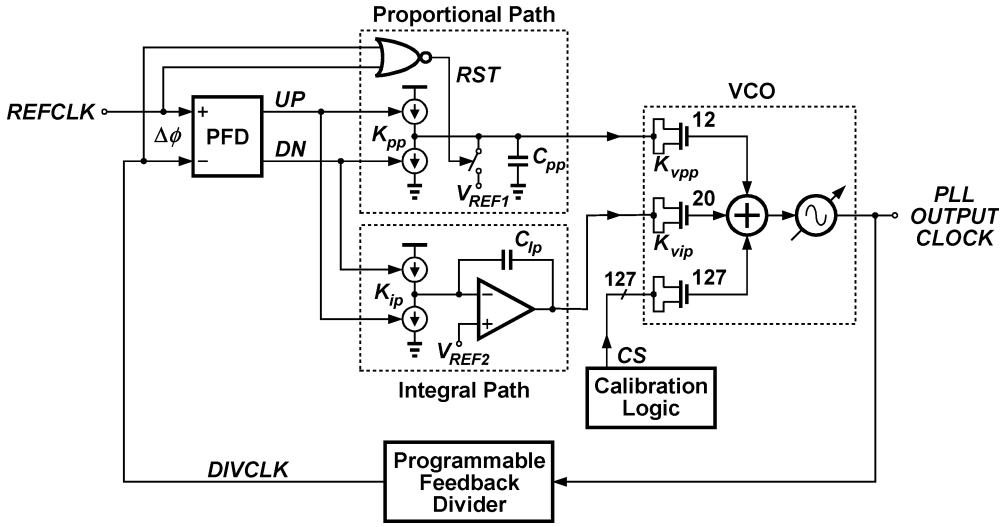


Fig. 2. Charge-pump PLL architecture with dual-path loop filter.

TABLE II
SECOND-ORDER CLOSED-LOOP PARAMETERS FOR SINGLE- AND DUAL-PATH PLL

Second-Order Parameter	Single-Path PLL	Dual-Path PLL
z_1	$\frac{1}{RC}$	$\frac{K_{ip}K_{vip}/C}{K_{pp}K_{vpp}}$
ω_n	$\sqrt{\frac{K_pK_v}{NC}}$	$\sqrt{\frac{K_{ip}K_{vip}/C}{N}}$
ζ	$\frac{R}{2}\sqrt{\frac{K_pK_vC}{N}}$	$\frac{K_{pp}K_{vpp}}{2\sqrt{N\cdot K_{ip}K_{vip}/C}}$

PLL operates in the overdamped case where $\zeta > 1$. Given this constraint, it can be shown that z_1 will effectively cancel p_1, leaving the pole farthest from the $j\omega$ axis (p_2) to set the closed-loop bandwidth. The proximity of p_1 and z_1 also reduces the amount of closed-loop peaking in the frequency domain.

Of particular interest is closed-loop bandwidth, with approximate expressions for the single- and dual-path PLL, respectively, given by (4) and (5):

$$\omega_{-3\mathrm{dB},sp} \approx \frac{K_pK_vR}{N} \tag{4}$$

$$\omega_{-3\mathrm{dB},dp} \approx \frac{K_{pp}K_{vpp}}{N}. \tag{5}$$

Eq. (5) shows that the dual-path PLL bandwidth is predominantly controlled by the proportional path gain K_{pp}. Also of interest is closed-loop peaking (inversely related to ζ) which dictates *REFCLK* jitter multiplication and time-domain step response behavior. Eqs. (6) and (7) show ζ relationships for the single- and dual-path PLL, respectively:

$$\zeta_{sp} \propto R\sqrt{\frac{K_p}{N}} \tag{6}$$

$$\zeta_{dp} \propto \frac{K_{pp}}{\sqrt{N\cdot K_{ip}}}. \tag{7}$$

Eqs. (5) and (7) demonstrate that the dual-path architecture allows for simple bandwidth adjustment by programming K_{pp} and subsequent adjustment of closed-loop damping by programming K_{ip}. In contrast, for the single-path PLL, it is difficult to independently adjust both bandwidth and damping using R and K_p as programmable parameters.

B. Architectural Overview

The PLL architecture is shown in Fig. 2. It consists of a sequential phase-frequency detector (PFD) feeding the phase error ($\Delta\phi$) between input reference (*REFCLK*) and feedback divider (*DIVCLK*) clocks into a programmable dual-path loop filter. The loop filter integral and proportional paths, respectively, perform frequency and rapid phase corrections. The integral path consists of a variable-gain charge pump and active integrator driving its VCO input. Operational amplifier feedback forces the charge pump output to $V_{\mathrm{REF2}} \approx (1/2)V_{\mathrm{DD}}$ in order to alleviate charge-pump output resistance limitation. This active filter topology also desensitizes the VCO integral path input to leakage sources. In the resistorless proportional path, a variable-gain charge pump samples $\Delta\phi$ as charge on C_{pp} which is later removed by the reset switch connected to V_{REF1} when both *REFCLK* and *DIVCLK* are low [12]. During each *REFCLK* cycle, this path provides a time-stretched voltage pulse to the VCO with an average voltage deviation of $K_{pp}\Delta\phi$ from V_{REF1}.

A differential *LC*-VCO is employed to produce a transmitter clock with low jitter and good supply noise rejection [13]. Each tank is tuned by 159 identical inversion-mode nMOS varactors [14]: 127 for coarse frequency centering, 12 for proportional path analog tuning, and 20 for integral path analog tuning. The varactors are configured with gates tied to the tank and shorted source/drain nodes independently controlled to enable the VCO to sum capacitance contributions from all three sets of varactors.

Prior to normal PLL operation, calibration logic determines the digital inputs for the 127 coarse-tuning varactors that tune the VCO to approximately its target frequency. During the calibration sequence, the PFD is disabled, and *REFCLK*

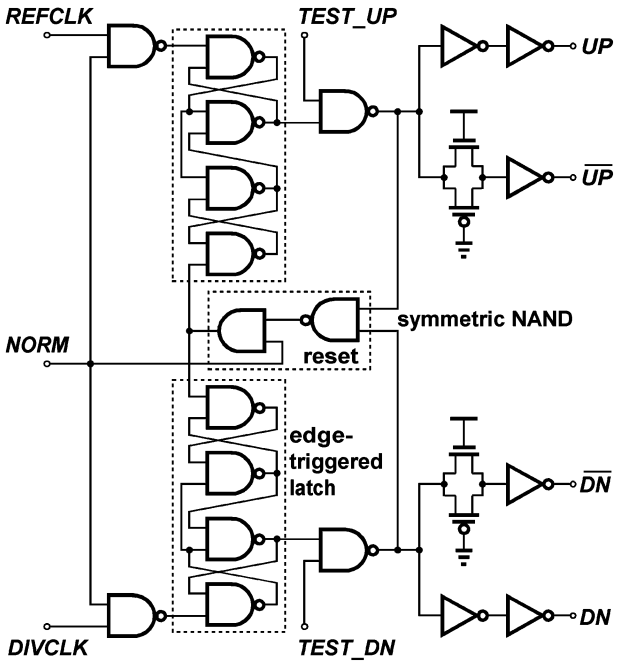


Fig. 3. Schematic of PFD with asynchronous output override.

and *DIVCLK* drive a pair of 12-bit counters that evaluate the polarity and magnitude of frequency difference between the two clocks. With *REFCLK* at its target frequency (f_{REFCLK}), the calibration routine sweeps through its 7-bit range in search of the calibration setting (*CS*) that produces a *DIVCLK* frequency (f_{DIVCLK}) closest to f_{REFCLK}. Calibration enables support of multiple data rates with low VCO gain without compromising VCO input sensitivity to noise. Since these 127 varactors (of the total of 159) are biased to where their nonlinear capacitance-voltage (*C–V*) characteristic is considerably flat, control voltage noise has minimal impact on modulating the tank frequency.

The feedback divider has a selectable divider ratio (N) of 10 to 100 in increments of 10 to allow significant flexibility in f_{REFCLK} input for a given range of VCO output frequencies. Though not shown, intermediate half- and quarter-VCO-rate frequencies are also derived in the divider. This approach mitigates the limited tuning range inherent in resonant oscillators.

III. Design Considerations

A. Phase-Frequency Detector

Phase comparison is achieved with the PFD shown in Fig. 3. To facilitate VCO calibration and PLL testing, additional control logic is incorporated with minimal latency penalty on normal operation to asynchronously force the UP and DN outputs to $\overline{TEST\_UP}$ and $\overline{TEST\_DN}$, respectively, when *NORM* is disabled [15]. Using faster NAND instead of NOR gates in the edge-triggered latches requires a logical inversion that is performed by input NAND gates. These input gates also sharpen input clock transitions to improve noise resilience against slow-rising edges and clock routing parasitic. Incorporating a symmetric NAND in the reset path, wide-channel latch devices, and completely symmetric layout minimizes input-referred phase offset error (ϕ_{os}) between *REFCLK* and *DIVCLK*.

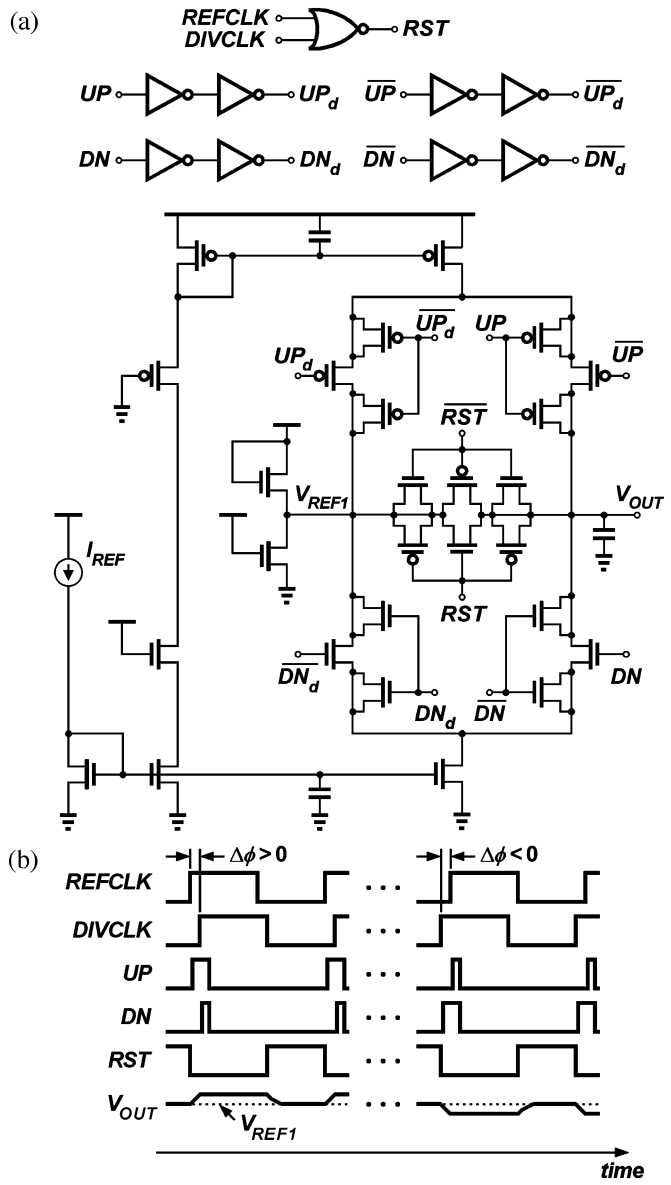


Fig. 4. (a) Schematic of loop filter proportional path and (b) timing diagram illustrating operation.

B. Loop Filter Proportional Path

Phase lead for loop stability compensation is introduced with the simple resistorless sample-reset proportional path depicted in Fig. 4(a) and (b). In migrating to an independent proportional path, we can naturally feed the charge-pump current pulses into a parallel *RC* network where the shunt capacitor (C) squashes control voltage bursts to suppress reference spurs. To save area, we forego the use of an *RC* network. Several resistorless implementations based on sample-reset techniques have been proposed [9], [16]. In this architecture, the charge-pump current pulse develops a small voltage shift that is maintained for approximately half the *REFCLK* period and is subsequently discharged to V_{REF1} through the *RST* switch when both *REFCLK* and *DIVCLK* are low (accomplished by a symmetric NOR gate). Phase error is not integrated from one phase update to the next since the output is reset to V_{REF1} prior to the next phase comparison. Since the transient pulsewidth stretches in proportion

to *REFCLK* period, the resulting time-averaged voltage deviation produced by the proportional path becomes independent of *REFCLK*. This self-compensating behavior significantly relaxes the range of charge pump current required to provide the same phase lead across a flexible range of *REFCLK* frequencies for a given VCO frequency.

Several charge pump design considerations are important. To achieve good voltage gain for a given charge pump current, the capacitive loading at the charge pump output must be minimized. To reduce charge-pump ϕ_{os}, we hold the output current source devices in saturation by steering current through a dummy branch when the output is not integrating charge. A short two-inverter delay is introduced when deactivating this dummy branch to avoid both branches being momentarily cut off during current steering to the output branch. We also cancel charge injection and clock feedthrough offsets created from UP and DN switching with half-width switches [17] instead of CMOS pass gates in order to mitigate mismatches in threshold voltage (V_T) and overlap capacitance between nMOS and pMOS devices.

To maximize bidirectional gain linearity across process, supply voltage, and temperature (PVT) variations, we generate V_{REF1} using $\sim V_T$ drop across a large diode-connected nFET implemented as replicas of the nMOS varactors tuning the VCO [18]. By tracking V_T, V_{REF1} consistently biases the proportional path output to the center of the varactor inversion-to-depletion transition. This biasing scheme also provides low PLL output jitter sensitivity to supply noise when the *RST* switch is enabled. Since V_{REF1} tracks V_{DD} noise and the *LC*-VCO tank swings about a V_{DD} common mode (shown later), both control input and tank nodes of the VCO proportional path varactors track the same V_{DD} noise. Hence, the capacitance contributed by these varactors is relatively immune to supply noise for about half of the *REFCLK* period. Additional noise immunity can be attained by increasing capacitive coupling of the proportional path output to V_{DD} but this coupling reduces the proportional path voltage gain.

Limited voltage headroom continues to pose challenges in low-V_{DD} design. With smaller gate overdrives, device mismatch [19] (particularly due to V_T) is a growing concern necessitating Monte Carlo simulations to statistically validate designs. Moreover, designers must be cognizant that worst-case headroom may occur at low instead of high operating temperature. Reducing temperature by 100 °C could result in a net increase in $|V_{GS}|$ since the increase in $|V_T|$ from bandgap expansion may exceed gate overdrive reduction from better channel mobility at lower temperature. Since cascoding is often not viable, designers should solicit the use of weak-halo devices which exhibit higher output resistance (r_{out}). Although halo implants near the source/drain extension suppress short-channel effects [20], they degrade r_{out} of longer channel devices by allowing drain voltage to modulate the drain-side halo potential barrier, an effect modeled as drain-induced threshold shift [21].

C. Loop Filter Integral Path

The integral path charge-pump gain is selected by mirroring a binary-weighted fraction of a reference current in the output current source devices. Feedback is employed to match UP and DN currents in order to minimize reference spurs created by mismatch particularly at low charge-pump currents. As in the proportional path, when the charge pump is inactive, current is steered into a dummy branch to keep the output current source devices in saturation.

The integral path capacitor (C_{ip}) is implemented as minimum-spaced interdigitated interconnect fingers staggered between consecutive metal levels to maximize interlevel capacitance. Greater area efficiency can be achieved without staggering where interlevel fingers are vertically shorted by vias but extra intralevel via-to-via capacitance comes at a cost of increased variation in capacitance (hence loop behavior) resulting from typical alignment errors between trench and via lithography in dual-damascene copper processing.

As with the proportional path output, the integral path output connects to the VCO with very high gain. Substantial noise injection onto the integral path output can induce significant jitter in the VCO output. One important source of noise comes from V_{DD} through the V_{REF2} bias generator that holds the integral path charge pump output at $(1/2)V_{\mathrm{DD}}$ through operational amplifier feedback. Since the VCO tank swings about V_{DD}, minimizing jitter induced by supply noise requires that the integral path control voltage (hence V_{REF2}) also track the same V_{DD} noise to which the VCO tank is subjected. A simple method of generating $(1/2)V_{\mathrm{DD}}$ is to use a voltage divider, as shown in Fig. 5(a), consisting of two identical diode-connected pFETs. However, in this configuration, V_{REF2} only tracks half of the V_{DD} noise. To improve the ability of V_{REF2} to track V_{DD} noise, one can reduce its AC impedance to V_{DD} by adding capacitance between V_{DD} and V_{REF2} as illustrated in Fig. 5(a). Unfortunately, this approach requires unrealistically large capacitance (and area) for some usable amount of noise reduction. To circumvent this impracticality, we implement an active V_{REF2} generator circuit shown in Fig. 5(b). The devices are sized to still produce a DC bias of $(1/2)V_{\mathrm{DD}}$ but in the AC sense, v_{REF2} is the result of voltage division between the diode-connected pFET $1/g_{m3}$ and the much larger nFET current source r_{out2}. For this V_{REF2} generator, the small-signal V_{DD} noise transfer function is

$$\frac{v_{\mathrm{REF2}}}{v_{V_{\mathrm{DD}}}} \approx 1 - \frac{g_{m2}}{g_{m1}}\frac{g_n}{g_{m3}} \tag{8}$$

where the reference current transconductance to V_{DD} noise, g_n, must be minimized for this approach to be effective, a constraint easily achieved with the use of a bandgap reference.

D. Voltage-Controlled Oscillator (VCO)

The PLL output clock is synthesized by the *LC*-VCO shown in Fig. 6(a). The resonant tank consists of a pair of juxtaposed helical inductors [22] and inversion-mode nMOS varactor arrays resonating around V_{DD}.

For a given inductance and quality factor (Q), multi-level helical inductors consume significantly less area compared to single-level top-metal planar spirals due to much tighter mutual magnetic coupling between windings. X turns perfectly coupled to each other, each with self-inductance L, exhibit a total inductance of $X^2 \times L$. Although tight coupling exacerbates the

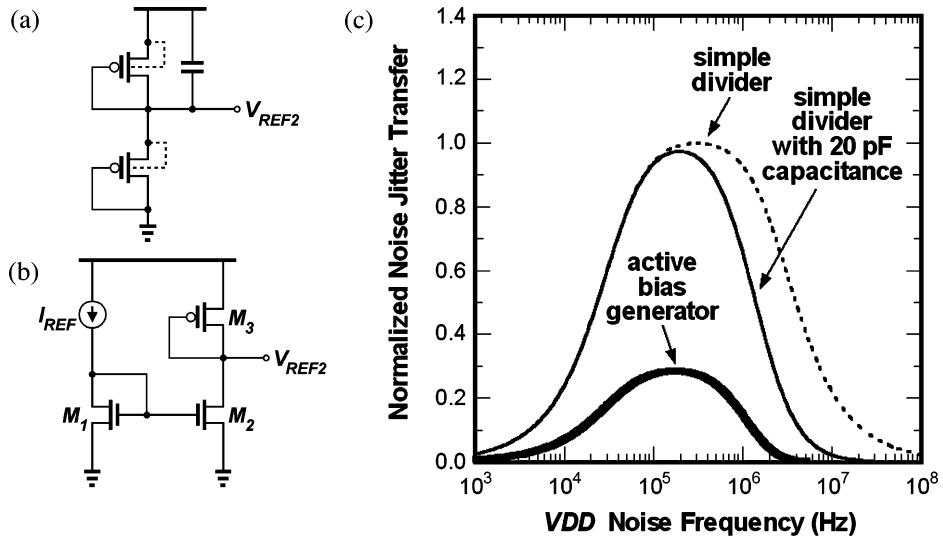


Fig. 5. (a) Basic voltage divider for $(1/2)V_{\rm DD}$ generation, (b) active $V_{\rm REF2}$ generator to track $V_{\rm DD}$ noise, and (c) PLL $V_{\rm DD}$ noise transfer function for both approaches.

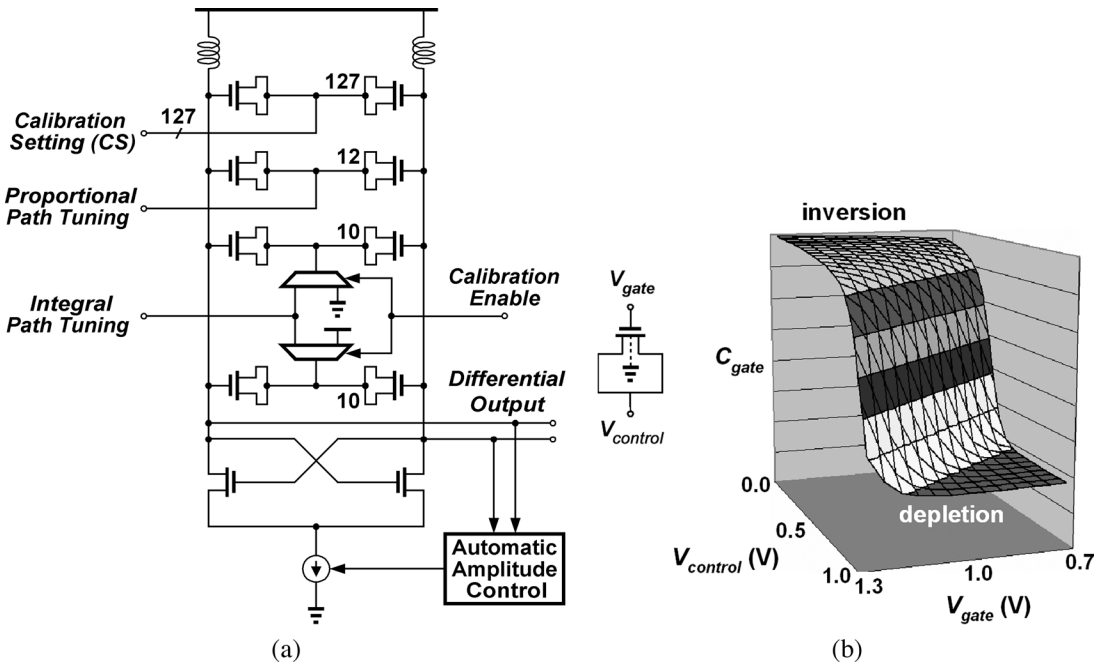


Fig. 6. (a) VCO schematic and (b) *C–V* characteristics of nFET varactor.

proximity effect which degrades series resistance at higher frequencies [23], higher Q inductors are not required in meeting performance targets. Also, despite the use of lower metal levels, capacitive coupling to the substrate is not so severe since the gradual potential drop along the inductor turns leaves the lowest turn exposing only a small fraction of the tank AC voltage to the substrate. An additional measure to mitigate substrate loss is to maximize substrate resistivity beneath the inductors by blocking all well implants in this area to preserve the native doping of $\sim 10^{15}$ cm^{-3}. Helical inductors may not necessarily find application in wireless blocks requiring extremely high Q inductors but certainly offer a distinct advantage in multi-channel wireline SerDes ICs where silicon area and cost are of paramount importance.

Inversion-mode nMOS varactors configured in Fig. 6(b) are chosen over accumulation-mode devices. First, the gate capacitance versus control voltage (*C–V*) characteristic is flatter for control voltages of both *GND* and $V_{\rm DD}$. Since control voltages for the majority coarse-tuning varactors are driven to either supply, the *C–V* flatness translates to superior supply noise immunity and lower jitter. *C–V* flatness at $V_{\rm DD}$ (depletion regime) is attributed to the flatband voltage of the MOS system while flatness at *GND* (inversion regime) is a consequence of poly gate depletion arising from limited gate doping. Interestingly, poly depletion is normally considered undesirable as it reduces gate coupling to the channel. Second, the overall tank Q is still limited by the inductor, so higher Q accumulation-mode varactors are unnecessary. Third, nMOS *C–V* modeling is mature and

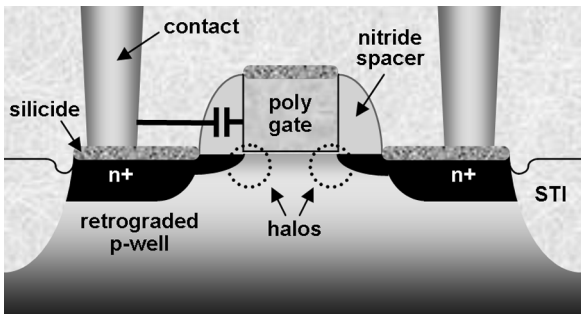


Fig. 7. Pictorial cross section of deep-submicron nMOS transistor.

relatively accurate, a critical consideration since the already limited tuning range in *LC* compared to ring VCOs leaves little to spare for frequency modeling error. Despite its limitations (such as non-quasistatic modeling of channel resistance), BSIM4 FET models [24] are still more accurate across PVT in comparison to *C–V* empirical fit models for accumulation-mode varactors. Accurate *C–V* modeling does, however, require use of higher order BSIM4 fitting parameters such as ACDE, MOIN, NOFF, and VOFFCV [24].

Inversion-mode varactors are also used for proportional and integral path analog tuning. Compared to accumulation-mode varactors, inversion-mode varactors exhibit reduced linearity range of input control voltage which we exploit to reduce *GND* and $V_{\rm DD}$ noise sensitivity. However, we observe that a variable body effect exists as the source/drain control voltage is swept from *GND* to $V_{\rm DD}$ since the substrate is always tied to *GND*. Through its effect on V_T, the modulating body voltage smears the *C–V* transition from inversion to depletion, and provides additional linearity range that is otherwise lost should the substrate be shorted to the source/drain control node (possible in a triple-well process).

Wide tuning range is obviously important for supporting multi-rate links. Core FETs offer better inversion-to-depletion capacitance ratio than I/O FETs but raise gate overvoltage reliability concern for large-signal oscillations about $V_{\rm DD}$. As a result, automatic amplitude control (AAC) feedback is incorporated to clamp the oscillation amplitude by limiting the VCO tail current. More importantly, current-limiting the oscillation improves VCO phase noise by keeping the tail current source in saturation to minimize upconversion of flicker noise into the tank [25]. Given the wide tuning range sought, AAC additionally minimizes the conversion of large-amplitude oscillations about the nonlinear varactor *C–V* into frequency (phase) noise [26], an especially pronounced effect for varactors in depletion. With its thinner gate oxide, core FETs also exhibit significantly higher direct tunneling gate leakage compared to I/O FETs. However, at GHz oscillation frequencies, the total gate current is already dominated by the reactive displacement current across the varactor. Hence, the tunneling leakage contributing to resistive loss does not noticeably degrade varactor Q.

Better tuning range is attained with longer channel varactors through reducing the relative contribution of overlap capacitance as well as higher substrate capacitance near the source/drain extension due to the halo implants. Moreover, longer (and wider) devices are less sensitive to geometry tolerances and provide tighter VCO tuning characteristics across process variations. Longer channels do degrade channel resistance and capacitor Q although some Q can be recovered. Illustrated in Fig. 7, extending the length of the source/drain regions relieves some mechanical compression in the channel induced by surrounding shallow trench isolation [27] and hence reduces mobility degradation in nFETs. This also enables landing active area contacts further away from the poly gate edge and nitride gate spacer (nitride ε_r ~6–8) to additionally improve tuning range. Contact coupling to poly gate, which is additive to Miller capacitance, is an increasingly important parasitic in deep-submicron CMOS. Even the number of contacts should be contemplated since unsparing use of contacts recommended by conventional practice could compromise circuit performance. By minimizing contact-to-poly parasitic, layout is also more resilient to capacitance variation caused by lithography misalignment, an unmodeled tolerance that is not scaling as aggressively as critical dimensions and will only grow as a design-for-manufacturability concern.

To maximize bidirectional tuning in the integral path following calibration, the tank must be loaded with the average integral path capacitance during calibration. A pair of analog multiplexers switches half of the varactor inputs to *GND* and the other half to $V_{\rm DD}$ during calibration, a configuration that overcomes varactor V_T variations across PVT. The PLL feedforward pole introduced by the multiplexer resistance is negligible.

E. Effect of Sampling on Closed-Loop Dynamics

The PLL closed-loop behavior can deviate noticeably from that predicted by traditional s-domain analysis. For a given loop bandwidth and VCO frequency, the validity of the continuous-time approximation degrades as sampling rate $(f_{\rm REFCLK})$ is reduced with a higher feedback divider ratio (N). Due to the wide range of divider ratios that must be supported (10 to 100), the analysis of PLL dynamics must include the effect of sampling in order to accurately predict closed-loop performance.

Numerous methods of discrete-time analysis of charge-pump PLLs have been proposed [28]–[30]. For this PLL architecture, an approach providing good accuracy is the *method of hold equivalence* [30]. Shown in Fig. 8, the zero-order hold equivalence method inserts a sampler and zero-order hold (ZOH) at the input to the loop filter and discretizes the VCO phase output with another sampler. For a given feedforward continuous-time transfer function $H(s)$, the zero-order hold equivalent transfer function $H_{zoh}(z)$ is given by

$$H_{zoh}(z) = (1 - z^{-1}) \cdot Z\left\{\frac{H(s)}{s}\right\}. \tag{9}$$

Applied to this PLL, the resulting discrete-time closed-loop transfer function is

$$H_{dp}(z) = \frac{\Phi_{\rm out}(z)}{\Phi_{\rm in}(z)} = N \times \frac{\alpha z^{-1} + \beta z^{-2}}{2\gamma + (\alpha - 4\gamma)z^{-1} + (\beta + 2\gamma)z^{-2}} \tag{10}$$

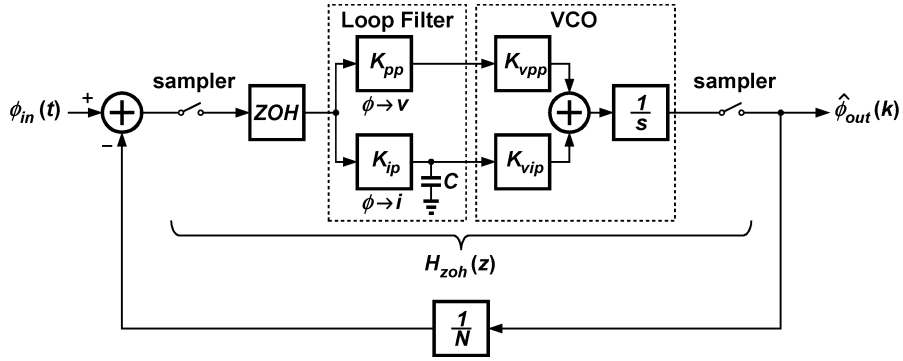


Fig. 8. Method of hold equivalence applied to PLL architecture.

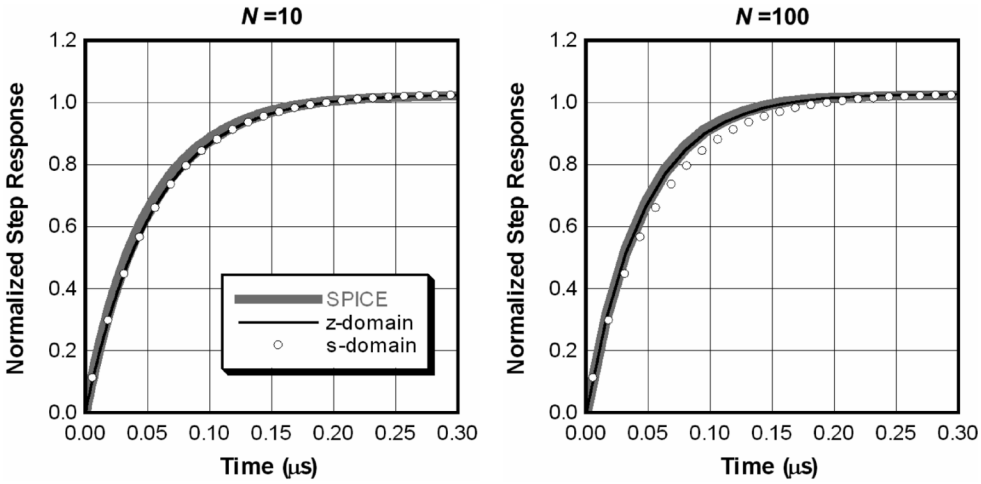


Fig. 9. Step response for divider ratios of (a) 10 and (b) 100 as predicted by s-domain analysis, z-domain analysis, and SPICE simulations.

TABLE III
CLOSED-LOOP BANDWIDTH CALCULATED FROM s- AND z-DOMAIN ANALYSIS

Divider Ratio	f_{REFCLK}	Closed-Loop Bandwidth, f_{BW}			f_{REFCLK}/f_{BW}
		s-Domain	z-Domain	Error	
10	625 MHz	3.05 MHz	3.10 MHz	1.6 %	205
20	312.5 MHz	3.05 MHz	3.15 MHz	3.3 %	102
50	125 MHz	3.05 MHz	3.31 MHz	8.5 %	41
100	62.5 MHz	3.05 MHz	3.66 MHz	20.0 %	21

where, in terms of the loop parameters defined in Fig. 1(b) and sampling period T_s

$$\alpha = 2K_{pp}K_{vpp}CT_s + K_{ip}K_{vip}T_s^2 \tag{11}$$

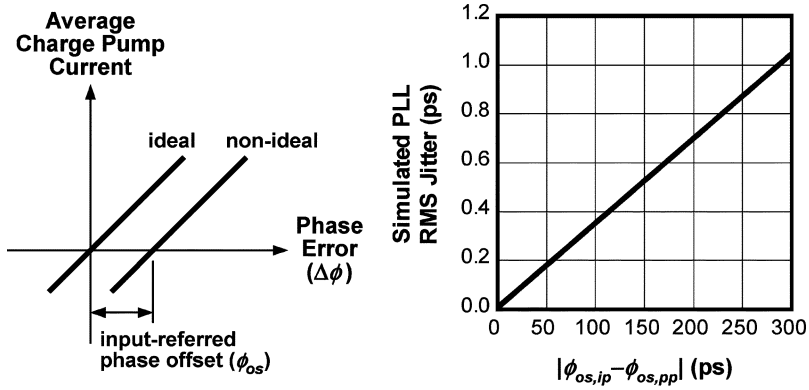
$$\beta = K_{ip}K_{vip}T_s^2 - 2K_{pp}K_{vpp}CT_s \tag{12}$$

$$\gamma = NC. \tag{13}$$

Fig. 9(a) and (b) compares the s- and z-domain transient step responses to SPICE simulations for a PLL with divider ratios of 10 and 100, respectively, having a common bandwidth of 3 MHz. In both cases, the z-domain results match well to SPICE simulations. However, for $N = 100$, the s-domain step response deviates noticeably from the z-domain and SPICE results. Table III tracks the s-domain model accuracy as the effect of sampling becomes more pronounced.

F. Effect of Mismatched Loop Filter Phase Offsets

PLL architectures employing multiple-path loop filter implementations are prone to higher reference spurs if significant mismatch exists between the input-referred phase offsets of the independent paths. A phase offset in the integral path charge pump



(a) (b)

Fig. 10. (a) Input-referred phase offset and (b) simulated impact of phase offset mismatch between proportional and integral paths on PLL jitter.

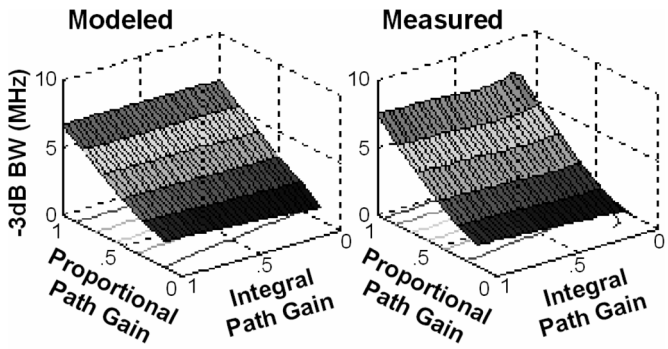


Fig. 11. Modeled versus measured closed-loop bandwidth as a function of normalized proportional and integral path gains (1.0 V, 85 °C, $N = 20$).

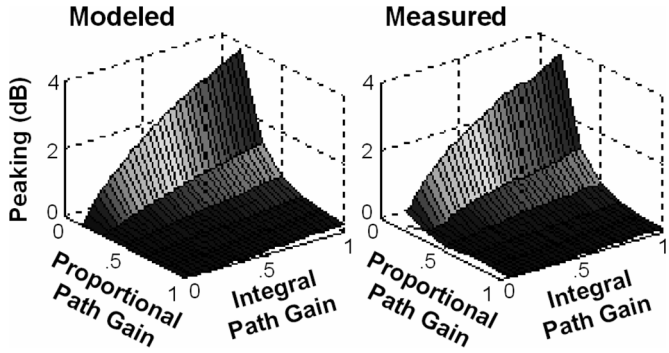


Fig. 12. Modeled versus measured closed-loop peaking as a function of normalized proportional and integral path gains (1.0 V, 85 °C, $N = 20$).

$(\phi_{os,ip})$ will create a steady-state phase offset between *REFCLK* and *DIVCLK* when the PLL is locked. If the proportional path exhibits a different phase offset $(\phi_{os,pp})$, the proportional path will drive its VCO input at every phase update with a voltage pulse proportional to $|\phi_{os,pp} - \phi_{os,ip}|$, thus creating additional jitter at the *REFCLK* rate when the PLL is locked. Fig. 10 illustrates an example of simulated impact of phase offset *mismatch* on PLL jitter. Both integral and proportional path charge pumps were designed to mitigate this effect.

G. Supply Filtering

Since the PLL floorplan was limited by bump pitch, some silicon real estate was available for populating with $V_{\rm DD}$-to-*GND* capacitance to absorb noisy supply grid transients that could induce jitter. Capacitance was implemented using native I/O nFETs ($N_A \approx 10^{15}$ cm^{-3}, $V_T \approx 0$ V) to suppress gate tunneling leakage while maximizing inversion charge to reduce channel resistance and associated thermal noise [31] as well as to extend filtering bandwidth.

All noise-sensitive analog and mixed-signal circuits within each transmitter PLL are powered by a pair of independent $V_{\rm DD}$ and *GND* bumps which are connected to additional package- and board-level filtering. For supply noise isolation, digital control circuitry including the calibration logic is powered by another set of supply bumps.

IV. Results and Discussion

A. Closed-Loop Dynamics

Closed-loop bandwidth and peaking were extracted from *REFCLK* jitter transfer measurements at 32 integral and 6 proportional path gain settings. Figs. 11 and 12 summarize a typical example of measured versus modeled closed-loop bandwidth and peaking. The discrete-time model demonstrates good agreement to silicon measurements. As predicted by (5) and (7), bandwidth is primarily set by the proportional path gain while peaking is minimized by maintaining a low integral path gain relative to proportional path gain. This flexibility enables the PLL closed-loop response to be tailored predictably to specifications (bandwidth, *REFCLK* jitter, spread spectrum modulation, etc.) dictated by the networking standard of interest. In complying with most wireline SerDes protocols, peaking typically must not exceed 1 dB although this PLL provides up to 3.9 dB. The faster step response times attained with more closed-loop peaking comes at the expense of increased jitter multiplication.

B. VCO Coarse Tuning

The VCO was fabricated with seven inductor variants to target coverage of practical combinations of SerDes rates highlighted in Table I. Fig. 13 shows the VCO continuous coarse tuning characteristics in terms of calibration setting (*CS*) as a function of VCO frequency $(= N \times f_{\rm REFCLK})$. In this measurement, the analog multiplexers in the VCO are activated

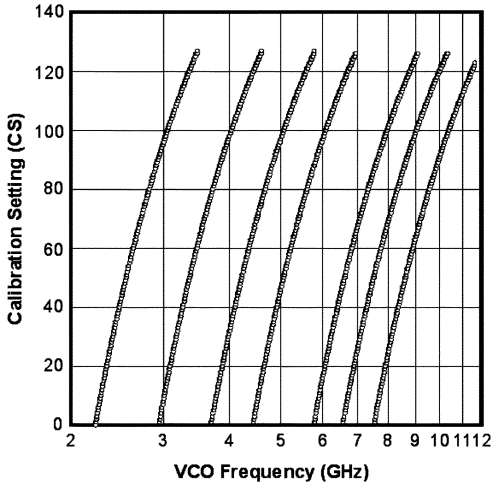


Fig. 13. Measured VCO coarse tuning characteristics for seven inductor variants, each spanning 45% calibration tuning range (1.0 V, 85 °C).

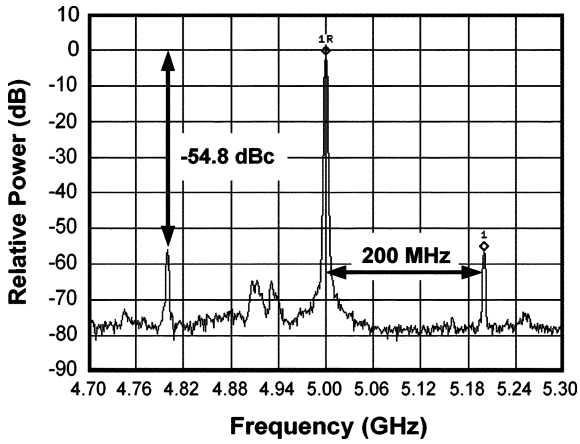


Fig. 14. Measured closed-loop transmitter output spectrum at data rate of 10 Gb/s (1.0 V, 85 °C, $N = 50$). Transmitter is launching NRZ data sequence of alternating ones and zeros. Spectrum illustrates Nyquist carrier at 5 GHz with reference spurs at $\Delta f = 200$ MHz.

to "midrail" the integral path capacitance. All inductor variants span a calibration tuning range of 45% (equivalent to frequency ratio of 1.6:1) which is in good agreement with SPICE prediction of 43%. This match requires FET *C–V* modeling that accurately reflects the increased substrate doping from halo implants.

C. Output Jitter

The PLL output jitter was measured with the transmitter launching a NRZ sequence of alternating ones and zeros. Jitter was extracted from the frequency spectrum as available time-domain instruments could not achieve sub-picosecond accuracy. To extract jitter, we relate the power of some frequency spur, in dBc, at an offset Δf from the carrier frequency, f_c, to the corresponding RMS jitter. From analysis of single-tone frequency modulation with small modulation index, it can be shown that

$$J_{\mathrm{rms}}^2(\Delta f) = \frac{10^{\frac{[dBc(\Delta f)]}{10}}}{2\pi^2 f_c^2}. \tag{14}$$

We extract the total RMS jitter by integrating (14) across Δf of 1 kHz to 100 MHz beyond which the spectrum analyzer noise floor is dominant. As an example, the transmitter output demonstrates 0.81 ps rms jitter at 10 Gb/s (corresponding to a Nyquist rate of 5 GHz since the transmitter output is NRZ) with reference spurs at −54.8 dBc (Fig. 14). Most of this random jitter falls within the loop bandwidth of a reasonable receiver PLL. In Fig. 14, jitter from the reference spurs falls outside the bandwidth of jitter integration and is excluded from the computed jitter as it contributes negligible error. The asymmetric spurs at −63 dBc is attributed to coupling from an adjacent SerDes channel.

D. VCO Post-Calibration Tuning

The post-calibration tuning characteristics of the integral path was characterized using an on-chip 8-bit analog-to-digital converter (ADC) connected to the VCO integral path input. A first-order $\Sigma\Delta$ topology was selected for its simplicity and

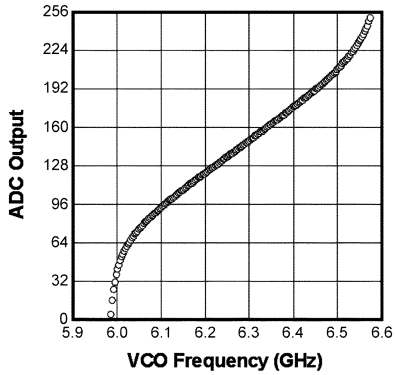


Fig. 15. ADC output versus VCO frequency after calibration at 6.25 GHz (1.0 V, 85 °C).

robustness. Shown in Fig. 15 is a plot of the ADC output versus VCO frequency after the VCO is calibrated at 6.25 GHz. The plot illustrates how the integral path control voltage traverses to maintain frequency lock as the VCO frequency is tuned around the calibration frequency. The shape directly maps the effective *C–V* characteristic of the 20 integral path varactors and enables accurate extraction of VCO gain which in turn facilitates accurate modeling of PLL loop dynamics.

The integral path provides ±10 varactors of post-calibration tuning to cover VCO frequency sensitivities dominated by V_{DD} and temperature variations as the PLL operating condition drifts from the calibration condition. In some applications such as SAS, SATA, and PCIe, post-calibration tuning must also accommodate spread-spectrum modulation but this typically consumes an insignificant amount of available frequency tuning. For a given inductor, this available tuning corresponds to a hold range of 4.8% (at minimum VCO frequency) to 11.4% (at maximum VCO frequency); the variation simply reflects the fixed integral path capacitance comprising a higher fraction of the total tank capacitance at higher frequency.

Incorporating excessive integral path tuning is not prudent as it compromises control voltage susceptibility to noise. We examine the *range* of coarse-tuning *CS* values at a given frequency

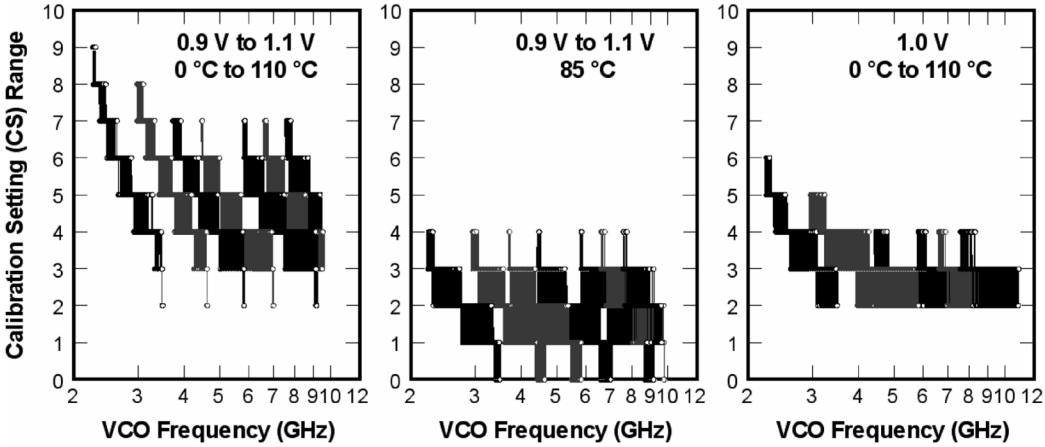


Fig. 16. Measured calibration setting (*CS*) range across operating $V_{\rm DD}$ and temperature (0.9–1.1 V, 0–110 °C) for seven inductor variants.

across all operating $V_{\rm DD}$ and temperature extremes to verify the PLL robustness to remain locked following calibration [32]. The *CS* range reflects the worst-case capacitance correction needed to maintain frequency lock over worst-case $V_{\rm DD}$ and temperature excursions from the calibration condition. As seen in Fig. 16, over an operating range of 0.9–1.1 V and 0–110 °C, the *CS* range does not exceed 10 for all frequencies attained by the seven inductor variants. Isolating the *CS* range to functions of only $V_{\rm DD}$ or temperature variation, we additionally learn that the VCO is more sensitive to temperature variations than $V_{\rm DD}$ variations, a result attributed to inductor Q limitation [33].

E. Analysis of LC-VCO Temperature Sensitivity

To understand the observed temperature sensitivity, we solve for the resonance condition of a lossy *LC* tank, with R_L and R_C parasitics, respectively, in series with L and C, to obtain

$$\omega^2 = \frac{1}{LC}\frac{1-\dfrac{C}{L}R_L^2}{1-\dfrac{C}{L}R_C^2} = \frac{1}{LC}\frac{1+\dfrac{1}{Q_C^2}}{1+\dfrac{1}{Q_L^2}} \tag{15}$$

where the expression in terms of $Q_L = \omega L/R_L$ and $Q_C = 1/\omega C R_C$ is derived via impedance transformation to a parallel tank. In this design, since tank Q is limited by the inductor, i.e., $Q_L \ll Q_C$, (15) reduces to

$$\omega^2 \approx \frac{1}{LC} - \frac{R_L^2}{L^2}. \tag{16}$$

In relating to our analysis, the capacitance sensitivity to temperature at constant ω is proportional to the measured *CS* range. Hence, we compute

$$\begin{aligned}\left.\frac{dC}{dT}\right|_{\omega} &= -\frac{2R_L C^2}{L}\frac{dR_L}{dT} + \left(\frac{2R_L^2C^2}{L^2} - \frac{C}{L}\right)\frac{dL}{dT} \\ &\approx -\frac{2R_L^2C^2}{L}TCR + \left(\frac{2R_L^2C^2}{L} - C\right)TCL \end{aligned} \tag{17}$$

where TCR and TCL are, respectively, the linear temperature coefficients of R_L and L. TCR is approximately the linear temperature coefficient of resistance of copper $(3 \times 10^{-3}\ \mathrm{K}^{-1})$. TCL reflects the change in enclosed magnetic flux with temperature due to inductor elongation (and current redistribution) and is a complex weighted average of the thermal expansion coefficients of copper $(17 \times 10^{-6}\ \mathrm{K}^{-1})$ and the underlying silicon substrate $(3 \times 10^{-6}\ \mathrm{K}^{-1})$. Using practical values of L, C, and R_L, it can be shown that the inductance sensitivity to temperature is numerically insignificant compared to that of R_L. This observation justifies simplifying (17) to

$$\left.\frac{dC}{dT}\right|_{\omega} \approx -\frac{2R_L^2C^2}{L}TCR. \tag{18}$$

Eq. (18) explains the trend common to all inductor variants in Fig. 16, namely reduced temperature sensitivity at lower C (higher frequency) for a given L. Higher frequency VCOs with smaller inductance do not exhibit worse temperature sensitivity due to a commensurate reduction in R_L made possible by shorting metal turns. Eq. (18) also emphasizes the importance of including the temperature coefficient of R_L as well as R_L itself when simulating the temperature sensitivity of an *LC*-VCO. Recall that the simplified relationship in (18) assumed that tank Q was limited by the inductor. If capacitor Q cannot be neglected, capacitance sensitivity to temperature must account for the effect of R_C which yields more tedious expressions for dC/dT.

The insight in (18) serves as an extra design criterion for *LC*-VCO optimization. Clearly, the temperature sensitivity can be reduced with the use of higher Q inductors but this improvement may require a substantial area penalty.

F. Performance Summary

The measured PLL performance is summarized in Table IV. See Fig. 17 for the accompanying die micrograph.

V. Conclusion

We have presented a charge-pump PLL architecture that offers significant versatility to meet a wide variety of SerDes transmitter clocking applications in the 1 to 10 Gb/s range. Much of the flexibility is derived from a dual-path loop filter that offers simple control of closed-loop bandwidth and peaking. Furthermore, the separated proportional path control enables an area-efficient resistorless implementation. In multiple-path loop

TABLE IV
SUMMARY OF MEASURED PERFORMANCE

Technology	90-nm CMOS (8M Cu/low-κ)
Supply Voltage	1.0 V (core)
Output RMS Jitter	0.81 ps @ 10 Gb/s (85 °C)
Selectable –3 dB Bandwidth	0.46 to 7.5 MHz
Selectable Peaking	0.0 to 3.9 dB
Feedback Divider Ratio	10 to 100 (increments of 10)
VCO f_{center} Range	2.9 to 9.8 GHz
Calibration Tuning Range	45% (frequency ratio of 1.6:1)
Post-Calibration Hold Range	4.8% minimum
Silicon Area	0.056 mm^2 (280 μm × 200 μm)
Power per SerDes Channel	96 mW @ 10 Gb/s (85 °C)

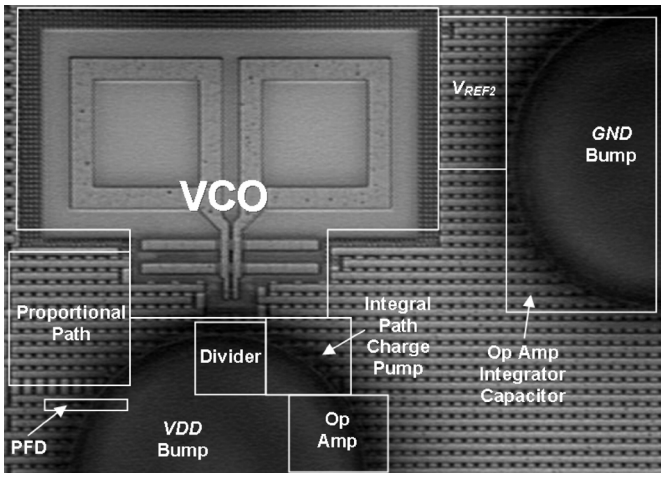


Fig. 17. Die micrograph of transmitter PLL integrated into SerDes macro.

filter architectures, it is prudent to minimize the mismatch between input-referred phase offsets of all paths in order to suppress reference spurs that degrade jitter performance. To optimize the PLL design for manufacturability, it was critical to consider deep-submicron CMOS technology effects such as mismatch, lithography misalignment, parasitics of growing importance such as contact-to-poly capacitance, halo implants, and mechanical strain in the device channels. These were especially important for maximizing the tuning range of the *LC*-VCO. We also analyzed the tradeoff between jitter sensitivity and available hold tuning range for compensating VCO sensitivities to $V_{\rm DD}$ and temperature. We achieved reduced $V_{\rm DD}$ sensitivity by biasing the majority of the VCO varactors into flat regions of their *C–V* characteristics and by tracking $V_{\rm DD}$ noise in the loop filter paths. Temperature sensitivity was an important consideration since inductor Q was compromised in order to exploit the significant area advantage of multi-level helical inductors.

ACKNOWLEDGMENT

The authors are indebted to T. Cynkar, B. Lai, J. Pfiester, P. Fisher, J. Xia, K.-S. Liew, C.-F. Loi, A. Volz, C. Wang, R. Owens, and L. Metz of Avago Technologies; J. Barnes of Hewlett-Packard; S. Sawyer of Intel; J. Nguyen of International Rectifier; and R. Hernandez of PMC-Sierra for valuable discussions. Design contributions from R. Zimmer, H. Pang, K. Arave, R. Martin, R. Miller, D. Hood, M. Wahl, K. Stafford, and T. Abeyta, as well as management support from G. Motley, E. Rojas, and T. Walley are gratefully acknowledged. The authors also thank Guest Editor J. Savoj and the anonymous peer reviewers for their valuable perusal, insights, and corrections.

REFERENCES

[1] M. Horowitz, C.-K. K. Yang, and S. Sidiropoulos, "High-speed electrical signaling: overview and limitations," *IEEE Micro*, vol. 18, no. 1, pp. 12–24, Jan. 1998.

[2] J. L. Zerbe, C. W. Werner, V. Stojanovic, F. Chen, J. Wei, G. Tsang, D. Kim, W. F. Stonecypher, A. Ho, T. P. Thrush, R. T. Kollipara, M. A. Horowitz, and K. S. Donnelly, "Equalization and clock recovery for a 2.5–10-Gb/s 2-PAM/4-PAM backplane transceiver cell," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2121–2130, Dec. 2003.

[3] M. Sorna, T. Beukema, K. Selander, S. Zier, B. Ji, P. Murfet, J. Mason, W. Rhee, H. Ainspan, and B. Parker, "A 6.4 Gb/s CMOS SerDes core with feedforward and decision-feedback equalization," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 62–63.

[4] S. Gondi, J. Lee, D. Takeuchi, and B. Razavi, "A 10 Gb/s CMOS adaptive equalizer for backplane applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 328–329.

[5] A. X. Widmer and P. A. Franaszek, "A DC-balanced, partitioned-block, 8 B/10 B transmission code," *IBM J. Res. Devel.*, vol. 27, no. 5, pp. 440–451, Sep. 1983.

[6] R. C. Walker, B. Amrutur, and R. W. Dugan, "Decoding method and decoder for 64 B/66 B coded packetized serial data," U.S. Patent 6,650,638, Nov. 18, 2003.

[7] K. Azadet, E. F. Haratsch, H. Kim, F. Saibi, J. H. Saunders, M. Shaffer, L. Song, and M.-L. Yu, "Equalization and FEC techniques for optical transceivers," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 317–327, Mar. 2002.

[8] F. M. Gardner, *Phaselock Techniques*, 3rd ed. New York: Wiley, 2005.

[9] A. Maxim, B. Scott, E. M. Schneider, M. L. Hagge, S. Chacko, and D. Stiurca, "A low-jitter 125–1250-MHz process-independent and ripple-poleless 0.18-μm CMOS PLL based on a sample-reset loop filter," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1673–1683, Nov. 2001.

[10] T.-C. Lee and B. Razavi, "A stabilization technique for phase-locked frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 888–894, Jun. 2003.

[11] J. G. Maneatis, J. Kim, I. McClatchie, J. Maxey, and M. Shankaradas, "Self-biased high-bandwidth low-jitter 1-to-4096 multiplier clock generator PLL," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1795–1803, Nov. 2003.

[12] A. L. S. Loke, J. O. Barnes, R. K. Barnes, M. M. Oshima, R. R. Kennedy, and C. E. Moore, "Low-jitter charge-pump phase-locked loop," U.S. Patent Application, submitted Nov. 2003.

[13] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential *LC* oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[14] P. Andreani and S. Mattisson, "On the use of MOS varactors in RF VCOs," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 905–910, Jun. 2000.

[15] A. L. S. Loke, R. K. Barnes, and J. O. Barnes, "Phase detector system with asynchronous output override," U.S. Patent Application, submitted Nov. 2003.

[16] J. Kim, J.-K. Kim, B.-J. Lee, N. Kim, D.-K. Jeong, and W. Kim, "A 20-GHz phase-locked loop for 40 Gb/s serializing transmitter in 0.13 μm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2005, pp. 144–147.

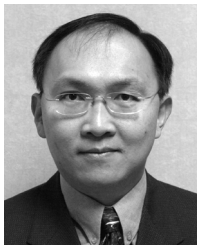
[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

[18] A. L. S. Loke, T. T. Wee, R. K. Barnes, K. L. Arave, T. E. Cynkar, and J. R. Pfiester, "Method of biasing a metal-oxide-semiconductor capacitor for capacitive tuning," U.S. Patent Application, submitted Nov. 2003.

[19] M. J. M. Pelgrom, H. P. Tuinhout, and M. Vertregt, "Transistor matching in analog CMOS applications," in *Proc. Int. Electron Device Meeting*, 1998, pp. 915–918.

[20] R. Rios, W.-K. Shih, A. Shah, S. Mudanai, P. Packan, T. Sandford, and K. Mistry, "A three-transistor threshold voltage model for halo processes," in *Proc. Int. Electron Device Meeting*, 2002, pp. 113–116.

[21] K. M. Cao, W. Liu, X. Lin, K. Vasanth, K. Green, J. Krick, T. Vrotsos, and C. Hu, "Modeling of pocket implanted MOSFETs for anomalous analog behavior," in *Proc. Int. Electron Device Meeting*, 1999, pp. 171–174.
[22] C. E. Moore, "Oscillator for SerDes," U.S. Patent 6,943,636, Sep. 13, 2005.
[23] C. P. Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 560–568, Mar. 2000.
[24] X. Xi, M. Dunga, J. He, W. Liu, K. M. Cao, X. Jin, J. J. Ou, M. Chan, A. M. Niknejad, and C. Hu, BSIM4.3.0 MOSFET Model User's Manual, Regents Univ. California. Berkeley, CA, 2003.
[25] B. D. Muer, M. Borremans, M. Steyaert, and G. L. Puma, "A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1034–1038, Jul. 2000.
[26] E. Hegazi and A. A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, Jun. 2003.
[27] R. A. Bianchi, G. Bouche, and O. Roux-dit-Buisson, "Accurate modeling of trench isolation induced mechanical stress effect on MOSFET electrical performance," in *Proc. IEEE Int. Electron Device Meeting*, 2002, pp. 117–120.
[28] J. P. Hein and J. Scott, "z-domain model for discrete-time PLLs," *IEEE Trans. Circuits Syst.*, vol. 35, no. 11, pp. 1393–1400, Nov. 1988.
[29] J. Lu, B. Grung, S. Anderson, and S. Rokhsaz, "Discrete z-domain analysis of high order phase locked loops," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2001, vol. 1, pp. 260–263.
[30] G. F. Franklin, J. D. Powell, and M. L. Workman, *Digital Control of Dynamic Systems*, 3rd ed. Menlo Park, CA: Addison-Wesley Longman, 1998.
[31] P. Larsson, "Parasitic resistance in an MOS transistor used as on-chip decoupling capacitance," *IEEE J. Solid-State Circuits*, vol. 32, no. 4, pp. 574–576, Apr. 1997.
[32] A. L. S. Loke and M. J. Gilsdorf, "Method and apparatus for measuring supply voltage and temperature sensitivities of a voltage-controlled oscillator," U.S. Patent Application, submitted Aug. 2005.
[33] T. Tanzawa, H. Shibayama, R. Terauchi, K. Hisano, H. Ishikuro, S. Kousai, H. Kobayashi, H. Majima, T. Takayama, K. Agawa, M. Koizumi, and F. Hatori, "A temperature-compensated CMOS LC-VCO enabling the direct modulation architecture in 2.4 GHz GFSK transmitter," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2004, pp. 273–276.



Alvin L. S. Loke (S'89-M'99-SM'04) received the B.A.Sc. degree in engineering physics (highest honors) from the University of British Columbia, Vancouver, BC, Canada, in 1992, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1994 and 1999, respectively. He was recipient of the Canadian NSERC 1967 Graduate Scholarship. His doctoral research focused on integration and reliability of copper and low-permittivity interconnects.

He has interned at Sumitomo Electric Industries, Osaka, Japan, studying CVD diamond surfaces as well as at Texas Instruments Inc., Dallas, TX, and Motorola, Austin, TX, developing interconnect technologies. In 1998, he joined Hewlett-Packard Laboratories, Palo Alto, CA, where he was involved in development of embedded ferroelectric memory. In 1999, when Agilent Technologies divested from Hewlett-Packard, he transferred to Chartered Semiconductor Manufacturing, Singapore, where he worked on copper and local interconnect integration. Two years later, he moved to Fort Collins, CO, where he designed CMOS PLL/DLL circuits for embedded SerDes and ASIC clocking in the Enterprise ASIC Laboratory of Agilent Technologies (now Avago Technologies). In 2006, he joined the Mile High Design Center of Advanced Micro Devices in Fort Collins, CO where he is presently Senior Member of Technical Staff. He has authored over 20 technical publications and holds three patents.

Dr. Loke is presently Chair of the IEEE Solid-State Circuits Society in Denver (named Outstanding Chapter in 2005) and currently serves on the CICC technical program committee.

Robert K. Barnes (S'77–M'81–SM'05) received the B.S. degree in electrical engineering (*summa cum laude*) from Washington State University, Pullman, WA, in 1980, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1987.

Prior to his undergraduate studies, he served in the U.S. Air Force repairing and maintaining ground-based navigation transmitters. In 1980, he joined the Disk Memory Division of Hewlett-Packard Company, Boise, ID, where he worked on disk drive head/servo characterization and advanced read channel designs. In 1996, he transferred to the Hewlett-Packard IC design center in Fort Collins, CO. He is currently Senior Design Engineer at Avago Technologies (formerly Agilent Technologies) in Fort Collins, CO, developing CMOS mixed-signal PLL architectures and circuits for low-jitter embedded SerDes for wireline applications. He holds five patents in areas of disk drive and IC design. His technical interests include high-speed design, PLLs, and control systems.

Mr. Barnes is presently Vice Chair and Treasurer of the IEEE Solid-State Circuits Society in Denver (named Outstanding Chapter in 2005). He is a member of Tau Beta Pi.

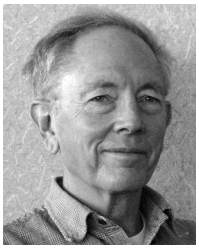
Tin Tin Wee (M'04–SM'05) received the B.Tech. degree in electronics engineering (with honors) and the M.S. degree in electrical engineering from the National University of Singapore, Singapore, in 1999 and 2001, respectively.

In 1992, she joined International Video Products, Singapore, where she was involved in RF test, measurement, and failure analysis of consumer video electronics. In 1996, she joined Chartered Semiconductor Manufacturing, Singapore, where she was engaged in 0.25 μm, 0.18 μm, and 0.15 μm technology development and transfer. Her activities ranged from SRAM development, yield enhancement, and failure analysis to aluminum, copper, and local interconnect integration. From 2004 to mid-2006, she was with Agilent Technologies (now Avago Technologies) in Fort Collins, CO, where she was involved in bench test, characterization, and troubleshooting of CMOS ASICs with low-jitter embedded SerDes transceivers and PLL/DLL circuits for ASIC clocking. She also contributed towards test development for the IEEE802.3ap Backplane Ethernet Task Force. She is now with the Mile High Design Center of Advanced Micro Devices in Fort Collins, CO. She holds two patents.

Ms. Wee is presently Secretary/Webmaster of the IEEE Solid-State Circuits Society in Denver (named Outstanding Chapter in 2005).

Michael M. Oshima (S'80-M'96-SM'06) received the B.S. and M.S. degrees in electrical engineering from the University of Hawaii at Manoa, Honolulu, HI, in 1983 and 1987, respectively.

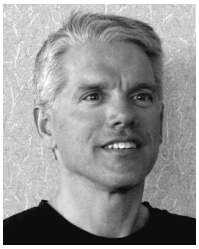
He joined the Hewlett-Packard Company, Santa Clara, CA, in 1987. From 1987 to 1995, he worked on custom high-speed bipolar ICs for test instruments and computer workstations. From 1995 to 1999, he designed CMOS PLLs and analog circuits for laser printer ASICs. From 1999 to early 2006, he was with Agilent Technologies (now Avago Technologies) designing *LC* oscillators, CDRs, and PLLs for standard-product SerDes and embedded SerDes transceivers. Presently, he is with PMC-Sierra in Santa Clara, CA. His technical interests include mixed-signal high-speed circuit design, CDRs, *LC* oscillators, and PLLs.



Charles E. Moore (M'04) received the B.S. degree in electrical engineering from the University of California, Berkeley, CA, in 1966, and the M.S. degree in optics from the University of Rochester, Rochester, NY, in 1978.

Prior to graduation, he served in the U.S. Army as a radar technician. In 1966, he joined the Hewlett-Packard Company, Loveland, CO, where he first worked on signal analysis instrument design, then on electronic surveying instrument design where he designed the first laser surveying total station. He continued his technical career in IC product engineering and design. In 1987, he transferred to the Colorado IC Division in Fort Collins, CO. When Agilent Technologies divested from Hewlett-Packard, he continued with Agilent Technologies (now Avago Technologies) where he is presently Chief SerDes Architect. He holds over 30 patents.

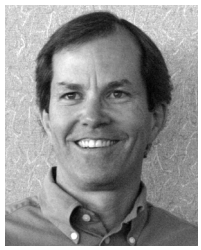
Mr. Moore presently serves as an *ad hoc* committee chair and co-editor in the IEEE802.3ap Backplane Ethernet Task Force. He is a member of the Optical Society of America and the American Association for the Advancement of Science.



Ronald R. Kennedy (S'80–M'06) received the B.S. degree in electrical engineering (with honors) from Tri-State University, Angola, IN, in 1982, and the M.S. degree in electrical engineering from Colorado State University, Fort Collins, CO, in 1984.

Upon graduation, he joined Total Logic Corporation, Fort Collins, CO, developing software and hardware for PC-based logic analyzers. In 1986, he joined Colorado Memory Systems, Loveland, CO, where he worked on read/write channels for tape drives. In 1992, when Colorado Memory Systems was acquired by Hewlett-Packard, he continued to work on both optical and magnetic channels. In 1999, coincident with the divestiture of Agilent Technologies from Hewlett-Packard, he transferred to the Agilent (now Avago Technologies) IC design center in Fort Collins, CO, where he currently focuses on the development of CMOS receivers for embedded SerDes applications. He holds four patents in the area of optical and magnetic recording devices. His technical interests include channel equalization, bang-bang PLLs, and high-speed design.

Mr. Kennedy is a member of Tau Beta Pi.



Michael J. Gilsdorf (M'96–SM'06) received the B.S. degree in electrical engineering from the University of Utah, Salt Lake City, in 1983, and the M.S. degree in computer engineering from National Technological University in 1993.

In 1983, he joined the Hewlett-Packard Company, Corvallis, OR, where he worked on analog sub-systems for calculator ICs. In 1990, he became R&D project manager for the Integrated Business Division overseeing design automation and services for the local design center. Since 1993, he has managed several R&D programs involving multiple mixed-signal ASIC designs. These projects have included A/D converters for multi-function printers, PRML R/W channels for DAT drives, as well as high-speed pin electronics and test processor ASICs for both FLASH memory and system-on-a-chip automated test equipment. The latter work for testers happened following his transfer to Fort Collins, CO, in 1996. Since 2000, as part of Agilent Technologies (now Avago Technologies), he has managed the design and development of high-speed SerDes and low-jitter PLL/DLLs for embedded applications. This work includes XAUI, SGMII, PCIe, SAS/SATA, and Fibre Channel SerDes. Of particular note is the volume production of 3.125 G SerDes, the industry's first implementation of IEEE 1149.6, and the introduction of 6.25 G and 8.5 G SerDes (including eBERT and DFE) for use over legacy backplanes. His work in SerDes now spans four generations of CMOS technology: 0.18 μm, 0.13 μm, 90 nm, and recently 65 nm. He holds two patents.

Mr. Gilsdorf is a member of Tau Beta Pi.