Bandwidth Extension Techniques for CMOS Amplifiers

Sudip Shekhar, *Student Member, IEEE*, Jeffrey S. Walling, *Student Member, IEEE*, and David J. Allstot, *Fellow, IEEE*

***Abstract*—Inductive-peaking-based bandwidth extension techniques for CMOS amplifiers in wireless and wireline applications are presented. To overcome the conventional limits on bandwidth extension ratios, these techniques augment inductive peaking using capacitive splitting and magnetic coupling. It is shown that a critical design constraint for optimum bandwidth extension is the ratio of the drain capacitance of the driver transistor to the load capacitance. This, in turn, recommends the use of different techniques for different capacitance ratios. Prototype wideband amplifiers in 0.18-μm CMOS are presented that achieve a measured bandwidth extension ratio up to 4.1 and simultaneously maintain high gain (>12 dB) in a single stage. Even higher enhancement ratios are shown through the introduction of a modified series-peaking technique combined with staggering techniques. Ultra-wideband low-noise amplifiers in 0.18-μm CMOS are presented that exhibit bandwidth extension ratios up to 4.9.**

***Index Terms*—Bandwidth extension, low-noise amplifier, low-power, peaking, staggering, T-coil, transformer, ultra-wideband (UWB), wireless, wireline.**

I. Introduction

COMMUNICATION trends foretell future CMOS solutions that transmit and receive data at high speeds with low error rates, low cost and low power. Wireline devices that operate at 10–40 Gb/s such as MUX/DEMUX circuits for Ethernet applications demand the design of broadband amplifiers [1], [2], and 40 Gb/s optical transceivers [Fig. 1(a)] require broadband amplification in constituent preamplifiers, drivers, transimpedance amplifiers, etc. [3]. Ultra-wideband (UWB) wireless receivers [Fig. 1(b)] that function in the 3.1–10.6 GHz spectrum also benefit from bandwidth extension techniques in low-noise amplifier (LNA) designs [4], [5].

Although CMOS is viable for system-on-chip solutions, its parasitics limit the performance of broadband amplifiers and motivate the use of bandwidth extension techniques such as distributed amplification. However, distributed amplifiers consume large area and high power and are difficult to design owing to delay line losses that necessitate extensive modeling and electromagnetic simulation.

Passive filtering (e.g., shunt and series peaking) has been used since the 1930s to extend amplifier bandwidth; it uses inductors to trade off bandwidth versus peaking in the magnitude response [6], [7]. Because conventional methods provide limited bandwidth extension to meet the critical requirements of high-speed applications, there is a need for techniques that achieve larger bandwidths without increased power consumption and design complexity.

Consider the common-source amplifier shown in Fig. 2 where R is the load resistance, and C_1 and C_2 represent the drain parasitic and load capacitance, respectively; it is used extensively in differential amplifiers in wireline applications with several stages cascaded to achieve high gain. Thus, C_2 includes the gate capacitance of the next stage. Depending on the scaling of adjacent stages, the ratio $k_C = C_1/C = C_1/(C_1 + C_2)$ typically varies from 0.2–0.5.[1] Note that k_C is a *design constraint* because the desired gain, voltage swing, and bias current set the transistor sizes in each stage. This observation leads to two important conclusions: 1) A given bandwidth extension technique may not be optimum for all k_C values, and 2) a multi-stage amplifier may achieve superior performance using different bandwidth extension techniques in different stages.

In wireless applications, a common-source LNA with an input matching network (e.g., a source-degenerated UWB LNA [8]) achieves a bandpass response. C_2 includes the gate capacitance of the buffer or mixer following the LNA, and typical values of k_C again range from 0.2–0.5 because the transistor sizing depends on gain, bias current, noise figure (NF), etc. In contrast, transistor sizes in a common-gate LNA are often smaller so k_C can be less than 0.2.

This paper describes broadband design approaches that achieve substantially larger bandwidth extension ratios (*BWER*s) than previously demonstrated, with an underlying theme that different drive/load conditions (k_C) and different applications (low-pass for wireline and bandpass for wireless) demand different techniques for best performance. In each of Sections II through IV, a conventional bandwidth extension technique based on passive filtering is first presented, and an improved approach with a larger *BWER* is then introduced. Sections V and VI describe the design of high-speed wideband amplifiers for wireline applications and give measured results, respectively. A series-peaking technique with large gain-peaking for low-k_C applications is proposed in Section VII. Next, stagger-tuning, a technique common in distributed amplifiers, is used in Section VIII to *compensate* the peaked response of the proposed series-peaking technique in the design of a single-stage UWB LNA [9]. Measured results of the LNA follow in Section IX. Conclusions are given

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The authors are with the Department of Electrical Engineering, University of Washington, Seattle, WA 98195 USA (e-mail: shekhar@ee.washington.edu; noyade@ee.washington.edu; allstot@ee.washington.edu).

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[1] k_C can be greater than 0.5 in some applications such as when a large photodiode junction capacitance (C_1) is followed by a smaller capacitive load (C_2) looking into the transimpedance amplifier (TIA) of Fig. 1(b).

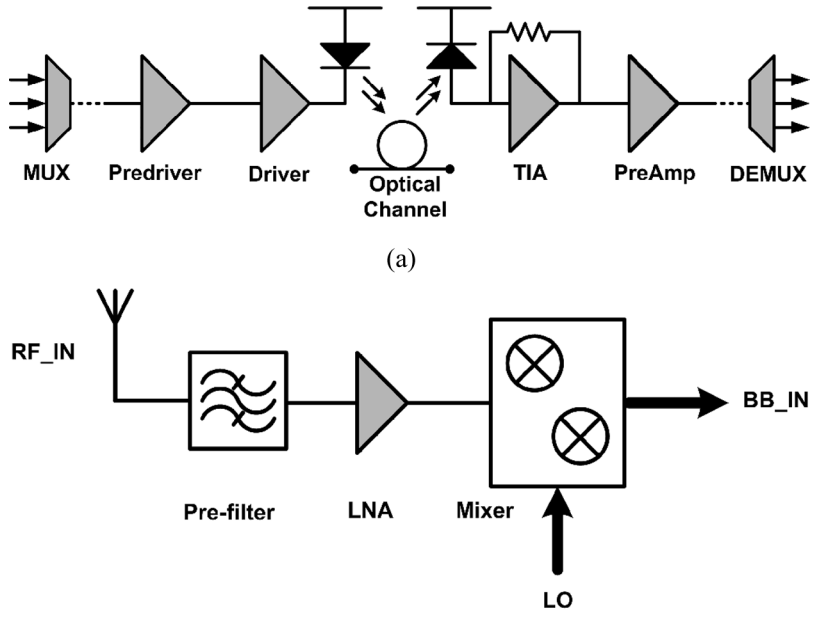

Fig. 1. (a) A typical optical communication transceiver [3]. (b) One implementation of a UWB receiver front-end [5].

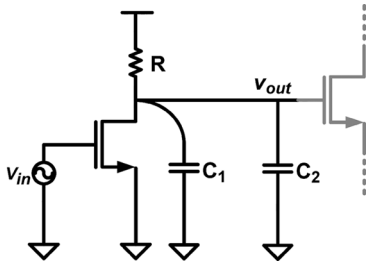

Fig. 2. A common-source amplifier.

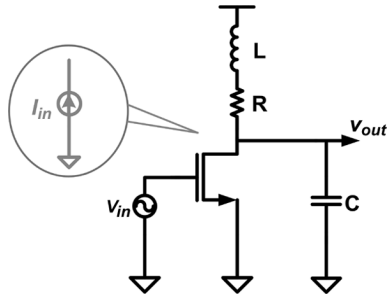

Fig. 3. A common-source amplifier with shunt peaking.

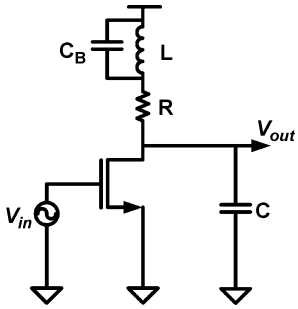

Fig. 4. A common-source amplifier with bridged-shunt peaking.

in Section X, and the design flow of asymmetric T-coils is highlighted in the Appendix.

II. Bridged-Shunt Peaking

Shunt peaking is a bandwidth extension technique in which an inductor L connected in series with the load resistor R shunts the output capacitor $C = (C_1 + C_2)$ (Fig. 3) [6], [7]. Treating the transistor as a small-signal dependent current source, $I_{\rm in} = g_m V_{\rm in}$, the gain is simply the product of the transimpedance $Z(s)$ and the transconductance g_m. As g_m is approximately constant, only transimpedance is considered hereafter. For the shunt-peaked network:

$$Z(s) = \frac{V_{\rm out}}{I_{\rm in}} = \left(\frac{1}{sC}\right) \| (R{+}sL) = \frac{R + sL}{1 + sRC + s^2LC}. \quad (1)$$

The inductor introduces a zero in $Z(s)$ that increases the impedance with frequency, compensates the decreasing impedance of C, and thus extends the -3 dB bandwidth. An equivalent explanation for increased bandwidth is reduced rise-time. That is, the inductor delays current flow to the resistive branch so that more current initially charges C which reduces risetime [7].

Substituting the -3 dB bandwidth of the reference common-source amplifier, $\omega_0 = 1/RC$, and the variable $m = R^2C/L$ into (1) and normalizing to the impedance at DC (R) gives

$$Z_N(s) = \frac{1 + s/m\omega_0}{1 + s/\omega_0 + s^2/m\omega_0^2}. \quad (2)$$

For shunt peaking, $m = \sqrt{2}$ gives the maximum *BWER* of 1.84 [6], [7], [10]. This extension comes with 1.5 dB of peaking. A maximally flat gain is achieved for $m = 1 + \sqrt{2}$ but *BWER* is reduced to 1.72.

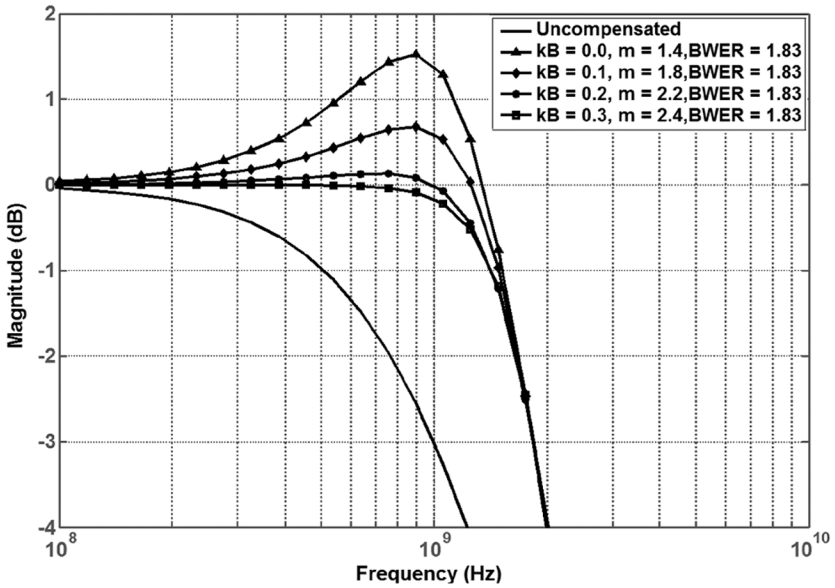

Fig. 5. Ideal bandwidth improvement with bridged-shunt peaking versus $k_B = C_B/C$.

Although the increased impedance of the inductor accounts for the bandwidth improvement, it also leads to peaking in the response. Hence, techniques to eliminate peaking with maximum *BWER* are desired. One remedy is to add in shunt with the inductor a capacitor that should be large enough to negate peaking but small enough to not significantly alter the gain response. A common-source amplifier incorporating such a *bridged-shunt* network [11], [12] is shown in Fig. 4 where

$$Z_N(s) = \frac{1 + \left(\frac{1}{m}\right)\frac{s}{\omega_0} + \left(\frac{k_B}{m}\right)\frac{s^2}{\omega_0^2}}{1 + \frac{s}{\omega_0} + \left(\frac{k_B+1}{m}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_B}{m}\right)\frac{s^3}{\omega_0^3}} \quad (3)$$

and $k_B = C_B/C$, $\omega_0 = 1/RC$, and $m = R^2C/L$. Compared to (2), C_B introduces another pole and zero in $Z_N(s)$. For $k_B = 0.3$, a *BWER* of 1.83 is achieved with a flat gain response, in contrast to the shunt-peaked design with a nearly identical *BWER* of 1.84 but 1.5 dB of peaking. Fig. 5 shows magnitude responses for the bridged-shunt-peaked circuit for several practical values of k_B along with the shunt-peaked ($k_B = 0$) and uncompensated (Fig. 2) cases. A subtle advantage of bridged-shunt peaking over shunt peaking is that the maximum bandwidth is achieved for a larger value of m, which translates to a smaller inductance with smaller die area, higher self-resonant frequency, etc.

An inductor implemented in silicon has significant shunt parasitic capacitances. By connecting L to the supply (Fig. 4), its parasitic contributes to C_B (note: there are no pure shunt-peaked designs in silicon because in practice $k_B > 0$). In a differential implementation, it also enables the use of symmetrical inductors to save area. On the other hand, connecting L to the drain adds a parasitic to C and reduces the bandwidth.

III. Bridged-Shunt-Series Peaking

In designs where the drain parasitic C_1 (Fig. 2) is significant, better *BWER* is achieved using *capacitive splitting*—an inductor is inserted to separate the total load capacitance into two constituent components. To understand this effect, consider the *series-peaked* amplifier (Fig. 6) whose normalized transimpedance with $k_C = C_1/C$ is

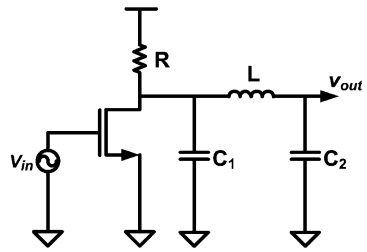

Fig. 6. A common-source amplifier with series peaking and drain parasitic capacitance.

TABLE I
Series Peaking Summary

$k_C=C_1/C$	Ripple (dB)	$m=R^2C/L$	*BWER*
0	0	2	1.41
0.1	0	1.8	1.58
0.2	0	1.8	1.87
0.3	0	2.4	2.52
0.4	1	1.9	2.75
	2	2.5	3.17
0.5	3.3	1.5	2.65

$$Z_N(s) = \frac{1}{1 + \frac{s}{\omega_0} + \left(\frac{1-k_C}{m}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_C(1-k_C)}{m}\right)\frac{s^3}{\omega_0^3}}. \quad (4)$$

As expected, the separation of C_1 from C creates another pole, which affects *BWER* versus k_C as shown in Table I. As the parasitic capacitance ratio k_C increases, *BWER* increases to a maximum of 2.52 for $k_C = 0.3$. If the passband peaking that occurs for higher values of k_C is acceptable, an even larger *BWER* is

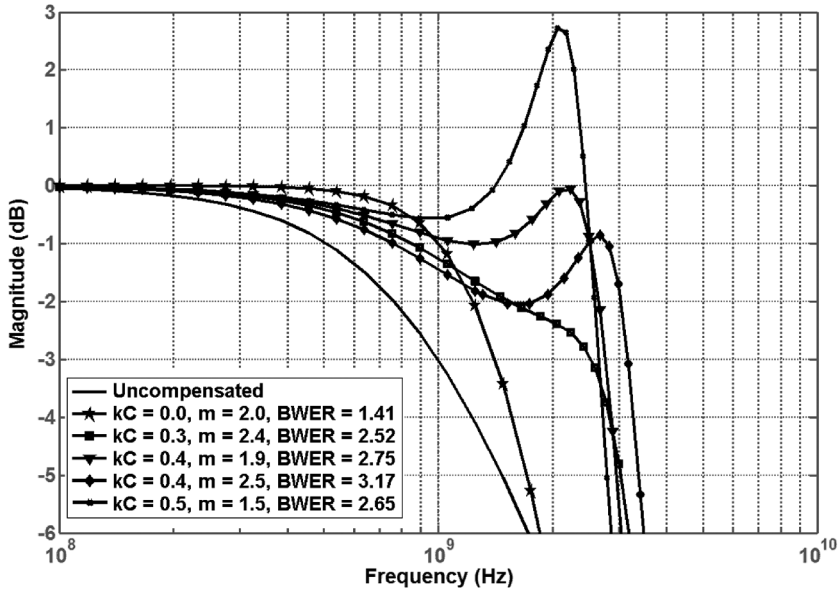

Fig. 7. Ideal bandwidth improvement with series peaking versus $k_C = C_1/C$.

achievable. Fig. 7 shows −3 dB bandwidth improvements for practical k_C values. Series-peaked designs with $C_1 = C_2$ (i.e., $k_C = 0.5$) have been reported [13], [14].

Additional insight into the increased bandwidth achieved by capacitive splitting is gained by considering the step response of the amplifier. Without L, the transistor charges $C = C_1 + C_2$, but with L only C_1 is charged initially because L delays current flow to the rest of the network. This reduces risetime at the drain and increases bandwidth [7].

Combining capacitive splitting of the series-peaked circuit and inductive peaking of the bridged-shunt approach results in the *bridged-shunt-series-peaked* network of Fig. 8. It uses two inductors but provides larger *BWER* values than its shunt-series-peaked counterpart.

Substituting $m_1 = R^2C/L_1$, $m_2 = R^2C/L_2$, and k_B, k_C, and ω_0, as defined before, the normalized transimpedance function of the bridged-shunt-series-peaked network is as shown in (5) at the bottom of the page. Table II shows results for a range of k_C and passband ripple values; for $k_C = 0.4$, a *BWER* of 4 is possible. Fig. 9 shows bandwidth improvements for several values of k_C. A response with no gain-peaking is achieved for $m_1 = 8$ and $m_2 = 2.4$, which affords pole–zero cancellation. However, such cancellations require precise component values that are difficult to realize due to distributed parasitic effects and process, voltage, and temperature (PVT) variations. Note that the shunt-series design reported by Galal *et al.* [3] that gives

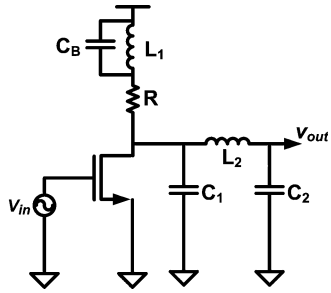

Fig. 8. A common-source amplifier with bridged-shunt-series peaking and drain parasitic capacitance.

TABLE II
BRIDGED-SHUNT-SERIES PEAKING SUMMARY

$k_C=C_1/C$	Ripple (dB)	$m_1=R^2C/L_1$	$m_2=R^2C/L_2$	$k_B=C_B/C$	*BWER*
0.4	0	8	2.4	0.3	3.92
	2	6	2.4	0.2	4
0.5	2	6	2	0.2	3.53

an ideal *BWER* of 3.5 with 1.8 dB peaking is a special case of bridged-shunt-series peaking with $k_C = 0.5$ and $k_B \sim 0$; it is sub-optimum in applications where the load capacitance is large ($k_C < 0.5$) [2]. In contrast, C_B in a bridged-shunt-series-peaked design adds a degree of freedom to control a zero that mitigates the effects of parasitics and leads to a larger *BWER*.

$$Z_N(s) = \frac{1+\left(\frac{1}{m_1}\right)\frac{s}{\omega_0}+\left(\frac{k_B}{m_1}\right)\frac{s^2}{\omega_0^2}}{1+\frac{s}{\omega_0}+\left(\frac{1+k_B}{m_1}+\frac{1-k_C}{m_2}\right)\frac{s^2}{\omega_0^2}+\left(\frac{k_B}{m_1}+\frac{k_C(1-k_C)}{m_2}\right)\frac{s^3}{\omega_0^3}+\left(\frac{(k_C+k_B)(1-k_C)}{m_1m_2}\right)\frac{s^4}{\omega_0^4}+\left(\frac{k_Bk_C(1-k_C)}{m_1m_2}\right)\frac{s^5}{\omega_0^5}} \quad (5)$$

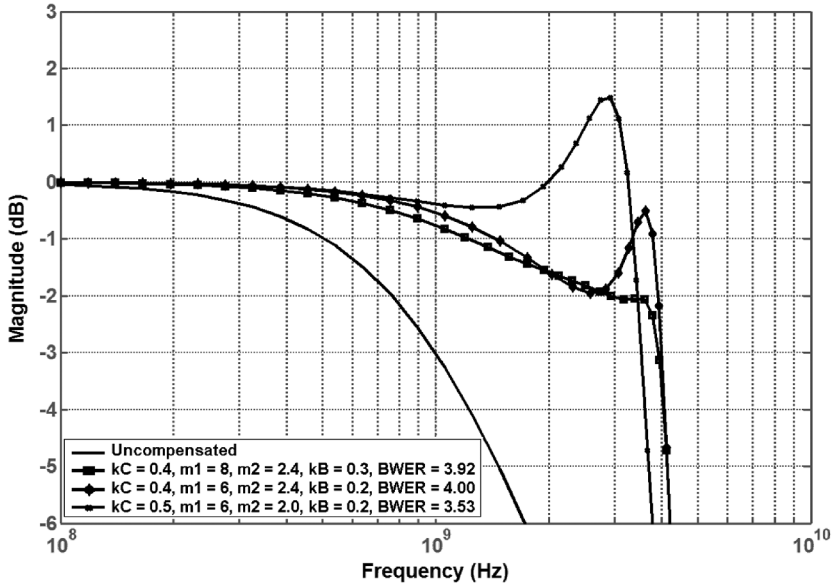

Fig. 9. Ideal bandwidth improvements with bridged-shunt-series peaking versus $k_C = C_1/C$.

For $k_C = 0.4$, for example, a simple shunt-series-peaked design gives *BWER* values of 3.51 and 3.78 for 0 dB and 2 dB peaking, respectively, which is inferior to the bridged-shunt-series design exemplified in Table II.

IV. Asymmetric T-Coil Peaking

Bridged-shunt-series peaking gives a large *BWER* for $k_C > 0.3$. However, as the load capacitance increases ($k_C \leq 0.3$), the capacitive-splitting action of L_2 and the bridging action of C_B become ineffective in achieving a large *BWER*. To overcome this drawback, the magnetic coupling action of a transformer is used. In an asymmetric ($L_1 \neq L_2$) T-coil-peaked amplifier [12] [Fig. 10(a)], the coils are wound to achieve a negative mutual inductance. As in bridged-shunt-series peaking, the secondary inductor L_2 facilitates capacitive splitting so that the initial charging current flows only to C_1. Next, the current begins to flow in L_2, which causes a proportional amount of current to flow to C_2. The negative magnetic coupling allows for an initial boost in the current flow to the load capacitance C_2, because the capacitor is effectively connected in series with the negative mutual inductance $(-M)$ element of the T-coil. This allows for an improvement in rise time and thus *BWER*. In Fig. 10(b), the equivalent small-signal network incorporates a T-model of the transformer. The coupling constant k_m is related to the mutual inductance M as $k_m = M/\sqrt{L_1 L_2}$. Substituting ω_0, m_1, m_2, k_m, and k_C, the normalized transimpedance is as shown in (6) at the bottom of the page. Table III shows the improvement in bandwidth versus k_C and passband ripple. Although the non-peaked cases show large *BWER*, the required pole–zero cancellation is again difficult to implement for the reasons mentioned earlier. For 2 dB peaking, a *BWER* of 5.59 is obtained

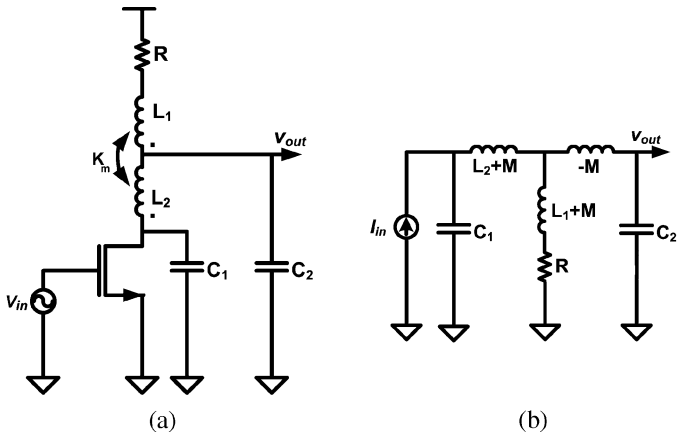

Fig. 10. (a) A common-source amplifier with asymmetric T-coil peaking and drain parasitic capacitance, and (b) an equivalent T-coil peaking network with a T-model of the transformer.

$$Z_N(s) = \frac{1 + \left(\frac{1}{m_1} + \frac{k_m}{\sqrt{m_1 m_2}}\right)\frac{s}{\omega_0}}{1 + \frac{s}{\omega_0} + \left(\frac{1}{m_1} + \frac{k_C}{m_2} + \frac{2k_C k_m}{\sqrt{m_1 m_2}}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_C(1-k_C)}{m_2}\right)\frac{s^3}{\omega_0^3} + \left(\frac{k_C(1-k_C)\left(1-k_m^2\right)}{m_1 m_2}\right)\frac{s^4}{\omega_0^4}} \tag{6}$$

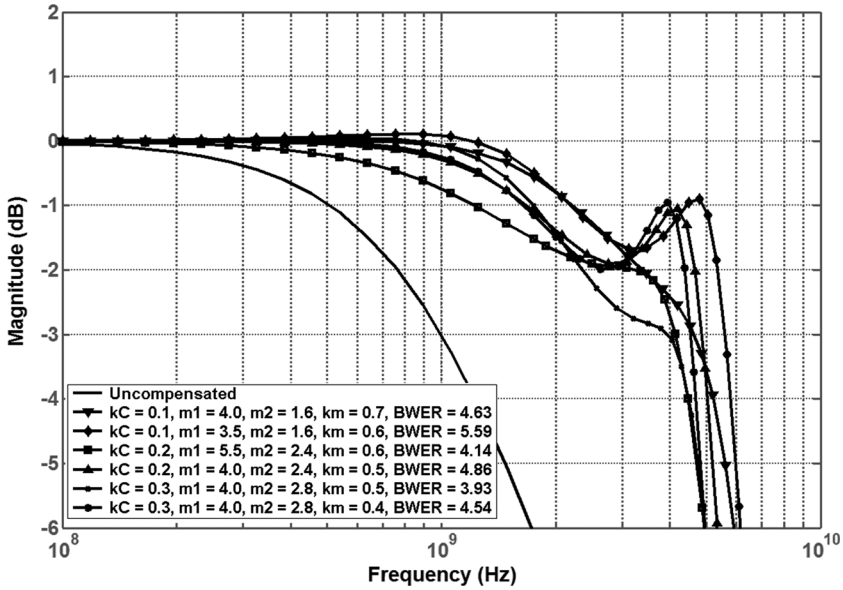

Fig. 11. Ideal bandwidth improvements with asymmetric T-coil peaking versus $k_C = C_1/C$.

TABLE III
ASYMMETRIC T-COIL PEAKING SUMMARY

$k_C=C_1/C$	Ripple (dB)	$m_1=R^2C/L_1$	$m_2=R^2C/L_2$	$k_m = M/\sqrt{L_1L_2}$	*BWER*
0.1	0	4	1.6	-0.7	4.63
	1	3.5	1.2	-0.6	4.92
	2	3.5	1.6	-0.6	5.59
0.2	0	5.5	2.4	-0.6	4.14
	1	3	2	-0.6	4.51
	2	4	2.4	-0.5	4.86
0.3	0	4	2.8	-0.5	3.93
	1	3.5	2	-0.4	3.98
	2	4	2.8	-0.4	4.54

for $k_C = 0.1$. Fig. 11 plots bandwidth improvements for various values of k_C.

Employing an asymmetric T-coil and properly utilizing the drain capacitance (C_1) leads to pole–zero locations that are optimized for a larger *BWER*—much larger, in fact, than with the classical bridged T-coil network with $L_1 = L_2$. The latter cancels a pole-pair with a zero-pair [7] by using a symmetric T-coil and neglecting the drain capacitance, but a *BWER* of only 2.83 is achieved. For an asymmetric T-coil, positive magnetic coupling [1] is suboptimal. It provides a *BWER* of only 3.23 because it does not fully exploit the magnetic coupling action of the transformer to improve rise time.

V. DESIGN OF HIGH-SPEED WIDEBAND DIFFERENTIAL AMPLIFIERS

A. High-Gain High-Bandwidth Design

In conventional single-stage wideband amplifier design, a tradeoff is made between bandwidth and gain due to the *fixed* gain–bandwidth (GBW) product. However, for fine-line CMOS technologies, the GBW product actually decreases with increased gain because of higher order parasitic effects [15]—mostly because g_{ds} becomes increasingly significant as the transistor W/L is increased. Thus, a compromise is made by designing each stage for relatively low gain and wide bandwidth, and then cascading several stages to provide the desired overall gain. This approach suffers bandwidth shrinkage with increased die area and power consumption.

The techniques presented herein provide large *BWER* in a single stage and span a wide range of k_C values. Hence, they provide leeway to sacrifice some bandwidth to increase the gain per stage so that the overall gain and bandwidth goals are met in the minimum number of stages.

To demonstrate this concept, three single-stage amplifiers with different k_C values are designed for gains greater than 12 dB and bandwidths of about 10 GHz. Two bridged-shunt-series amplifiers [Fig. 12(a)] with $k_C = 0.4$ and 0.5, and one asymmetric T-coil amplifier [Fig. 12(b)] with $k_C = 0.3$ are designed, along with an uncompensated reference amplifier for comparison. The bridged-shunt-series amplifiers utilize standard library inductor values whereas the asymmetric T-coil amplifier requires the design of a custom T-coil. After choosing the inductor values using the results given earlier, the initial amplifier designs are optimized to maximize bandwidth, gain and gain-flatness; it is observed that the higher order parasitics of the coils and the g_{ds} and C_{gd} of the transistors substantially affect pole–zero placements, and thus the component values for optimal performance. To insure first-pass success, parasitic-aware optimization [16] is performed to determine the final component values. Like the GBW product, it is observed that *BWER* also depends on the gain of the amplifier; i.e., as gain is increased, the effect of g_{ds} and C_{gd} increases and *BWER* decreases from its theoretical value. If the gain is decreased, *BWER* approaches, but never reaches, the ideal value.[2] So, the two bridged-shunt-series amplifiers designed for 14 dB gain, exhibit a larger deviation from the calculated (4, 3.5) to

[2]Similarly, the deviation from the theoretical component values is small for amplifiers with smaller gain (smaller W/L transistors). For amplifiers with large gain, the higher order effects significantly change the inductor values and a parasitic-aware optimization is employed for a robust design.

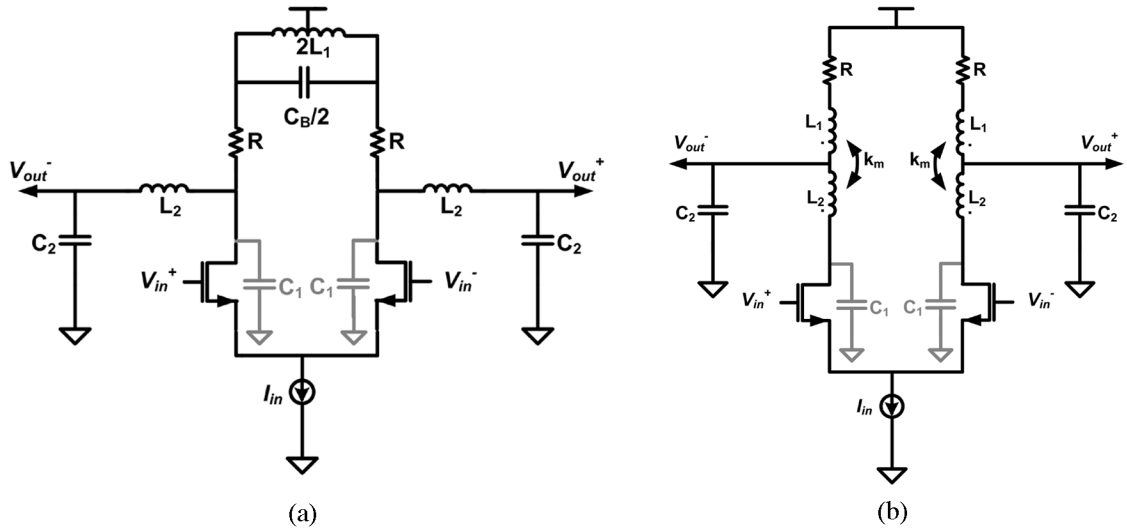

Fig. 12. (a) A bridged-shunt-series peaked amplifier, and (b) an asymmetric T-coil peaked amplifier.

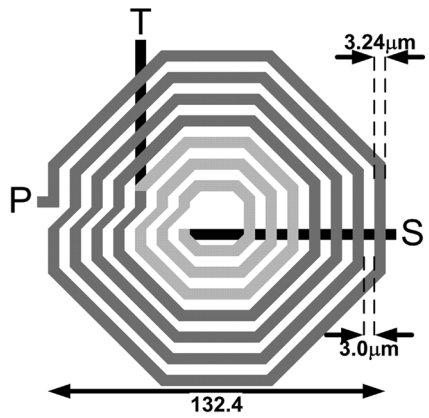

Fig. 13. T-coil winding structure used in the asymmetric T-coil peaked amplifier.

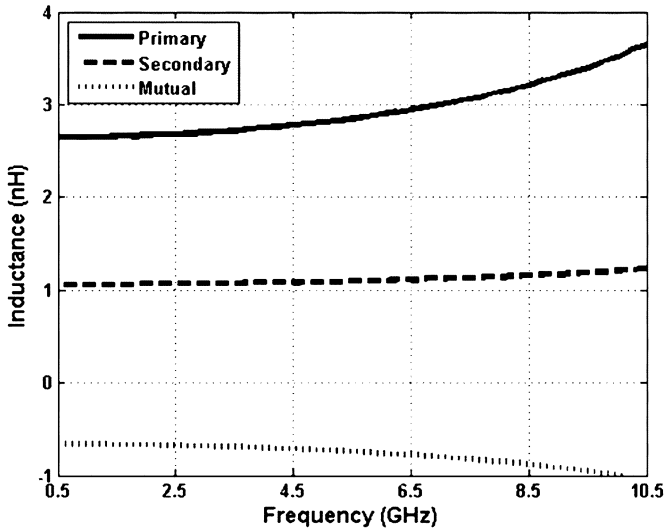

Fig. 14. Electromagnetic simulation results for the T-coil design.

simulated *BWER* values (3.3, 3.2) than the asymmetric T-coil amplifier, which is designed for a smaller gain of 12 dB. It has simulated and calculated *BWER* values of 4.2 and 4.6, respectively. Nevertheless, the single-stage amplifiers of Fig. 12 achieve the largest combined gain and *BWER* values reported to date, and the total current consumption in each differential amplifier is only 15 mA.

B. Design of Asymmetric T-Coils

Designing the asymmetric T-coil involves several factors. Most notably, the required magnetic coupling ratio k_m is relatively low, in the range of 0.3–0.7, which typically excludes interleaved T-coil structures [17]. Furthermore, the complexity associated with the design of a symmetric coil is avoided owing to the required non-unity turns ratio. Finally, structures that minimize parasitic effects between windings are desirable. For these reasons, the asymmetric concentric winding structure or tapped inductor depicted in Fig. 13 is chosen [18].

The T-coil used in the asymmetric T-coil-peaked amplifier is designed using the procedure outlined in the Appendix. It consists of four windings of the primary and three windings of the secondary, with 3.24 μm trace width and 3 μm spacing. Fig. 14 shows the simulated winding inductances. To facilitate accurate simulations, a wideband compact circuit model is implemented (Fig. 15) which incorporates elements that estimate bulk eddy current losses as well as skin and proximity effects [19]. The T-coil has a simulated self-resonance frequency of 19.2 GHz and a Q of 9.

VI. Measurement Results of High-Speed Wideband Differential Amplifiers

A typical application of these circuits does not include driving a real impedance load, so they are not designed to drive such loads. This creates a dilemma in measurements as standard high-frequency equipment typically has a real port impedance of 50 Ω, which leaves limited options for making measurements.

Although input matching is easily achieved by connecting a 50-Ω resistor in shunt with the input at the expense of noise

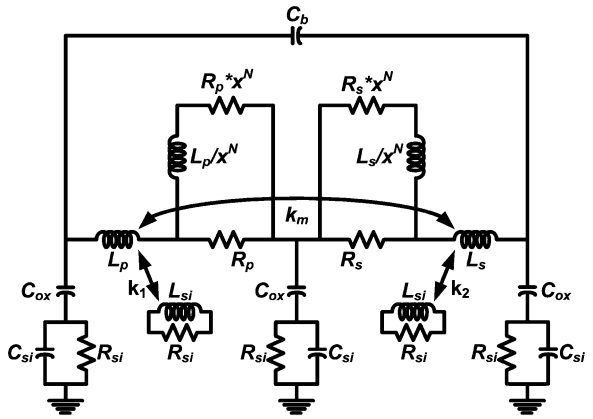

Fig. 15. Wideband compact circuit model for the asymmetric T-coil.

performance, this matching option is not viable at the output due to its negative impact on gain. Buffering the amplifiers using matched unity-gain amplifiers is another option. However, the design of the buffer is challenging, as it must have frequency performance similar to that of the wideband amplifier under test. Finally, the use of passive matching techniques is difficult owing to the relatively poor quality on-chip passives that contribute loss and thermal noise.

Another choice is to design the amplifier without matching networks, and use familiar measurement techniques to obtain its S-parameters, which are then used to calculate gain through simple manipulations. The S-parameter matrix obtained from measurement is transformed to a mixed-mode S-parameter matrix that gives parameters for both differential- and common-mode performance [20]:

$$\begin{bmatrix} S_{\rm DD} & S_{DC} \\ S_{CD} & S_{CC} \end{bmatrix} = \begin{bmatrix} S_{DD11} & S_{DD12} & S_{DC11} & S_{DC12} \\ S_{DD21} & S_{DD22} & S_{DC21} & S_{DC22} \\ S_{CD11} & S_{CD12} & S_{CC11} & S_{CC12} \\ S_{CD21} & S_{CD22} & S_{CC21} & S_{CC22} \end{bmatrix} \tag{7}$$

To determine the differential-mode voltage gain, the upper left quadrant S-parameter sub-matrix is converted into a Z-parameter sub-matrix using a reference impedance of 50 Ω [21]. The voltage gain is then simply the ratio of Z_{DD21} to Z_{DD11}.

The bridged-shunt-series and asymmetric T-coil amplifiers along with the unpeaked reference amplifier are designed and fabricated in a six-metal 0.18-μm CMOS process with a top metal thickness of 2 μm. The chip microphotographs are shown in Fig. 16. The circuits are measured using a Cascade probe station and an Agilent PNA network analyzer. The differential circuits draw 15 mA from a 2-V supply. The bridged-shunt-series amplifiers show 14.1 dB gain and 8 GHz bandwidth, and the asymmetric T-coil design gives 12 dB gain with 10.4 GHz bandwidth. Fig. 17 shows measured frequency responses of the peaked amplifiers relative to the reference amplifier. The measured *BWER* factors achieved from the bridged-shunt-series and asymmetric T-coil amplifiers are 3.0 and 4.1, respectively; the asymmetric T-coil design yields the largest measured *BWER* reported so far for a low-pass peaking response. A comparison of bandwidth extension results is presented in Table IV.

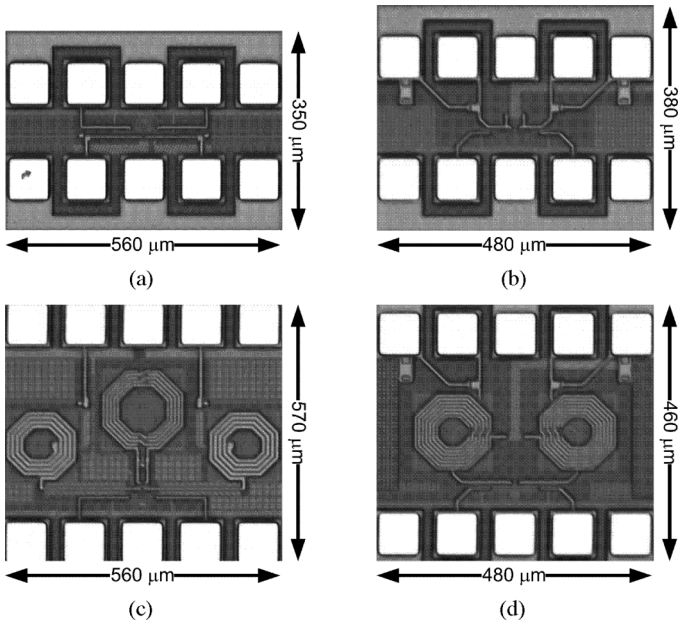

Fig. 16. Chip microphotographs of (a) reference amplifier with $k_C = 0.4$, (b) reference amplifier with $k_C = 0.3$, (c) bridged-shunt-series peaked amplifier with $k_C = 0.4$, and (d) asymmetric T-coil peaked amplifier with $k_C = 0.3$. [The $k_C = 0.5$ case is not shown but the amplifier design is similar to (c)].

VII. Series Peaking Technique For Low k_C Values

The peaking techniques described above use passive filter networks to shape the gain response above the original −3 dB frequency. However, if the network is designed to introduce a larger peaking above the −3 dB frequency, and this peaking is then compensated, a larger *BWER* is achievable.

In the conventional series-peaked network of Fig. 6, the load resistor shunts the drain node. Rewriting (4) with $R \equiv R_L$, its transimpedance is

$$Z(s) = \frac{V_{\rm out}}{I_{\rm in}} = \frac{R_L}{1 + sR_LC + s^2L_1C_2 + s^3L_1C_2R_LC_1}. \tag{8}$$

In the proposed modified version (Fig. 18) where R_L shunts $V_{\rm out}$, $Z(s)$ is

$$Z(s) = \frac{V_{\rm out}}{I_{\rm in}} = \frac{R_L}{1 + sR_LC + s^2L_1C_1 + s^3L_1C_2R_LC_1}. \tag{9}$$

Equation (9) for $Z(s)$ is similar to that of conventional series peaking (8) except that by moving the position of the load impedance, the third denominator term now contains C_1 instead of C_2. In the earlier sections, we described techniques that give larger *BWER* values for $0.2 < k_C < 0.5$. The peaking technique of (9) is proposed for $k_C < 0.1$; i.e., $C_1 \ll C_2$ where $Z_N(\omega)$ is

$$\begin{aligned} Z_N(\omega) &= \frac{Z(\omega)}{R_L} \\ &\approx \frac{1}{(1-\omega^2L_1C_1) + j\omega R_L(C_1 + C_2 - \omega^2L_1C_1C_2)} \\ &\approx \left.\frac{1}{(1-\omega^2L_1C_1)(1+j\omega R_LC_2)}\right|_{C_1+C_2\approx C_2}. \end{aligned} \tag{10}$$

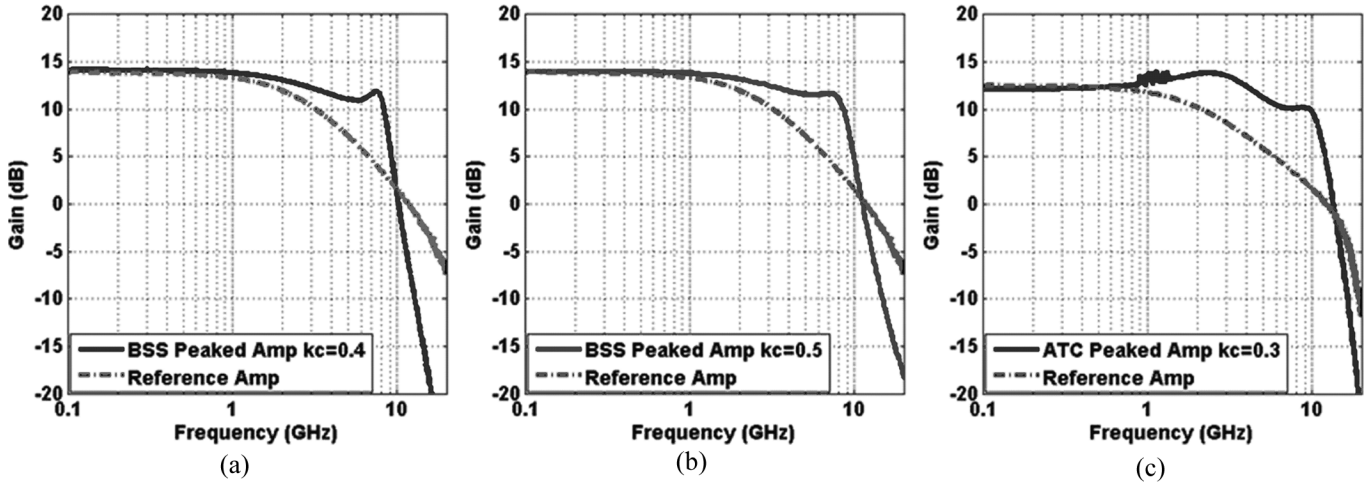

Fig. 17. Measured frequency responses. (a) Bridged-shunt-series (BSS) peaked amplifier with $k_C = 0.4$. (b) Bridged-shunt-series (BSS) peaked amplifier with $k_C = 0.5$. (c) Asymmetric T-coil (ATC) peaked amplifier with $k_C = 0.3$.

TABLE IV
COMPARISON OF BANDWIDTH EXTENSION TECHNIQUES

Reference	Bandwidth Extension Technique	CMOS Tech. (nm)	Single-stage		Multi-stage			
			Peaking (dB)	Single-stage BWER (Theory/Measured)	# Stages	Total Vol. Gain (dB)	Total Power (mW)	Total BW (GHz)
This work	Bridged-Shunt-Series	180	0.7	4.0/3.0	1	14.1	30	8
This work	Bridged-Shunt-Series	180	0.3	3.5/3.0	1	14.1	30	8
This work	Asymmetric T-coil with Negative Mutual Inductance	180	1.5	4.6/4.1	1	12.1	30	10.4
[3]	Shunt-Series	180	1.8	3.5/NA	5	15/20.3*	190	22
[1]	Asymmetric T-coil with Positive Mutual Inductance	130	0	3.23*/NA	-	-	-	42
[2]	Shunt-Series	90	2.4	2/NA	2	-	21.6	20
[13]	Series Peaking	180	1.84-3	2.46/NA	3	56dBΩ	137.5 (single-ended)	9.2

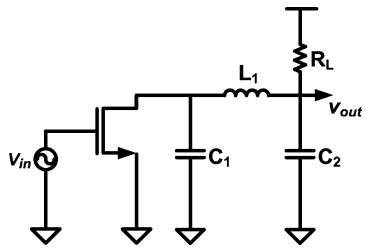

Fig. 18. Proposed series peaking technique with $k_C < 0.1$.

For $\omega_0 \approx 1/R_L C_2$, $\omega_1 = 1/\sqrt{L_1 C_1}$, and with $\omega_0 < \omega_1$, the gain response is shown in Fig. 19. At low frequencies, gain is constant where the normalized transimpedance is unity. As frequency is increased, the pole created by C_2 that sets ω_0 causes the amplitude to roll off. As the frequency approaches ω_1, the impedance of L_1 rises and the overall gain increases. At ω_1, the ideal inductor $L_1(Q_L = \infty)$ resonates with C_1 and gives a sharp peak. Beyond ω_1 the network is capacitive and a steep roll-off in gain is observed.

By modifying L_1, the peak frequency ω_1 is moved relative to ω_0 for a given load (R_L) and k_C (<0.1). Two possibilities exist to decrease the peaking in the gain response: 1) the overall quality factor Q of the network is decreased, and 2) the input current source itself is designed for a gain response with an inverse relationship to the transimpedance of the network. The second method is inspired by pre-emphasis techniques that are used in wireline transceivers for equalization; the technique described above, however, more resembles de-emphasis. Both techniques are combined in this work to shape the bandpass response of a UWB LNA.

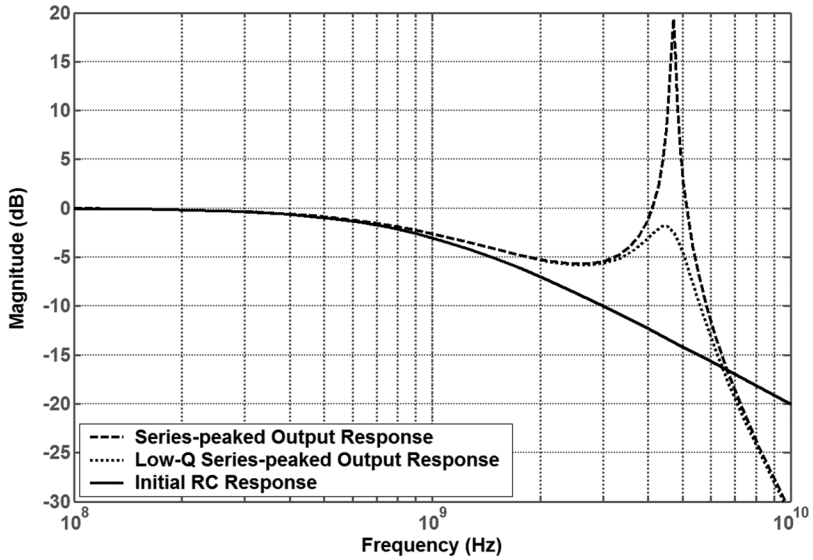

Fig. 19. Simulated normalized responses of proposed series peaking with L_1 ideal, and L_1 including typical parasitic affects in a CMOS implementation (π-model).

VIII. Stagger-Compensated Series Peaking for a UWB LNA

A. Low-Q Series-Peaked Network

Utilizing a low-Q monolithic inductor for L_1 decreases the overall Q of the network (Fig. 18), which reduces peaking and broadens the magnitude response. Fig. 19 also shows an example of the response when the ideal inductor $L_1(Q_L = \infty)$ is replaced with its parasitic-laden π-model $(Q \sim 5)$. In the final implementations, a small series resistor $(r \approx 10\,\Omega)$ is added to L_1 to further reduce its Q.

B. Stagger-Compensation in a Common-Gate UWB LNA

When several narrowband amplifiers with different resonant frequencies are cascaded, the resulting multi-stage amplifier can have an overall response that is broadband with adequate gain flatness. This is the stagger-tuning technique that has been used extensively in distributed amplifiers [22], [23]. Simulation results have been reported for a two-stage common-source-based UWB LNA that also employed stagger-tuning [24]. Here, an approach is presented wherein stagger-tuning within a *single stage* is used to flatten the overall gain response associated with the series-peaked π-network described above.

An LNA is a critical component in the front-end of a UWB receiver. It should have low return loss, low noise figure, high gain across the entire 7.5 GHz UWB band (3.1–10.6 GHz), and minimum power and die area. For narrowband amplifiers, the source-degenerated common-source LNA is currently more popular than the common-gate LNA because of superior gain and noise performance at the expense of higher power. Previous implementations of 3.1–10.6 GHz UWB amplifiers have been based on the common-source configuration [8], [24]. To obtain a wideband response, shunt peaking has been used at the load. By adopting the techniques described in Sections II–IV, a larger *BWER* is possible which allows an increase in the load resistance and larger gain.

To obtain broadband input matching, the input impedance of the amplifier should be resistive and equal to 50 Ω over the entire bandwidth. For input matching, the common-source-based UWB LNA has employed bandpass filters with multiple inductors [8], [24]. Compared to a common-source LNA, a common-gate LNA offers design simplicity, low power, good linearity, and a frequency-independent noise factor of $F = 1 + \gamma/\alpha$ (neglecting induced gate noise) where γ and α are empirical process- and bias-dependent parameters [25]. The low power consumption and negligible frequency-dependence of F suggest that a common-gate topology is amenable to broadband applications.

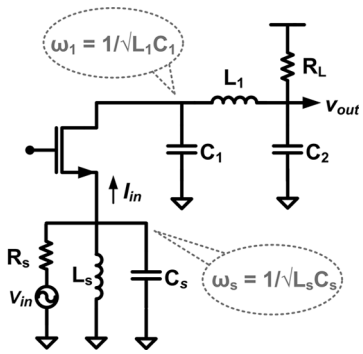

Fig. 20. Proposed series peaking in a common-gate low-noise amplifier with stagger compensation.

In a common-gate LNA, the input match condition $(g_m = 1/R_s)$ keeps the size of the transistor small so that the gate-source and gate-drain capacitances also remain small. Thus, k_C is usually smaller than 0.2. The gain of the common-gate LNA depends on the ratio of load to source impedances, R_L/R_S. As the value of R_S is fixed (50 Ω), R_L is necessarily large for high gain. Because a high R_L, together with the total load capacitance, sets a bandwidth constraint, a technique for bandwidth extension is needed which has a large *BWER* for $k_C < 0.2$. Thus, the low-Q series-peaked network is utilized at the output as shown in Fig. 20 for a broadband response.

As stated before, the input matching is achieved by making the effective input resistance $(1/g_m)$ equal to R_s (50 Ω); the

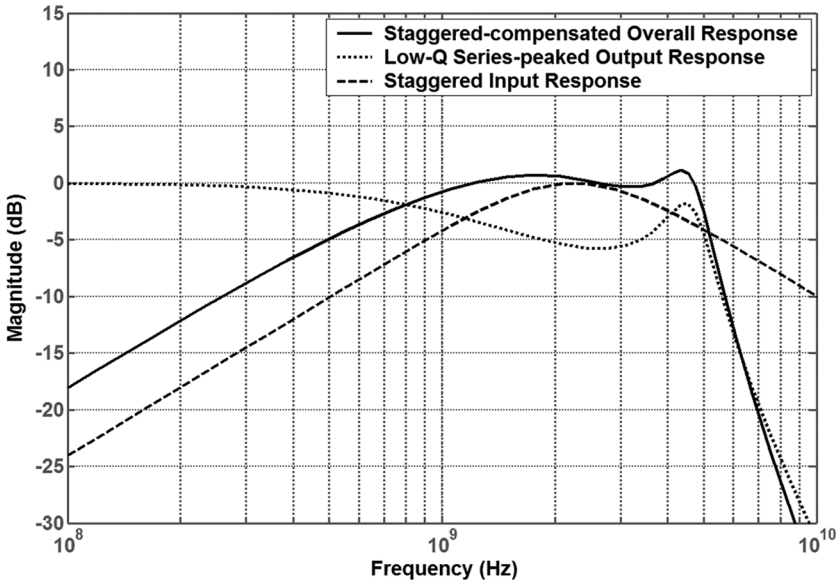

Fig. 21. Simulated normalized responses for the LNA of Fig. 20.

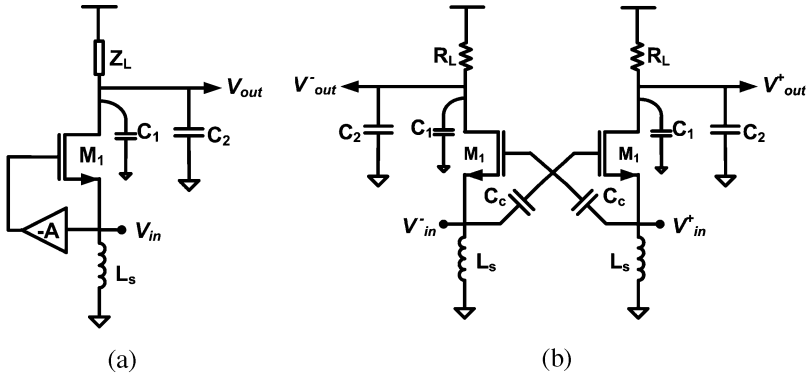

Fig. 22. (a) A general g_m-boosting common-gate LNA, and (b) its capacitor cross-coupled implementation.

total source capacitance C_s is tuned out by a source inductor L_s at the resonant frequency ω_s. L_s and C_s form a shunt parallel resonant network with $Q = \omega_s C_s R_s/2 < 1$ [25]. A low Q for the input shunt network suggests a possible broadband impedance match.

For the UWB LNA, $S_{11} < -10$ dB is needed from 3.1–10.6 GHz. By properly sizing the source inductor (L_s) and the input transistor (W/L), ω_s is optimized to meet this specification over the entire band. The requirement for a single inductor for the input match in the common-gate UWB LNA gives it an advantage over its common-source counterparts.

Because of the low-Q shunt network, the input match is best at the resonant frequency (ω_s) and degrades on either side. Note that for a tuned output load, as in a narrowband LNA, this is desirable because the gain is maximum at the desired operating frequency, and lower at other frequencies, thus giving a highly selective response. However, for a broadband response where the load is resistive, there is a significant roll-off in the transconductance gain after ω_s. We *utilize* this roll-off for canceling the peaking at ω_1 in the transimpedance gain at the output, as well as to flatten the overall gain of the amplifier. This is done through proper staggering of ω_1 and ω_s. Consider the input network of the common-gate amplifier shown in Fig. 20. It can be shown that the normalized input transconductance is

$$Y_N(s) = \frac{2s\left(\frac{L}{R_S}\right)}{1 + 2s\left(\frac{L}{R_S}\right) + \frac{s^2}{\omega_s^2}}. \tag{11}$$

Fig. 21 shows the normalized plots of transconductance response of the input network, the transimpedance response of the low-Q series-peaked output network, and the overall stagger-compensated response of the amplifier.

C. Design Considerations for a g_m-Boosted Stagger-Compensated UWB LNA

For a common-gate LNA, significant improvement in F is achieved through the use of g_m-boosting [26]. Fig. 22(a) shows a g_m-boosted common-gate LNA, where an inverting gain of A between the source and the gate terminals reduces the power

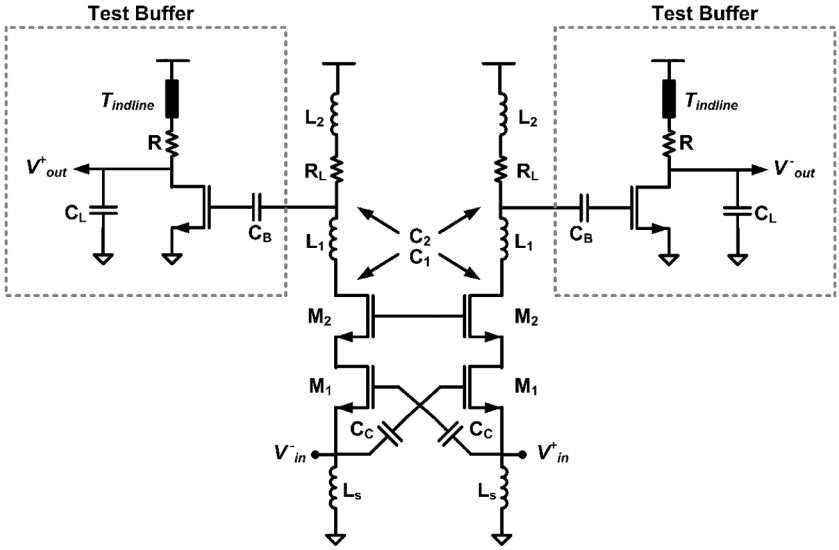

Fig. 23. A UWB LNA employing stagger-compensated series peaking (DC biasing not shown).

consumption by a factor $(1+A)$, and simultaneously improves F to

$$F = 1 + \left.\frac{\gamma}{\alpha(1+A)}\right|_{(1+A)g_m R_S=1} \approx 1 + \frac{\gamma}{2\alpha} \qquad (12)$$

for $A = 1$ and input matching condition $(1+A)g_m R_s = 2g_m R_s = 1$. An inverting gain of unity is easily realized in a differential configuration by capacitor cross-coupling the two branches [Fig. 22(b)] [27]. The inverting gain is approximately $A = C_c/(C_c + C_{gs})$, where C_c and C_{gs} are the coupling and gate-source capacitances, respectively. By making $C_c \gg C_{gs}$, $A \approx 1$, and induced gate noise is negligible.

A schematic of the g_m-boosted stagger-compensated UWB LNA is shown in Fig. 23. The input match condition sets $g_m (= 1/2R_s)$ of M_1, and linearity determines its overdrive voltage $(V_{gs} - V_{th})$. With knowledge of g_m and the overdrive voltage, W/L of M_1 is determined. Minimum channel length (0.18 μm) is chosen for all devices due to noise and f_T considerations. With the transistor size and overdrive known, the supply current and the gate capacitance are easily calculated. Next, total source capacitance C_s is determined from C_{gs} and the pad capacitance $C_{\rm pad}$. (Another advantage of a common-gate topology is that it is easy to absorb $C_{\rm pad}$ into the total source capacitance C_s). The resonant frequency of the input tank (ω_s) is chosen next, and an estimate of L_s is obtained. The desired gain dictates the value of R_L; as R_L also sets the dominant pole frequency, it cannot be arbitrarily high. A cascode transistor M_2 is added to improve reverse isolation. The size of M_2 determines the drain parasitic capacitance C_1. If the width of M_2 equals that of M_1, their source and drain nodes can be merged which reduces parasitic capacitance. This avoids the deterioration of bandwidth and noise figure. On the other hand, sizing M_2 differently from M_1 gives another degree of freedom to optimize gain and C_1. With the knowledge of C_1, R_L, and load capacitance C_2, ω_0 is determined. Next, the series-peaked network is added to the load (Fig. 23). To introduce staggering to flatten the overall gain response and achieve a large *BWER*, ω_1 is kept larger than the resonant frequency of the input-matching network $\omega_s = 1/\sqrt{L_s C_s}$. As the input match deviates from the input source impedance beyond ω_s, the effective gate-source voltage decreases so that peaking at ω_1 is suppressed and an effective compensation is achieved in a single-stage configuration.

To facilitate testing, a buffer is needed to drive the off-chip 50-Ω load. A unity-gain common-source stage is chosen for the buffer. Its initial bandwidth (about 7.5 GHz) falls short of the core LNA bandwidth, but shunt peaking using a slab inductor is sufficient to extend it. A slab inductor is used because the required inductance is small and substantial area is saved. In the actual implementation of a complete receiver front-end, this buffer is not needed. Care is taken to ensure a gain of near unity over its maximum bandwidth for accurate gain-flatness characterization of the LNA. The value of coupling capacitor C_B in Fig. 23 is also carefully chosen. A large value of C_B adds to the overall parasitic capacitance at the output node, affecting the overall bandwidth. A small value, on the other hand, has significant ac impedance that leads to reduced gain.

After choosing the component values from the above design flow, the design is then optimized to maximize bandwidth, gain, gain-flatness and input matching; a clear trade-off is observed between bandwidth and gain-flatness. S_{11} is maintained better than -13 dB over the UWB band (3.1–10.6 GHz). M_1 and M_2 are of equal sizes to trade off gain and optimal C_1 for NF and the parasitic capacitance at the drain of M_1. A small series resistor ($r \approx 10\ \Omega$, not shown in Fig. 23) is added to L_1 to trade off gain-flatness for a slight degradation in gain and NF. Finally, a shunt peaking inductor L_2 is added at the output (Fig. 23) to reduce the roll-off in the gain response between ω_s and ω_1, for which simulations show an improvement of 0.3–0.8 dB in the roll-off. This improvement is traded off against silicon area, and is expendable if area is the major concern. Finally (not implemented in this work), the use of symmetric center-tapped inductors is suggested for L_s and L_2, as well as the use of 3-D inductors for L_1 and L_2 for area savings.

In a narrowband g_m-boosted common-gate LNA [26], [27], the input and output are matched to the same resonant frequency,

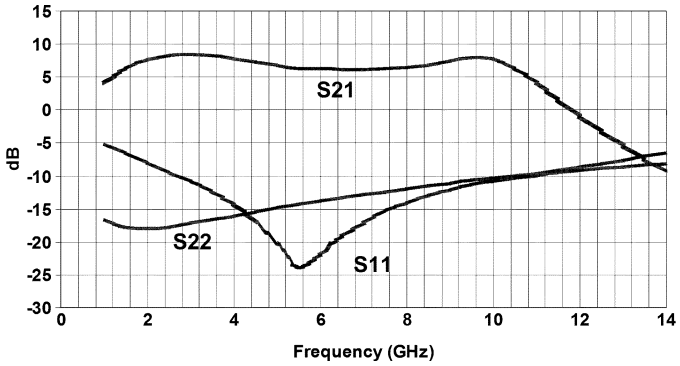

Fig. 24. Measured S-parameters of LNA #1.

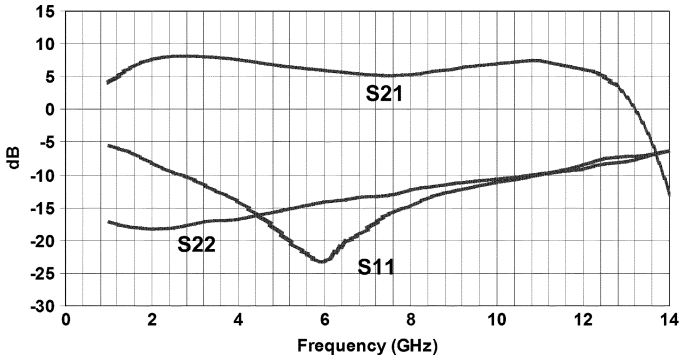

Fig. 25. Measured S-parameters of LNA #2.

and the main contribution to the overall NF comes from M_1 (Fig. 22). In the proposed UWB LNA (Fig. 23), the input and output resonances are staggered. Although (12) is valid at the resonance frequency of the input shunt network $(L_s||C_s)$ where $g_m = 1/2R_s$, the input match is kept better than -10 dB throughout the UWB band so that the in-band deviation in the NF is maintained at a low value. Although M_1 is still the dominant source of noise, the load resistor R_L, cascode device M_2, peaking inductor L_1, and its series resistance r, source-inductor L_s, and the unity-gain buffer all contribute to the overall NF.

IX. Measurement Results of UWB LNA

Two versions of the UWB LNA are fabricated in a six-metal 0.18-μm RF CMOS process. Figs. 24 and 25 show typical measured S-parameter responses. Before extension, the BW of LNA #1 as determined by simulations using layout-extracted load resistance (190 Ω) and node capacitance (320 fF) values is $f_0 = 2.62$ GHz; for LNA #2, $f_0 = 2.5$ GHz. (Experience with similar amplifiers shows agreement within 5% between such simulated and measured values.) To move the second peak (ω_1) to a higher frequency in LNA #2, L_1 is reduced and L_s and L_2 are optimized. The measured upper -3 dB BW of LNA #1 (#2) is 10.7 GHz (12.26 GHz) corresponding to a *BWER* of 4.1 (4.9). S_{21} peaks at 8.5 dB (8.2 dB) with 2.4 dB (3.0 dB) in-band gain variation; S_{11} is better than -10 dB between 2.8–10.8 GHz (2.7–11 GHz), and S_{22} is better than -10 dB up to 10.3 GHz (11 GHz).

NF performance is plotted in Fig. 26; the minimum is 4.4 dB (4.6 dB) at 6.25 GHz (6.25 GHz), the maximum is 5.3 dB

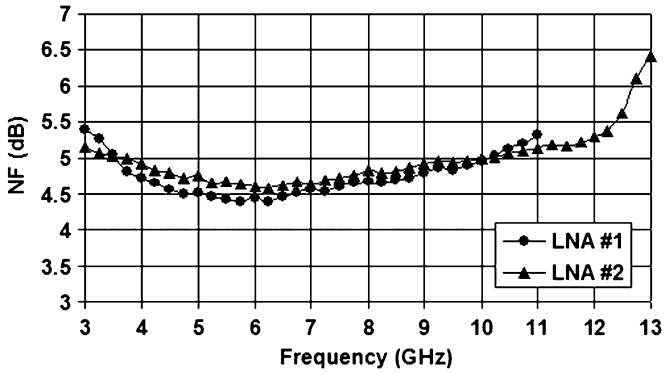

Fig. 26. Measured noise figures of the two versions of the UWB LNA.

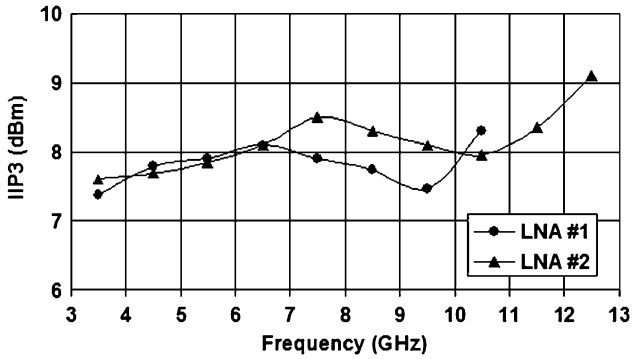

Fig. 27. Measured IIP3 of the two versions of the UWB LNA.

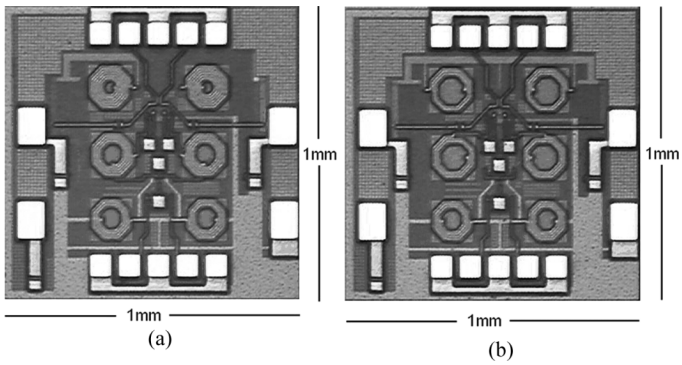

Fig. 28. Chip microphotographs. (a) LNA #1. (b) LNA #2.

(5.5 dB) at 3.1 GHz (12.25 GHz), and the average over the corresponding -3 dB BW is 4.75 dB (4.98 dB).

Fig. 27 shows the two-tone IIP3 values across the -3 dB bandwidths; the minimum and maximum values are 7.4 dBm (7.6 dBm) and 8.3 dBm (9.1 dBm), respectively. Power consumption in the differential cores is only 4.5 mW. Thus, tradeoffs among BW, gain flatness, and NF are illustrated in the two versions.

The UWB LNA using the stagger-compensated series-peaking technique achieves a measured *BWER* of 4.9. More generally, the new topology also exhibits superior figure-of-merit (FOM) performance (Table V):

$$\mathrm{FOM} = \frac{\mathrm{Gain}_{\mathrm{abs}}\mathrm{BW}_{\mathrm{GHz}}}{(F-1)P_{\mathrm{mW}}}. \tag{13}$$

TABLE V
WIDEBAND LNA PERFORMANCE COMPARISON

Reference	CMOS Tech. (nm)	-3dB BW (GHz)	Power (mW)	NF (dB)	Max. S_{21} (dB)	IIP3 (dBm)	Area (mm^2)	FOM	FOM x $IIP3_{mW}$
LNA #1	180	1.3-10.7	4.5	4.4-5.3	8.5	7.4 to 8.3	1.0	2.33-3.17	12.8-21.4
LNA #2	180	1.3-12.3	4.5	4.6-5.5	8.2	7.6 to 9.1	1.0	2.69-3.64	15.5-29.6
[8]	180	2.3-9.2	9	4.0-9.0	9.3	-8.2 to –5.6	1.1	0.32-1.48	0.05-0.41
[30]	180	0.5-14	52	3.4-5.4	10.6	9.4	1.6	0.36-0.74	3.11-6.45
[30]	180	0.6-22	52	4.3-6.1	7.3	8.7	1.35	0.31-0.56	2.3-4.18
[31]	180	0-12.6	19.8	2.9	9.6	-3.4	0.76	2.02	0.92
[32]	180	0-25	54	4.8-7.0	9.1	4.7	1.32	0.33-0.65	0.97-1.93

Note: LNA #1, LNA #2, and [31] are differential LNAs; hence, their differential power, area, and FOMs are given.

Further improvements in this design are expected though the use of aggressive optimization methods [16]. Fig. 28 shows a chip area including pads of 1 mm^2 for each version. The layouts are similar, with the main difference being the sizes of the active and passive devices.

X. CONCLUSION

CMOS implementations of the bridged-shunt-series and asymmetric T-coil-peaked amplifiers demonstrate a trade off between delay and gain flatness to achieve measured *BWER* values up to 4.1. Wide bandwidth is achieved simultaneously with high gain, which means fewer stages with concomitant power and area advantages. Another important result is that different approaches achieve maximum *BWER* for different k_C values: specifically, bridged-shunt-series is best for $0.3 > k_C > 0.5$ and the asymmetric T-coil is best for $k_C < 0.3$.

A fully integrated common-gate UWB LNA employs a stagger-compensated series-peaking technique in a single stage, applicable for $k_C < 0.1$, to extend bandwidth, and a capacitor cross-coupled g_m-boosting technique to reduce NF and power. A simple input-matching scheme obviates the use of multiple inductors and complex filters. Two versions in 0.18-μm CMOS show *BWER* factors of 4.1 and 4.9 and the highest reported FOMs.

APPENDIX

Electromagnetic simulations are necessary because accurate characterization of the inductor is critical, not only for estimation of the winding inductances, L_p (primary) and L_s (secondary), but also for estimation of k_m and associated capacitive and resistive parasitics. To decrease the relatively long simulation times associated with complex electromagnetic field solvers, a two-step design cycle is adopted to insure accurate characterization of the inductors and maintain a shorter design cycle. In the first step, the inductance is estimated using a concentric windings approximation [28], by breaking down the inductors into concentric rings. The partial self-inductances (l_{self}) and mutual-inductances (l_m) are then calculated for each loop, using standard Grover calculations [29] yielding an inductance matrix:

$$L = \begin{bmatrix} l_{11} & . & . & . & l_{1N} \\ . & l_{22} & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ l_{N1} & . & . & . & l_{NN} \end{bmatrix} \tag{14}$$

Here, N is the total number of complete windings with the diagonal elements representing l_{self} and all others representing l_m. With the knowledge of the structure (i.e., which rings belong to the secondary, which belong to the primary, etc.), summation of the elements of l_{self}, along with the elements of l_m of the primary loops, yields L_p. L_s is calculated similarly. To estimate M, the sum of the mutual inductive elements that consist of a loop of the primary to a loop of the secondary is computed:

$$L_P = \sum_{i=S+1}^{P} \sum_{j=S+1}^{P} L_{ij},\ L_S = \sum_{i=1}^{S} \sum_{j=1}^{S} L_{ij},\ M = \sum_{i=1}^{S} \sum_{j=S+1}^{P} L_{ij}. \tag{15}$$

The calculations can be made quickly based upon the physical dimensions of the spiral structure, along with quick estimates for parasitic resistive and capacitive elements. With these estimates, the second step is electromagnetic simulation albeit with fewer iterations. A comparison of these inductance values to the DC estimates in Table VI shows that errors in the inductance values at DC are less than 10%.

TABLE VI
COMPARISON OF DC INDUCTANCES FROM GROVER CALCULATIONS VERSUS ELECTROMAGNETIC SIMULATIONS

Inductance	Grover Estimation (nH)	Momentum Simulation (nH)
L_p	2.59	2.65
L_s	0.95	1.06
M	0.62	0.66

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Sudip Shekhar (S'00) received the B.Tech. degree (Hons.) in electronics and communications engineering from the Indian Institute of Technology, Kharagpur, in 2003. He received the M.S. degree in electrical engineering from the University of Washington, Seattle, in 2005, where he is currently working toward the Ph.D. degree.

In the summer of 2005 and 2006, he was an intern with Intel Corporation, Hillsboro, OR, where he worked on the modeling and design of serial links. His current research interests include RF transceivers, frequency synthesizers and mixed-signal circuits for high-speed I/O interfaces.

Mr. Shekhar is a recipient of the Intel Foundation Ph.D. Fellowship for 2006–2007.

Jeffrey S. Walling (S'03) received the B.S. degree from the University of South Florida, Tampa, in 2000, and the M.S. degree from the University of Washington, Seattle, in 2005, both in electrical engineering. He is currently working toward the Ph.D. degree at the University of Washington.

Prior to starting his graduate education, he was with Motorola, Plantation, FL, working in cellular handset development. He interned for Intel, Hillsboro, OR, in the summer of 2006, where he worked on highly digital transmitter architectures. He is currently with the University of Washington, where his research interests include high-efficiency transmitter architectures and power amplifier design.

Mr. Walling was a recipient of the Analog Devices Outstanding Student Designer Award in 2006.

David J. Allstot (S'72–M'72–SM'83–F'92) received the B.S. degree from the University of Portland, Portland, OR, the M.S. degree from Oregon State University, Corvallis, and Ph.D. degree from the University of California, Berkeley.

He has held several industrial and academic positions and has been the Boeing-Egtvedt Chair Professor of Engineering at the University of Washington, Seattle, since 1999. He is currently the Chair of Electrical Engineering. He has advised approximately 80 M.S. and Ph.D. graduates and published about 225 papers.

Dr. Allstot is a Member of Eta Kappa Nu and Sigma Xi. He has received several outstanding teaching and advising awards. Other awards include the 1978 IEEE W.R.G. Baker Prize Paper Award, 1995 IEEE Circuits and Systems Society (CAS-S) Darlington Best Paper Award, 1998 IEEE International Solid-State Circuits Conference (ISSCC) Beatrice Winner Award, 1999 IEEE CAS-S Golden Jubilee Medal, 2004 Technical Achievement Award of the IEEE CAS-S, and the 2005 Aristotle Award of the Semiconductor Research Corporation. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING from 1990 to 1993 and its Editor from 1993 to 1995. He was on the Technical Program Committee, IEEE Custom Integrated Circuits Conference, from 1990–1993, Education Award Committee, IEEE CAS-S, from 1990 to 1993, Board of Governors, IEEE CAS-S, from 1992 to 1995, Technical Program Committee, IEEE International Symposium on Low-Power Electronics and Design, from 1994 to 1997, Mac Van Valkenberg Award Committee, IEEE CAS-S, from 1994 to 1996, and Technical Program Committee, IEEE ISSCC, from 1994 to 2004. He was the 1995 Special Sessions Chair, IEEE International Symposium on CAS (ISCAS), an Executive Committee Member and the Short Course Chair, ISSCC, from 1996–2000, Co-Chair, IEEE Solid-State Circuits (SSC) and Technology Committee, from 1996 to 1998, Distinguished Lecturer, IEEE CAS-S, from 2000–2001, Distinguished Lecturer, IEEE SSC Society, from 2006–2007, and the Co-General Chair, IEEE ISCAS in 2002.