Compact Modeling and Simulation of PD-SOI MOSFETs: Current Status and Challenges

(Invited Paper)

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***Abstract*- This paper reviews the status and challenges of the modeling Partially-Depleted Silicon-On-Insulator transistors. Many challenges stem from the floating-body potential, which offers advantages in terms of performance and leakage, but presents complex electrical behavior. Circuit simulator considerations and the importance of model standardization are also highlighted.**

I. Introduction

Compact modeling, defined as numerical modeling using electrical elements to approximate semiconductor physics, is an essential part of chip design in both analog and digital applications. In this work, the compact modeling focus is on partially depleted silicon-on-insulator (PD-SOI) transistors that have been successfully manufactured in ULSI CMOS from the 225nm [1] through the 45nm nodes [2]. PD-SOI provides multiple benefits for CMOS scaling, including threshold (V_t) lowering due to the floating-body effect and reduced V_t versus L_{poly} sensitivity, reduced capacitive loading because of the buried insulator and the floating-body, reduced body effects in stack transistor circuits [3], and reduced soft-error rates [4]. The buried oxide further benefits SOI designs through the elimination of latch-up, well-implant proximity effects (WPE), and natural isolation of auxiliary device elements such as embedded DRAM, passives, high-voltage, and RF devices.

Compact models for PD-SOI transistors are necessarily more complex than bulk transistors due to the presence of the floating-body (FB). In reality, the floating-body is a complex 3D potential distribution that is influenced by many factors. In PD-SOI compact models, a single body-potential describes the electrical effects of the floating-body since local potential variations within the body charge are small compared to other non-uniformities under ordinary circumstances.

This paper is organized as follows. Section II describes general strategies for assembling a PD-SOI compact model. Section III discusses the complexities and challenges of modeling the FB potential, while section IV introduces the SOI body-contacted (BC) structure and its modeling and challenges. Section V discusses some of the simulator considerations for SOI circuit analyses. Section VI reviews current work towards standardizing compact model best practices and section VII concludes the paper.

II. Strategies for PD-SOI Compact Model Calibration

A. PD-SOI Compact Model Topology

The element topology guides the procedure for calibrating compact model parameters. Figure 1 shows a typical circuit element topology for a PD-SOI transistor. This topology follows the BSIMSOI model [5] and another similar construction is given in [6] with an excellent overview. A key feature differentiating PD-SOI from conventional bulk models is that the parasitic currents that drive charge into and out of the isolated body region must be explicitly included: gate-to-body, source and drain junction diodes, Gate Induced Drain Leakage (GIDL), and impact ionization. A simplified bipolar transistor model is used to model the source-body-drain regions (analogous to a lateral bipolar structure) to capture bipolar-driven base charge dump. A single-pole thermal sub-circuit is employed to model power dissipation out of the channel region through the buried oxide and other structures such as contact studs.

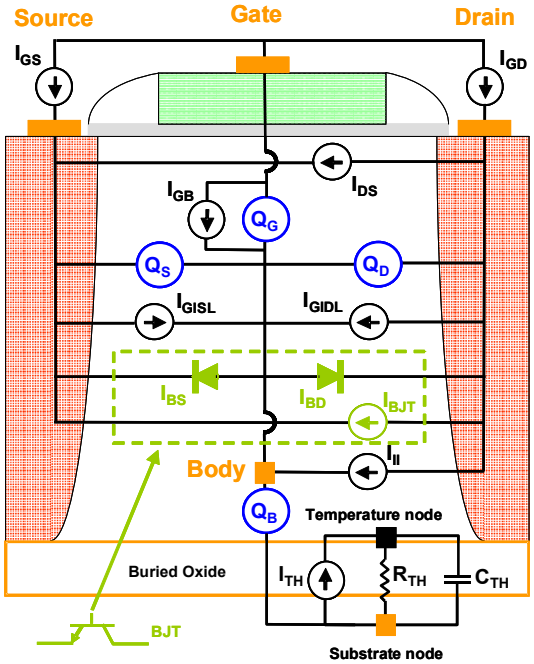

Fig. 1. PD-SOI compact model electrical element topology.

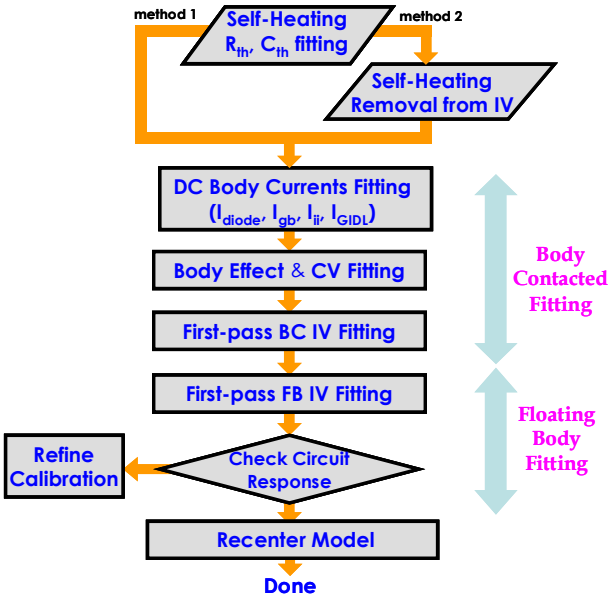

Fig. 2. Model parameter calibration flowchart for PD-SOI MOSFETs.

B. Overview of Model Calibration Process

Figure 2 summarizes the major steps used to calibrate PD-SOI model parameters. One of the unique steps in PD-SOI modeling is the treatment of self-heating that, like other parasitic effects, must be analyzed before calibrating the intrinsic MOSFET. One approach is to characterize the model thermal resistance and capacitance using MOSFET power versus temperature trends under both DC and transient conditions. Subsequent model calibration proceeds using these derived quantities (method 1 in Fig. 2). Figure 3 illustrates the DC extraction of thermal resistance.

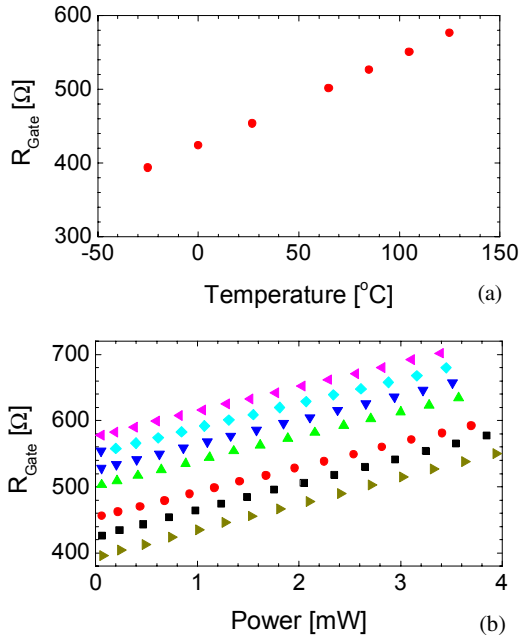

Fig. 3. (a) Calibration of temperature response of the gate resistance. (b) Measurment of the gate resistance as a function of FET power dissipation. $R_{th} = (dT/dR_g) \times (dR_g/dPower) = dT/dPower$.

Another approach (method 2) is to directly compensate the measured model I-V data for self-heating effects. This method can reduce the need to simultaneously tune temperature-dependent and temperature-independent parameters in the previous method. Hence, it is desirable to generate "self-heating free" data before parameter calibration. It should be mentioned that self-heating removal is not only implemented for the channel current but also for other parasitic currents such as the impact ionization current [7]. Figure 4 compares self-heated measurements to self-heating-free post-processed I-V curves assuming that a linear temperature interpretation is appropriate. Note also that some currents in some regions will have an exponential dependence on temperature, which requires a different algorithm for interpolation to remove self-heating.

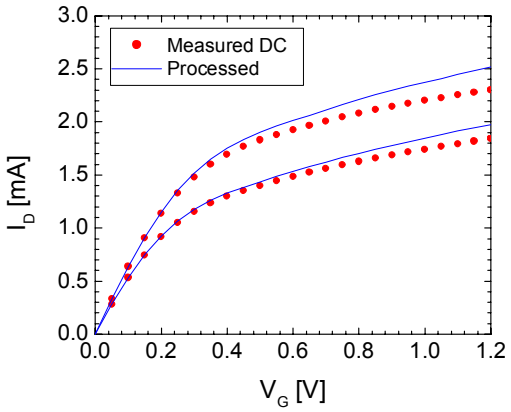

Fig. 4. Data is processed (solid line) to remove self-heating from DC measured data (circle). Shown for ambient of 27°C.

Model parameter calibration proceeds by using BC devices to characterize capacitance and parasitic DC currents because parameters related to several fundamental components such as MOS channel body effect, impact ionization, and junction diode characteristics cannot be directly measured on floating-body devices. Initial I-V fits for both BC and FB configurations are performed. Another unique PD-SOI consideration is that multiple parameters are shared between the FB and BC calibrations. This can introduce the need to refine the BC calibration by verifying parameter consistency for FB effects such as the SOI history-effect. It is not uncommon to iteratively fine-tune some model aspects to improve the fitting due to the increasingly challenging characterization tasks of these components.

While adjustment of MOSFET channel current characteristics has very limited impact on parasitic currents, adjustment of parasitic currents leads to noticeable change in channel current. Therefore, it is strongly recommended to begin the calibration flow with parasitic currents and then to evaluate high-level effects like history before refining the overall MOSFET model characteristics [8].

Once satisfactory model-to-hardware comparison results are achieved, the model is re-centered (*i.e.*, tuned slightly) to match desired technology targets as needed. When this base model is completed, other features like statistical models and

systematic variation (*e.g.*, layout-dependent stress [9]) can be incorporated by expanding the basic calibration flow in Fig. 2.

C. Challenges

Going forward from one node to another can introduce modeling difficulties. Some issues and solutions that have proven effective in past work are as follows:

1) Small body currents not easily measurable because of larger BC-specific parasitic currents (such as the bridge region I_{gb} which can overwhelm both channel-region I_{gb} in inversion and reverse-biased diode leakage, particularly at lower temp). Solution: choose bias regions carefully to highlight the intended signal, and to implicitly fit with history-effect and/or DC FB Drain Induced Barrier Lowering (DIBL) from I-V data.
2) Limited range for reverse-biased diode DC leakage due to the onset of full depletion in the body region. Solution: fit implicitly with history-effect and/or DC floating-body DIBL.
3) Limited range of DC body effect (V_t vs. V_{bs}) measurements due to large (non-linear bias-dependent) body resistance. Solution: choose data range with care.
4) Limited range of AC junction capacitance measurements due to large junction leakage. Solution: choose data range to emphasize intrinsic capacitive response.

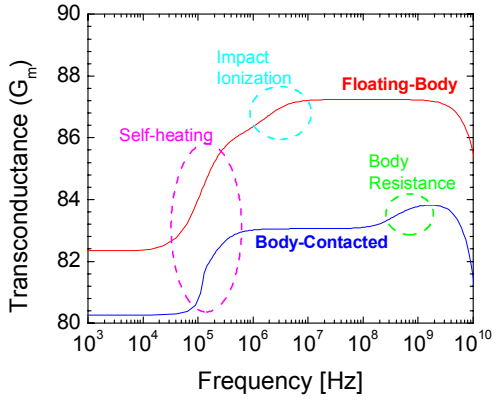

Fig. 5. Simulated G_m frequency response of a PD-SOI nMOSFET. These curves can be used to study detailed model response.

Figure 5 illustrates implicit calibration using RF data. In this figure, MOSFET Gm is plotted against frequency for a BC device and an FB device. This figure identifies the time constants associated with the transition of the body contact to floating-body mode; operation faster than the self-heating time constant; and, impact ionization currents interacting with the body charge.

III. PD-SOI Floating-Body Effects Modeling

The threshold voltage of the MOSFET is a function of the body potential, which affects the amount of the channel depletion charge. While multiple bodies are tied to a fixed potential in the conventional bulk CMOS, each thin-film body region of the PD-SOI CMOS is isolated; thus, its potential is determined by numerous components. For simplicity, this paper will only use nMOSFETs in the rest of discussion.

A. DC Floating-Body Effects

It has been known that a high drain bias can cause a kink in I_D vs. V_D characteristics due to an abrupt turn-on of majority carrier injection into the floating-body generated by the impact ionization [10]. This kink can occur even for drain voltages below the band-gap voltage owing to various energy gain mechanisms [11],[12].

The abrupt turn-on in inversion of gate-to-body tunneling of the ultra-thin gate oxide in the state-of-the-art PD-SOI technologies adds another charging mechanism to the body, leading to a second peak in linear transconductance [13].

Other mechanisms lead to more subtle changes in DC characteristics. At lower drain voltages, diode recombination and band-to-band junction tunneling currents will increase DIBL and off-current due to various highly non-linear components that control the floating-body charge. Clearly, these dependencies make it imperative to fit parasitic body effects prior to fitting the channel current in an FB SOI MOSFET.

B. Transient Floating-body Effects (History-Effect)

The body potential is determined by majority carrier density in the floating-body. Depending on the switching conditions, the majority carrier density increases or decreases by various DC and AC coupling effects. Some charging and discharging mechanisms are reversible, which means if the device returns to its initial state, the body potential on return will be the same as the initial one. On the other hand, some mechanisms are irreversible, making each individual device subject to their switching history; thus, this behavior is called the history-effect [14]. The history-effect can be characterized by measuring propagation delays in the following three extreme conditions [14]:

- 1^{st} switch: This condition refers to the first transition after holding the circuit's input constant for a long time so that the body potentials can reach DC equilibrium. Depending on the direction of the input signal switching, the history-effect can be further distinguished as "1^{st} switch 0→1" or "1^{st} switch 1→0." This paper will use only the 0→1 condition for sake of simplicity .
- 2^{nd} switch: This refers to the transition immediately after the 1^{st} switch transition.
- DSS: Most circuits switch frequently thus may not return to the DC equilibrium. If a circuit switches constantly with a 50% duty cycle like an oscillator, the body potentials of the PD-SOI devices gradually converge to a steady-state condition (see Fig. 7); in turn, the rise-to-rise and fall-to-fall delays become the same. This state is often called DSS (Dynamic Steady State) [15] or SSS (Switching Steady State) [16].

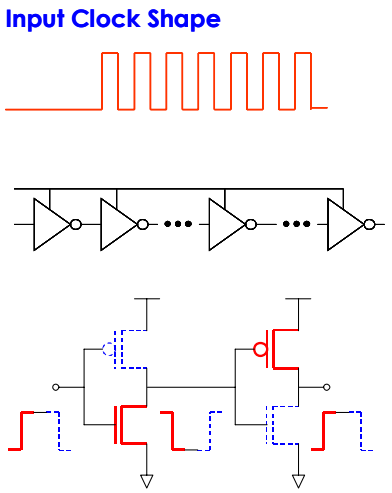

Fig. 6. Inverter delay-chain and its input pulse for characterizing the history-effect. Monitoring the stage delay in alternating stages gives 1st and 2nd switch delays.

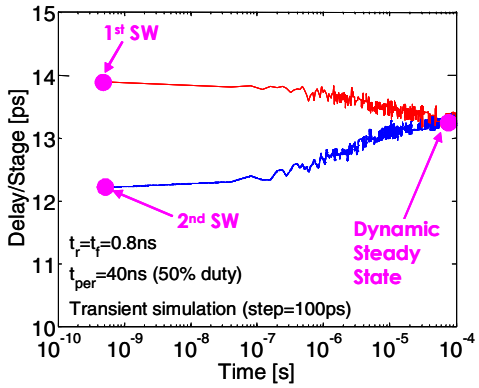

Fig. 7. Evolution of switching delay in a floating-body PD-SOI inverter chain.

Most circuits neither switch every cycle nor sit at DC equilibrium for long periods of time. Nevertheless, these three conditions well represent the extreme situations that most circuits encounter. Generally, the DSS condition tends to be somewhere between the 1st and 2nd switch delays but, in some MOSFET device designs under high voltage conditions, it is possible for the DSS condition to result in the fastest delay as high impact ionization rates prevalent at high voltages drive body voltages higher than equilibrium condition values. As a metric for the worst-case delay offset, this paper quantifies the history-effect (H) as the relative difference of the propagation delay (τ) between the 1st and 2nd switches:

$$H = (\tau_{1st} - \tau_{2nd}) / \tau_{2nd}$$

C. What Determines the History-Effect?

The mechanisms that influence history can be roughly categorized by their response time [17]:

- Very fast capacitive couplings from the gate, source, and drain (reversible unless it triggers fast discharging process);
- Fast discharging through forward-biased source and drain junctions (irreversible); and,
- Slow charging through reverse-biased junctions, impact ionization, and gate tunneling current (irreversible) .

In CMOS digital circuits, the nMOSFET typically determines the pull-down delay. As illustrated by the inverter body potentials in Fig. 8, $V_{body,1st}$ (the body potential of the 1st switch) is purely determined by the initial DC conditions and a capacitive coupling is added to the initial DC condition for $V_{body,2nd}$.

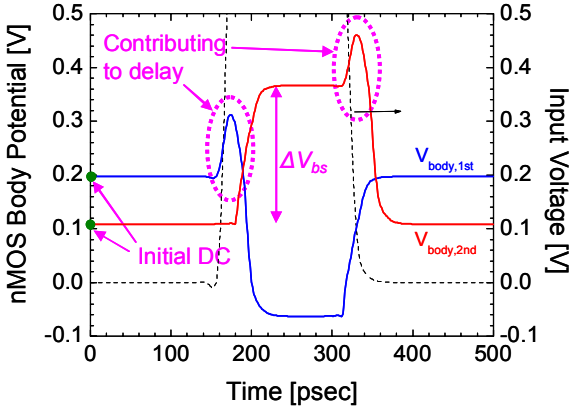

Fig. 8. Evolution of the nMOSFET floating-body potential in an inverter delay chain during a switching event. An extra boost in the body potential is introduced by gate coupling during switching.

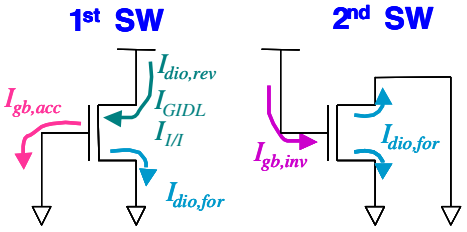

Fig. 9. Key current components to determine the initial DC body potential.

Figure 9 illustrates the current components that interact to generate the initial DC V_{body}. Down to 130nm technology, the initial DC condition was determined by the reverse and forward diode currents (consisting of diffusion, generation-recombination, band-to-band tunneling components) and GIDL. From 90nm onward, the gate-to-body valence band tunneling current (I_{gb}) has shown a visible impact, mostly on the 2nd switch [18]-[20]. GIDL and impact ionization currents are becoming essential factors in determining the body potential [21].

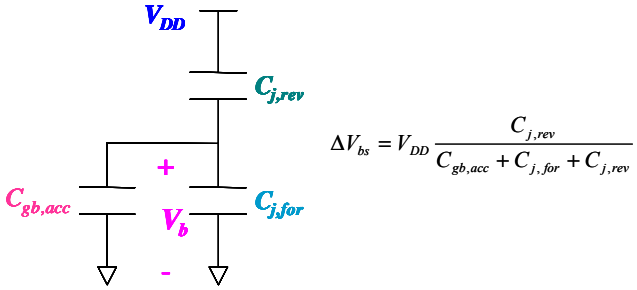

Fig. 10. Key current components to determine the capacitive coupling of body potential.

As illustrated in Fig. 10, the capacitive coupling amount in the 2nd switch condition can be simply understood as a capacitive voltage divider, consisting of gate-to-body capacitance and forward/reverse junction capacitance.

Finally, the body-effect of the MOSFET (V_t vs. V_{bs}) is the main transfer function of V_{bs} into propagation delay; thus, its fitting is critical in history-effect modeling. Figure 11 demonstrates that the measured history-effect can be successfully reproduced by simulation across a wide range of conditions when all the key components are properly modeled.

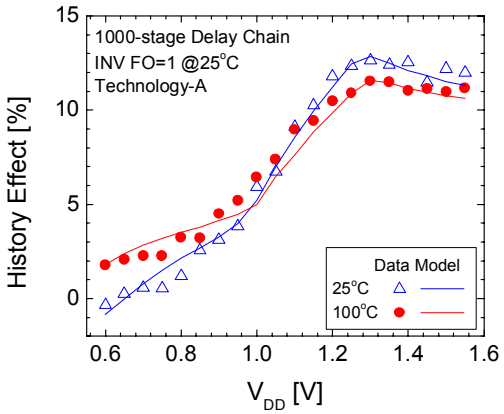

Fig. 11. History-effect of an inverter chain at different bias and temperature conditions, comparing measured data with simulation results.

D. Other Floating-Body Effects

The positive body potential in the floating-body PD-SOI tends to stay in the positive side for most of the time, which can result in elevated FET leakage following a switching event and activate the parasitic bipolar transistor. Combined with capacitive coupling, the body potential can exceed 0.7V in logic circuits and therefore approach the operating regime in which bipolar effects can be significant. The pass-gate logic operation is particularly vulnerable to bipolar effects [22]. Fortunately, the parasitic bipolar problem is partially alleviated by the trend toward lower power supply voltages.

E. Challenges

Statistical modeling of the history-effect, including corner model definitions, is a challenge due to the need for accurate floating-body effect characterization. Monte Carlo simulations can be used to investigate statistical history-effects, in which the variation of key statistical sensitivities include the model parameters for the parasitic currents and capacitances that drive floating-body effects.

Direct measurement of the floating-body effect using a single-stage logic gate requires very high accuracy test equipment, and test throughput is extremely low because of the duration of the measurement. One of the most widely used structures for characterizing the history-effect is a delay chain (as shown in Fig. 6) consisting of hundreds or thousands of stages of logic gates that allows characterization in the MHz range. However, the measured history-effect is averaged over all stages; thus, measuring the switching details of the history-effect is virtually impossible. The test structure also occupies a fairly large area. Figure 12 shows statistical data for the history-effect and its comparison with the simulation results including corners.

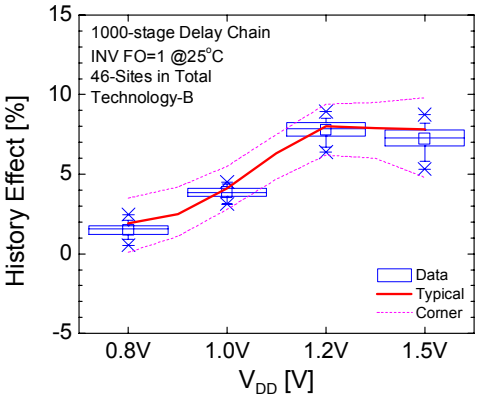

Fig. 12. Statistical history-effect data collected from all sites across a wafer and compared with corner model simulation results.

Recently, a novel in-line test circuit in a relatively compact macro has been proposed that enables fully automated test for quantifying the history-effect using only simple DC equipment [23]. This design trades the ability to monitor history in-line using digital test equipment for approximate precision in the measurement.

IV. PD-SOI Body-Contacted Device Modeling

In principle, a BC device can help eliminate or reduce the floating-body variation in sensitive circuits. It also offers an additional degree of freedom in circuit design.

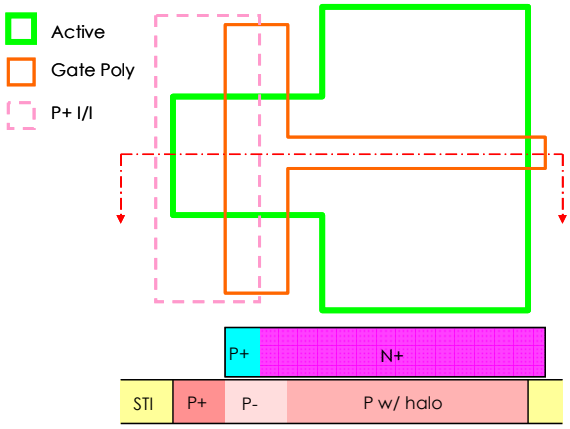

Fig. 13. An example of body-contacted PD-SOI nMOSFET layout and its cross-section.

A. Extra Parasitic Capacitance of the Extended-Gate

As illustrated in Fig. 13, the body-contacted PD-SOI MOSFET has an extended gate to bridge the channel implants to body contact diffusion (P- region in Fig. 13)[24]. The body contact structure adds extra overlap, gate-to-body, and body-to-substrate capacitance that introduces a substantial penalty in switching speed. Importantly, the gate-to-body capacitance of the bridge-region needs to be carefully modeled, as it is the most significant capacitive component since the P+ over P (or

N+ over N for a BC pMOSFET) region (as shown in the left portion of Fig. 13) is in accumulation.

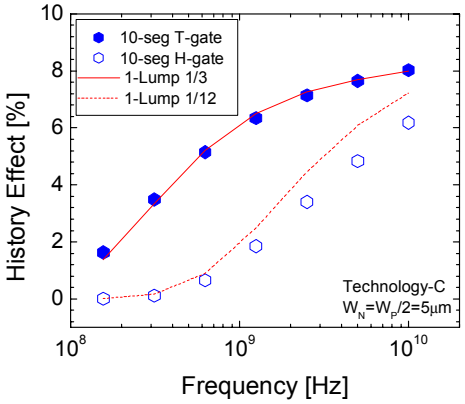

Fig. 14. History-effect of a body-contacted PD-SOI CMOS, comparing partitioned (into 10 segments) case with a single MOSFET case (with scaled body resistance).

B. Body Resistance

The combination of thin Si body regions and low channel doping can create a body RC time constant that is substantially higher than other circuit elements; thus, the electrical element network for the body has to be carefully modeled [25],[26]. The most accurate body resistance consists of several parallel resistances (well and halo implants) and series resistances (distributed or segmented body resistance) [24] and it is desirable to capture the bias-dependence as well [6]. A switching event causes a strong capacitive coupling to the body potential even in BC devices, and this leads to the history-effect similar to the one present in a floating-body device, *i.e.*, no body contact structure is completely ideal. The distributed effect of the body resistance is an essential element that is needed to capture the BC history-effect correctly. In principle, the MOSFET can be partitioned into smaller segments along the width direction then connected in series [6],[24], but the cost is a significant penalty in simulation time. Alternatively, as demonstrated in Fig. 14, a single MOSFET approximation can reasonably reproduce a multi-partition channel by scaling the body resistance with mathematically-derived R equivalence factors: 1/3 for one-side body-contact (T-gate) and 1/12 for two-side body-contacts (H-gate). The same equivalence factors are also found in the BJT base resistance model [27] and MOSFET gate resistance model [5],[28].

V. PD-SOI Floating-Body Effects Simulation

A. Accuracy Options in SPICE

Since the evolution of the floating-body potential is on a much smaller voltage scale than the supply voltage level, the accuracy options in circuit simulations are crucial. First, the PD-SOI circuit simulations require higher accuracy in voltage convergence criteria than bulk circuit simulation. Otherwise, the change of the body potential can be incorrect, especially during fast switching at high supply voltage, leading to a significant error in propagation delay prediction, as demonstrated in Fig. 15.

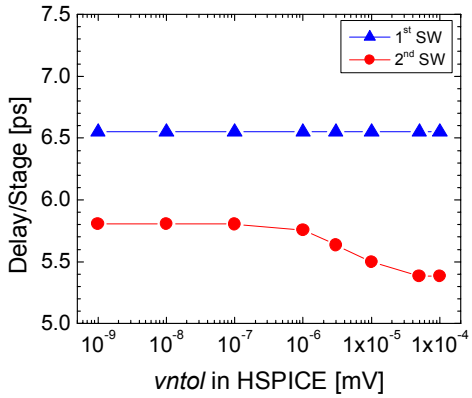

Fig. 15. Impact of SPICE transient voltage tolerance on switching delay accuracy of a floating-body PD-SOI circuit.

Common techniques to help simulation convergence also need to be carefully reviewed. One example is that SPICE adds a conductance across all capacitors, including junction diodes and gate oxides of MOSFET devices, during initial DC operating point calculations. In bulk circuits, this conductance causes virtually no impact in solutions. However, this conductance sometimes can be larger than parasitic currents in the PD-SOI device such as the gate-to-body tunneling current or the reverse diode current.

In this case, the initial DC operating point solutions from SPICE are incorrect. Special attention should be paid to numerical convergence criteria at low temperature because diode currents show much stronger thermal voltage sensitivity at lower temperatures.

B. Dynamic-Steady-State Simulation

One of the challenges in PD-SOI circuit simulations is computational efficiency in the steady-state assessment that is particularly critical for large multiple-input circuit macros, SRAMs, clock drivers, I/O devices, and analog circuits such as PLLs. Reaching steady-state generally takes an order of micro- (or even milli-) seconds due to the slow nature of charging and discharging components. This is an impractically long time period to run a straightforward SPICE simulation for large scale circuits. Several techniques have been proposed for steady-state simulation to achieve a reasonable computational cost.

The harmonic balance method directly finds the steady-state solution by solving the circuit equations in the frequency domain using a Fourier series [29]. Generally, this method is efficient but requires over-sampling and more than six harmonics to achieve consistent results with transient simulations [30] in some simulators. A more recently proposed technique tracks the net body charges for a single cycle of the specified periodic input pattern, then projects its evolution using the Newton method until the change of the net body charges becomes zero [31],[32],[33].

In case the simulation tool does not support such techniques mentioned before, there are approximate methods such as [33] in which it has been empirically found that the body potential can be initialized close to the steady-state

solution for ring oscillators by setting all switching gate nodes to $V_{DD}/2$.

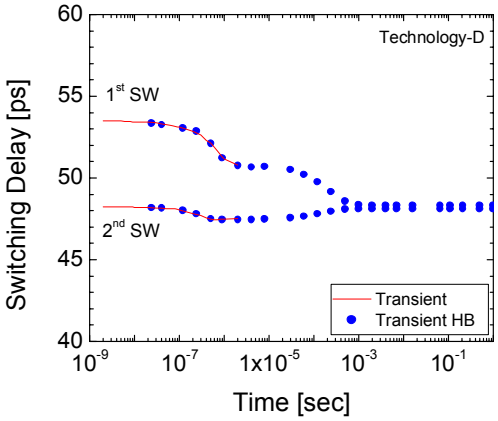

Fig. 16. History-effect in ten-stage inverter chain. Complete transient harmonic balance results are obtained in under 10min, while (incomplete) transient results run for more than a day. These results demonstrate the ability of harmonic balance to efficiently capture complex body effects.

C. Charging and Discharging Time

Many modern circuits experience sleep and wake-up modes to minimize power consumption. In such a case, it is crucial to estimate the charging time required to restore the steady-state and the discharging time to reset the potentials to DC 1st and 2nd switch values. The transient harmonic balance method enables running such simulations within affordable runtime by solving slow transients in the time domain (transient analysis), simultaneously with fast transients in the frequency domain (harmonic balance analysis) [34],[35]. Figure 16 shows the history-effect simulated using transient harmonic balance methods.

D. Considerations for Self-Heating Simulations

As previously mentioned, self-heating is modeled using an auxiliary node inside the MOSFET model and the solved potential on that node is interpreted inside the model as an increase in operating temperature. A side effect of this modeling approach is that the matrix stamp for each MOSFET grows due to the addition of the temperature node and simulation runtimes increase correspondingly. Fortunately, in high-performance logic simulations, switching occurs faster than the thermal time constant, so approximately the same simulation results can be obtained with self-heating disabled. However, self-heating should be enabled in circuits with lower operating frequencies or circuits with mixed fast and slow time constants.

VI. Standards for SOI MOSFET Models

An important facet of compact modeling that spans academia, ULSI foundries, and chip design shops is standardization. Standardization helps ensure consistency in model implementation across circuit simulator platforms [36]. In addition, model developers receive recognition and academic funding for their contributions and circuit designers benefit from improved model accuracy and features that are honed through detailed review during in the standardization process [37]. Today the compact model standards-setting body is the Compact Model Council (CMC) [38], which is hosted by the Government Electronics and Information Association (GEIA). The CMC evaluates a candidate model's ability to reproduce relevant fundamental phenomena and its numerical properties such as symmetry, continuity, convergence, and runtime.

The current CMC-standard model is BSIMSOI from the University of California at Berkeley. In 2006, the CMC began a process to develop a standard for next-generation SOI MOSFET models. The CMC has published documents outlining model requirements [39] that are applicable to PD- and FD-SOI technologies, as well as the procedure for standardization [40]. The CMC is currently soliciting candidate models.

VII. Conclusion

The modeling, characterization, and simulation of PD-SOI MOSFETs have been reviewed while highlighting the current and future challenges in building PD-SOI compact models. PD-SOI circuit simulation and model standardization efforts have also been summarized. Much of the complexity in PD-SOI compact modeling originates from the floating-body, which has attributes that can be difficult to measure. Despite these challenges, compact model structures, calibration methods, and circuit simulation approaches have been developed and implemented for accurate simulation of PD-SOI circuit behavior.

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