Copper Interconnect Technology for the 32 nm Node and Beyond

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Abstract - Copper interconnects have gained wide acceptance in the microelectronics industry due to improved resistivity and reliability compared to Al interconnects. However, there are many challenges with implementation of Cu interconnects at the 32 nm node and beyond, including increased resistivity, integration with porous low-k materials, and reliability. In addition, for RF and mixed signal technology, integration of passive devices is required. In this paper, each of these topics is addressed.

I. INTRODUCTION

On-chip copper interconnects have gained wide acceptance in the microelectronics industry due to improved resistivity and reliability compared to Al interconnects [1]. Initially, copper interconnects were only used for high performance logic circuits. However, Cu interconnects are now used in a wide variety of integrated circuits, including dynamic random access memories (DRAM) [2], RF circuits [3], and CMOS image sensors [4]. Copper interconnects will continue to be used for the 32 and 22nm technology nodes. However, there are many challenges with implementation of Cu interconnects at these nodes, including increased resistivity, integration with porous low-k materials, and reliability. In addition, for RF circuits, integration of passive devices is required. In this paper, each of these topics is addressed.

II. BASIC PROCESS FLOW

Copper cannot be easily patterned by reactive ion etching (RIE), due to the low volatility of Cu chlorides and Cu fluorides. Hence, Cu interconnects are formed using the "dual damascene" process (Fig. 1) [1,5]. After processing of M1, the V1/M2 dielectric is deposited (SiCOH, for example) and V1 vias are patterned (Fig. 1a), stopping on the SiCN layer that protects the Cu from oxidation. Next, the M2 trenches are patterned (Fig. 1b and 1c), the final step being the removal of the SiCN etch stop from the bottom of the via. The first part of the metallization is sputter deposition of a TaN/Ta barrier layer (which prevents Cu from diffusing into the dielectric) and a Cu seed layer (Fig. 1d). The vias and trenches are then filled with Cu by electroplating (Fig. 1e). The excess metal over the field regions is removed by chemical mechanical polishing (CMP). The final step is deposition of an SiCN capping layer, that protects the Cu from oxidation (Fig. 1f). These steps are repeated for each metal level. After the last metal layer is fabricated, thick dielectric passivation layers are deposited and vias are opened to the bond pads.

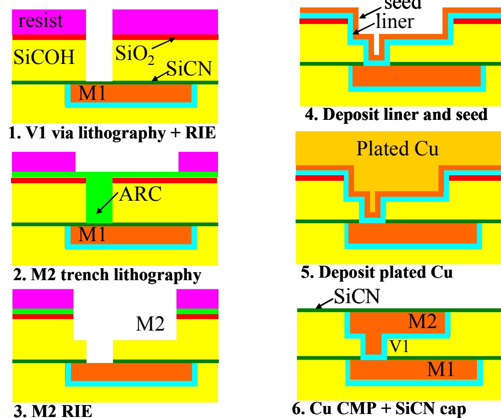

Figure 1. Schematic of process flow for dual damascene Cu.

Note that from the design perspective, there are a number of important differences between Al interconnects and Cu interconnects. Because Cu is patterned by polishing, there are more restrictions on pattern density compared to Al technology, and dummy metal shapes are required to minimize differences in pattern density across a chip [6]. In addition, the Cu must be capped with hermetic barrier layers (SiN or SiCN) to protect it from oxidation during processing or during device operation. These materials have much higher dielectric constants than that of the interlevel dielectric; for SiN, k ~ 7, and for SiCN, k ranges from ~ 4 to 5, depending on the processing. Hence, the effective dielectric constant is typically 10% higher than that of the interlevel dielectric.

III. COPPER RESISTIVITY

As the dimensions of Cu interconnects are reduced, the resistivity increases due to surface scattering, grain boundary scattering, and an increasing fraction of refractory metal liner in the trench (Fig. 2) [2,7]. In the past, it has been noted that for pure metals, the increase in resistivity with reduced thickness is less for Al than for Cu, because Al has a shorter electron mean free path compared to Cu (15 nm versus 39 nm) [8]. Hence, simulations show there is a cross-over point in resistivity of the pure metals, with Al having lower resistivity than Cu for line widths below 30 nm (Fig. 2). So should we go

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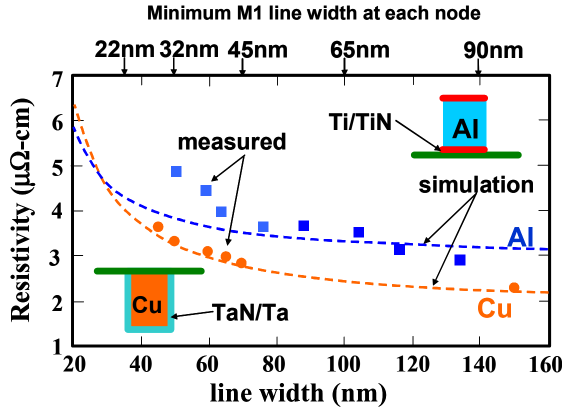

Figure 2. Data from Lee et al. [2] on resisitivity of Al versus Cu interconnects as a function of line width

back to Al for on-chip interconnects? The answer is no, for two reasons. First, the resistivity of real Al wires goes up faster than that of pure Al, due to refractory metal layers that are required for reliability (Fig. 2) [2]. In addition, Cu has better reliability than Al in terms of electromigration. Hence, Cu will continue to be used for interconnects down to the 22 nm node and beyond.

What can be done to avoid problems associated with the increasing resistivity of Cu as wire dimensions are reduced? In principle, increasing the grain size of Cu in narrow lines would be very beneficial, but it is difficult to achieve in practice. A more promising approach is to reduce the thickness of the refractory metal liner, by using improved sputtering methods, atomic layer deposition (ALD) instead of sputter deposition, or by using self-forming barrier layers such as Mn silicate.

There are also design solutions to this problem. The interconnects with the largest increase in resistivity are at the lowest levels, where the length is typically short, so the resistance increase is less critical [9]. For layers where the high resistivity of the Cu is critical, changes in the design may be necessary, such as increasing the wiring pitch or adding a metal layer.

IV. LOW-K DIELECTRICS

Initially, SiO_2 was used as the interlevel dielectric surrounding the Cu wires (Fig. 3). For process integration, SiO_2 has many good properties [10]. It is thermally and chemically stable, and therefore does not degrade during processing. It is mechanically rigid (i.e. high elastic modulus) and is relatively impermeable to moisture (at least at the operating temperature of integrated circuits), which simplifies packaging. In addition, high quality films can be deposited by plasma enhanced chemical vapor deposition (PECVD). Of course, the disadvantage of using SiO_2 is that the dielectric constant is higher than desired.

The dielectric constant of SiO_2 can be reduced to ~3.5 by doping with F [11]. The F-doped SiO_2 (fluorosilicate glass, FSG) has mechanical, chemical, and thermal properties that are similar to SiO_2. As a result, FSG replaced SiO_2 as the interlevel dielectric at the 130 nm technology node.

But further reductions in dielectric constant are required as the device dimensions are reduced. The dielectric constant of SiO_2 can be further reduced by using carbon doping instead of fluorine [12]. Bridging Si-O bonds are replaced by non-bridging Si-CH_3 bonds (Fig. 3), resulting in a lower density, and hence a lower dielectric constant. In addition, the Si-C bonds have lower polarizability than Si-O bonds. The C-doped SiO_2 is often called SiCOH, which corresponds to the chemical components in the film. The dielectric constant of non-porous SiCOH is typically 2.7 to 3.0. However, even lower dielectric constants (2.2 or less) are possible by adding pores to the SiCOH.

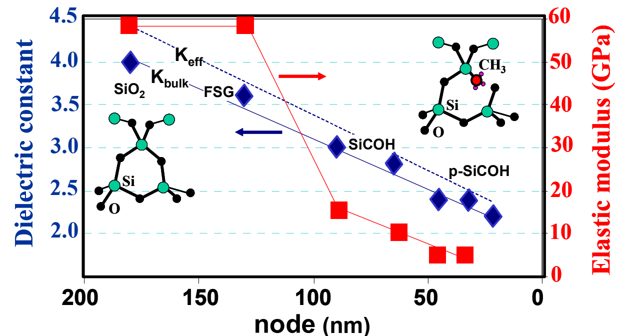

Figure 3. Trend for low-k dielectrics, based on ITRS roadmap [24].

Because of the improved performance associated with the lower dielectric constant, non-porous SiCOH is used at the 90 nm and 65 nm technology nodes, and porous SiCOH is used at the 45 nm node and below. However, the integration of Cu interconnects in SiCOH dielectrics requires many process changes, both during wafer processing and during packaging, especially for porous SiCOH. The modulus of SiCOH dielectrics is much lower than that of SiO_2 (Fig. 3) and the films are brittle. Hence, a number of design and process changes must be made to avoid delamination of the stack during Cu polishing, such as optimizing the layout of the dummy metal shapes, use of low down-force CMP, and maximizing the adhesion of all layers in the stack. Design and process changes must also be made to allow reliable packaging of these die. Design solutions include improved layout of the crack stop and edge seal [13], and the bond pads [14]. An example is the addition of dummy vias underneath bond pads to mechanically reinforce the dielectric stack [14]. Packaging process changes include optimizing the dicing process (two-step dicing or laser dicing), the underfill (lower modulus) [15], and the molding compound (lower coefficient of thermal expansion, CTE) [16]. In addition, SiO_2 is used as the interlevel dielectric (rather than a low-k material) for the last one or two metal levels, to provide increased mechanical strength underneath the bond pads.

The low density of SiCOH and porous SiCOH can cause problems during device operation. The diffusivity of H_2O is very fast in both of these materials [17,18], and is a potential reliability problem during device operation. To ensure reliability, each Cu layer is capped with hermetic barrier layers (such as SiN or SiCN) and an edge seal is used around the perimeter of the chip to block H_2O diffusion. Thermal

conductivity is also degraded due to the lower density of SiCOH and porous SiCOH compared to SiO_2 [10,19]. A possible design solution is to add dummy vias, to increase the effective thermal conductivity of the structure [19].

V. AIR GAP TECHNOLOGY

Because of all the problems associated with porous low-k dielectrics, there is renewed interest in using air gap technology [20]. There are two basic air gap approaches: the localized airgap method (Fig. 4a-c) and the global air gap method (Fig. 4d-f). The localized air gap method is the preferred approach, though an extra mask is required for each level where air gaps are used [20]. With the localized method, air gaps are only formed in critical regions of the circuit. Hence, the mechanical integrity and thermal conductivity are maintained in most regions of the die, allowing the use of conventional wafer processes and packaging processes. The localized air gap approach has been demonstrated on a 65 nm microprocessor, with effective k values as low as 2.0. The disadvantage of the air gap process compared to porous low-k materials is that there is extra cost associated with lithography and etching of the air gaps. However, there are also extra costs associated with processing low-k materials, so air gap technology is an attractive option for 32 and 22 nm nodes.

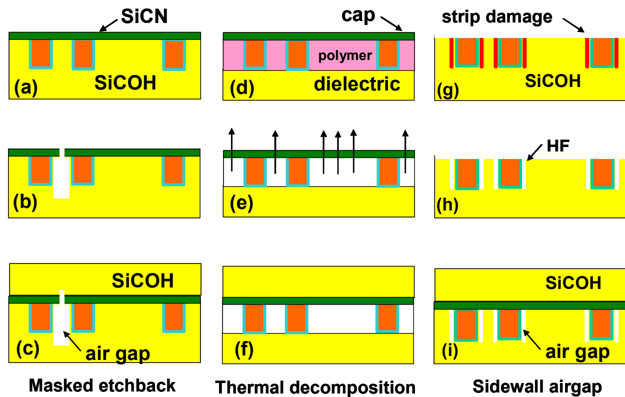

Figure 4. Schematic of three different air gap processes

VI. RELIABILITY

One of the main reasons for switching from Al to Cu interconnects was the improved reliability of Cu (for electromigration in particular) [1]. For the first generations of Cu technology, the improvement in electromigration was more than adequate for the needs of circuit designers. However, as device dimensions shrink, the electromigration lifetime of conventional Cu is no longer adequate. In addition, there are new reliability problems associated with the small dimensions, such as dielectric breakdown (Fig. 5). Low-k dielectrics cause additional problems for device reliability, especially in terms of package reliability, due to the low mechanical strength and brittleness of these materials. In this section, we will describe reliability challenges for Cu interconnects in low-k dielectrics.

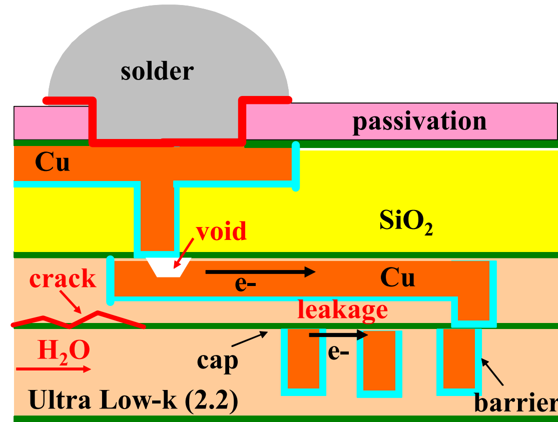

Figure 5. Possible reliability failure mechanisms for Cu interconnects in low-k dielectrics.

A. Electromigration

Electromigration is the migration of metal atoms in a conductor due to an electrical current (Fig. 5) [21]. For Cu interconnects, the TaN/Ta barrier layers at the bottom of the via act as blocking boundaries. Hence, during an electromigration stress, metal atoms will be depleted at the upstream side of the wire, and eventually voids will form. At the downstream end of the wire, metal will accumulate, resulting in a hydrostatic stress. This stress produces a back flux of atoms, that is opposite in direction to the flux from electromigration [22], and is called the Blech effect. For short wires (i.e. below a critical threshold of current density times length), the back flux of atoms prevents killer voids from forming and the wires are immortal [23]. Therefore, it is possible to avoid electromigration problems in local interconnects by limiting the length of the wires.

The electromigration lifetime for Cu is much greater than that for Al, by > 100x [1], due to the lower diffusivity of Cu compared to Al. This allows circuit designers to use higher current densities in circuits, and thereby achieve higher switching speeds. However, as device dimensions and wire dimensions are reduced, it is desirable to increase the electromigration lifetime of Cu [24], because both the drive current in the devices and the switching speed increase. At the same time, the dimensions of the minimum size wires (ie. used for local wiring) decreases. Hence, a higher current density is required in the wires (Fig. 6). However, the electromigration lifetime decreases as wire dimensions decrease. The main reason is that the void size required to cause a fail decreases as the via size and wire size decreases [25]. Hence, a shorter time is required to form a "killer" void.

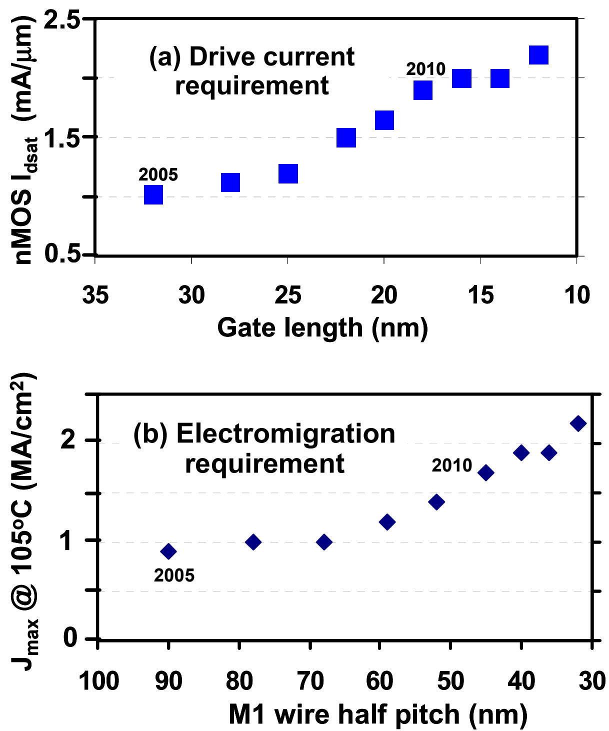

Figure 6. Technology requirements for nMOS drive current and electromigration based on ITRS roadmap [24].

There are a number of ways to improve the electromigration lifetime of Cu. The electromigration lifetime for Cu interconnects is determined by mass transport at the interface between Cu and the capping layer [25], and can be improved by increasing the adhesion between these layers [26]. Hence, the capping layer process is critical to achieving a long electromigration lifetime. A typical dielectric capping process (Fig. 7a-d) consists of a plasma clean to remove Cu oxides, a

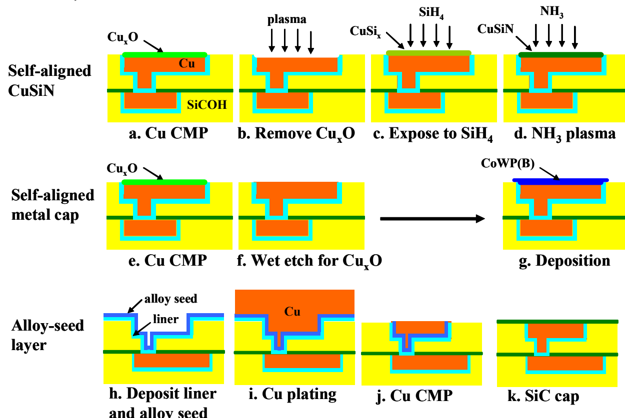

Figure 7. Methods to improve electromigration lifetime of Cu interconnects.

brief SiH_4 exposure to form a thin Cu silicide layer for improved adhesion, and finally, the dielectric deposition (either SiN or SiCN). A further reduction in interface diffusion can be achieved by using a metal capping layer (Fig. 7e-g), rather than a dielectric capping layer [25]. Improvements in electromigration lifetime of over 300X have been reported with a CoWP cap. The main problem with this approach is that line-to-line leakage may be increased if selectivity of the deposition is not adequate.

Another method to improve the electromigration lifetime is to dope the Cu with impurities, such as Al [27], Ag, or Mn [28]. The dopants are typically introduced into the Cu seed layer (Fig. 7h-k). During subsequent anneals, the impurities segregate at grain boundaries and interfaces, including the critical interface between the Cu and the capping layer. The presence of the impurities at the interfaces reduces Cu diffusion, resulting in an enhancement of electromigration lifetimes of over 10x, with higher doping concentrations resulting in higher electromigration lifetimes. The main problem with this approach is that the impurities increase the resistivity of Cu [27].

B. Time dependent dielectric breakdown (TDDB)

During a prolonged stress at high electric fields, damage can occur in dielectrics, eventually resulting in a conducting path and electrical breakdown [21]. Historically, this was mainly a problem for gate dielectrics, because the spacing between metal wires was relatively large, so the electric field across the BEOL dielectric was low. However, as device dimensions are reduced, the lateral electric field across the BEOL dielectric increases (Fig. 8). Although the maximum

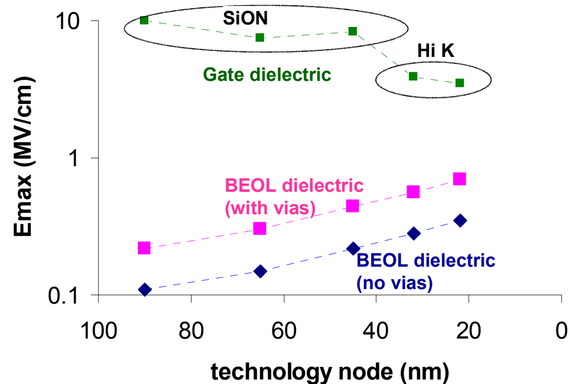

Figure 8. Maximum electrode field across gate dielectric and between minimum pitch interconnects as a function of technology node based on ITRS roadmap [24].

electric field across the BEOL dielectric is still considerably lower than that across the gate dielectric, the breakdown strength of the BEOL dielectric is considerably less. There are a number of reasons for the low breakdown strength of BEOL dielectrics, including a high density of defect sites in the as-deposited dielectric (especially for low-k materials) [29], damage or contamination of the dielectric from processes such as CMP, Cu diffusion into the dielectric through the barrier layers [30,31], and patterning problems such as line-edge-roughness or via misalignment. As a result, dielectric reliability becomes more challenging as device dimensions

shrink and as the dielectric constant of the BEOL insulator is reduced.

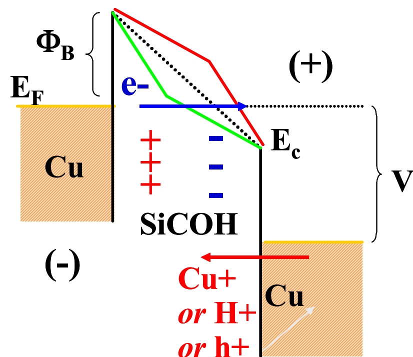

Figure 9. Band diagram of low-k dielectric between two Cu wires during high field electrical stress. Injection of electrons into the dielectric can cause Cu ionization at the anode, eventually leading to breakdown [30].

Dielectric reliability is assessed using a time dependent breakdown test (TDDB). The test structure consists of a comb-comb or comb-serpent layout at the appropriate metal level (typically M1, because this has the smallest pitch). Dielectric breakdown occurs due to either bond damage or metal diffusion into the insulator as a result of the high electric field. One model [30] assumes that the injected charge causes ionization of Cu in the interconnect, resulting in drift into the dielectric, and creation of traps (Fig. 9). An alternate model [29] assumes that damage occurs because the activation energy for bond breakage is reduced because of the electric field.

Dielectric breakdown between neighboring Cu wires generally occurs at the interface between the capping layer and the dielectric (Fig. 10) [31]. The electric field is highest at this location because the Cu wires are generally tapered (wider at

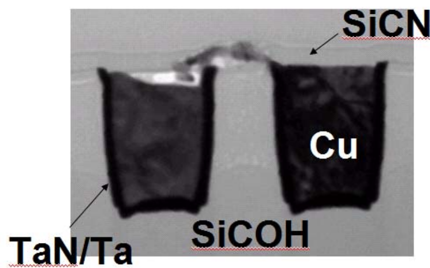

Figure 10. Transmission electron microscope image of Cu interconnects after dielectric breakdown [31].

the top than at the bottom), so the space is smallest at the top of wires. In addition, the interface is expected to have a higher trap density than the bulk dielectrics, due to bond mismatch between the different materials or due to contaminants from the Cu CMP process. It is expected that the interface between the capping layer and the dielectric is the preferred leakage path due to the combination of the high electric field and the high defect density.

The TDDB lifetime is very sensitive to the materials and processes used to form the interconnect layers. The TDDB lifetime typically decreases as the dielectric constant of the material decreases [29]. In particular, porous materials have lower TDDB lifetime than non-porous materials. Possible reasons for the lower TDDB lifetime are weaker bonds, higher trap densities, or lower barrier heights at the metal-insulator interface. Despite the lower TDDB lifetime of porous materials compared to non-porous materials, the intrinsic reliability is still adequate for integrated circuits.

C. Package Reliability

Packaging processes such as dicing, wirebonding, and flip-chip die attach can damage the low-k dielectrics due to mechanical stress [13-16]. Standard tests for assessing the reliability of packaged parts include high temperature storage (HTS), temperature-humidity-bias (THB), high temperature operating life (HTOL), and thermal cycle T/C) (Table I). These tests are designed to accelerate fails associated with mechanical damage in the die, the wirebond, the flip-chip solder bump, or in the encapsulant.

TABLE 1. Tests for package reliability

High temperature storage	125°C, no bias, 1000 h
Temperature-humidity-bias (THB)	85°C, 85% RH*, V_{dd} + 20%, 1000 h
High temperature operating life (HTOL)	85°C, V_{dd} + 20%, 1000 h
Thermal cycle	- 55°C to +125°C, 1000 cycles

Flip-chip attach is a good example of the mechanical stress problems that can occur during packaging. The substrate typically has a much higher coefficient of thermal expansion (CTE) than the silicon die. The die is joined to the substrate at the solder reflow temperature (~180°C for Pb-based eutectic solder, ~ 220°C for Pb-free solder). During cooling back to room temperature, there is stress in the solder and in the chip (especially at the corners of the die) due to the thermal expansion mismatch between the die and the substrate [32].

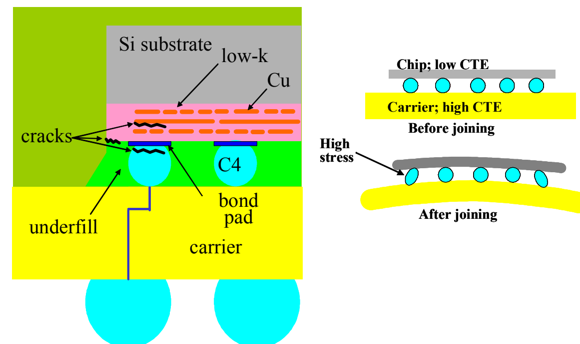

Figure 11. Schematic of cracks that can form in die or in solder due to stress from flip-chip attach or during device operation

Cracks can form in the die or in the solder during chip joining or during subsequent thermal cycling, resulting in device failure. Historically, underfills have been used to reduce the stress in the solder bumps (Fig. 11) [15]. Underfills are epoxy-based materials that are typically dispensed between the die and the substrate after chip joining. With SiO_2 dielectrics, a high modulus underfill (> 9 GPa) can be used, which minimizes the stress on the solder. However, if a high

modulus underfill is used, the stress on the die is increased, and can crack low-k dielectrics. Hence, a lower modulus underfill must be used to avoid cracking the die. Note that if the modulus of the underfill is too low (5 GPa), then fails will occur in the solder. Hence, underfills with intermediate values of modulus must be used, to minimize stress in the die as well as in the solder bump [15].

The stress on the die in a flip-chip package is even higher when Pb-free are solders are used. Pb-free solders have a higher melting point and higher elastic modulus than Pb-based solders. Hence, additional modifications are required to assure reliable device operation, including optimizing the solder composition, solder reflow conditions, and pad layout [33].

VII. PASSIVE DEVICES

Passive devices such as resistors, capacitors, and inductors, are an important component of RF and mixed signal technology [34]. (Fig. 12). Historically, the passive devices

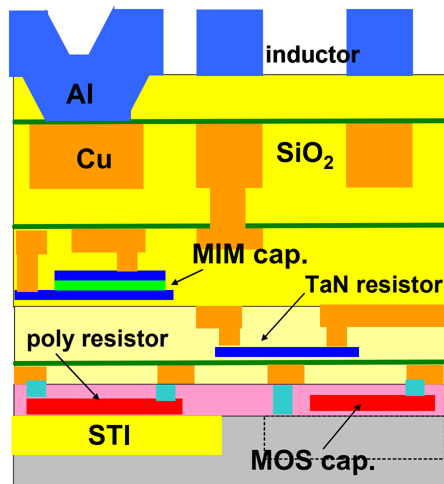

Figure 12. Schematic of on-chip passive devices [3,34].

were surface mounted discrete devices. However, for mobile consumer devices, a smaller form factor and lower cost can be achieved by integrating the passive devices on the chip [34].

A. Resistors

Important parameters for resistors are the resistance, tolerance, parasitic capacitance, voltage coefficient of resistance (VCR), and temperature coefficient of resistance (TCR) [34]. The most common resistors for these applications are p+ polysilicon resistors or metal thin film resistors. Resistors fabricated from p+ polysilicon have low cost (they can be formed with minimal additional processing), low parasitic capacitance (because they are formed over isolation), good matching, and low temperature coefficient of resistance (Table II). Thin film metal resistors have a number of advantages compared to p+ polysilicon resistors, including lower parasitic capacitance (because the greater distance from the substrate) and the ability to make design changes with

TABLE II. Electrical parameters of on-chip resistors

resistor	sheet resistance	tolerance	parasitic capacitance	temperature linearity	ref.
p+ polysilicon	200-300 ohm/sq	10-15%	0,1 fF/um^2	~ 20 ppm/^{o}C	[34]
TaN	140 ohm/sq	10%	0,03 fF/um^2	~730 ppm/^{o}C	[34]
	25 ohm/sq			0 ppm/^{o}C	[35]
	50 ohm/sq			500 ppm/^{o}C	[35]
	100 ohm/sq			800 ppm/^{o}C	[35]
SiCr	440 ohm/sq			100 ppm/^{o}C	[35]

shorter lead time [34]. TaN is commonly used as a thin film resistor with Cu interconnect technology [34,35], because TaN deposition tools are readily available in the factory. The main disadvantage of TaN resistors compared to p+ polysilicon resistors is the TaN has a higher TCR (Table II). The TCR for TaN depends on the nitrogen concentration in the film. At low nitrogen concentrations, the TCR can be close to zero [35], but the resistivity is low. For practical values of resistivity, the TCR is much higher. It is possible to achieve a lower TCR with other thin film materials, such as SiCr. However, this requires unique processes in a Cu process flow and therefore adds to cost.

B. Capacitors

There are a number of options for on-chip capacitors, including metal-oxide-semiconductor (MOS) capacitors (polysilicon gate on single crystal silicon), polysilicon-insulator-polysilicon (PIP) capacitors, metal-insulator-metal (MIM) capacitors, and vertical parallel plate (VPP) capacitors [34]. Simple MOS capacitors can be formed with no

TABLE III. Electrical parameters of on-chip capacitors.

capacitor	dielectric	capacitance	tolerance	voltage linearity	temperature linearity	ref.
MOS	SiO_2	1.2 - 3.1 fF/um^2	10 - 15%	> 1000 ppm/V	20 - 50 ppm/^{o}C	[34]
PIP	SiO_2	1.6 fF/um^2	25%	> 2000 ppm/V	~20 ppm/^{o}C	[34]
MIM	50 nm SiO_2	0.7 fF/um^2	7%	< 25 ppm/V	~50 ppm/^{o}C	[3,34]
MIM	50 nm SiN	1.35 fF/um^2	13%			[3]
MIM	33 nm SiN	2.1 fF/um^2	11%			[3]
MIM	Ta_2O_5	3 fF/um^2		~ 100 ppm/V	84 ppm/^{o}C	[36]
MIM	Al_2O_3	3 fF/um^2		~ 400 ppm/V	255 ppm/^{o}C	[36]
MIM	25nm HfO_2-Al_2O_3	6.6 fF/um^2		109 ppm/V	196 ppm/^{o}C	[37]
MIM	13nm HfO_2-Al_2O_3	13 fF/um^2		236 ppm/V	183 ppm/^{o}C	[37]
VPP	90 nm node 7 metal layers	> 3 fF/um^2				[38]

additional processing and have high capacitance per unit area, but are not useful for RF applications because of the high resistance of the well doping and because of a poor voltage linearity. MOS capacitors can be improved by heavily doping the silicon substrate to reduce the parasitic resistance (Table III)[34].

In the 2 to 10 GHz range, both MOS capacitors and PIP capacitors suffer from low quality factors, due to the high resistance of the plates and due to capacitive losses. For high frequency applications, MIM capacitors are preferred, due to higher quality factor (energy stored / energy dissipated) at high frequencies [34]. MIM capacitors have other desirable properties (Table III), such as high capacitance per unit area

[36-38], and good voltage linearity [34]. The main problem with using MIM capacitors is the additional process steps are required, adding to the cost.

The cost of MIM capacitors is greater for Cu technology than for Al technology. For Al technology, MIM capacitor fabrication is relatively simple (Fig. 13a) [39]. The MIM capacitor is built on top of an Al interconnect layer, requiring an extra deposition for the dielectric and top plate, and one extra mask and etch to pattern the top plate. An analogous process for Cu is to fabricate that MIM capacitor directly on top of a copper layer, using the SiN capping layer as the capacitor dielectric (Fig. 13b). However, there are a number of problems with this approach. First, the MIM capacitor

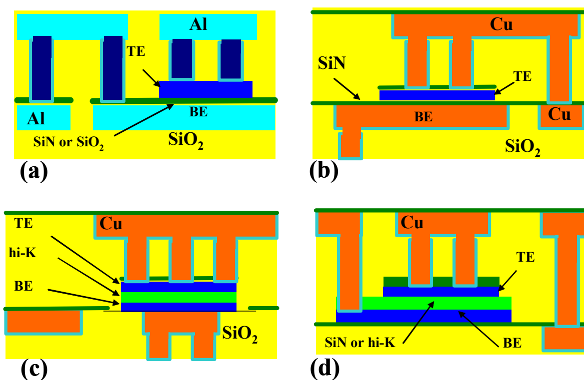

Figure 14. MIM capacitor processes in Al and in Cu technology [39].

dielectric is coupled to the Cu capping layer, which limits the choice of materials and thicknesses that can be used (for example, it is not possible to use high-k dielectrics). In addition, there are a number of process steps between the lower electrode formation and the dielectric deposition (i.e., Cu CMP and cleans), resulting in poor reliability of the dielectric. Finally, there must be restrictions on the layout of the bottom Cu electrode to avoid dishing during CMP.

Hence, for manufacturability, an extra mask is required to form a MIM capacitor in Cu technology (compared to Al technology). The basic approach is to deposit the entire MIM capacitor stack (lower electrode + dielectric + upper electrode), then pattern both electrodes (Fig. 13c and 13d). This minimizes defects between the different layers in the stack, resulting in reliable devices.

A lower cost alternative to the MIM capacitor is the VPP capacitor. The VPP capacitor has many properties that are comparable to the MIM capacitor, including high capacitance density, good voltage linearity, and high quality factor [38,39]. The main disadvantage of the VPP capacitor is higher mismatch than the MIM capacitor (typically > 0.2 % versus < 0.05%), especially for high capacitance densities.

C. Inductors

The key parameters for inductors are the quality factor, inductance, and inductor area [34]. The quality factor is limited by resistive losses in the metal at low frequencies and by parasitic capacitances and resistances at high frequencies [40]. Hence, high performance inductors require thick metallization with low resistance vias, to reduce the series resistance. With thick Cu and/or Al metal layers (thickness of 3 µm or more), quality factors of over 25 are possible (1 nH inductor at 2 to 4 GHz) [34]. Further improvements in quality factor are possible by using a patterned ground shield at of polysilicon or a lower metal layer to reduce coupling between the inductor and the substrate [41]. Another approach is to etch out the silicon underneath the inductor, though this results in extra process steps and cost.

Another problem with inductors is that they consume large amounts of area on the chip. A simple solution is to use stacked spiral inductors [42]. However, the quality factor is reduced compared to a monolayer spiral inductor. Another approach is to integrate magnetic materials in the inductor, to increase inductance while maintaining high quality factors. This approach requires special materials such as high resistivity CoZrTa, and requires extra processing, so cost is increased [43].

VIII. CONCLUSION

There are many challenges with implementation of Cu interconnects at the 32 nm node and beyond, including increased resistivity, integration with porous low-k materials, and reliability. In addition, for RF and mixed signal technology, integration of passive devices is required. Interconnect technology will continue to be an active area of research and development for advanced technology nodes.

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